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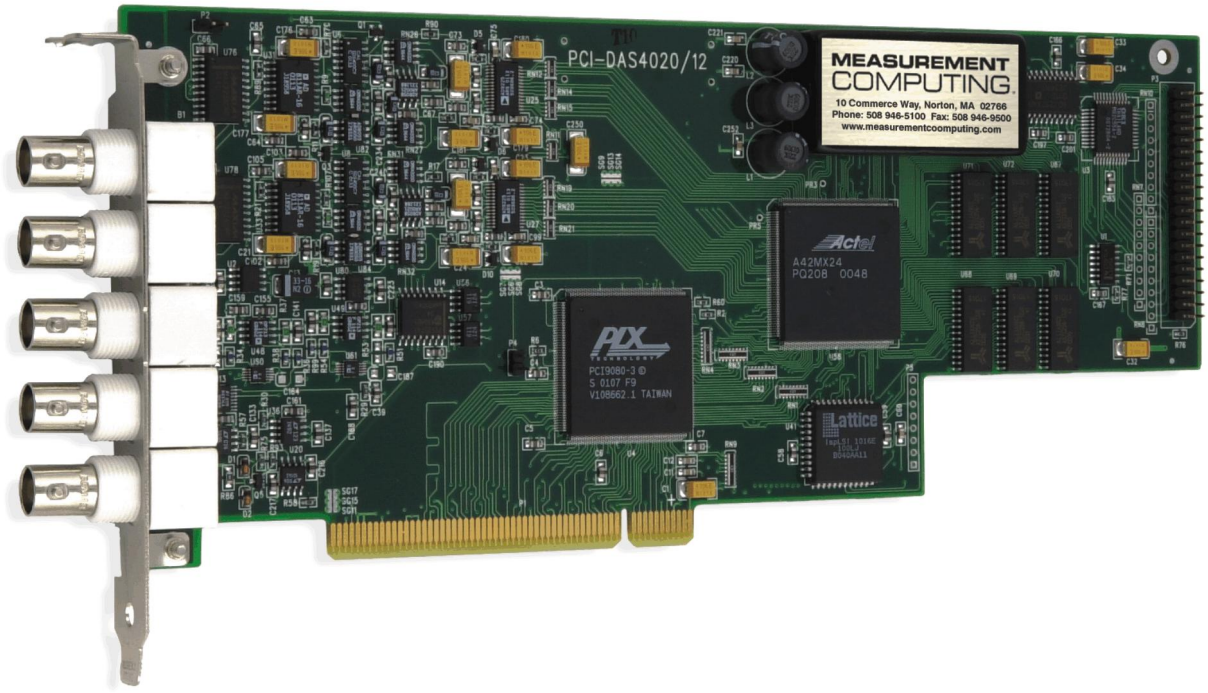
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Find the *Measurement Computing / ComputerBoards PCI-DAS4020/12* at our website: *Click HERE*

PCI-DAS4020/12

Analog and Digital I/O Board

User's Guide



MEASUREMENT COMPUTING™

PCI-DAS4020/12

Analog & Digital I/O

User's Guide



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About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-DAS4020/12 so that you get the most out of its analog and digital I/O features.

This user's guide also refers you to related documents available on our web site, and to technical support resources.

Conventions in this user's guide

For more information on …

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#> Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

bold text **Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:
1. Insert the disk or CD and click the **OK** button.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:
The *Insta*Cal installation procedure is explained in the *Quick Start Guide*.
Never touch the exposed pins or circuit connections on the board.

Where to find more information

For additional information relevant to the operation of your hardware, refer to the *Documents* subdirectory where you installed the MCC DAQ software (C:\Program Files\Measurement Computing\DAQ by default), or search for your device on our website at www.mccdaq.com.

If you need to program at the register level in your application, refer to the *Register Map for the PCI-DAS4020/12 Series* (available at www.mccdaq.com/registermaps/RegMapPCI-DAS4020-12.pdf

Introducing the PCI-DAS4020/12

Overview: PCI-DAS4020/12 features

This manual explains how to install and use the PCI-DAS4020/12 board.

The PCI-DAS4020/12 is a multi-function high-speed data acquisition I/O board that is designed for the PCI bus. It provides the following features:

- Four high-speed 12-bit analog input channels

  The input range for each channel is software-configurable for ±1 V or ±5 V. The sample rate is from 10 to 20 MHz, depending on the number of channels accessed. Triggering sources and A/D gating are via hardware or software, and can be internal or external. Four different modes are software selectable. Analog input connectors are standard BNC types.
- Two 12-bit analog output channels

  Each analog output channel can be configured by software for an output range of ±10 V or ±5 V. Throughput is system-dependent. Triggering mode is software gate. D/A pacing is software paced. The analog output channels terminate at a 40-pin auxiliary connector.
- 24 digital I/O channels

  An on-board industry standard 82C55A I/O chip provides 24 digital I/O channels configured as two banks of eight and two banks of four. You can configure each bank independently as input or output. Signal levels are TTL. The digital I/O channels terminate at a 40-pin auxiliary connector.

Software features

For information on the features of *Insta*Cal and the other software included with your PCI-DAS4020/12, refer to the *Quick Start Guide* that shipped with your device. The *Quick Start Guide* is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Check www.mccdaq.com/download.htm for the latest software version or versions of the software supported under less commonly used operating systems.

Installing the PCI-DAS4020/12

What comes with your PCI-DAS4020/12 shipment?

The following items are shipped with the PCI-DAS4020/12.

Hardware

- PCI-DAS4020/12



Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your PCI-DAS4020/12 and information regarding installation of that software. Please read this booklet completely before installing any software or hardware.

Optional components

If you ordered any of the following products with your board, they should be included with your shipment.

- Cables



C40FF-x



C40-37F-x



BP40-37F-x

Signal termination and conditioning accessories

MCC provides signal termination products for use with the PCI-DAS4020/12. Refer to "Field wiring, signal termination and conditioning" on page 16 for a complete list of compatible accessory products.

Unpacking the PCI-DAS4020/12

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-DAS4020/12 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the PCI-DAS4020/12

The PCI-DAS4020/12 board is completely plug-and-play, with no switches or jumpers to set. Configuration is controlled by your system's BIOS. To install your board, follow the steps below.

Install the MCC DAQ software before you install your board

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   If you are using an operating system with support for plug-and-play (such as Windows 2000 or Windows XP), a dialog box opens as the system loads, indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you are prompted for the disk containing this file. The *Measurement Computing Data Acquisition Software* CD supplied with your board contains this file. If required, insert the disk or CD and click **OK**.
3. To test your installation and configure your board, run the *Insta*Cal utility installed in the previous section. Refer to the *Quick Start Guide* that came with your board for information on how to initially set up and load *Insta*Cal.

If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 15 minutes before acquiring data. This warm-up period is required in order for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time.

Configuring the PCI-DAS4020/12

All of the hardware configuration options on the PCI-DAS4020/12 are software controlled. Use *Insta*Cal to select the number of channels to sample (one, two or four channels), and the analog output range (±10 V or ±5 V.) Once selected, any program that uses the Universal Library will initialize the hardware according to your selections.

Connecting the board for I/O operations

Connectors, cables – I/O connectors

The table below lists the board connectors, applicable cables, and compatible accessory products for the PCI-DAS4020/12.

Board connectors, cables, compatible hardware

Connector type	▪ BNC connector: five standard female connectors ▪ Auxiliary connector (P3): 40-pin header connector
Compatible cables (for the 40-pin auxiliary connector)	▪ C40FF-x ▪ C40-37F-x ▪ BP40-37-x
Compatible accessory products with the C40FF-x cable	CIO-MINI40
Compatible accessory products with the C40-37F-x cable or with the BP40-37-x and the C37FF-x or C37FFS-x cable	▪ CIO-MINI37 ▪ SCB-37 ▪ CIO-ERB24 ▪ CIO-ERB08 ▪ SSR-RACK24 ▪ SSR-RACK08

Information on signal connections

General information regarding signal connection and configuration is available in the *Guide to Signal Connections*. This document is available on our web site at www.mccdaq.com/signals/signals.pdf.

BNC connectors

The board's analog input and trigger input connectors are standard female BNC connectors that are visible from the rear of the computer when you install the board.

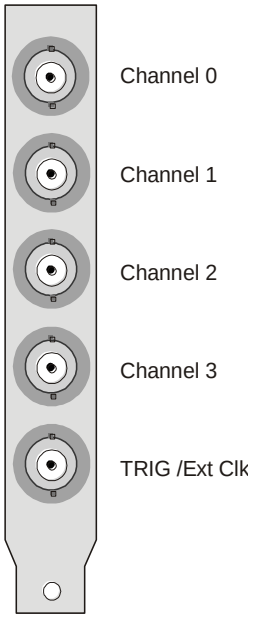


Figure 1. Analog inputs and trigger input BNC connectors

Pin out – auxiliary connector

The pin out for the board's 40-pin on-board auxiliary connector (labeled **P3** on the board) is listed below. Pin 1 is identified by a beveled edge on the board silkscreen.

40-pin auxiliary connector P3

Signal Name	Pin		Pin	Signal Name
D/A OUT 1	40		39	D/A OUT 0
D/A GND	38		37	GND
FIRSTPORTA Bit 0	36		35	+5V
FIRSTPORTA Bit 1	34		33	GND
FIRSTPORTA Bit 2	32		31	n/c
FIRSTPORTA Bit 3	30		29	GND
FIRSTPORTA Bit 4	28		27	n/c
FIRSTPORTA Bit 5	26		25	GND
FIRSTPORTA Bit 6	24		23	n/c
FIRSTPORTA Bit 7	22		21	GND
FIRSTPORTC Bit 0	20		19	FIRSTPORTB Bit 0
FIRSTPORTC Bit 1	18		17	FIRSTPORTB Bit 1
FIRSTPORTC Bit 2	16		15	FIRSTPORTB Bit 2
FIRSTPORTC Bit 3	14		13	FIRSTPORTB Bit 3
FIRSTPORTC Bit 4	12		11	FIRSTPORTB Bit 4
FIRSTPORTC Bit 5 (Start Trigger In/Ext Clock)	10		9	FIRSTPORTB Bit 5
FIRSTPORTC Bit 6 (A/D Stop Trigger In)	8		7	FIRSTPORTB Bit 6
FIRSTPORTC Bit 7 (A/D Pacer Gate)	6		5	FIRSTPORTB Bit 7
GND	4		3	INTERRUPT ENABLE *
+5V	2		1	INTERRUPT IN *

PCI slot ↓

***** Pin 1 and pin 3 have 10 K pull-up resistors installed.

Use pin 38 for analog output return

When using the analog output pins D/A OUT 0 (pin 39) and D/A OUT 1 (pin 40), use D/A GND only (pin 38) for the return.

Cabling

For signal connections and termination, you can use the CIO-MINI40 screw terminal board and C40FF-x cable. For connections to 37-pin screw terminal boards, you can use the C40-37F-*x* cable.

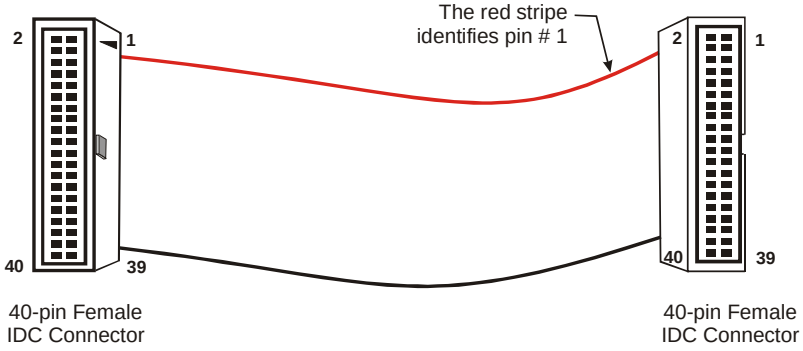


Figure 2. C40FF-*x* cable

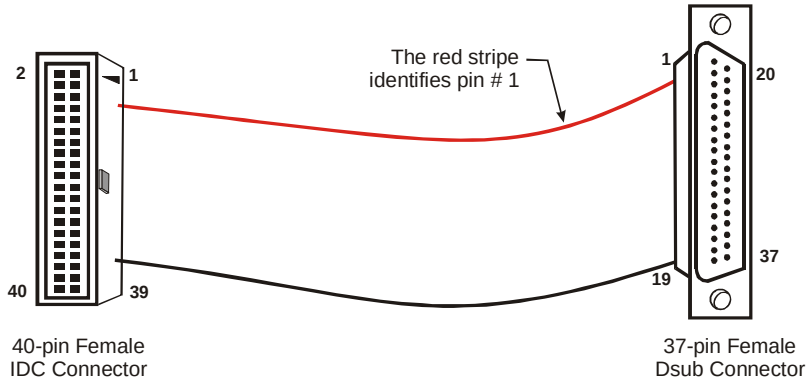


Figure 3. C40-37F-*x* cable

If you don't need to connect to the PCI-DAS4020/12 analog outputs (pins 38 to 40), you can connect to a BP40-37 cable. The BP40-37 cable brings pins 1 through 37 of the 40-pin connector out to 37-pin male "D" connector mounted on a backplane bracket.

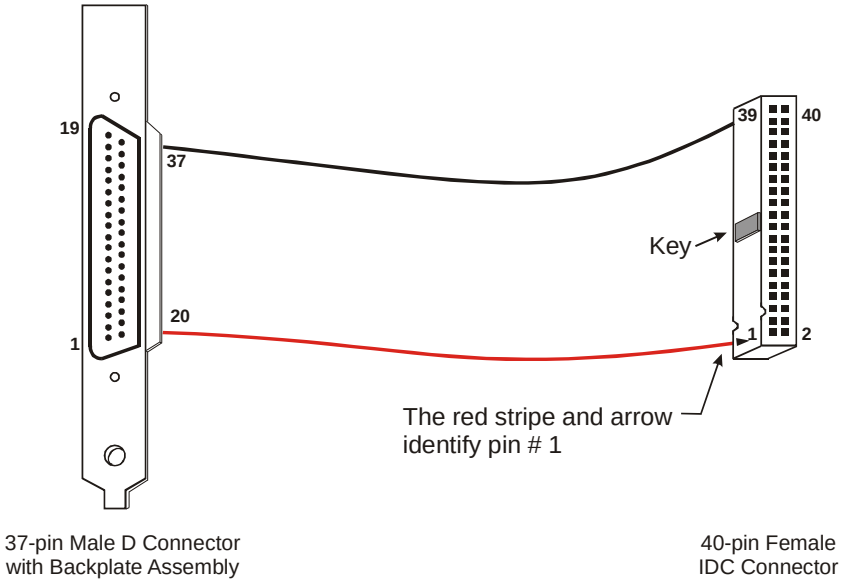


Figure 4. BP40-37 cable

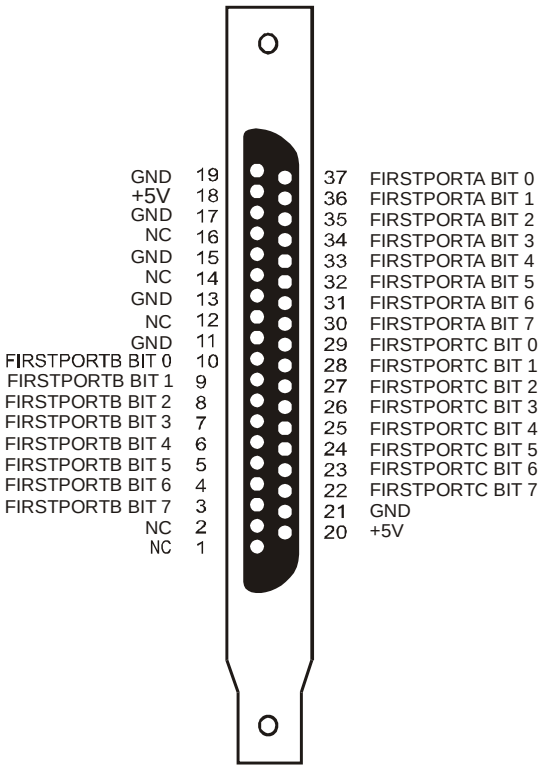


Figure 5. BP40-37 cable pin out

40-pin to 37-pin signal mapping

Signal mapping on the C40-37F-x and the BP40-37 cables is not 1:1. The following table lists the pin numbers of the signals on the 40-pin end and the pin numbers of the associated signals on the 37-pin end.

Signal mapping on the C40-37F-x and BP40-37F cables

40-pin cable end		37-pin cable end	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	INTERRUPT IN	1	INTERRUPT IN
2	+5V	20	+5V
3	INTERRUPT ENABLE	2	INTERRUPT ENABLE
4	GND	21	GND
5	Port B 7	3	Port B 7
6	Port C 7	22	Port C 7
7	Port B 6	4	Port B 6
8	Port C 6	23	Port C 6
9	Port B 5	5	Port B 5
10	Port C 5	24	Port C 5
11	Port B 4	6	Port B 4
12	Port C 4	25	Port C 4
13	Port B 3	7	Port B 3
14	Port C 3	26	Port C 3
15	Port B 2	8	Port B 2
16	Port C 2	27	Port C 2
17	Port B 1	9	Port B 1
18	Port C 1	28	Port C 1
19	Port B 0	10	Port B 0
20	Port C 0	29	Port C 0
21	GND	11	GND
22	Port A 7	30	Port A 7
23	N/C	12	N/C
24	Port A 6	31	Port A 6
25	GND	13	GND
26	Port A 5	32	Port A 5
27	N/C	14	N/C
28	Port A 4	33	Port A 4
29	GND	15	GND
30	Port A 3	34	Port A 3
31	N/C	16	N/C
32	Port A 2	35	Port A 2
33	GND	17	GND
34	Port A 1	36	Port A 1
35	+5V	18	+5V
36	Port A 0	37	Port A 0
37	GND	19	GND
38	N/C		
39	N/C		
40	N/C		

For digital signal conditioning, you can connect the BP40-37 cable to a C37FF-*x* or C37FFS- *x* cable, and then connect one of these cables to the 37-pin connector on MCC's digital signal conditioning boards. Refer to page 16 for a list of compatible boards.

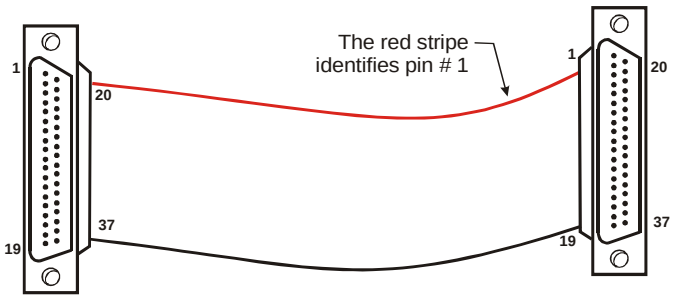


Figure 6. C37FF-*x* cable

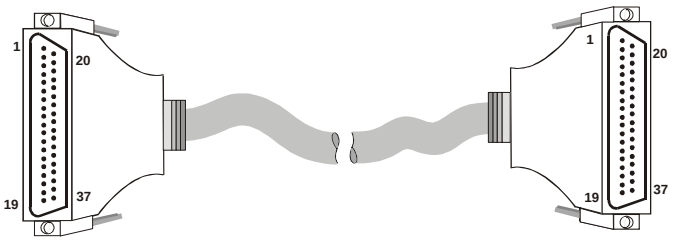


Figure 7. C37FFS-*x* cable

Field wiring, signal termination and conditioning

You can use the following MCC screw terminal board to terminate field signals and route them into the PCI-DAS4020/12 board using the C40FF-x cable:

- **CIO-MINI40** – 40-pin universal screw terminal board.

You can use the following MCC screw terminal boards to terminate field signals and route them into the PCI-DAS4020/12 board using the C40-37F-x cable directly or by combining the BP40-37-x cable with the C37FF-x or C37FFS-x cable:

- **CIO-MINI37** – 37-pin universal screw terminal board.
- **SCB-37** – 37 conductor, shielded signal connection/screw terminal box.

Details on these products are available on our web site at www.mccdaq.com/products/screw_terminal_bnc.aspx.

Digital Signal Conditioning

For digital signal conditioning, you can connect the PCI-DAS4020/12 to the following boards using the C40-37F-x cable directly or by combining the BP40-37-x cable with the C37FF-x or C37FFS-x cable.

- **CIO-ERB24** – 24 Form C, 6A relays.
- **CIO-ERB08** – Eight Form C, 6A relays.
- **SSR-RACK24** – 24-channel solid state module rack.
- **SSR-RACK08** – 24-channel solid state module rack.

Details on these products are available on our web site at www.mccdaq.com/products/signal_conditioning.aspx.

Functional Details

PCI-DAS4020/12 block diagram

PCI-DAS4020/12 functions are illustrated in the block diagram shown here.

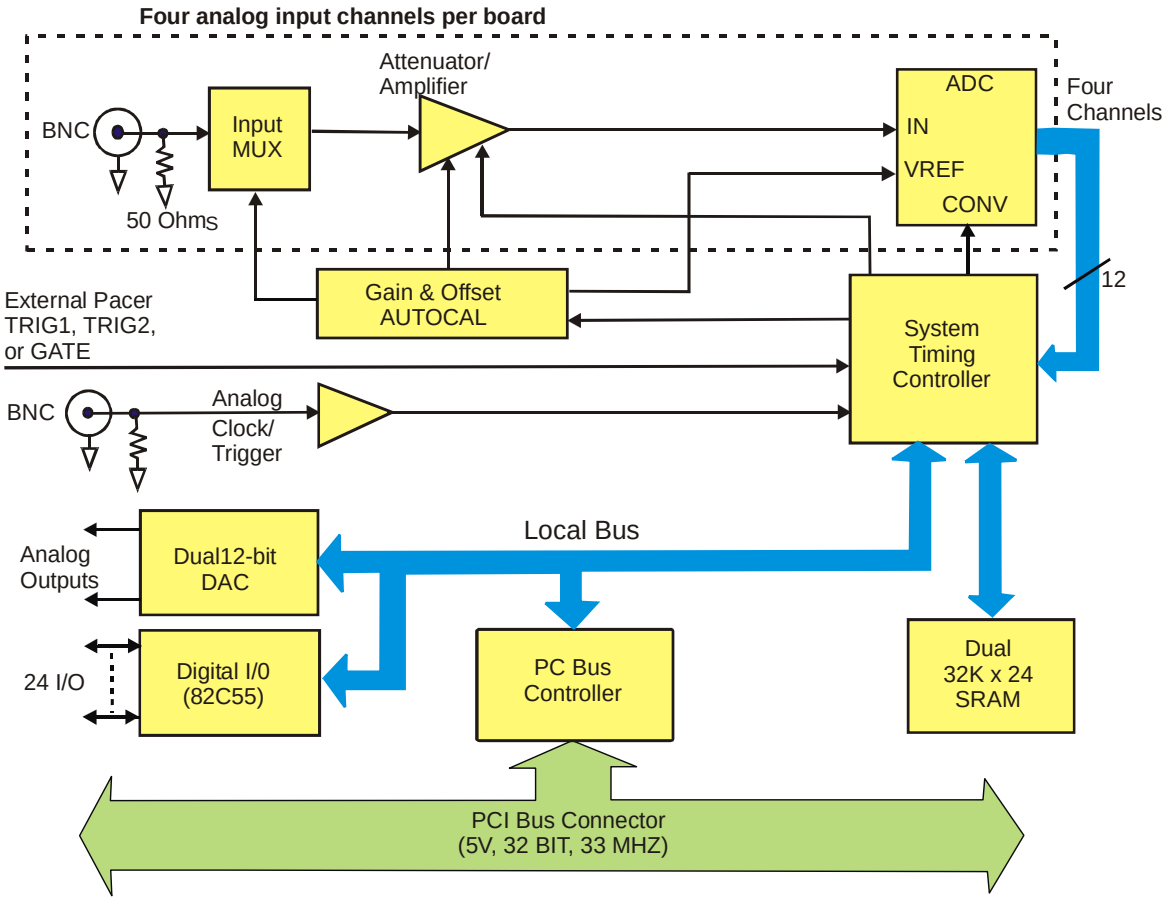


Figure 8. PCI-DAS4020/12 functional block diagram

Analog input signal path

Four single-ended analog input channels, connect from BNC connectors to individual amplifiers and then connect to dedicated ADC's. Each path allows for:

- 50 ohm or high-Z termination, selected by solder gap
- ±1 V or ±5 V bipolar ranges, software-selectable (refer to the table below)
- Auto-calibration for offset and gain adjustments for each channel and each range

Input range

Full Scale Input Range	Attenuation	Divider Output
+5 V to -5 V	5	±1 V
+1 V to -1 V	1	±1 V

Analog output

Two 12-bit voltage outputs are software programmable for ±10 V or ±5 V. The D/A is the Analog Devices AD7237 Dual DAC. Since the DAC is dual buffered, the DAC output voltage is updated after the MS nibble is written to the DAC.

The DACs initially power-up and are reset to 0 V. There is no calibration on these DACs. The offset and gain errors are minimized by using precision components. The following table shows the DAC input coding.

DAC input coding

DAC Range	Input Code Binary	12 bit Input Code Hex	12 bit Output Voltage
± 10 V	0000 0000 0000	000h	–10.000 V
± 10 V	1000 0000 0000	800h	0 V
± 10 V	1111 1111 1111	FFFh	+9.99513 V
± 5 V	0000 0000 0000	000h	–5.000 V
± 5 V	1000 0000 0000	800h	0 V
± 5 V	1111 1111 1111	FFFh	+4.99756 V

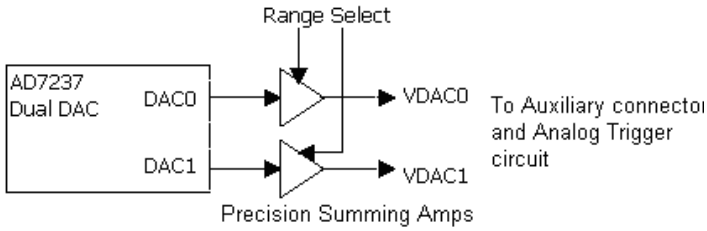


Figure 9. Analog output block diagram

Digital I/O

The digital I/O is an 82C55 digital logic device. An external interrupt source pin (pin 1) and external interrupt enable pin (pin 3) on the auxiliary 40-pin connector (**P3**) are used for external interrupts. These lines are pulled up and an OR operation is performed on them to generate the external interrupt signal. Both are active low.

Power distribution

The PCI-DAS4020/12 board is powered by the PCI bus. The only power used is +5 V.

Input impedance configuration

Each analog input and the trigger/clock input channel on the PCI-DAS4020/12 has a dedicated solder gap. A solder gap consists of two copper pads that you can solder together to change the input impedance of the channel. When the solder gaps are open (default), the input impedance is 1.5 MΩ. When the solder gaps are closed, the input impedance is 50 Ω.

To close the solder gaps and change the impedance to 50 ohm, solder the two copper pads together. To close the solder gap, touch a soldering iron to the two contacts until some rosin core solder flows across the copper pads and forms a small blob of solder. Be careful not to overheat the pads, or they may delaminate from the circuit board. Do not add too much solder, as it could flow onto other components and cause an electrical short or other defect.

Solder Gap Configuration	Input Impedance
Open	1.5 MΩ typical
Close	50 Ω

The board designation for the analog input channels and the trigger/clock BNC input are listed below.

Solder Gap board label	Channel
SG1	Channel 0
SG2	Channel 1
SG3	Channel 2
SG4	Channel 3
SG5	TRIG/Ext Clock input

Solder gaps for the analog input channels are located on the rear of the board (circuit-side) and are labeled **SG1** to **SG4**. See Figure 10.

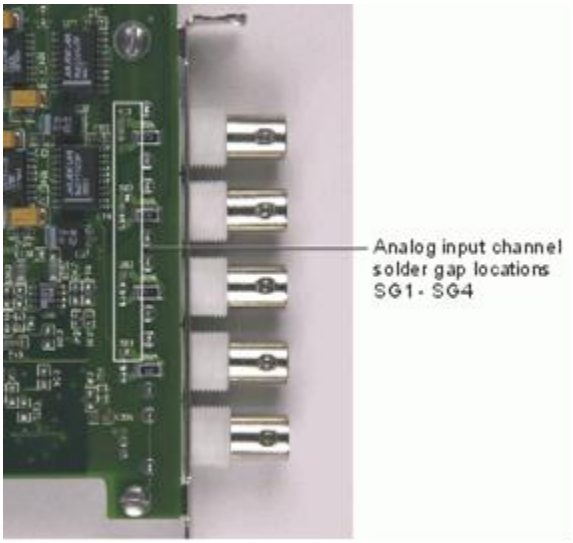


Figure 10. Analog input channel solder gap locations (circuit-side)

The solder gap for the trigger/clock input is located on the front of the board (component-side) and is labeled **SG5**. See Figure 11.

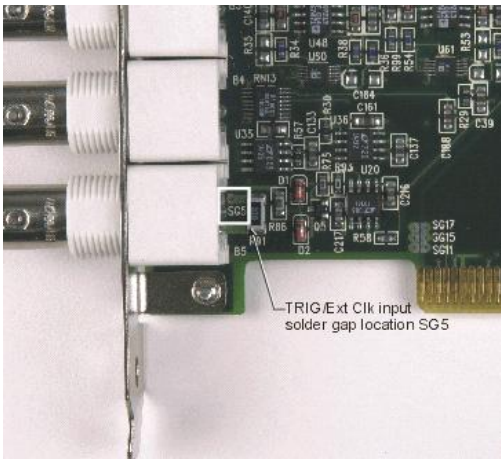


Figure 11. Trigger/clock input solder gap location (component-side)

An example of each input impedance configuration option is shown in Figure 12.

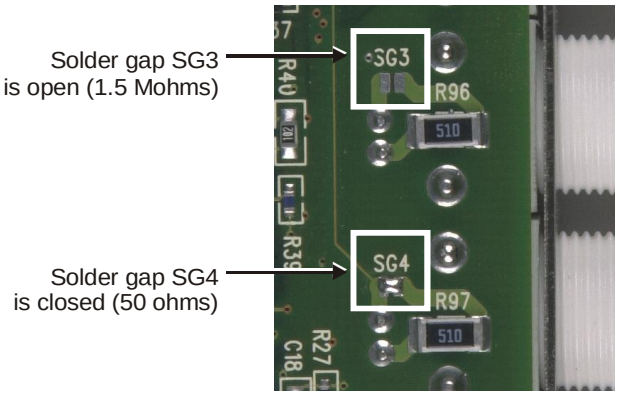


Figure 12. Open and closed solder gaps

Calibrating the PCI-DAS4020/12

Use the *Insta*Cal utility program to calibrate the PCI-DAS4020/12. *Insta*Cal calibrates the PCI-DAS4020/12 using on-board digital potentiometers and trim D/A converters. No external equipment or user adjustments are required.

The PCI-DAS4020/12 is factory calibrated. The calibration coefficients are stored in nvRAM. Analog input adjustments are made via 10-bit calibration DACs that are referenced to the on-board factory calibrated standard. Each channel has a pair of dedicated 10-bit DACs that trim out offset and gain errors. *Insta*Cal calibrates the offset by adjusting the offset voltage at the input of each ADC, and adjusts the gain via the ADC reference pin.

At run time, the calibration factors are loaded into system memory and are automatically retrieved each time a different ADC range is specified. You can recalibrate any time using factory voltage standards with *Insta*Cal. A full calibration typically takes less than two minutes.

Before you calibrate the board, turn your computer on and allow at least 30 minutes for the internal case temperature to stabilize. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are sensitive to temperature. Pre-measurement calibration insures that your board is operating with optimum calibration values.

Calibration theory

Analog inputs are calibrated for offset and gain. Offset calibration is performed directly on the input amplifier, with coarse and fine trim DACs acting on the amplifier.

For input gain calibration, a precision calibration reference is used in conjunction with coarse and fine trim DACs acting on the ADC. See Figure 13.

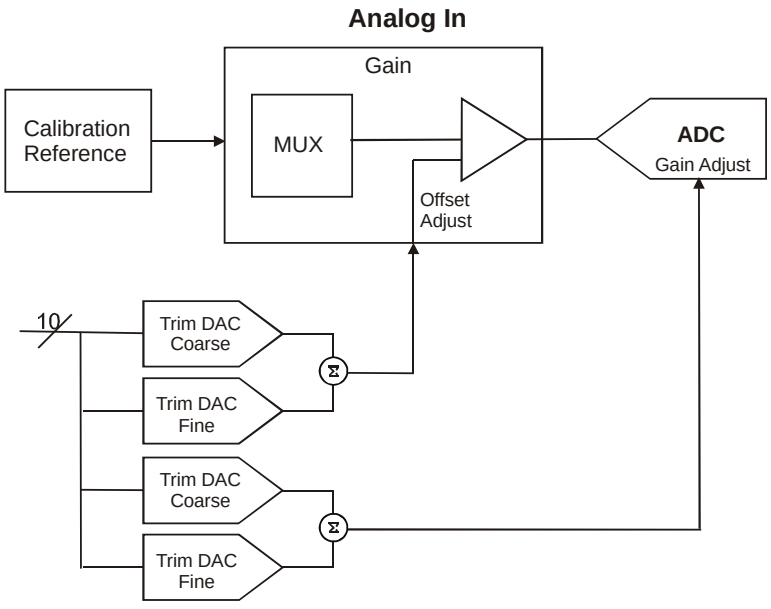


Figure 13. Analog input calibration

Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	AD9225, 25 MSPS pipelined A/D
Resolution	12-bits
Programmable ranges	±5 V, ±1 V
Number of channels	4 single-ended, independent ADC's per channel
Connection	4 independent BNC
Bandwidth	17 MHz typical
Coupling	DC
Input leakage current	*2 uA typ, 10 uA max*
Input impedance	1.5 Mohm typ, or 50 ohm, selectable (coaxial cable termination)
Absolute maximum input voltage	±15 V

Timing and throughput

Table 2. Timing and throughput specifications

Simultaneous sampling	Software selectable option - 1, 2, or 4 channels
A/D Convert clock source	Internal: ▪ On-card crystal oscillator ▪ Frequency: 40 MHz ▪ Frequency accuracy: 50% duty cycle, 50 ppm External: ▪ Trig/Ext Clk BNC, or A/D External Clock on the 40-pin connector ▪ 24-bit internal pre-scale counter (min pre-scale = 2) ▪ Clock Rate: 40 MHz max, 2 kHz min ▪ Duty Cycle: 50% ± 5%
A/D Gate source	Digital: Trig/Ext Clk BNC or A/D Pacer Gate on 40-pin connector Analog: Any of the four input channels
A/D Gate modes	Digital: Programmable active high/low, level/edge Analog: Above/below reference, positive/negative Hysteresis, inside/outside window Resolution: 12-bit Slew rate: 10V/sec. minimum
A/D Start Trigger (TRIG1)	Software: Using a DAQ start command. Digital: Trig/Ext Clk BNC, A/D Start Trigger In (on the 40-pin connector) Analog: Any of the four input channels
A/D Stop Trigger (TRIG2)	Digital: Trig/Ext Clk BNC, A/D Stop Trigger In (on the 40-pin connector) Analog: Any of the four input channels
A/D Triggering modes	Digital: Programmable rising or falling edge Analog: Trigger above/below reference Resolution: 12-bit
Pre-trigger mode	Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. Compatible with both digital and analog trigger/gate options. Data acquisition initiated via TRIG1. Post-trigger phase initiated via TRIG2.

Data transfer	Via dual 32 K x 24 sample FIFO, SRAM based, with Bus-Master DMA and scatter-gather, interrupt, or software polled.
A/D Conversion time	40 ns
Sample rate	20 MHz max, 1 kHz min
Throughput	Single channel: 20 MHz continuous Two channels (0 and 1 or 2 and 3): 20 MHz continuous Four channels: 10 MHz continuous In background mode, the maximum throughput may be impacted by bus or interrupt activity.

Accuracy

Table 3. Analog input accuracy specifications

Absolute accuracy	±5.5 LSB worst case error (either range)
Typical accuracy	±3.0 LSB error (either range)
Accuracy components:	
Gain error	±2.0 LSB max, ±1.0 LSB typ
Offset error	±1.5 LSB max, ±1.0 LSB typ
Integral linearity error	±2.5 LSB max, ±1.0 LSB typ
Differential linearity error	*±1.0 LSB max , ±0.4 LSB typ (No missing codes guaranteed)*

Board error is a combination of gain, offset, integral linearity, and differential linearity error. The overall absolute worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are both at their maximum level, and causing error in the same direction. Though this is very uncommon, it is still possible, and the calculated worst case error of the PCI-DAS4020/12 board is ±7.0 LSB.

Each PCI-DAS4020/12 board is tested at the factory to make sure that its actual worst case error is less than ±5.0 LSB. Allowing for a 10% guard-band, the absolute worst-case error of a board is ±5.5 LSB. Typical accuracy can be calculated from the various component typical errors in a similar fashion. This typical maximum error calculation for the PCI-DAS4020/12 board yields ±3.4 LSB. However, this again assumes that each of the errors is forcing an error in the same direction. Empirical evidence supports a conservative typical error budget of ±3.0 LSB.

Table 4. Calibration specifications

Calibration	Auto-calibration. Calibration factors for each range stored on board in non-volatile RAM

Temperature

Table 5. Temperature specifications

Gain drift	±5 V range: ±0.10 LSB/°C max ±1 V range: ±0.13 LSB/°C max
Offset drift	±0.11 LSB/°C max, all ranges
Overall board temperature drift	±5 V range: ±0.21 LSB/°C max ±1 V range: ±0.24 LSB/°C max

Overall, worst-case temperature drift is calculated by adding the drifts corresponding to the gain and offset drifts. This worst case number is unlikely to occur, as it requires both gain and offset drifts to be at their maximum levels, and to be affecting the measurement in the same direction. However, the overall board D/A drift specifications have been calculated in this fashion.

Dynamics and noise

Table 6. Dynamics and noise specifications

SNR (Signal-to-noise ratio)	66.6 dB	
SINAD (signal-to-noise and distortion ratio)	66.5 dB	
SFDR (spurious free dynamic range)	80 dB	
THD (total harmonic distortion)	80 dB	
Noise distribution:		
(Rate = 10 KHz-20 MHz, Average % ± 2 bins, Average % ± 1 bin, Average # bins)	Bipolar (5V):	100% / 98% / 5 bins
	Bipolar (1V):	100% / 98% / 5 bins

Trig/Ext Clk BNC

Software selectable for A/D Start Trigger (TRIG1), A/D Stop Trigger (TRIG2) or A/D Pacer Gate (AGATE); also used as an A/D clock input 2X clock source (DAQ_CLK).

Table 7. Trig/Ext Clk BNC specifications

Input impedance	50 ohm, 1 Mohm selectable (coaxial cable termination)
Input threshold	Programmable 2.5 V threshold or 0 V threshold
Input slew rate	1 V/µsec min
Input range	±5 V
Bandwidth	40 MHz
Coupling	DC

Analog output

Table 8. Analog output specifications

D/A converter type	AD7237
Resolution	12-bits
Number of channels	2
Output range	±10 V, ±5 V software selectable
D/A pacing	Software paced
Throughput	System dependent. Using the Universal Library programmed output function (`cbAout`) in a loop in Visual Basic, a typical update rate of 500 Hz (± 50 Hz) can be expected. The rate was measured on a 330 MHz Pentium II based PC.
Data transfer	Programmed I/O
Monotonicity	Guaranteed monotonic over temperature
Analog output drift	±0.11 LSB/°C max, all ranges
Settling time (20 V step to ± ½ LSB)	5 µs max
Slew rate	5 V/µs
Current drive	±5 mA
Output short-circuit duration	25 mA indefinite
Output coupling	DC
Output impedance	0.5 Ohm max
Miscellaneous	▪ Single buffered output latch ▪ Update DACs individually On power-up and reset, the inputs to both D/A output buffers are grounded and the board's D/A outputs will be set to 0 volts ± 6 mV. Upon writing to the D/A converters, the output buffers will reflect the D/A outputs and achieve rated accuracy. However, upon writing a 0 to the D/A's, a small output change may be noted (up to 10 LSB).

Accuracy

Table 9. Analog output accuracy specifications

Absolute accuracy	±13 LSB max
Offset error	±6 LSB max
Gain error	±5 LSB max
Differential non-linearity	±1 LSB max
Integral non-linearity	±1 LSB max

Total analog output error is a combination of gain, offset, integral linearity, and differential linearity error. The overall absolute worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are both at their maximum level, and causing error in the same direction. Though this is very uncommon, it is still possible.

Digital input / output

Table 10. DIO specifications

Digital type (40-pin connector)	8255A
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output high	3.0 volts min @ 2.5 mA
Output low	0.4 volts max @ 2.5 mA
Input high	2.0 volts min, Vcc + 0.5 volts absolute max
Input low	0.8 volts max, GND – 0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)

Interrupts

Table 11. Interrupt specifications

Interrupts	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Software programmable
ADC Interrupt sources	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active. DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected. DAQ_DONE: Interrupt is generated when a DAQ sequence completes. DAQ_FIFO_1/2_FULL: Interrupt is generated when ADC FIFO is ½ full. DAQ_SINGLE: Interrupt is generated after each conversion completes.
External	Interrupt is generated via edge-sensitive transition on the Interrupt In pin on the 40-pin connector. Rising/falling edge polarity selection. The Interrupt In pin is pulled up to 5 V through a 10 K resistor.
External Interrupt Enable	Active low Interrupt Enable signal on the 40-pin connector. The Interrupt Enable pin is pulled up to 5 V through a 10 K resistor.

Environmental

Table 12. Environmental specifications

Operating temperature range	0 to 70 °C
Storage temperature range	–40 to 100 °C
Humidity	0 to 90% non-condensing

Power consumption

Table 13. Power consumption specifications

+5 V Operating (A/D to FIFO)	1.5 A typical, 2.0 A max

Connector and pin out

Table 14. Connector specifications

Connector type	BNC connector: five standard female connectors Auxiliary connector (P3): 40-pin header connector
Compatible cables (for the 40-pin auxiliary connector)	C40FF-x
	C40-37F-x
	BP40-37-x
Compatible accessory products with the C40FF-x cable	CIO-MINI40
Compatible accessory products with the C40-37F-x cable or with the BP40-37-x and the C37FF-x or C37FFS-x cable	CIO-MINI37 SCB-37 CIO-ERB24 CIO-ERB08 SSR-RACK24 SSR-RACK08

Auxiliary connector P3 pinout

Table 15. Auxiliary connector (P3) pin out

Pin	Signal Name	Pin	Signal Name
1	INTERRUPT IN *	2	+5V
3	INTERRUPT ENABLE *	4	GND
5	FIRSTPORTB Bit 7	6	FIRSTPORTC Bit 7 (A/D Pacer Gate)
7	FIRSTPORTB Bit 6	8	FIRSTPORTC Bit 6 (A/D Stop Trigger In)
9	FIRSTPORTB Bit 5	10	FIRSTPORTC Bit 5 (Start Trigger In/Ext Clock)
11	FIRSTPORTB Bit 4	12	FIRSTPORTC Bit 4
13	FIRSTPORTB Bit 3	14	FIRSTPORTC Bit 3
15	FIRSTPORTB Bit 2	16	FIRSTPORTC Bit 2
17	FIRSTPORTB Bit 1	18	FIRSTPORTC Bit 1
19	FIRSTPORTB Bit 0	20	FIRSTPORTC Bit 0
21	GND	22	FIRSTPORTA Bit 7
23	n/c	24	FIRSTPORTA Bit 6
25	GND	26	FIRSTPORTA Bit 5
27	n/c	28	FIRSTPORTA Bit 4
29	GND	30	FIRSTPORTA Bit 3
31	n/c	32	FIRSTPORTA Bit 2
33	GND	34	FIRSTPORTA Bit 1
35	+5V	36	FIRSTPORTA Bit 0
37	GND	38	D/A GND
39	D/A OUT 0	40	D/A OUT 1

***** Pins 1 and 3 have 10 K pull-up resistors installed.

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
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Norton, MA 02766
USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS4020/12

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: General Requirements, EN 61326-1:2006 (IEC 61326-1:2005).

Emissions:

- EN 55011 (2007) / CISPR 11(2003): Radiated emissions: Group 1, Class A
- EN 55011 (2007) / CISPR 11(2003): Conducted emissions: Group 1, Class A

Immunity: EN 61326-1:2006, Table 3.

- IEC 61000-4-2 (2001): Electrostatic Discharge immunity.
- IEC 61000-4-3 (2002): Radiated Electromagnetic Field immunity.
- IEC 61000-4-4 (2004): Electric Fast Transient Burst Immunity.
- IEC 61000-4-5 (2001): Surge Immunity.
- IEC 61000-4-6 (2003): Radio Frequency Common Mode Immunity.
- IEC 61000-4-11 (2004): Voltage Interrupts.

To maintain compliance to the standards of this declaration, the following conditions must be met.

- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to ground.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326-1:2006, or IEC 61326-1:2005.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in September, 2001. Test records are outlined in Chomerics Test Report #EMI3053.01. Further testing was conducted by Chomerics Test Services, Woburn, MA. 01801, USA in January, 2009. Test records are outlined in Chomerics Test report #EMI5243.09.

We hereby declare that the equipment specified conforms to the above Directives and Standards.



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