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Document UM-06160-F

User Manual
for

DT2811

Low Cost Analog and Digital
I/O Board for
IBM PC, PC XT, PC AT and Compatible
Computer Systems

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Sixth Edition
November, 1992

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PREFACE

This hardware manual is written for users of the Data Translation DT2811 analog and digital input/output board. It describes the functions performed by the three subsystems of the board--A/D conversion, D/A conversion, and digital I/O--and provides all information necessary to successfully program and operate the board in an IBM PC/XT/AT or compatible personal computer system. The manual assumes that you have a general knowledge of electronic circuitry, are familiar with the IBM PC bus, understand data conversion, and possess enough proficiency in software to write your own application and diagnostic programs. The following list provides summaries of all sections in the manual.

CHAPTER 1 - INTRODUCTION

Chapter 1 provides an overview of the DT2811 boards and gives a summary of compatible data acquisition accessories available from Data Translation.

CHAPTER 2 - SPECIFICATIONS

Chapter 2 provides the complete electrical and physical specifications of the DT2811 and compatible accessories.

CHAPTER 3 - CONFIGURATION

Chapter 3 discusses the selection of various board parameters and the configuration of the board for specific application requirements.

CHAPTER 4 - INTERCONNECTIONS

Chapter 4 describes the interconnection of the DT2811 with the host computer system and user inputs. The chapter also discusses connection schemes for analog inputs.

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CHAPTER 5 - ARCHITECTURE AND OPERATION

Chapter 5 discusses the main elements of the DT2811 architecture and operation. It describes the on-board registers which control the operations of the three subsystems, and details the functions performed by the register bits.

CHAPTER 6 - OPERATING PRINCIPLES

Chapter 6 highlights the main principles governing the operations of the A/D subsystem. It pinpoints trigger sources available to the user, discusses the operating modes of the board, and details the requirements for proper operation of the board. Chapter 6 also provides example programs which illustrate the use of the DT2811 in various applications.

CHAPTER 7 - CALIBRATION

Chapter 7 describes the calibration of the A/D and D/A subsystems.

APPENDIX A - DT707 AND DT752 SCREW TERMINAL PANELS

Appendix A describes the DT707 and DT752 screw terminal panels recommended for use with the DT2811.

APPENDIX B - TROUBLESHOOTING AND FACTORY SERVICE

Appendix B describes a procedure for field troubleshooting the DT2811 and tells how to ship a troubled board to the Data Translation factory for service.

APPENDIX C - ENGINEERING DRAWINGS

Appendix C provides the assembly drawings of the DT2811, DT707, and DT752, and the jumper map of the DT2811.

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CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

The DT2811* is a half-size, low-cost analog and digital I/O board designed for use with the IBM PC/XT/AT and compatible microcomputer systems. The DT2811 features three subsystems, each of which performs a distinct function: analog to digital conversion (A/D); digital to analog conversion (D/A); and digital I/O. The DT2811 is typically used for industrial process control and laboratory research in low noise environments. The board can be plugged into any one of the fully bussed expansion slots in the IBM PC/XT/AT or compatible computer backplane. Table 1-1 highlights the main features of the DT2811.

TABLE 1-1: MAIN FEATURES OF DT2811

MODEL	A/D				D/A	
	RANGE	RES	GAIN	MAX THRUPUT	RANGE	RES
DT2811-PGH	0-5V ±5V ±2.5V	12	1,2, 4,8	20kHz 20kHz	0-5V ±5V ±2.5V	12
DT2811-PGL	0-5V ±5V ±2.5V	12	1,10, 100, 500	20kHz 2.5kHz 2.5kHz	0-5V ±5V ±2.5V	12

NOTE:
- o RES = Resolution in bits.

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* Throughout this manual, the designation DT2811 is used to refer to the two boards, DT2811-PGH and DT2811-PGL. The full designation (DT2811 with suffix PGH or PGL) is used when referring to specific models.

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1.1.1 A/D SUBSYSTEM

The main component of the A/D subsystem is a monolithic analog to digital converter which acquires analog voltage inputs from the outside world through sensors such as thermocouples and pressure transducers, and converts them into 12-bit digital codes. The board then transmits this code to the host computer which processes it according to the software preloaded in the computer's memory and commands issued to the processor by the operator during the execution of the program. The A/D subsystem is equipped with a gain circuit which permits software programmable amplification of the input signal. Model DT2811-PGH provides a gain of 1, 2, 4, or 8 for high-level inputs, while model DT2811-PGL provides a gain of 1, 10, 100, or 500 for low-level inputs.

The A/D subsystem provides 16 single-ended or 8 differential input channels for A/D conversions. It can be configured for unipolar or bipolar input ranges of 0 to +5V, ±5V, and ±2.5V. The DT2811 provides 12-bit resolution of the input voltage. The output code is straight binary for unipolar inputs and offset binary for bipolar inputs.

The DT2811 can operate in single or continuous conversion modes. In the single conversion mode, the DT2811 performs conversion on a selected channel and stops at the completion of the conversion. Another channel (or the same channel) must be selected for the next conversion operation. In the continuous conversion mode, repetitive hardware triggered conversions can be performed on a selected channel. The conversions come to a halt when the trigger is disabled.

A/D conversion operations can be monitored either by polled I/O or by interrupts. In the polled I/O mode, the program polls the A/D Control/Status Register repeatedly for an indication of the completion of the ongoing A/D conversion. In the interrupt mode, the board automatically generates an interrupt to the host processor at the completion of an A/D conversion.

The throughput of the A/D subsystem depends on a variety of factors, such as the triggering method and the gain applied to the input signal. In the polled I/O mode, a maximum throughput of 20kHz (20K conversions per second) can be achieved with repetitive hardware triggers applied to a single channel.

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1.1.2 D/A SUBSYSTEM

The D/A subsystem consists of two 12-bit D/A converters, DAC0 and DAC1. The DACs convert a digital input received from the host processor into a voltage output required by the application. The DACs provide two independent channels, each capable of operating at a throughput of up to 50kHz. Output ranges can be independently configured to be unipolar (0 to +5V) or bipolar (±5V or ±2.5V).

1.1.3 DIGITAL I/O SUBSYSTEM

The digital I/O subsystem provides an interface for the transfer of digital data between the PC bus and one or more peripheral devices connected to the DT2811. It consists of two digital I/O ports, Port 0 and Port 1. Port 0 is dedicated to inputs, while Port 1 is dedicated to outputs. In a data input operation, the processor reads the status of the digital I/O lines and data is transferred from an I/O device to the computer. In a data output operation, the processor sends data to the digital I/O lines, and data is transferred from the computer to an I/O device.

1.2 INTERFACE LOGIC

The DT2811 is accessed via a 10-bit address received from the host processor. The most significant 7 bits select the board. The three least significant bits are decoded on-board and select various registers in the three subsystems. The DT2811 ignores all address bits beyond the 10th.

The DT2811 occupies 8 byte locations in the PC bus I/O space. Five of these locations are occupied by the A/D subsystem, two by the D/A subsystem, and one by the digital I/O subsystem. The base address can be configured to be located anywhere between 200 (hex) and 3F8 (hex) in increments of 8 (hex).

The DT2811 operates from the +5V, +12V, and -12V power lines on the IBM PC bus.

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1.3 ACCESSORIES

In many applications, the DT2811 may require accessories to interface with the input/output signals. Some of these accessories--such as the Data Translation DT701-50 and DT707--are simple screw terminal panels whose main function is to provide connection points to the interface. Others--such as the Data Translation DT709-Y, DT756-Y, and DT6700 series--contain circuitry to provide signal conditioning functions in addition to serving as interface connection points. Compatible accessories available from Data Translation are discussed briefly in this section.

DT707

The DT707 screw terminal panel provides direct connection points to all three subsystems of the DT2811 as well as to the external trigger and external oscillator inputs. This screw terminal panel is recommended for use with the DT2811 when no secondary signal conditioning panels are required. User connections are made through convenient screw terminals which are labeled in silkscreen. The connection to the host computer system is made via an integral 50-conductor flat ribbon cable (3.3 feet) which plugs directly into the DT2811 board's J1 connector. The DT707 is designed for table-top mounting and comes equipped with rubber feet. Further details on the DT707 are given in Appendix A.

DT752

The DT752 connects to the host processor via a 50-pin 3M type connector, as with the DT707. Unlike the DT707, however, not all screw terminals lead to pins on the J1 connector. The DT752 divides the 50-pin connection to the host computer into two separate 30-pin and 20-pin user connections. The 30-pin connection provides the interface for the D/A, digital I/O, clock signals, and trigger inputs via on-board terminal screws. The 20-pin connection extends off-board via a 20-conductor integral cable and can be used to interface a variety of compatible signal conditioning panels to the A/D input channels of the DT2811. The DT752 can be used whenever a secondary signal conditioning source is required for A/D inputs. Compatible Data Translation signal conditioning panels include the non-isolated DT709-Y, DT756-Y, and the isolated DT6700 series of signal conditioning modules (see later in this section). Further details on the DT752 are given in Appendix A.

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DT701-50

This is a 19-inch, rack-mountable, screw terminal panel which provides a 50-pin header for connection of input lines to the DT2811. It contains blank pads for user-supplied passive signal conditioning components. The DT701-50 can be used to connect all three subsystems to the outside world. Connecting cable: EP035 or EP066.

DT709-Y

This signal conditioning panel provides 16 differential input channels and 16 single-ended outputs. It contains a differential amplifier at each input channel for common mode rejection ratio of 60dB at 60Hz. The DT709-Y effectively converts the DT2811 single-ended inputs into differential inputs, doubling the number of differential input channels. When using the DT709-Y, the DT2811 should be jumpered for single-ended inputs. The DT709-Y obtains +12V and -12V supply from the DT2811 power output lines. Requires DT752 to connect to the DT2811.

DT756-Y

This board is designed for low level inputs, such as signals from thermocouples and bridges. It contains circuits for thermocouple cold-junction compensation, gain of up to 200, and channel-to-channel offset of ±1.5mV. The DT756-Y provides 16 differential input channels and 16 single-ended outputs. The DT756-Y effectively converts the DT2811 single-ended inputs into differential inputs, doubling the number of differential input channels. The board provides common mode rejection of 100dB at 60Hz. When using the DT709-Y, the DT2811 should be jumpered for single-ended inputs. The DT756-Y obtains +12V and -12V supply from the DT2811 power output lines. Requires DT752 to connect to the DT2811.

DT6700

The DT6700 series of isolated signal conditioning modules can be used with the DT2811 when high immunity is required for the input signals. The DT6700 series are mounted on the DT750 backplane which accommodates up to 16 modules. Each channel requires one signal conditioning module. Each module provides isolation for one of the following input types: differential voltage input, RTD or bridge completion input, tachometer input, or thermocouple input. The DT750 backplane is powered from the 110 Vac line. Requires DT752 to connect to the DT2811.

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EP035
This is a 50-conductor, 8ft (2.4m) flat ribbon cable assembly with a 50-pin socket connector (3M-3425) on each end. It connects the J1 connector of the DT2811 to the 50-pin, 3M-type connector of the DT701-50. The EP035 comes in two versions: EP035 (8 feet) and EP035-1 (18 inches).

EP066
This is a 50-conductor, 8ft (2.4m) flat twisted pair cable assembly with a 50-pin socket connector (3M-3425) on each end. It connects the J1 connector of the DT2811 to the 50-pin, 3M-type connector of the DT701-50. The EP066 is 8 feet long and is used for differential inputs only.

1.4 SOFTWARE SUPPORT

Data Translation has developed a real-time software package, LPCLAB, which supports all the functions performed by the DT2811. LPCLAB is written in Assembly Language and provides subroutine libraries callable from the following languages:

- Microsoft C (all memory models--compact, small, medium, large, and huge)
- Microsoft FORTRAN
- Microsoft PASCAL
- Microsoft compiled BASIC
- IBM interpreted BASIC

LPCLAB includes routines to perform the following functions:

1. Single-value A/D, D/A, and DIO transfers
2. Multiple-value A/D transfers to memory
3. Full thermocouple support
4. On-board clock set-up
5. Error handling

Besides the DT2811, LPCLAB also supports other Data Translation analog and digital I/O boards such as the DT2814 (IBM PC compatible A/D converter), DT2815 (IBM PC compatible D/A converter), and DT2817 (IBM PC compatible digital I/O board). LPCLAB can service up to four boards of any combination per system.

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1.5 TROUBLESHOOTING

Data Translation maintains a Technical Support department which provides assistance to customers using Data Translation boards. Technical Support can be contacted whenever a problem is encountered with a Data Translation board. Appendix B provides you with a troubleshooting guide and tells you what to do in case of a persistent problem with your board.

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CHAPTER 2

SPECIFICATIONS

2.1 INTRODUCTION

This chapter lists the specifications of the DT2811 board and related accessories. Specifications are provided for the following items:

- o A/D Subsystem
- o D/A Subsystem
- o Digital I/O Subsystem
- o Internal Clock
- o External Trigger
- o External Oscillator
- o Interface Characteristics
- o Power Requirements
- o Physical/Environmental
- o Accessories

Unless noted otherwise, the specifications are typical at +25°C and rated voltage.

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2.2 A/D SUBSYSTEM

ANALOG INPUTS	
Number of Analog Inputs	16SE/8DI
Input Ranges (Jumper-selectable)	0 to +5V (unipolar) ±5V, ±2.5V, (bipolar)
Output Data Codes	Straight binary (unipolar) or offset binary (bipolar)
Gain	
DT2811-PGH	1,2,4,8
DT2811-PGL	1,10,100,500
Input Impedance	
Off Channel	100MΩ, 10pF in parallel;
On Channel	100MΩ, 100pF in parallel
Bias Current	±50nA
Common Mode Input Voltage, Maximum	±11V
Common Mode Rejection Ratio	
Gain = 1	70dB at 60Hz, 1kΩ unbalance;
Gain = 500	100dB at 60Hz, 1kΩ unbalance
Maximum Input Voltage Without Damage, Power On	±32V
Maximum Input Voltage Without Damage, Power Off	±20V
Amplifier Input Noise	2.0μV RMS
ACCURACY	
Resolution	12 bits
Nonlinearity	Less than ±3/4 LSB
Differential Nonlinearity	Less than ±1/2 LSB
Inherent Quantizing Error	±1/2 LSB

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System Accuracy		
DT2811-PGH,	Gain = 1	Within ±.03% FSR
	Gain = 2	Within ±.035% FSR
	Gain = 4	Within ±.04% FSR
	Gain = 8	Within ±.05% FSR
DT2811-PGL,	Gain = 1	Within ±.03% FSR
	Gain = 10	Within ±.05% FSR
	Gain = 100	Within ±.07% FSR
	Gain = 500	Within ±.15% FSR
Channel Crosstalk		-80dB at 1kHz
Gain Error		Adjustable to 0
Zero Error		Adjustable to 0

DYNAMIC PERFORMANCE

Channel Acquisition Time	
Gains of 1,2,4,8,10	20µs (average)
Gains of 100,500	370µs (average)
A/D Conversion Time	30µs
A/D Converter Throughput	
Gains of 1,2,4,8,10	20kHz
Gains of 100,500	2.5kHz
Dynamic Error	±.75 LSB for a 10V change (max.)

THERMAL CHARACTERISTICS

A/D Zero Drift	±10ppm of FSR/°C
Gain Drift	±30ppm of FSR/°C
Differential Linearity Drift	+/-3ppm of FSR/°C
Monotonicity	0 to 70°C

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2.3 D/A SUBSYSTEM

ANALOG OUTPUTS

Number of Channels	2 (DAC0, DAC1)
Output Ranges	0 to +5V (unipolar) ±2.5V (bipolar) ±5V (bipolar)
Input Data Codes	Straight binary (unipolar); Offset binary (bipolar)
Output Drive Current	±5mA max.
Source Impedance (dc)	0.1Ω max.
Capacitive Drive Capability	0.004μF typical
Protection Against	Short circuit indefinitely to Analog Common
Power-up state	Indeterminate

ACCURACY

Resolution	12 bits
Nonlinearity	To within 0.01% FSR
Differential Nonlinearity	Less than ±3/4 LSB
Inherent Quantizing Error	Less than ±1/2 LSB
Gain Error	Adjustable to 0
Zero Error	Adjustable to 0
System Accuracy	±0.025% FSR

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DYNAMIC PERFORMANCE	
Settling Time to 0.01%	
10V Step	7µs max.
100mV Step	1µs max.
Slew Rate	10V/µs (up) min. 10V/µs (down) min.
DAC Throughput	50kHz max. (single channel)
Output Noise	0.2 LSB's max.
THERMAL CHARACTERISTICS	
Offset Drift (Bipolar)	±10ppm/°C max.
Gain Drift (Bipolar)	±30ppm/°C max.
Differential Linearity Drift	3ppm of FSR/°C
Monotonicity	0 to 70°C

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2.4 DIGITAL I/O SUBSYSTEM

Number of Ports	Two 8-line ports
Logic Family	Positive true (ALSTTL)

DIGITAL INPUTS

Number of Lines	8
Logic Family	LSTTL
Logic Load	1 ALSTTL
Logic High Input Voltage	2.0V min.
Logic Low Input Voltage	0.8V max.
Logic High Input Current	20.0µA
Logic Low Input Current	-0.1mA

DIGITAL OUTPUTS

Number of Lines	8
Fanout	20 LSTTL loads
Logic High Output Voltage	2.4V min.
Logic Low Output Voltage	0.4V max.
Logic High Output Current	-15mA max.
Logic Low Output Current	24.0mA min.

2.5 INTERNAL CLOCK

Base Frequency	600kHz ±100ppm
Divisor Values	1 to 120,000,000
Usable Frequency Range	.005Hz - 20kHz

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2.6 EXTERNAL TRIGGER

Logic	Asserted Low LSTTL
Trigger Pulse Width (Low)	500ns min.
High Level Input Voltage	2.0V min.
Low Level Input Voltage	.8V max.
High Level Input Current	20µA max.
Low Level Input Current	-.2mA max.

2.7 EXTERNAL OSCILLATOR

Logic	High to low transition LSTTL
Pulse Width (Low)	500ns min.
Frequency	DC to 1MHz
High Level Input Voltage	2.0V min.
Low Level Input Voltage	.8V max.
High Level Input Current	20µA max.
Low Level Input Current	-.2mA max.

2.8 INTERFACE CHARACTERISTICS

Connector J1	3M-3596-5002; mating connector: 3M-3425
Compatible Bus	IBM PC/XT/AT and compatibles
Interface Type	I/O mapped with 10-bit addressing
Number of Locations Occupied	8 consecutive I/O locations
Number of I/O Registers	8
Address Range	200 to 3F8 (hex)
Factory Assigned Base Address	218 (hex)

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SPECIFICATIONS
INTERFACE CHARACTERISTICS

Data Path	Eight bits
Interrupt Options	Selectable to level 2,3,5, or 7
Interrupt Source	A/D Done bit or Error bit in A/D Control/Status Register
Analog Data Format	12-bit, right justified

2.9 POWER REQUIREMENTS

Power Supply Range	+5V, ±.5V, @ 290mA +12V, ±.5V, @ 50mA -12V, ±.5V, @ 100mA

2.10 PHYSICAL ENVIRONMENTAL

Dimensions	4.5"HX7.0"WX0.75"D (11.4X17.8X1.9cm)
Weight	6 oz (168g)
Altitude	To 7500ft (2286m)
Operating Temperature Range	0 to +50°C (32 to 122°F)
Storage Temperature Range	-25 to +70°C (13 to 158°F)
Relative Humidity	To 95%, non-condensing

2.11 ACCESSORIES

DT707	Screw terminal panel with integral 50-conductor cable assembly to connect to the DT2811
DT752	Screw terminal panel with integral

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	cable assembly; provides off-board connection to analog inputs
DT701-50	Screw terminal panel with a single 50-pin connector
DT709	Screw terminal/ signal conditioning panel; 20-pin connector; requires DT752.
DT756	Screw terminal/ signal conditioning panel; 20-pin connector; requires DT752.
DT6700	Isolated series of signal conditioning modules; 20-pin connector; requires DT752.
EP035	50-conductor flat ribbon cable assembly for use with DT701-50
EP066	50-conductor twisted pair cable assembly for use with DT701-50

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CHAPTER 3

CONFIGURATION

3.1 INTRODUCTION

Certain operational parameters of the DT2811 are selectable by the user to suit particular applications. These parameters are:

- o Board Base Address
- o A/D Input Range
- o A/D Input Mode
- o Interrupt Level
- o D/A Output Range

The selection of parameters is made by appropriate jumper configurations. Each selection is illustrated in a table where the factory-standard configuration of the parameter is indicated by "FC". The board should be fully configured for the specific needs of the application before it is placed in operation.

Jumpers are designated by "W" numbers. A single "W" number refers to a pair of jumper posts. For example, W19 designates a unique jumper which consists of two adjacent jumper posts. Jumper configuration is performed by connecting the pair of jumper posts designated by the "W" number. In some instances, a pair of jumpers may share a post. Jumpers W10 and W11, for instance, form such a pair. These pairs of jumpers are mutually exclusive, that is, if one jumper is in, the other jumper is necessarily out. In all instances, jumpers are installed by connecting two adjacent posts with a wire wrap or a jumper plug. Jumper designations are indicated on the component side of the DT2811 board. A jumper map is included in the Engineering Drawings in Appendix C.

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3.2 BASE ADDRESS

The DT2811 requires eight contiguous byte locations in the I/O address space of the IBM PC/XT/AT computer system. All the address locations are occupied by registers of the A/D, D/A, and digital I/O subsystems. The base address is the lowest location on the I/O address segment assigned to the DT2811. This location is occupied by the A/D Control/Status Register (see Chapter 5). The other registers are assigned locations relative to the base address. The base address can be located anywhere between 200 (hex) and 3F8 (hex) in increments of 8 (hex). Table 3-1 shows all the base addresses assignable to the DT2811. The table also indicates the locations within the available address range which are normally mapped to IBM devices and are not recommended for assignment to the DT2811.

IMPORTANT

Each address location used by a DT2811 board must be unused by any other device in the system, INCLUDING ANOTHER DT2811 BOARD. Multiple DT2811 boards must be assigned different base addresses, and must not occupy address locations used by other devices in the system.

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TABLE 3-1: DT2811 BASE ADDRESSES

BASE ADDRESS	JUMPERS W19	W20	W21	W27	W24	W23
200	In	In	In	In	In	In
208	In	In	In	In	In	Out
210	In	In	In	In	Out	In
218 (FC)	In	In	In	In	Out	Out
220	In	In	In	Out	In	In
228	In	In	In	Out	In	Out
230	In	In	In	Out	Out	In
238	In	In	In	Out	Out	Out
240	In	In	Out	In	In	In
248	In	In	Out	In	In	Out
250	In	In	Out	In	Out	In
258	In	In	Out	In	Out	Out
260	In	In	Out	Out	In	In
268	In	In	Out	Out	In	Out
270	In	In	Out	Out	Out	In
278*	In	In	Out	Out	Out	Out
280	In	Out	In	In	In	In
288	In	Out	In	In	In	Out
290	In	Out	In	In	Out	In
298	In	Out	In	In	Out	Out
2A0	In	Out	In	Out	In	In
2A8	In	Out	In	Out	In	Out
2B0	In	Out	In	Out	Out	In
2B8	In	Out	In	Out	Out	Out
2C0	In	Out	Out	In	In	In
2C8	In	Out	Out	In	In	Out
2D0	In	Out	Out	In	Out	In
2D8	In	Out	Out	In	Out	Out
2E0	In	Out	Out	Out	In	In
2E8	In	Out	Out	Out	In	Out
2F0	In	Out	Out	Out	Out	In
2F8*	In	Out	Out	Out	Out	Out
300	Out	In	In	In	In	In
308*	Out	In	In	In	In	Out
310	Out	In	In	In	Out	In
318*	Out	In	In	In	Out	Out
320	Out	In	In	Out	In	In
328	Out	In	In	Out	In	Out
330	Out	In	In	Out	Out	In
338	Out	In	In	Out	Out	Out

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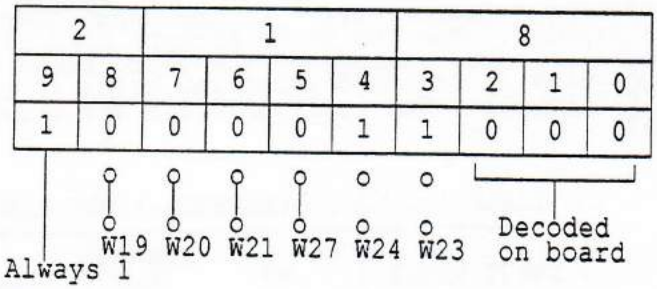
TABLE 3-1 (CONT'D): DT2811 BASE ADDRESSES

BASE ADDRESS	JUMPERS W19	W20	W21	W27	W24	W23
340	Out	In	Out	In	In	In
348	Out	In	Out	In	In	Out
350	Out	In	Out	In	Out	In
358	Out	In	Out	In	Out	Out
360	Out	In	Out	Out	In	In
368*	Out	In	Out	Out	In	Out
370	Out	In	Out	Out	Out	In
378*	Out	In	Out	Out	Out	Out
380	Out	Out	In	In	In	In
388*	Out	Out	In	In	In	Out
390	Out	Out	In	In	Out	In
398	Out	Out	In	In	Out	Out
3A0	Out	Out	In	Out	In	In
3A8*	Out	Out	In	Out	In	Out
3B0	Out	Out	In	Out	Out	In
3B8*	Out	Out	In	Out	Out	Out
3C0	Out	Out	Out	In	In	In
3C8*	Out	Out	Out	In	In	Out
3D0	Out	Out	Out	In	Out	In
3D8*	Out	Out	Out	In	Out	Out
3E0	Out	Out	Out	Out	In	In
3E8	Out	Out	Out	Out	In	Out
3F0	Out	Out	Out	Out	Out	In
3F8*	Out	Out	Out	Out	Out	Out

NOTES:
- All base address values are given in hex.
- FC = Factory Configuration.
- Asterisked locations are normally assigned to IBM devices and are not recommended to be used for the DT2811.

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Figure 3-1 shows the configuration of the base address. The factory default base address of 218 (hex) is illustrated. Note that an installed jumper selects the value of 0 for the bit it controls.



NOTES:

- The first row from the top represents the factory selected base address. The second row indicates the bit numbers of the base address. The third row shows the binary value of each address bit. A value of 0 indicates that the jumper is installed, and a value of 1 indicates that the jumper is removed.
- Address bits 0 to 2 select the board registers. They are decoded by the board and are not jumper-configured.
- Address bits 10 through 19 are ignored by the board.

FIGURE 3-1: BASE ADDRESS SELECTION

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3.3 A/D SUBSYSTEM INPUT RANGE

The A/D subsystem of the DT2811 permits selection of three voltage input ranges: one unipolar (0 to +5V) and two bipolar (±2.5V and ±5V). If the board is configured for the unipolar input range, it accepts positive voltages only. If the input range selected is bipolar, then the board accepts both positive and negative input voltages. The input range of the A/D subsystem is selected using the group of jumpers W9, W10, and W11. The configurations are shown in Table 3-2.

TABLE 3-2: A/D SUBSYSTEM INPUT RANGE

INPUT RANGE	JUMPERS W9	W10	W11
0 to +5V	Out	In	Out
+/-2.5V	In	In	Out
+/-5V (FC)	In	Out	In

NOTE:
- FC = Factory Configuration.

3.4 A/D SUBSYSTEM INPUT MODE

The DT2811 accepts signals in three different input modes: single-ended, differential, and pseudo-differential. The selection depends on the user application. In single-ended input mode, a board provides maximum channel density, because all signals share a common return point, Analog Ground. In differential input mode, each signal has a separate return path. This input mode provides common noise rejection, but reduces the number of input channels by half. The pseudo-differential input mode is a variation of the single-ended input which provides some common mode rejection without sacrificing channel density. Table 3-3 shows the jumper configurations for the selection of the input mode. Connection schemes for the three input modes are discussed in Chapter 4.

NOTE

Model DT2811-PGL must be used in differential input mode at gain of 100 or 500.

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TABLE 3-3: A/D SUBSYSTEM INPUT MODES

INPUT MODE	JUMPERS W30	W14	W15	W13	W18	W22
Single-ended (FC)	In	Out	Out	In	In	In
Differential	Out	In	Out	Out	Out	Out
Pseudo-diff.	In	Out	In	Out	In	In

NOTES:
- o FC = Factory Configuration.
- o Model DT2811-PGL must be jumpered for differential inputs when used at gain of 100 or 500.

3.5 A/D SUBSYSTEM INTERRUPT LEVEL

The DT2811 can issue interrupts to the processor on any one of four different levels. The interrupt levels usable by the DT2811 are, in order of decreasing priority, 2 (highest), 3, 5, and 7 (lowest). Table 3-4 lists the jumpers controlling the interrupt level selection for the DT2811 board. The factory-shipped configuration of level 2 interrupt is indicated with "FC".

IMPORTANT

Each interrupt level used by the DT2811 in the IBM PC/AT/XT must be unused by any other device in the system including another DT2811 board. If multiple DT2811 boards are installed in the system, each board must be assigned to a distinct interrupt request line. Note that if there are no available interrupt request lines for the A/D subsystem, the DT2811 may still be installed for D/A and digital I/O operations. Consult the IBM PC/AT/XT Personal Computer's Technical Reference Manual and the technical information supplied with any other boards being used to determine the interrupt level used by other devices in the system.

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TABLE 3-4: A/D SUBSYSTEM INTERRUPT LEVEL SELECTION

INTERRUPT LEVEL	JUMPERS W29	W25	W26	W28
2 (FC)	In	Out	Out	Out
3	Out	In	Out	Out
5	Out	Out	In	Out
7	Out	Out	Out	In
None	Out	Out	Out	Out

NOTE:
- FC = Factory Configuration.

3.6 D/A SUBSYSTEM OUTPUT RANGE

The D/A subsystem of the DT2811 includes two independently operable digital to analog converters (DAC0 and DAC1). Each DAC can be configured for one of three output ranges: one unipolar (0 to +5V) and two bipolar (±2.5V or ±5V). The DAC outputs are controlled by two separate groups of jumpers. Table 3-5 shows the jumper configurations for the selection of the output range for each DAC.

TABLE 3-5: D/A SUBSYSTEM OUTPUT RANGE

D/A SUBSYSTEM OUTPUT RANGE	JUMPERS W7	W8	W5	W6	W3	W4	W1	W2
DAC0								
0 to +5V	Out	In	Out	In	N/A	N/A	N/A	N/A
±2.5V	Out	In	In	Out	N/A	N/A	N/A	N/A
±5V (FC)	In	Out	In	Out	N/A	N/A	N/A	N/A
DAC1								
0 to +5V	N/A	N/A	N/A	N/A	Out	In	Out	In
±2.5V	N/A	N/A	N/A	N/A	Out	In	In	Out
±5V (FC)	N/A	N/A	N/A	N/A	In	Out	In	Out

NOTES:
- FC = Factory Configuration.
- N/A = Not Applicable.

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3.7 JUMPER SUMMARY

Table 3-6 gives a summary of the configurations of jumpers on the DT2811. All the jumpers are user-configurable for the selection of various parameters. The factory default configuration of each jumper is also indicated.

TABLE 3-6: DT2811 JUMPER SUMMARY

JUMPER	FUNCTION	FACTORY CONFIGURATION
W1	Selects DAC1 output range	In
W2	Selects DAC1 output range	Out
W3	Selects DAC1 output range	In
W4	Selects DAC1 output range	Out
W5	Selects DAC0 output range	In
W6	Selects DAC0 output range	Out
W7	Selects DAC0 output range	In
W8	Selects DAC0 output range	Out
W9	Selects A/D input range	In
W10	Selects A/D input range	Out
W11	Selects A/D input range	In
W13	Selects A/D input mode	In
W14	Selects A/D input mode	Out
W15	Selects A/D input mode	Out
W16	Factory set	Out
W17	Factory set	In
W18	Selects A/D input mode	In
W19	Selects base address	In
W20	Selects base address	In
W21	Selects base address	In
W22	Selects A/D input mode	In
W23	Selects base address	Out
W24	Selects base address	Out
W25	Selects int. req. level	Out
W26	Selects int. req. level	Out
W27	Selects base address	In
W28	Selects int. req. level	Out
W29	Selects int. req. level	In
W30	Selects A/D input mode	In

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CHAPTER 4

INTERCONNECTIONS

4.1 INTRODUCTION

The DT2811 plugs into the IBM PC/XT/AT or compatible expansion slot at connector P1, and connects to the user interface at connector J1. This chapter details the P1 and J1 connections. It also illustrates the connection of some Data Translation screw terminal panels to the DT2811, and provides a discussion with diagrams of the A/D connection schemes.

4.2 CONNECTION TO BACKPLANE

The DT2811 plugs into an expansion slot of the IBM PC/XT/AT backplane via its 62-pin P1 edge connector. All communication between the host processor and the DT2811--A/D, D/A, and digital I/O--is carried through this connector. The pin assignments of the P1 connector are given in Table 4-1.

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TABLE 4-1: P1 PIN ASSIGNMENTS

PIN	MNEMONIC	SIGNAL DESCRIPTION
A1	-I/O CH CK	No Connection
A2	+D7	Data Bit 7 (MSB)
A3	+D6	Data Bit 6
A4	+D5	Data Bit 5
A5	+D4	Data Bit 4
A6	+D3	Data Bit 3
A7	+D2	Data Bit 2
A8	+D1	Data Bit 1
A9	+D0	Data Bit 0 (LSB)
A10	-I/O CH RDY	No Connection
A11	+AEN	Address Enable
A12	+A19	No Connection (MSB)
A13	+A18	No Connection
A14	+A17	No Connection
A15	+A16	No Connection
A16	+A15	No Connection
A17	+A14	No Connection
A18	+A13	No Connection
A19	+A12	No Connection
A20	+A11	No Connection
A21	+A10	No Connection
A22	+A9	Address Bit 9
A23	+A8	Address Bit 8
A24	+A7	Address Bit 7
A25	+A6	Address Bit 6
A26	+A5	Address Bit 5
A27	+A4	Address Bit 4
A28	+A3	Address Bit 3
A29	+A2	Address Bit 2
A30	+A1	Address Bit 1
A31	+A0	Address Bit 0 (LSB)

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TABLE 4-1 (CONT'D): P1 PIN ASSIGNMENTS

PIN	MNEMONIC	SIGNAL DESCRIPTION
B1	GND	Ground
B2	+RESET DRV	Reset Driver
B3	+5V	+5 Volt Power
B4	+IRQ2	Interrupt Request 2
B5	-5VDC	No Connection
B6	+DRQ2	No Connection
B7	-12V	-12 Volt Power
B8	OWS	No Connection
B9	+12V	+12 Volts Power
B10	GND	Ground
B11	-SMEMW	No Connection
B12	-SMEMR	No Connection
B13	-IOW	I/O Write
B14	-IOR	I/O Read
B15	-DACK3	No Connection
B16	+DRQ3	No Connection
B17	-DACK1	No Connection
B18	+DRQ1	No Connection
B19	REFRESH	No Connection
B20	CLK	No Connection
B21	+IRQ7	Interrupt Request 7
B22	+IRQ6	No Connection
B23	+IRQ5	Interrupt Request 5
B24	+IRQ4	No Connection
B25	+IRQ3	Interrupt Request 3
B26	-DACK2	No Connection
B27	+T/C	No Connection
B28	BALE	No Connection
B29	+5V	+5 Volt Power
B30	OSC	No Connection
B31	+GND	Ground

4.3 USER CONNECTION

The DT2811 is connected to the user interface via the 50-pin, 3M-type J1 connector (P/N 3425). The J1 connector accommodates 16 single-ended or 8 differential A/D input channels, 2 D/A channels, 16 digital I/O lines, and the external trigger and oscillator. J1 also provides +12V and -12V power supply lines with limited current output. These lines can be used to power compatible Data Translation signal conditioning panels. Table 4-2 gives the pin assignments of the J1 connector.

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TABLE 4-2: J1 PIN ASSIGNMENTS

PIN FUNCTION	PIN		PIN FUNCTION
Ch 0	1	2	Ch 8 (Ch 0 Ret)
Ch 1	3	4	Ch 9 (Ch 1 Ret)
Ch 2	5	6	Ch 10 (Ch 2 Ret)
Ch 3	7	8	Ch 11 (Ch 3 Ret)
Ch 4	9	10	Ch 12 (Ch 4 Ret)
Ch 5	11	12	Ch 13 (Ch 5 Ret)
Ch 6	13	14	Ch 14 (Ch 6 Ret)
Ch 7	15	16	Ch 15 (Ch 7 Ret)
Analog Ground	17	18	Amp Lo
+12V Out	19	20	-12V Out
Power Ground	21	22	DAC0 Output
DAC0 Ground	23	24	DAC1 Output
DAC1 Ground	25	26	Digital Ground
Digital Ground	27	28	Dig. Input Line 0
Dig. Input Line 1	29	30	Dig. Input Line 2
Dig. Input Line 3	31	32	Digital Ground
Dig. Input Line 4	33	34	Dig. Input Line 5
Dig. Input Line 6	35	36	Dig. Input Line 7
Digital Ground	37	38	Dig. Out. Line 0
Dig. Out. Line 1	39	40	Dig. Out. Line 2
Dig. Out. Line 3	41	42	Digital Ground
Dig. Out. Line 4	43	44	Dig. Out. Line 5
Dig. Out. Line 6	45	46	Dig. Out. Line 7
Digital Ground	47	48	Digital Ground
External Trigger	49	50	Ext. Oscillator

NOTE:
- The ±12V on pins 19 and 20 is intended only to power active circuitry on Data Translation screw terminal panels. Very little current is available on those pins. The ±12V should NOT be used to power external, user-supplied circuits.

4.4 CONNECTIONS TO SCREW TERMINAL PANELS

This section illustrates connections of the DT2811 to some compatible screw terminal panels available from Data Translation.

Three Data Translation screw terminal panels are recommended to be used with the DT2811: DT707, DT752, and DT750. The DT707 and DT752 connect directly to the DT2811 via integral, one meter cable assemblies. The DT701-50 requires the 50-conductor EP035 flat-ribbon cable assembly. Some signal conditioning panels available from Data Translation--such as the DT709-Y, DT756-Y, and

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DT6700 series--can be used in conjunction with the DT752. The connections of the screw terminal panels to the DT2811 are illustrated in Figures 4-1 through 4-3.

Figure 4-1 shows the connection of the DT2811 to the DT707.

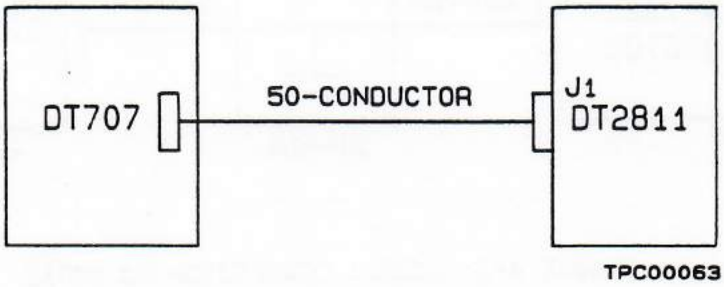


FIGURE 4-1: DT2811 CONNECTION TO DT707

Figure 4-2 shows the connection of the DT752 to the DT2811. This figure also indicates compatible screw terminal/signal conditioning panels which connect to the DT2811 via the DT752 and can be used for analog inputs to the DT2811.

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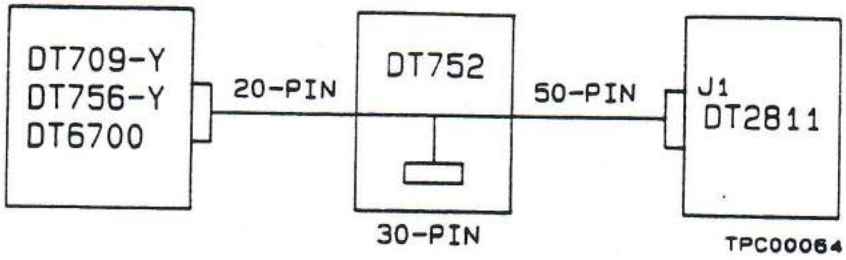


FIGURE 4-2: DT2811 CONNECTION TO DT752

Figure 4-3 illustrates the connection of the DT701-50 screw terminal panel to the DT2811. This connection requires an EP035 or EP066 cable assembly.

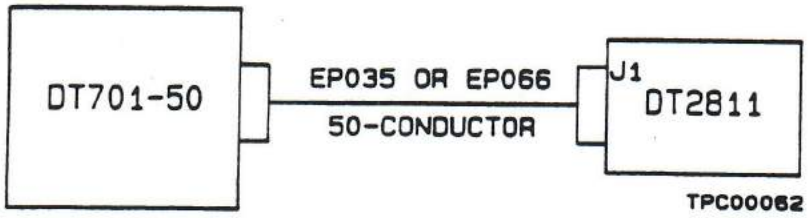


FIGURE 4-3: DT2811 CONNECTION TO DT701-50

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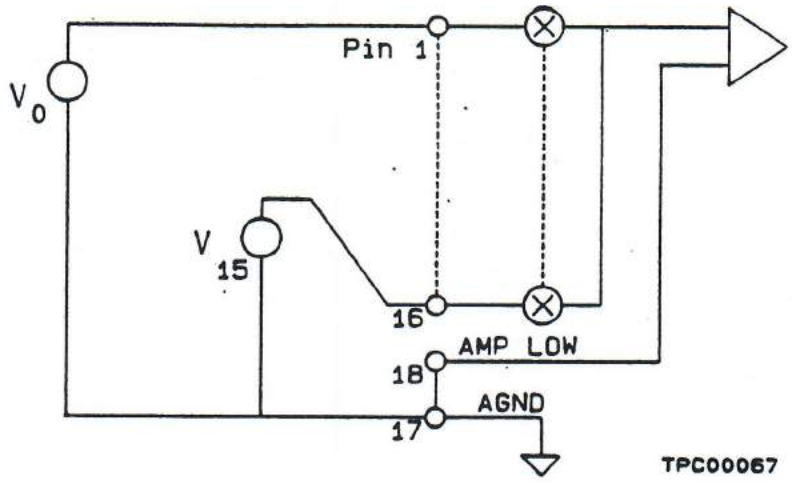
4.5 RECOMMENDED ANALOG INPUT CONNECTION SCHEMES

Analog signals can be input to the A/D subsystem of the DT2811 in three possible connection schemes--single-ended, pseudo-differential, and differential.

4.5.1 SINGLE-ENDED INPUTS

In single-ended connections, input signals share a common low side which is connected to Analog Ground (AGND, pin 17). The connection between Analog Ground and Amp Low (pin 18) is made internally via board jumper W13. The advantage of this input mode is that it provides maximum channel density. The major disadvantage is the loss of common mode rejection obtainable from a differential input. Since single-ended inputs are very sensitive to electrical noise, their use should be restricted to lead lengths no more than 15 feet (4.6m) and gains no more than 10. Figure 4-4 shows the connection scheme for single-ended inputs.

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NOTES:

- All signal inputs must be referenced to Analog Ground.
- All unused analog input channels should be connected to Analog Ground. Failure to do so can result in inaccurate A/D conversions on all other channels, those closest to the floating channel(s) being affected most.

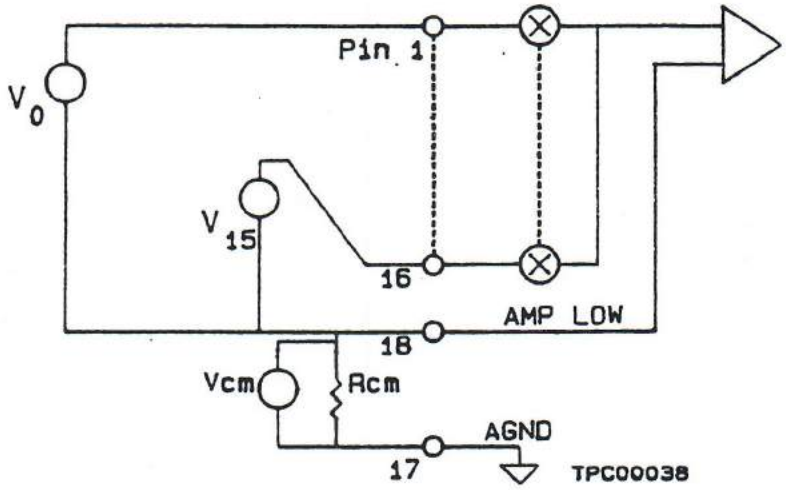
FIGURE 4-4: SINGLE-ENDED INPUT CONNECTION

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4.5.2 PSEUDO-DIFFERENTIAL INPUTS

The pseudo-differential input is a variation of the single-ended input and provides you with some degree of common mode noise rejection without sacrificing the number of input channels. In this mode, the return sides of all input signals are tied to the low side of the instrumentation amplifier (Amp Lo). This is possible because the Amp Lo connection (pin 18, J1) is brought out to the input connector, such as a screw terminal panel. Amp Lo in turn is connected externally to Analog Ground through a 1 to 10kΩ resistor. This type of connection permits the instrumentation amplifier to reject the common mode noise. Since this connection scheme is sensitive to electrical noise just as the single-ended connection, it should be used with lead lengths not exceeding 25 feet (7.6m) and with gains no more than 10. Figure 4-5 shows how to connect the Amp Lo and AGND pin for pseudo-differential operation.

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NOTES:

- All signal inputs must be referenced to Analog Ground.
- All unused analog input channels should be connected to Analog Ground. Failure to do so can result in inaccurate A/D conversions on all other channels, those closest to the floating channel(s) being affected most.
- Rcm is a user-supplied bias return resistor. Its value is typically between 1 and 10 kilohm.

FIGURE 4-5: PSEUDO-DIFFERENTIAL INPUT CONNECTION

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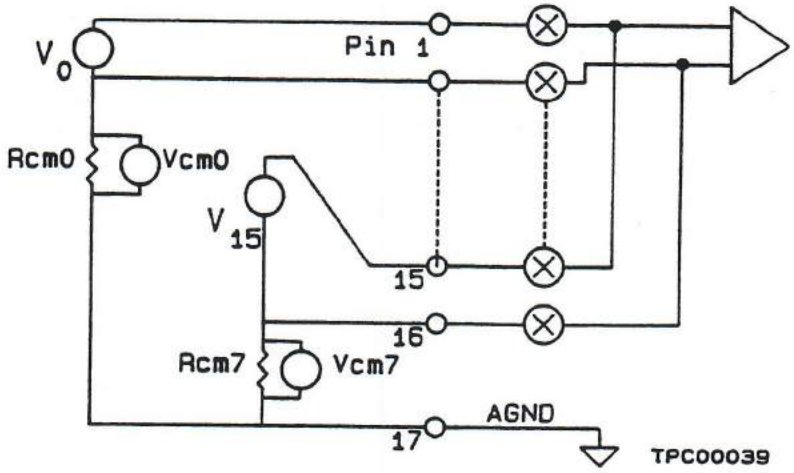
4.5.3 DIFFERENTIAL INPUTS

In a differential input mode, two multiplexer switches are used on each channel. Thus the number of channels which can be accommodated is cut in half. The benefits are that the common mode voltages (voltages common to both the high and low side of an analog input) can be rejected by the differential instrumentation amplifier, resulting in a much quieter system. The differential input configuration can be used with input ranges as low as 20mV full scale with twisted pair (low level) shielded input cables. Lead lengths may suit user requirements but should be kept as short as possible. Figure 4-6 shows the connection scheme for differential inputs.

NOTE

The low end of each differential input must be referenced to Analog Ground. This can be done by connecting a 1 to 10 kilohm resistor between the low end of each differential input and Analog Ground. If all inputs share a common ground, a single 10 kilohm resistor can be connected between the input signal common and the board Analog Ground.

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NOTES:

- All signal inputs must be referenced to Analog Ground.
- All unused analog input channels should be connected to Analog Ground. Failure to do so can result in inaccurate A/D conversions on all other channels, those closest to the floating channel(s) being affected most.
- Rcm 0 through Rcm 7 are user-supplied bias return resistors. Their value is typically between 1 and 10 kilohm.

FIGURE 4-6: DIFFERENTIAL INPUT CONNECTION

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4.6 ANALOG OUTPUT CONNECTION

The analog outputs of the DACs are present on pins 22 through 25 of the J1 connector. The output signals can be brought out to screw terminals when a compatible screw terminal panel is connected to the DT2811.

4.7 CONNECTION GUIDELINES

To optimize the performance of a system, certain guidelines must be considered in connecting analog signals to the A/D board. Following the guidelines and observing some precautions minimize the pickup of electrical noise.

4.7.1 TWISTED PAIR INPUT LINES

The effects of magnetic coupling on the input signals can be reduced in differential input schemes by twisting the input lines of the signal. This is effective since the induced voltages on the two lines are of opposite polarity and tend to match, canceling out any common voltage. This cable type should not be used with single-ended inputs.

4.7.2 SHIELDED INPUT LINES

The effects of electrostatic coupling can be reduced by shielding the input lines. This becomes important if the source has a high impedance. The shield should only be tied to ground at the instrument end, preventing ground loop currents.

4.7.3 INPUT SETTLING WITH HIGH SOURCE IMPEDANCE

Solid state multiplexers inject a small amount of charge into the input lines when channels are switched. This can cause a transient error due to the input source impedance time constants. All Data Translation A/D boards allow for input settling upon new channel selection. The settling time varies for the different systems available and is controlled by the board.

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4.8 INSTALLATION

The DT2811 can operate in any expansion slot on the IBM PC/XT/AT or compatible backplane. Follow the procedure recommended in your system manual for the installation of the DT2811.

NOTE

The DT2811 does not function if placed in the J8 slot of the IBM PC/XT. The reason is that pin B8 on slot J8 of the IBM PC/XT backplane requires the bus signal -CARDSLCT, whereas on all other slots, pin B8 is "reserved". This restriction also applies to all compatibles.

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CHAPTER 5

ARCHITECTURE

5.1 INTRODUCTION

This chapter describes the architecture and operation of the three subsystems on the DT2811. The block diagram of Figure 5-1 highlights the major functions of the board elements and shows how they are interrelated and interfaced to the IBM PC bus. The diagram should help you throughout the discussions in this chapter.

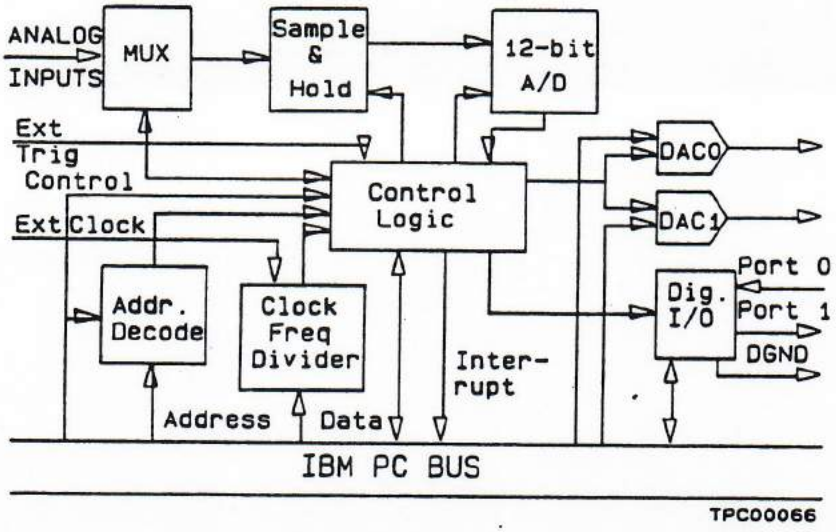


FIGURE 5-1: DT2811 BLOCK DIAGRAM

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5.2 REGISTERS

The DT2811 performs all its operations--A/D conversion, D/A conversion, and digital I/O transfers--by means of eight registers which form the main elements of its architecture. Each register occupies a unique address in the I/O space of the computer system. The address of a register is assigned relative to a base address which is selectable within a specified range as discussed in Chapter 3. Note that only the base address is selectable. The relative address of each register is fixed and the address bits that select a specific register are decoded by the on-board interface logic. Table 5-1 lists all the registers of the DT2811 and indicates the relative address and accessibility of each register. All registers are byte-operable.

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TABLE 5-1: DT2811 REGISTERS

REGISTER NAME	ADDRESS	ACCESS
A/D Control/Status (ADCSR)	Base + 0	Read/Write
A/D Gain/Channel (ADGCR)	Base + 1	Read/Write
A/D and DAC0 Data Low Byte (ADDAT/DADAT0)	Base + 2	Read/Write
A/D and DAC0 Data High Byte (ADDAT/DADAT0)	Base + 3	Read/Write
DAC1 Data Low Byte (DADAT1)	Base + 4	Write
DAC1 Data High Byte (DADAT1)	Base + 5	Write
DIO Port0/DIO Port1 (DIOP1/DIOP2)	Base + 6	Read/Write
Timer/Counter (TMRCTR)	Base + 7	Read/Write

NOTE:

- The terms enclosed in parentheses are the mnemonics of the registers.

Descriptions of the DT2811 registers and the functions they perform follows.

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5.2.1 A/D CONTROL/STATUS REGISTER (ADCSR)

Address: Base + 0
Access: Read/Write

The A/D Control/Status Register (ADCSR) is a read/write register which controls the operation of the A/D subsystem. The ADCSR also contains status information on the current A/D conversion. The bit functions of the ADCSR are shown in Figure 5-2 and described in detail subsequently. Mnemonics used to refer to individual bits are given in parentheses.

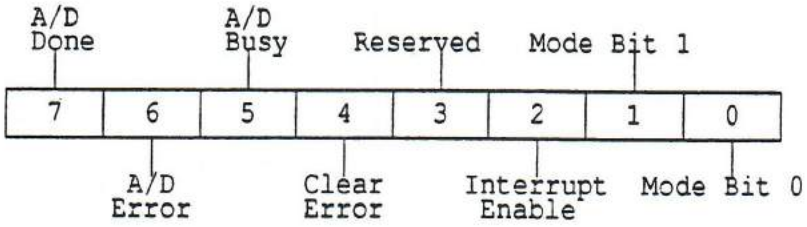


FIGURE 5-2: A/D CONTROL/STATUS REGISTER

BIT FUNCTIONS

BIT 7 - A/D Done, Read
This flag is set by the A/D converter to indicate the completion of an A/D conversion. An interrupt is generated when this bit is set if interrupts are enabled (bit 2 of the ADCSR set). This bit is cleared by a read of the ADDAT/DADAT0 (high byte) and on initialization.

BIT 6 - A/D Error, Read
This flag is set when an error condition occurs during an A/D conversion operation. The error condition results from the following two causes:
1. Completion of the current conversion while data from the previous conversion is not completely read (ADDATA/DADAT0 high byte not read). This is a data overflow error.

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2. An attempt to initiate a new conversion while the current conversion is in process. This is a trigger error.

An interrupt is generated when this bit is set if interrupts are enabled (bit 2 of the ADCSR set). This bit is cleared by writing a 1 to bit 4 of the ADCSR. It is also cleared on initialization.

BIT 5 - A/D Busy, Read
This bit is set by an A/D trigger to indicate that a conversion operation is in progress. It is cleared at the end of the conversion. Any trigger while this bit is set will cause an error condition.

BIT 4 - Clear Error, Write
Writing a 1 to this bit clears A/D ERR (bit 6 of ADCSR). This bit reads as 0.

BIT 3 - Reserved
This bit is not used. It reads back as zero and writes to it are ignored.

BIT 2 - Interrupt Enable, Read/Write
When set, this bit enables both A/D Done and A/D Error interrupts. Clearing this bit disables all interrupts. This bit is controlled by the program.

BIT 1 - Mode Bit 1, Read/Write
See Bit 0, Mode 0.

BIT 0 - Mode Bit 0, Read/Write
Mode bits 1 and 0 control the four operational modes of the A/D conversion subsystem as shown in Table 5-2.

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TABLE 5-2: A/D OPERATIONAL MODES

MODE	BIT 1	BIT 0	FUNCTION
0	0	0	Single conversion on ADGCR load
1	0	1	Continuous conversion, internal clock. Clk enabled on ADGCR load
2	1	0	Continuous conversion, internal clock, external trigger
3	1	1	Continuous conversion, external oscillator, external trigger

See Chapter 6 for a more detailed discussion of the operating modes.

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5.2.2 A/D GAIN/CHANNEL REGISTER

Address: Base + 1
Access: Read/Write

The A/D Gain/Channel Register (ADGCR) is a read/write register which controls the gain of the instrumentation amplifier (gain of input signal to the A/D subsystem) and the selection of the MUX input channel. For single-channel operations (Mode 0; see Section 6.3), this register should be loaded with the selected gain and channel number for each conversion. If repetitive conversions are desired on a selected channel with no change in the gain (Mode 1, 2, or 3; see Section 6.3), this register need be loaded only once. The bit functions of the ADGCR are shown in Figure 5-3.

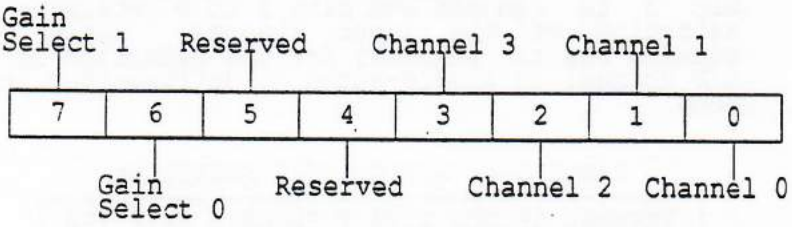


FIGURE 5-3: A/D GAIN/CHANNEL REGISTER

BIT FUNCTIONS

BIT 7 - Gain Select 1, Read/Write
See bit 6, Gain Select 0.

BIT 6 - Gain Select 0, Read/Write
Bits 7 and 6 select the gain of the instrumentation amplifier. The configuration of these bits for the four possible gains are given in Table 5-3.

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TABLE 5-3: AMPLIFIER GAIN

GS1 (BIT 7)	GS0 (BIT 6)	GAIN PGH	GAIN PGL
0	0	1	1
0	1	2	10
1	0	4	100
1	1	8	500

BIT 5 - Reserved
Reads as 0. Writes to this bit are ignored.

BIT 4 - Reserved
Reads as 0. Writes to this bit are ignored.

BITS 3 to 0 - Channel Select
This bit field specifies the input channel for the current A/D conversion. Bits 3 to 0 are used for the selection of the channel in the single-ended or pseudo-differential input mode. If the board is jumpered for differential inputs, bit 3 is ignored and bits 2 to 0 determine the selection of the input channel. Table 5-4 details the bit settings for the selection of the A/D channel in single-ended or differential input mode.

TABLE 5-4: A/D CHANNEL SELECTION

CHANNEL SELECT BITS 3	2	1	0	CHANNEL SELECTED SE	DI
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	0
1	0	0	1	9	1
1	0	1	0	10	2
1	0	1	1	11	3
1	1	0	0	12	4
1	1	0	1	13	5
1	1	1	0	14	6
1	1	1	1	15	7

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5.2.3 A/D AND DAC0 DATA REGISTER (LOW BYTE)

Address: Base + 2
Access: Read/Write

The A/D and DAC0 Data Register (ADDAT/DADAT0) low byte is a read/write register which contains the low byte of the A/D converted data or the low byte of the digital code to be converted into an analog signal by DAC0. In an A/D operation, this register is loaded with digital data by the A/D converter module at the end of the conversion. The user performs a read operation to this register to retrieve converted data. In a D/A operation, this register is loaded by the user software with digital code for D/A conversion. The bit functions of the ADDAT/DADAT0 (low byte) are shown in Figure 5-4 and are described subsequently. Bit 0 is the least significant bit (LSB).

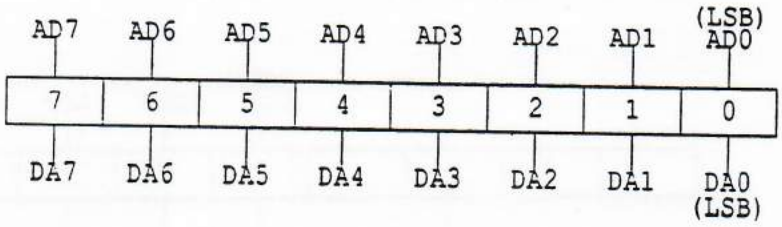


FIGURE 5-4: A/D AND DAC0 DATA REGISTER (LOW BYTE)

BIT FUNCTIONS

BITS 7-0 - A/D data (AD) and DAC0 data (DA)
These bits form the low byte of the 12-bit data resulting from an A/D conversion, or the low byte of the 12-bit code loaded by software into DAC0 for D/A conversion.

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5.2.4 A/D AND DAC0 DATA REGISTER (HIGH BYTE)

Address: Base + 3
Access: Read/Write

The A/D and DAC0 Data Register (ADDAT/DADAT0) high byte contains the high byte of the A/D converted data or the high byte of the digital code to be converted into an analog signal by DAC0. In an A/D operation, this register is loaded with digital data by the A/D converter module at the end of the conversion. The user software performs a read operation to this register to retrieve converted data. This read clears A/D Done (ADCSR bit 7). In a D/A operation, writing to this register causes a D/A conversion to begin on DAC0. The bit functions of the ADDAT/DADAT0 (high byte) are shown in Figure 5-5 and are described subsequently. Data is right-justified and bit 3 (AD11 or DA11) is the most significant bit (MSB).

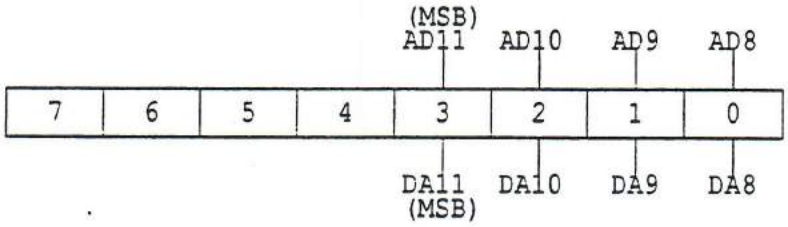


FIGURE 5-5: A/D AND DAC0 DATA REGISTER (HIGH BYTE)

BIT FUNCTIONS

BITS 7-4 - Not used.

BITS 3-0 - A/D data (AD) and DAC0 data (DA)
These are the four higher bits of the 12-bit data resulting from an A/D conversion, or the four higher bits of the 12-bit code loaded by the software into DAC0 for D/A conversion.

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