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User Manual

for

DTX350

DTX350 iSBX-COMPATIBLE

DIGITAL INPUT/OUTPUT MODULE

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PREFACE

The DTX350 module is a board option designed to interface with an iSBX connector on a host board or microcomputer. All references to the "host" will be considered to refer to these.

This manual discusses the hardware reference information for the DTX350 iSBX-compatible DIO module. It is divided into the following sections:

Chapter 1 INTRODUCTION
This chapter describes the DTX350 DIO Module's functional operation, its specifications and a list of compatible accessory products.

Chapter 2 PREPARATION FOR USE
This chapter describes procedures to inspect the packaged DTX350 for shipping damage, unpack it and install it. Jumper configuration information and connector assignments are also provided.

Chapter 3 PROGRAMMING INFORMATION
This chapter describes the programming of the DTX350 module, including the 8255A-5 Programmable Peripheral Interface, its port/register definitions, addressing, control word format, initialization, and operation.

Chapter 4 PRINCIPLES OF OPERATION
This chapter describes the principles of operation, including interfaces to the DTX350, and the interrupt system.

Chapter 5 SERVICE INFORMATION
This chapter discusses service and repair information for the DTX350.

Appendix A DTX350 DIAGRAMS
This appendix contains the DTX350 assembly drawing and the schematic diagram associated with this module.

Appendix B 8255A-5 PPI SPECIFICATIONS
This appendix contains the Intel data sheet for the 8255A-5 Programmable Peripheral Interface as found in the 1984 Volume II of the Intel Microsystem Components Handbook, copyright 1983.

Appendix C SAMPLE PROGRAMS
This appendix contains DTX350 sample programs.

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The DTX350 Digital Input/Output (DIO) module is an iSBX-compatible expansion interface board which connects at one end to an iSBX connector, (usually on a host board or microcomputer) and at the other end to a user interface, providing the user with three 8-bit parallel interface ports for complete bidirectional data transfer. This manual contains a general description of the module and its use, as well as programming and operational information.

1.2 GENERAL DESCRIPTION

The DTX350 module is a 3 5/8 inch by 2 1/2 inch board which contains two resident 8226 bidirectional bus driver devices (transceivers) in sockets for external interface, and permits expansion of any host board (or microcomputer) with iSBX connectors by the addition of twenty-four programmable parallel I/O lines. The additional I/O lines can be configured using the system software and the transceivers on the DTX350 module. Also contained on the DTX350 is an 8255A-5 Programmable Peripheral Interface (PPI). Its operation is discussed in detail in Chapter 3.

The DTX350 module is compatible with any device that meets iSBX bus standards, including iSBX microcomputers, the Data Translation DT2806 Multi-Function Output board, and the DT901 Series BITBUS Slave Remote Acquisition boards.

1.3 FUNCTIONAL DESCRIPTION

The DTX350 has the following features:

- o iSBX-compatible I/O expansion
- o Twenty-four programmable I/O lines with sockets for interchangeable line drivers
- o Three jumper-selectable interrupt request sources
- o Capability to be accessed as I/O port locations (registers)
- o A single +5V low power requirement
- o iSBX bus on-board expansion which eliminates system bus latency and increases system throughput.

The DTX350 Digital I/O module is a member of Data Translation's line of iSBX-compatible interface modules, and plugs into any iSBX-compatible host board offering incremental on-board expansion. The iSBX module is closely coupled to the host board through the iSBX connector. As such, it offers maximum on-board performance, and frees the host system traffic for other system resources. In addition, power dissipation is minimal, requiring only 1.6 watts in the factory configuration.

1.3.1 PROGRAMMABLE INTERFACE

The Intel 8255A-5 is a general purpose Programmable Peripheral Interface (PPI), that provides twenty-four parallel I/O lines on the DTX350. The host board system software is used to configure the I/O lines in many combinations of unidirectional input/output and transceiver registers.

In order to take full advantage of all possible I/O configurations, sockets are provided for interchangeable I/O line drivers. In this way, the flexibility of the I/O interface is enhanced by selecting the appropriate combination of optional line drivers to provide the required source current and driver characteristics for each application (see Table 1-2).

In addition, inverting transceivers (8226) are provided in sockets to allow for convenient user replacement (optional) to non-inverting drivers (8216). The twenty-four programmable I/O lines, signal ground, and +5 volt power (jumper-configurable) run to a 50-pin edge connector (J1) that mates with flat (EP036) or twisted pair (EP086) cable.

1.3.2 INTERRUPT REQUEST GENERATION

Interrupt requests can originate from three jumper-selectable sources. Two interrupt requests can be automatically generated by the PPI when a byte of information is ready to be transferred to the host CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). A third interrupt source can originate directly from the user I/O interface (J1 connector). Interrupt control functions are discussed in detail in Chapter 4.

Figure 1-1 shows a block diagram of the DTX350 DIO module.

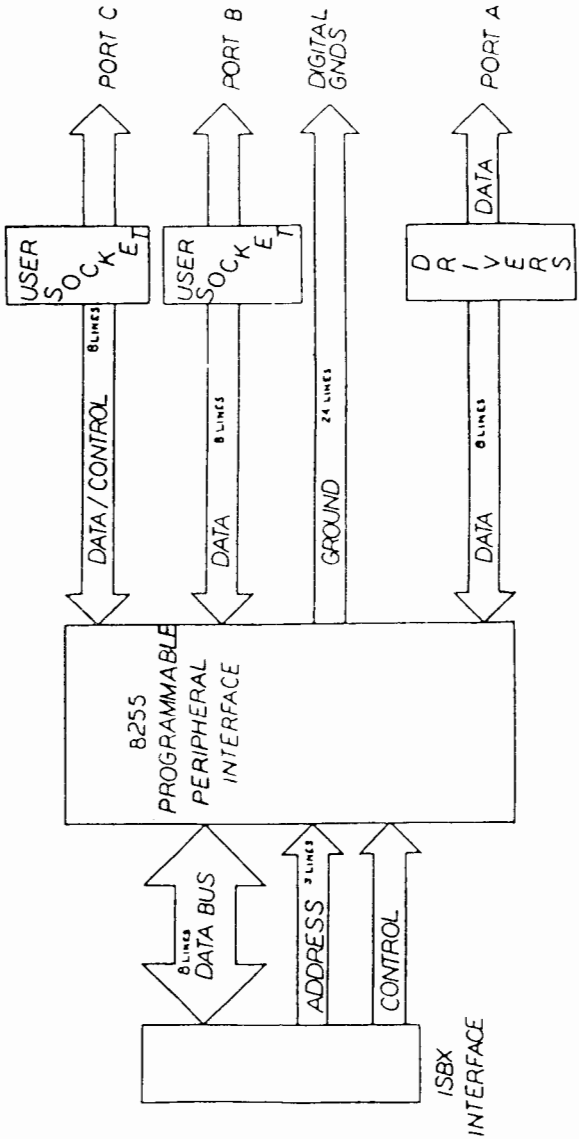


FIGURE 1-1: DTX350 DIGITAL I/O MODULE BLOCK DIAGRAM

1.4 SPECIFICATIONS

This section gives the physical, electrical, environmental, and performance specifications for the DTX350, typical at +25° C. and standard power, unless otherwise specified.

1.4.1 PHYSICAL SPECIFICATIONS

Length	3.7 in (9.4 cm)
Width	2.9 in (7.2 cm)
Height (alone - see Figure 1-2)	.8 in. (2.0 cm)
Height (installed - see Figure 1-3)	1.1 in. (2.8 cm)
Weight	1.8 oz. (51 gm)

1.4.2 ELECTRICAL SPECIFICATIONS

Sockets U1, U2 shipped with 8226s	+5V ±10% at 320 mA

1.4.3 ENVIRONMENTAL SPECIFICATIONS

Storage Temperature	+9° to +185° F (-25° to +85° C)
Operating Temperature	+32° to +131° F (0° to +55° C)
Operating Humidity	0 to 90% (non-condensing)

1.4.4 PERFORMANCE SPECIFICATIONS

Word Size	Data - 8 bits
I/O Capacity	24 programmable lines
Access Time*	
Read	250 nanoseconds max.
Write	300 nanoseconds max.

* Actual transfer speed is dependent upon the cycle time of the host microcomputer.

Interrupts

Interrupt requests may originate from the programmable peripheral interface (2) or the user-specified I/O (1).

1.4.5 INTERFACE COMPATIBILITY

iSBX Bus and Parallel I/O

Logic Family/Logic Load	1 TTL Load
Output Pull-Up Resistors (Port A)	1 kilohm
Data Throughput	1 MHz
Fanout	See Tables 1-1 and 1-2
Threshold Voltages	See Table 1-1
Logic Sense/Level**	
Read/Write	Negative edge sensitive
Enable	Negative level sensitive
Reset	Positive level sensitive
Data and Address	Positive level logic

** Additional information in Appendix B.

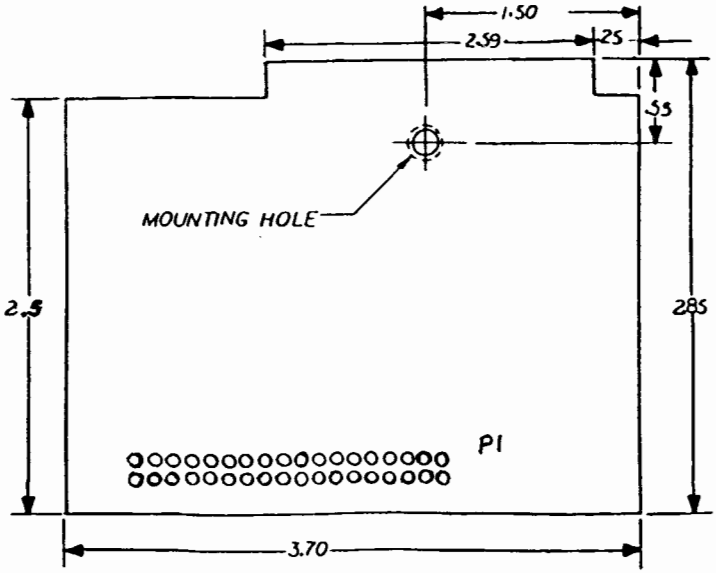


FIGURE 1-2: DTX350 MODULE DIMENSIONS (inches)
(SOLDER SIDE)

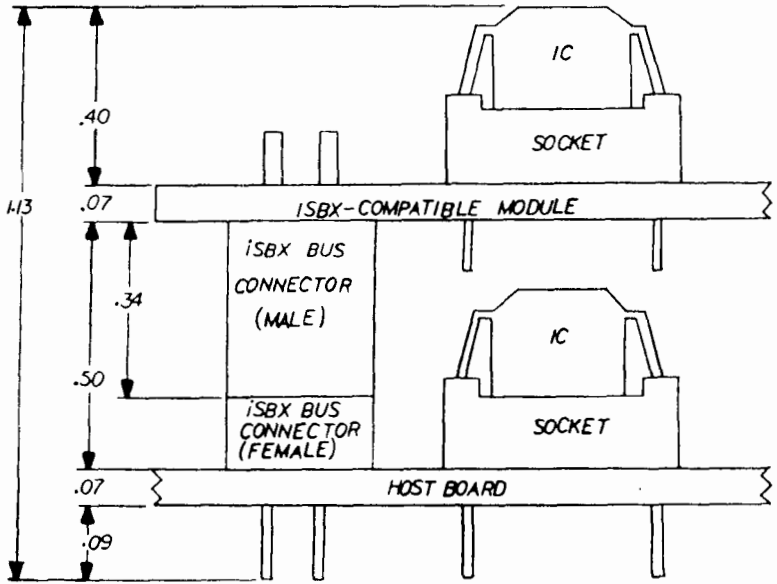


FIGURE 1-3: DTX350 MODULE AND HOST BOARD MOUNTING CLEARANCES (inches)

TABLE 1-1: DC CHARACTERISTICS AT J1 CONNECTOR

OUTPUT SIGNAL	DRIVER TYPE	Iol MAX	Vol MAX (Iol=MAX)	Ioh MAX	Voh MIN (Ioh=MAX)	C0 MIN (pF)
Port A	TTL	20mA	0.45	-10mA	2.4	18
INPUT SIGNAL	REC-EIVER TYPE	Iil MAX (Vil=.45)	Vil MAX	Iih MAX (Vih=2.4	Vih MIN	C1 MAX (pF)
Port A 1k Pull-up	TTL*	-5.2mA	0.80	-2.2mA	2.0	18
Ports B & C:	TTL	-5.0mA	0.80	-2.2mA	2.0	20

* Refers to standard Totem Pole output. (See Table 1-2 for Ports B & C output characteristics.) If header dips with one-to-one signal jumpers are used instead of drivers, the characteristics of the 8255A-5 apply (see Chapter 2, Line Drivers). Capacitance values are approximations.

The following abbreviations are used to define the threshold levels in Table 1-1:

Iol	Current Output Low	Ioh	Current Output High
Iil	Current Input Low	Iih	Current Input High
Vol	Voltage Output Low	Voh	Voltage Output High
Vil	Voltage Input Low	Vih	Voltage Input High

For additional information, see Appendix B.

NOTE

Timing characteristics of user-installed chips in sockets U1 through U6 must be compatible with those of the 8255A-5 PPI. See the 8255A-5 specifications in Appendix B.

Parallel Interface

Twenty-four programmable lines with eight lines per port; one port includes a bidirectional bus driver. Dip sockets are included for user-installed line buffers/drivers, if required.

System Bus Compatible with iSBX bus standards.

Line Drivers

The I/O line drivers shown in Table 1-2 are all compatible with the I/O driver sockets on the DTX350.

TABLE 1-2: LINE DRIVERS

DRIVER	SOURCE CURRENT (mA) Iol	Ioh	SUPPLY CURRENT (mA)	STANDARD TTL FANOUT* Icc (mA) Max.
7438	-48	-	54	30
7437	-48	1.2	54	30
7432	-16	0.8	38	10
7426	-16	-	22	10
7409	-16	-	33	10
7408	-16	0.8	33	10
7403	-16	-	22	10
7400	-16	0.4	22	10

Note: The following abbreviations are used in Table 1-2:

Iol specified for Vol = 0.4 volt
Ioh specified for Voh = 2.4 volt.
*Iil assumed to be TTL 1.6 mA.
Icc is supply current required from +5V.

Port A has 25 mA Totem Pole drivers and 1k ohm terminators.

1.5 ACCESSORY PRODUCTS

The following subsections briefly describe the Data Translation products which can be used in association with the DTX350. Table 1-3 lists the product numbers to use when ordering these accessory products.

1.5.1 DT2806 Multi-Function Output Subsystem

The DT2806 is an iSBX interface board for use with IBM and IBM-compatible PCs. It has three counter/timers and three iSBX connectors.

1.5.2 DT901 BITBUS Slave Remote Acquisition Board

The DT901 is a BITBUS intelligent remote node with four iSBX connectors.

1.5.3 DT901I Isolated BITBUS Slave Remote Acquisition Board

The DT901I is the same as the DT901, with isolation up to 1500V.

1.5.4 DT708 Screw Terminal Panel

The DT708 Screw Terminal Panel was designed for use with the DTX350 module to permit the user connector (J1) to be mated to barrier screw terminals. The DT708 contains two 50-pin connectors, one 20-pin connector, and can support up to two DTX350's. An EP036, EP086 or equivalent cable assembly is required to connect to the DTX350.

1.5.5 CABLES

Two types of 8-foot cables can be used with the DTX350 module: the EP036 flat cable and the EP086 twisted pair cable.

TABLE 1-3: PRODUCT ORDER NUMBERS

PART NUMBER	DESCRIPTION
DTX350	Digital Input/Output Module
DT2806	Multi-function Output Subsystem
DT901	BITBUS Slave Remote Acquisition Board
DT901I	Isolated BITBUS Slave Remote Acquisition Board
DT708	Screw Terminal Panel
EP036 Cable	Flat Cable
EP086 Cable	Twisted Pair Cable

CHAPTER 2

PREPARATION FOR USE

2.1 INTRODUCTION

This chapter provides information necessary for the user to inspect, unpack, configure, and install the DTX350 Digital I/O module. The following subsections discuss:

- o Inspection and unpacking
- o Operating environment, including power and ventilation requirements
- o Connector configuration
- o Jumper configurations
- o Line drivers
- o Installation information and procedures.

2.2 INSPECTION AND UNPACKING

The following subsections cover inspection for shipping damage and unpacking instructions for the DTX350 Digital I/O module.

2.2.1 INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If any damage is discovered, proceed as follows:

1. Observe standard static electricity precautions when handling boards or components, as follows:

PREPARATION FOR USE

A. While placing one hand firmly on a metal portion of the system chassis, pick up the shrink-wrapped item.

B. After allowing a moment for the discharge of any static electricity into the computer chassis, carefully remove the wrapping from the module.

C. Examine the item for the extent of shipping damage.

2. Do NOT perform any repair or installation of the damaged item prior to an insurance claim inspection.

3. Retain all packing material for future use.

4. If the delivering carrier's agent is not present when the carton is opened and the contents of the carton are damaged, set the carton and packing material aside for the agent's inspection.

5. Have the agent inspect the damage and arrive at an agreement to repair or replace the damaged item.

6. If the item is to be repaired, call or write:

Customer Service Department
Data Translation, Inc.
100 Locke Drive
Marlboro, MA 01752
(617) 481-3700

7. Call and request a Return Material Authorization (RMA) number. This must be obtained before any item will be accepted for return.

NOTE

If the item is not wrapped in anti-static (electrically conductive) packaging, ensure that it is handled with ground protection. Static electricity is potentially damaging to electrical components on Data Translation products.

8. Return the damaged item, with the RMA number, to the address in step 6.

2.2.2 UNPACKING INSTRUCTIONS

The DTX350 module is packaged shrink-wrapped on a piece of heavy cardboard and placed in the shipping carton on a piece of half-inch foam. Any installation hardware is included, packaged in a sealed plastic envelope. Loose styrofoam is then used to fill the remainder of the carton before sealing. To unpack the DTX350 module, proceed as follows:

1. If exterior damage was noted, refer to section 2.2.1, Inspection.

2. If no exterior damage is found and there is no reason to suspect shipping damage to the packaged item, place the container on a stable surface and cut the shipping tape.

3. Grasp the front of the flat carton underneath and lift forward and up to open the top (see Figure 2-1).

4. Remove the module(s) and hardware (if any) from the packing and retain the carton and packing material for future use.

5. Verify that all items listed on the packing slip are accounted for.

6. Observe the grounding procedures covered in the Inspection section in this chapter, and remove the module from its plastic wrapping.

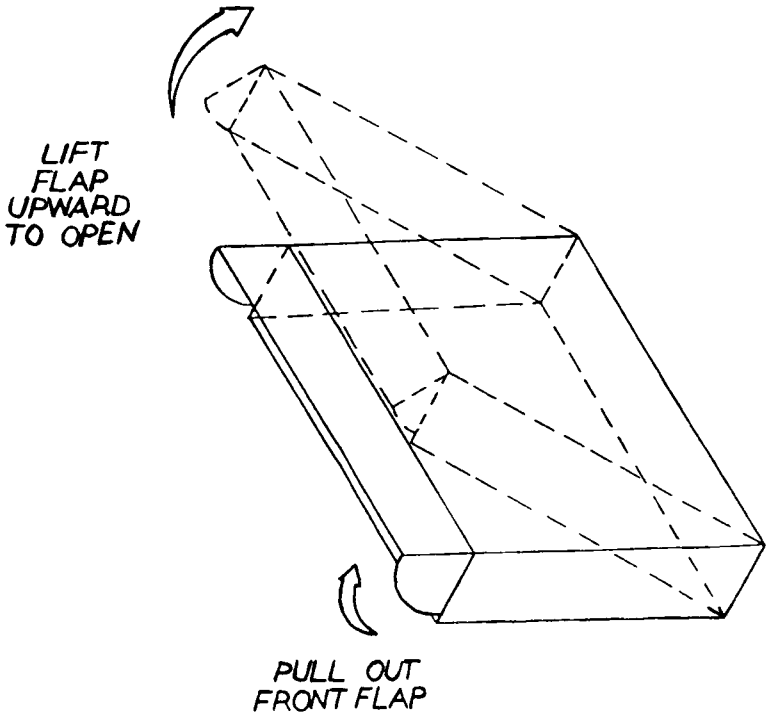


FIGURE 2-1: OPENING THE MODULE CARTON

2.3 OPERATING ENVIRONMENT

Operating environment information for the DTX350 DIO module, such as power and ventilation, are discussed in the following subsections:

2.3.1 POWER REQUIREMENTS

The power requirements for the DTX350 vary, depending on the configuration of the module:

- The DTX350, with no user-installed drivers (sockets U3 through U6 empty), requires +5V (±0.25V) at 320 mA (maximum).
- With user-installed drivers in sockets U3 through U6, the DTX350 requires additional supply current. Table 1-2 gives current requirements of typical drivers.

All power for the module is derived from the iSBX host and drawn through the iSBX connector (P1) on the module.

2.3.2 VENTILATION REQUIREMENTS

The DTX350 DIO dissipates 44.1 gram-calories/minute (0.18 BTU/minute) and adequate air circulation is required to prevent a temperature rise above 131 degrees F (55 degrees C).

2.4 CONNECTOR CONFIGURATION

Connector P1 is a 36-pin iSBX connector which carries all the data and control signals between the host and the DTX350. The DTX350 module can mount directly on the P1 connector. The signals found on each pin of the P1 connector are listed in Table 2-1. Signal descriptions may be found in Chapter 4.

Connector J1 on the DTX350 provides user connections to the module. The pins of the J1 connector are identified in Table 2-2. All odd-numbered pins are Ground; even-numbered pins represent connections to bits 0-7 for each of the ports A, B, and C. Also shown in the table are the socket and pin numbers associated with the port and bit.

NOTE

The J1 connector pins are non-standard to usual industry configurations. Information pertaining to mating cable connectors (such as Fujitsu FCN767J050-AU) and their pin-to-pin compatibility to the J1 connector is given in Table 2-3.

TABLE 2-1: CONNECTOR P1 PIN ASSIGNMENTS

PIN	MNEMONIC	DESCRIPTION
1	+12V	+12 Volts
2	-12V	-12 Volts
3	AGND	Signal Ground
4	+5V	+5 Volts
5	RESET	ResetH
6	CLK	Expansion Module Clock
7	AB2	Address 2
8	MPSTL	Module Present
9	AB1	Address 1
10	-	Reserved
11	AB0	Address 0
12	INTR1H	Interrupt 1
13	WRITEL	IO Write Command
14	INTR0H	Interrupt 0
15	READL	IO Read Command
16	WAITL	Expansion Module Wait
17	DGND	Signal Ground
18	+5V	+5 Volts
19	DB7	Data Bit 7
20	CS1L	Chip Select 1
21	DB6	Data Bit 6
22	CS0L	Chip Select 0
23	DB5	Data Bit 5
24	-	Reserved
25	DB4	Data Bit 4
26	TDMA	Terminate DMA
27	DB3	Data Bit 3
28	OPT1	Option 1
29	DB2	Data Bit 2
30	OPT0	Option 0
31	DB1	Data Bit 1
32	DACKL	DMA Acknowledge
33	DB0	Data Bit 0
34	DRQTH	DMA Request
35	DGND	Signal Ground
36	+5V	+5 Volts

TABLE 2-2: CONNECTOR J1 PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL	SOCKET	PIN
1	GROUND	2	PORT B - BIT 7 -->	U6	3
3	GROUND	4	PORT B - BIT 6 -->	U6	6
5	GROUND	6	PORT B - BIT 5 -->	U6	8
7	GROUND	8	PORT B - BIT 4 -->	U6	11
9	GROUND	10	PORT B - BIT 3 -->	U5	3
11	GROUND	12	PORT B - BIT 2 -->	U5	6
13	GROUND	14	PORT B - BIT 1 -->	U5	8
15	GROUND	16	PORT B - BIT 0 -->	U5	11
17	GROUND	18	PORT C - BIT 3 -->	U4	3
19	GROUND	20	PORT C - BIT 2 -->	U4	6
21	GROUND	22	PORT C - BIT 1 -->	U4	8
23	GROUND	24	PORT C - BIT 0 -->	U4	11
25	GROUND	26	PORT C - BIT 4 -->	U3	11
27	GROUND	28	PORT C - BIT 5 -->	U3	8
29	GROUND	30	PORT C - BIT 6 -->	U3	6
31	GROUND	32	PORT C - BIT 7 -->	U3	3
33	GROUND	34	PORT A - BIT 7 -->	U2	3
35	GROUND	36	PORT A - BIT 6 -->	U2	6
37	GROUND	38	PORT A - BIT 5 -->	U2	10
39	GROUND	40	PORT A - BIT 4 -->	U2	13
41	GROUND	42	PORT A - BIT 3 -->	U1	3
43	GROUND	44	PORT A - BIT 2 -->	U1	6
45	GROUND	46	PORT A - BIT 1 -->	U1	10
47	GROUND	48	PORT A - BIT 0 -->	U1	13
49	GROUND	50	OPTION A*		

* +5V or GND or External Interrupt input (refer to CAUTION under Interrupt/Options section 2.5.2).

The Intel connector pin configuration shown in Table 2-3 is not industry-standard. Pin mating to the J1 connector is shown for the user's information.

TABLE 2-3: J1 CONNECTOR/CABLE PIN MATING

CABLE PIN	J1 CONNECTOR PIN	CABLE PIN	J1 CONNECTOR PIN
2	1	1	2
4	3	3	4
6	5	5	6
8	7	7	8
10	9	9	10
12	11	11	12
14	13	13	14
16	15	15	16
18	17	17	18
20	19	19	20
22	21	21	22
24	23	23	24
26	25	25	26
28	27	27	28
30	29	29	30
32	31	31	32
34	33	33	34
36	35	35	36
38	37	37	38
40	39	39	40
42	41	41	42
44	43	43	44
46	45	45	46
48	47	47	48
50	49	49	50

2.5 JUMPER CONFIGURATION

The DTX350 iSBX-compatible module contains twenty-six wirewrap posts (E1 through E26). These jumper posts may be user-configured to provide the flexibility needed to support all three modes of operation of the Programmable Peripheral Interface. Figure 2-2 shows the jumper posts and their electrical connections. Refer also to the schematic diagram in Appendix A.

The following is a list of the different jumper types:

- Port Enable jumpers
- Interrupt and Option jumpers
- Driver Control jumpers

The jumper posts of the DTX350 are on the component side of the board parallel to the Data Translation logo on the upper left corner of the module. They consist of 13 rows of pins, with each pin labeled from left to right and top to bottom, E1 and E2, E3 and E4, etc. (see Figure 2-2). Standard jumper plugs may be used for parallel-pair jumpering. If the posts to be jumpered are not parallel, the jumpers must be wire-wrapped in place. Use Table 2-4 to obtain the jumper function information for the correct operational mode and module configuration. Modes are defined in Chapter 3, section 3.3.1.

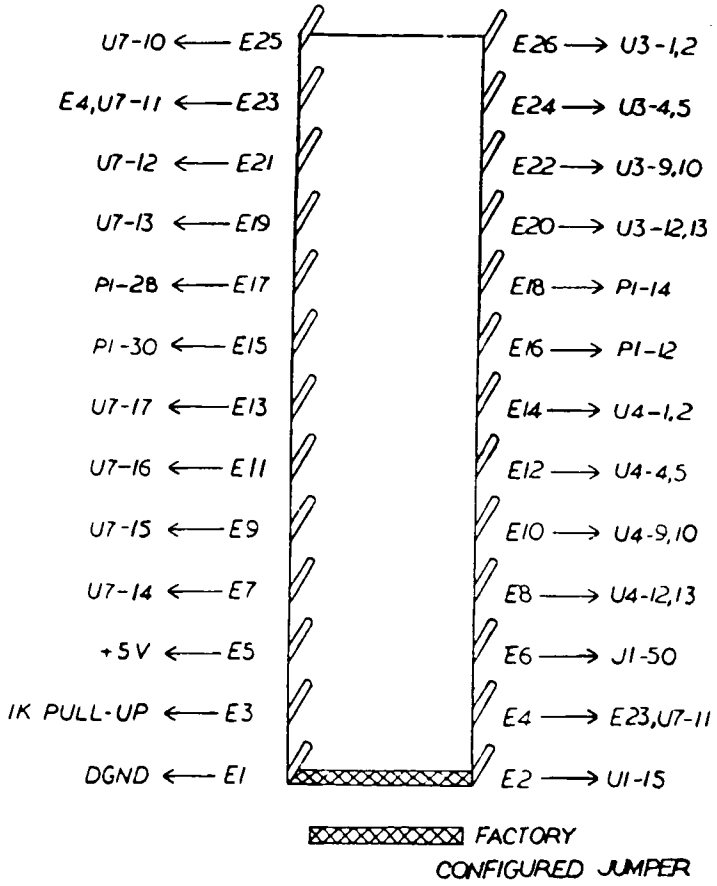


FIGURE 2-2: JUMPER POST MATRIX ON DTX350 MODULE

TABLE 2-4: DTX350 PORT CONFIGURATION JUMPERS

PORT	MODE	DRIVERS	DELETE JUMPER	ADD JUMPER	FUNCTION	PORT	RESTRICTION
A	0 INPUT	8226:U1,U2	*E1-E2	E3-E2	8226 = INPUT ENABLED	B C	None: can be in Mode 0 or 1, input or output. None: can be in Mode 0, input or output, unless Port B is in Mode 1.
A	0 OUTPUT (latched)	8226: U1,U2		*E1-E2	8226 = OUTPUT ENABLED	B C	None: can be in Mode 0 or 1, input or output None: can be in Mode 0, input or output, unless Port B is in Mode 1.
A	1 INPUT (strobed)	8226: U1,U2	*E1-E2	E3-E2	8226 = INPUT ENABLED	B	None: can be in Mode 0 or 1, input or output
				E19-E20	Connects J1-26 to STBa/ input	C	None: Port C data register bits perform the following: o Bits - 0,1,2 - Control for Port B, if Port B is in Mode 1 o Bit 3 - Port A Interrupt (PA INTR) to interrupt jumper matrix o Bit 4 - Port A Strobe (STB/) input o Bit 5 - Port A Input Buffer Full (IBF) output o Bits 6,7 - Port C input or output (both must be in the same direction)
			E21-E22 & E13-E14	E21-14	Connects IBFa output to J1-18		
				E13-E16 or E13-E18	Connects INTa output INTR1H Connects INTa output INTR0H		

TABLE 2-4: DTX350 PORT CONFIGURATION JUMPERS (Cont.)

PORT	MODE	DRIVERS	DELETE JUMPER	ADD JUMPER	FUNCTION	PORT	RESTRICTION
A	1 OUTPUT (latched)	8226: U1,U2		*E1-E2	8226= OUTPUT ENABLED	B C	None: can be in Mode 0 or 1, input or output Port B Data Register bits perform the following:
				E23-E24	Connects J1-30 ACKa/ input		o Bits 0,1,2 - Control for Port B if Port B is in Mode 1
			E13-14 &E25-E26	E25-E14	Connects OBFa output to J1-18		o Bit 3 - Port A interrupt (PA INTR) to interrupt jumper matrix
				E13-E16 or E13-E18	Connects INTa output to INTR1H Connects INTa output to INTR0H		o Bits 4,5 - Port C input or output (both must be in the same direction) o Bit 6 - Port A Acknowledge (ACK/) input o Bit 7 - Port A Output Buffer Full (OBF/) output.
A	2 BIDIREC-TIONAL	8226:U1,U2	*E1-E2	E4-E2	Allows ACKa/ input to control 8226 in/out direction	B C	None: can be in Mode 0 or 1, input or output. Port C Data Register bits perform the following:
				E19-E20	Connects J1-26 to STBa/ input		o Bits 0, 1, 2 - can be used for input or output if Port C is in Mode 0
			E7-E8 &E21-E22	E21-E8	Connects IBFa output to J1-24		o Bit 3 - Port A interrupt (PA INTR) to interrupt jumper matrix
				E23-E24	Connects J1-30 to ACKa/ input		o Bit 4 - Port A Strobe (STB/) input
			E13-E14 &E25-E26	E25-E14	Connects OBFa/ output to J1-18		o Bit 5 - Port A Input Buffer Full (IBF) output o Bit 6 - Port A acknowledge (ACK/) input
				E13-E16	Connects INTa output to INTR1H		o Bit 7 - Port A Output Buffer Full (OBF/) output
				E13-E18	Connects INTa output to INTR0H		

TABLE 2-4: DTX350 PORT CONFIGURATION JUMPERS (Cont.)

PORT	MODE	DRIVERS	JUMPER	JUMPER	FUNCTION	PORT	RESTRICTION
B	0 INPUT		None	None		A	None
						C	None: Port C can be in Mode 0, input or output, if Port A is also in Mode 0
B	0 OUTPUT (latched)		None	None		A	None
						C	None: Port C can be in Mode 0, input or output, if Port A is also in Mode 0.
B	1 INPUT (strobed)			E9–E10	Connects IBFb output to J1–22	A	None
						C	Port C data register bits perform the following: o Bit 0 – Port B interrupt (PB INTR) to interrupt jumper matrix o Bit 1 – Port B Input Buffer Full (IBF) output. o Bit 2 – Port B Strobe (STB/) input. o Bits 3,4,5,6,7 – Depend on Port A mode.
			E25–E26 E11–E12 E7–E8	E26–E11	Connects J1–32 STBb/ input.		
				E7–E16 or E7–E16	Connects INTb output to INTR1H Connects INTb output to INTR0H		

TABLE 2-4: DTX350 PORT CONFIGURATION JUMPERS (Cont.)

PORT	MODE	DRIVERS	DELETE JUMPER	ADD JUMPER	FUNCTION	PORT	RESTRICTION
B	1 OUTPUT (latched)			E9-E10	Connects OBFb/ output to J1-22	A	None
			E11-E12 &E25-E26	E11-E26	Connects J1-32 to ACKb/ input	C	Port C data register bits perform the following: o Bit 0 - Port B interrupt (PB INTR) to Interrupt Jumper Matrix o Bit 1 - Port B Output Buffer Full (OBF/) output o Bit 2 - Port B acknowledge (ACK/) input o Bits 3,4,5,6,7 - Depends on Port A mode
			E7-E8	E7-E16 or E7-E18	Connects INTb output to INTR1H Connects INTb output to INTR1H		
C (upper)	0 INPUT		None	E19-E20	Connects bit 4 to J1-26	A	Port A must be in Mode 0 for all four bits to be available
				E21-E22	Connects bit 5 to J1-28	B	Port B must be in Mode 0 for all four bits to be available
				E23-E24	Connects bit 6 to J1-30		
				E25-E26	Connects bit 7 to J1-32		

TABLE 2-4: DTX350 PORT CONFIGURATION JUMPERS (Cont.)

PORT	MODE	DRIVERS	DELETE JUMPER	ADD JUMPER	FUNCTION	PORT	RESTRICTION
C (lower)	0	INPUT	None	E7-E8	Connects bit 0 to J1-24	A	Port A must be in Mode 0 for all four bits to be available
				E9-E10	Connects bit 1 to J1-22	B	Port B must be in Mode 0 for all four bits to be available
				E11-E12	Connects bit 2 to J1-20		
				E13-E14	Connects bit 3 to J1-18		
B (upper)	0	OUTPUT (latched)	None		Same as for Port C (upper) Mode 0 input	A	Same as for Port C (upper) Mode 0 input
B (lower)	0	OUTPUT (latched)	None		Same as for Port C (lower) Mode 0 input	C	Same as for Port C (lower) Mode 0 input.

*Default jumper connected at the factory.

2.5.1 PORT ENABLES

Each of the Port C I/O lines contains enable/disable jumper options (E7-E14 for Bits 0-3 and E19-E26 for Bits 4-7). Additional jumpers (E15-E18) provide the capability to input or output four other signals (INTR0H, INTR1H, OPT0, OPT1) via Port C; thus the user can buffer these signals to the interface (see schematic diagram in Appendix A).

2.5.2 INTERRUPT/OPTIONS

E6 provides a convenient method to send the INTR0H, INTR1H, OPT0, or OPT1 signal to pin 50 of the J1 connector. E6 may also be jumpered to +5 volts or Ground when the application dictates (refer to schematic diagram in Appendix A).

CAUTION

If E6 is wired to +5V, ensure that the connector is properly installed on J1; the +5V signal must always interface to pin 50 of J1. Failure to comply with these guidelines could result in damage to the driver devices in U1 through U6.

2.5.3 DRIVER CONTROL

E2 provides direction control for the bidirectional bus drivers, and may be jumpered to E1 (GND) or any of the Port C control lines.

In Mode 0, Port C transfers data to or from a peripheral device. In Mode 1 or 2, Port C generates or accepts "handshaking" signals to or from the peripheral device. Reading the contents of Port C allows testing or verification of the status of each peripheral device, and permits the program flow to be changed accordingly. For more detail, refer to the 8255A-5 specifications in Appendix B.

2.6 LINE DRIVERS

All twenty-four I/O lines on the DTX350 module can be buffered with drivers at sockets U1, U2, U3, U4, U5, and U6 on the module. The twenty-four I/O lines may be divided into three groups of eight. The group labeled Port A is connected to the socketed 8226 transceivers. Unlike Ports B and C, Port A may be used in the "as-shipped" configuration with no additional components; however, all sockets (U1 through U6) must have either a chip or header dip

inserted in them if signals are intended to pass through the sockets to connector J1 as shown on the schematic (see Figure 2-3). If other configurations of the header dip are required, use the schematic to determine where the user-connections will be needed.

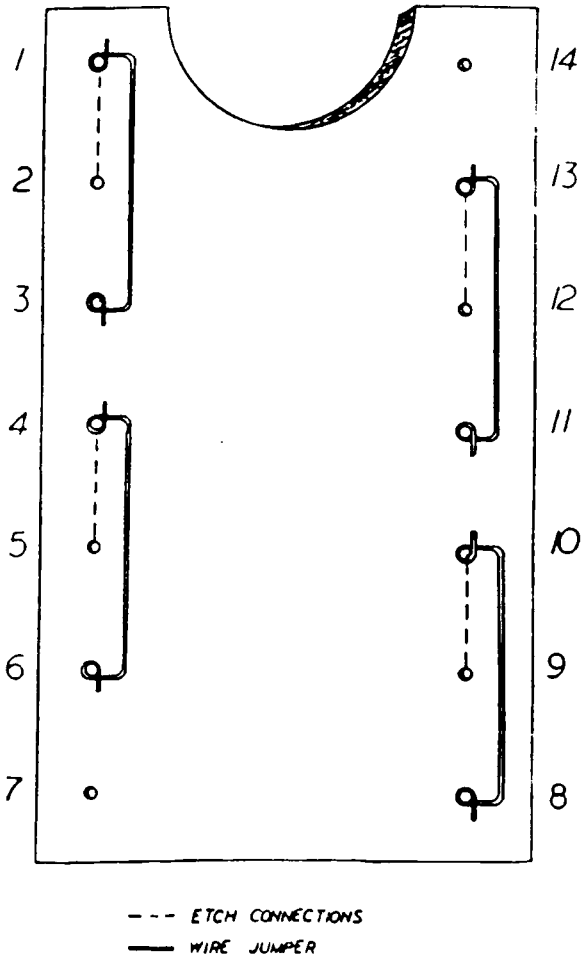


FIGURE 2-3: USER-CONFIGURED HEADER DIP (SOCKETS U1-U6)

NOTE

The 8226's are inverting devices. If required by the application, 8216 non-inverting transceivers may be substituted.

Port B interfaces to sockets U5, U6, and Port C interfaces to sockets U3, U4; all four will accept any 14-pin, 7400 pinout type driver. A list of some of the common drivers and their characteristics is found in Table 1-2.

Each of the Port C lines also includes two jumper posts (E7-E14, and E19-E26) that provide the flexibility needed to support all three modes of operation of the PPI. Information required to configure the jumpers may be found in Figure 2-2, and Table 2-4; refer also to the schematic provided in Appendix A.

2.7 INSTALLATION PROCEDURE

The DTX350 module mounts by plugging directly into the female iSBX connector of any host. The module is then secured at one additional point with nylon hardware (shipped with the module) to ensure the mechanical security of the assembly. Figure 1-2 shows the P1 connector and mounting hole location on the board of the DIO module. The mounting hardware shipped with the DTX350 includes:

- 1 plastic spacer, 1/2 x 6/32, separate from the module.
- 36-pin connector P1, factory-installed onto the module.
- 2 plastic screws, 1/4 x 6/32, separate from the module.

NOTE

When installing the host board in a backplane, space allocation should be planned in advance. The DTX350 module occupies the space of an additional card slot adjacent to the component side of the host board.

In order to configure the output ports, the user must supply line drivers for DTX350 module sockets U3, U4, U5, and U6, for Ports B and C, as well as an

interconnecting cable and connector. Use the following instructions to install the DTX350 to the host board.

1. Insert one of the plastic 1/4 x 6/32 screws from below to secure the 1/2 inch plastic spacer to the top of the host board (see Figure 2-4).

2. Locate pin 1 on the DTX350 iSBX bus connector (P1) and align it with pin 1 of the iSBX bus connector on the host board.

3. Align the DTX350 module mounting hole with the spacer on the host board (see Figures 1-2 and 2-4).

4. Gently press the two boards together until the connector seats.

5. Secure the DTX350 module to the top of the spacer with the other 1/4 x 6/32 screw.

NOTE

The placement of an installed DTX350 and the host board connector number may vary according to the type of host board that is used.

FIGURE 2-4: INSTALLATION OF THE DTX350 MODULE

CHAPTER 3

PROGRAMMING INFORMATION

3.1 INTRODUCTION

This chapter describes the programming of the DTX350 DIO module which entails programming the 8255A-5 Programmable Peripheral Interface (PPI).

3.2 8255A-5 (PPI) FUNCTIONAL DESCRIPTION

The 8255A-5 is a programmable peripheral interface device which functions as a general purpose I/O component to interface peripheral equipment to the host system bus. See Figure 3-1 for the Block Diagram of the PPI.

3.2.1 DATA BUS BUFFER

The 8255A-5 interfaces to the system bus via a 3-state bidirectional 8-bit buffer. Data is transmitted to or received by the buffer upon execution of input or output instructions by the CPU. The buffer is also used for the transfer of control words and status information.

3.2.2 READ/WRITE AND CONTROL LOGIC

The read/write and control logic manages all of the internal and external transfers of both the data and the control or status words. It accepts input from the CPU Address and Control buses and issues commands to both of the control groups. The signals associated with this section control the communication between the CPU and the 8255A-5, and are discussed in detail in Chapter 4.

3.3 PPI OPERATIONAL DESCRIPTION

The PPI has three 8-bit registers; each connects to an associated port with the same letter designation. Herein, references to port functions in the PPI will designate registers. Each register may be configured for a variety of functional characteristics by the system software, but still retains its own personality. Individual features of the port/registers are as follows:

- Port A - consists of one 8-bit data output latch/buffer and one 8-bit input latch.
- Port B - consists of one 8-bit data input/output latch/buffer and one 8-bit data input buffer.
- Port C - consists of one 8-bit data output latch/buffer and one 8-bit data input buffer (no input latch). Under mode control, this register can be two 4-bit registers (each one containing a 4-bit latch), and can be used to output control signals to the J1 connector and receive status signals from the J1 connector, in conjunction with Port/Registers A and B.

3.3.1 MODE SELECTION

The 24 I/O pins may be programmed in two groups (A and B) of 12, (one complete set of eight associated with either Port A or B, and four from Port C) and used in three major software-selectable modes of operation (see Figure 3-2):

- Basic Input/Output mode (Mode 0)
- Strobed Input/Output mode (Mode 1)
- Bidirectional Bus mode (Mode 2).

In Mode 0, each group of 12 I/O pins can be programmed in sets of four for input or output. In Mode 1, each group can be programmed to have eight lines of input or output. Of the remaining four pins, three are used for handshaking and interrupt control signals. (The fourth pin is not used.) Mode 2, the third mode of operation, is a bidirectional bus mode, which uses eight lines for a bidirectional bus, and five lines, using one from the other group, for handshaking.

The functional configuration of each port/register is programmed by the system software. The processor sends a control word to the Control Word Register in the PPI, which contains information to define the mode, bit set, and bit reset. The Control Word Register can be written to but cannot be read.

Two control blocks are recognized, Group A and Group B. Each group receives commands from the Read/Write Control Logic (see Figure 3-1), and control words from the internal data bus, as well as issues commands to its associated ports. The control groups consist of the following (see Figure 3-2):

Control Group A - Port A and upper 4 bits of Port C

Control Group B - Port B and lower 4 bits of Port C

The modes for Ports A and B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition may be tailored to nearly any I/O structure. For example: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results; Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Mode definitions and possible mode combinations allow the 8255A-5 the functional flexibility to support almost any external device with no external logic. For additional information, refer to Appendix B for the 8255A-5 component specifications.

3.3.2 PROGRAMMING

The PPI programming presented in the following text consists of subsections on addressing, control word format, initialization, and operation of the PPI. Examples are included for a typical PPI port READ and port WRITE subroutine.

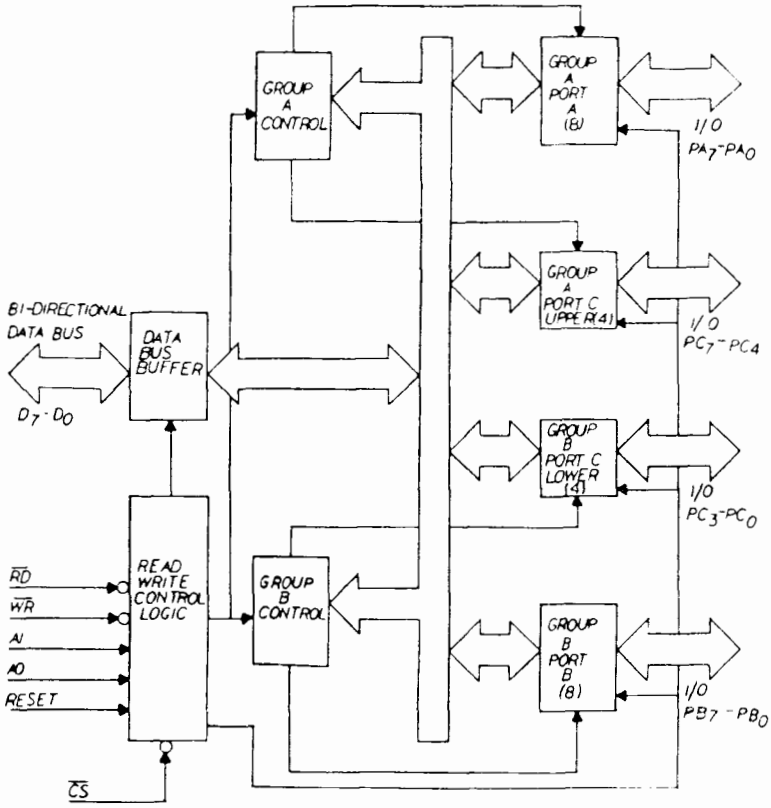


FIGURE 3-1: PPI (8255A-5) BLOCK DIAGRAM

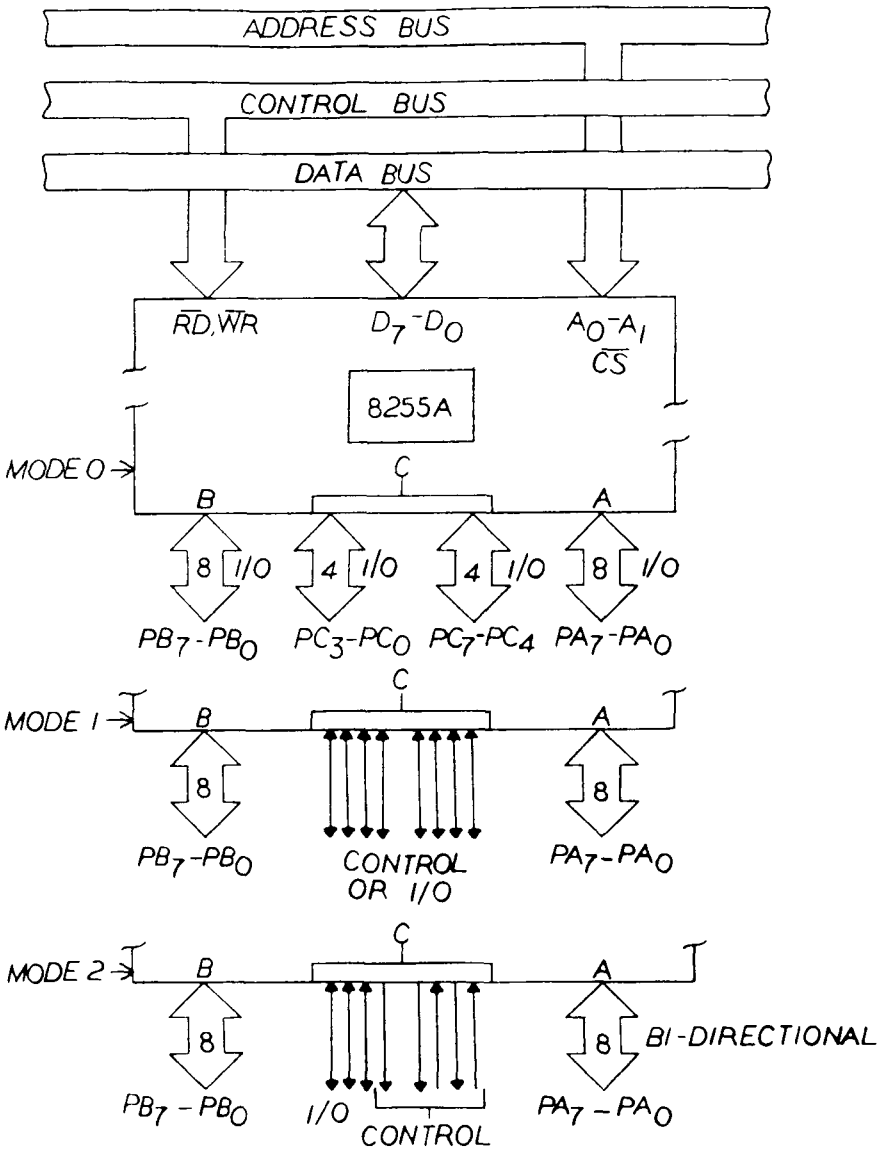


FIGURE 3-2: PPI (8255A-5) MODE DIAGRAM

3.3.2.1 Addressing - The PPI uses four consecutive hexadecimal addresses on the DTX350, either BASE+0 through BASE+3, or BASE+4 through BASE+7, for data transfer and for port control. All addressing for the parallel I/O ports on the DTX350 is contingent on the iSBX connector on the host board (see Table 3-1). If there is more than one iSBX connector on the host, and more than one DTX350 is used, each DTX350 requires its own port address. In Table 3-1, the first digit of the port address (BASE) is determined by the iSBX host.

NOTE

Addresses BASE+8 through BASE+F (hexadecimal) on the host are reserved for the DTX350 module and must not be used by any other device when the DTX350 is installed.

TABLE 3-1: I/O ADDRESSING

8255A-5 PORT REGISTERS	DTX350 ADDRESS (Hex)*
Port A Data Register	Base+0 or Base+4
Port B Data Register	Base+1 or Base+5
Port C Data Register	Base+2 or Base+6
Control Word Register	Base+3 or Base+7
Reserved	Base+8 to Base+F

* The first digit of each port I/O address is listed as "Base" since its value is dependent upon the type of host board. See the manual on the iSBX host to determine the first digit of the port address.

3.3.2.2 Control Word Format - The control word format shown in Figure 3-3 is used to initialize the PPI to define the operating mode of the three ports. The control word is 7 bits, with four bits assigned to Group A and three bits assigned to Group B, as shown below. The last bit, Bit 7, reflects the mode set flag.

- Group A (control word bits 3 through 6) defines the operating mode for Port A (address BASE+0 or BASE+4) and the upper four bits of Port C (address BASE+2 or BASE+6).

- Group B (control word bits 0 through 2) defines the operating mode for Port B (address BASE+1 or BASE+5) and the lower four bits of Port C (address BASE+2 or BASE+6).

3.3.3 INITIALIZATION

iSBX defines three address bits, of which the 8255A-5 uses only two, resulting in address foldover. To initialize the PPI, write a control word to port address BASE+3 or BASE+7, the location of the Control Word Register. If the control word is 92H (see Figure 3-3), the PPI initializes as follows:

1. Mode Set Flag active ("1" sets mode definition)
2. Port A (BASE+0 or BASE+4) set to Mode 0 Input
3. Port C (BASE+2 or BASE+6) upper set to Mode 0 Output
4. Port B (BASE+1 or BASE+5) set to Mode 0 Input
5. Port C (BASE+2 or BASE+6) lower set to Mode 0 Output

3.3.4 OPERATION

After the PPI has been initialized, the operation is simply to perform a READ or a WRITE to the appropriate port.

PROGRAMMING INFORMATION

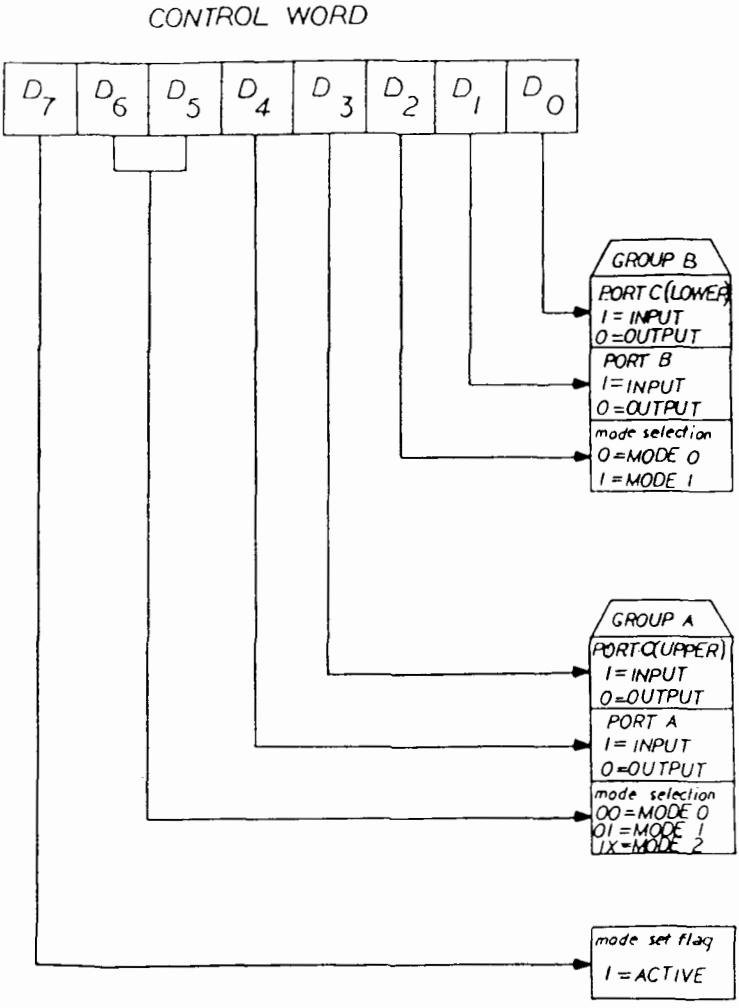


FIGURE 3-3: PPI CONTROL WORD BIT FORMAT

CHAPTER 4

PRINCIPLES OF OPERATION

4.1 INTRODUCTION

This chapter discusses operating principles of the DTX350 DIO module. Included are sections on the interfaces between the host and the DTX350, and between the parallel I/O lines and the DTX350. The interrupt system is also discussed.

4.2 ISBX BUS INTERFACE

The interface to the host iSBX connector consists of several signals which control the DTX350 functions. These are as follows:

RESETH (Reset) - This active high signal to the PPI provides initialization for the chip, resets the control register to 0, and conditions all 8255A-5 ports to the input mode (all outputs go to inte high-impedance state). RESET is derived from the microprocessor Reset signal in the host microcomputer.

WRITEL/(Write) - This active low input to the DTX350 module indicates that data or a command is to be written into the PPI from the iSBX bus (DB0-DB7) (reference Table 4-1).

READL/(Read) - This active low input indicates that data is to be read from the PPI and made available on the iSBX bus (DB0-DB7) (reference Table 4-1).

CS0L/(Chip Select 0) - This active low input selects the PPI, enabling communication between it and the host (see Table 4-1).

AB0, AB1 (Address lines) - The active high inputs to the DTX350 module in conjunction with the READL/ and WRITEL/ lines, control selection of one of the three port registers or the Control Word Register in the

PRINCIPLES OF OPERATION

PPI (reference Table 4-1).

DB0-DB7 (Bidirectional Data Bus) - These active high lines provide the interface for data and command transfer between the PPI and the host microcomputer.

MPSTL/ (Module present) - This active low output signal indicates to the host microcomputer that a DTX350 module has been installed.

TABLE 4-1: PPI OPERATIONS

AB1	AB0	READL/	WRITEL/	CSOL/	INPUT OPERATION (READ)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Illegal Condition
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus - 3-state
X	X	1	1	X	Data Bus - 3-state

OPT0, OPT1 (Option signals) - These user-defined signals are included to provide application flexibility for the DTX350 module. These signals, if required by the application, must be user-configured via jumpers. Refer to the schematic diagram in Chapter 5.

INTR0H, INTR1H (Interrupt signals) - These signals are included to provide interrupt generation to the host board by the DTX350. These signals, if required by the application, must be user-configured via jumpers (see schematic in Chapter 5).

4.3 PORT INTERFACE

The DTX350 parallel port I/O (via connector J1) consists of three 8-bit ports that may be configured in one of several modes, as listed in Table 4-2. The eight bits of Port A and eight bits of Port B must be configured as units to either input or output mode, but Port C may be broken into two groups of four, either of which can be used in input or output mode.

Data I/O through Port A passes through two 8226 transceivers (U1 and U2) which control the direction of data flow according to the condition of DIEN/, the signal on jumper post E2. When DIEN/ is low, data flows from PPI to the port data lines. Conversely, when DIEN/ is high, data flows from the port data lines to the PPI.

Four 14-pin DIP sockets are provided for user-supplied line driver installation onto the Port B and Port C data lines. The type of line driver is determined by the application.

4.4 INTERRUPT CONTROL FUNCTIONS

When Port C is used as status control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if these were data output ports (see Figure 4-1).

When the 8255A-5 PPI is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from the Port C data register, can be inhibited or enabled by setting or resetting the associated INTE (interrupt) flip-flop.

This function permits the programmer to enable or disable an interrupt to the CPU from a specific I/O device without affecting any other device in the interrupt structure.

PRINCIPLES OF OPERATION

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt Enable

(BIT-RESET) - INTE is RESET - Interrupt Disable

When the Reset input goes high, all ports are set to the input mode (i.e., all 24 lines are in the high impedance state). After the reset is removed, the 8255A-5 can remain in the input mode with no further initialization required. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 8255A-5 to service a variety of peripheral devices with a simple software maintenance routine.

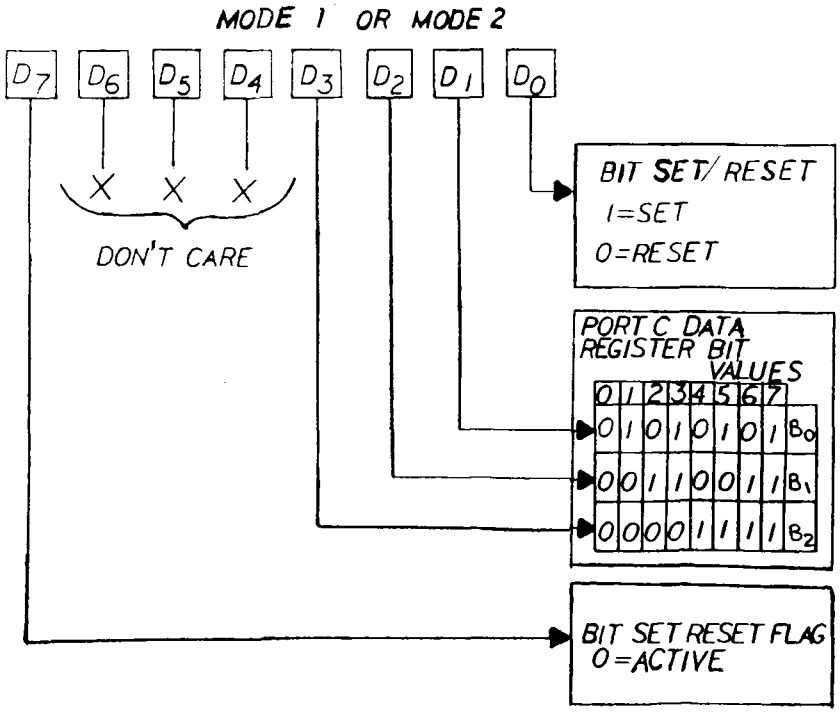


FIGURE 4-1: BIT SET/RESET FORMAT

TABLE 4-2: MODE DEFINITION SUMMARY TABLE

PORT	BIT	MODE 0 IN	MODE 0 OUT	MODE 1 IN	MODE 1 OUT	MODE 2 GROUP A ONLY
PA	0	In	Out	In	Out	Bidirectional
PA	1	In	Out	In	Out	Bidirectional
PA	2	In	Out	In	Out	Bidirectional
PA	3	In	Out	In	Out	Bidirectional
PA	4	In	Out	In	Out	Bidirectional
PA	5	In	Out	In	Out	Bidirectional
PA	6	In	Out	In	Out	Bidirectional
PA	7	In	Out	In	Out	Bidirectional
PB	0	In	Out	In	Out	-
PB	1	In	Out	In	Out	-
PB	2	In	Out	In	Out	-
PB	3	In	Out	In	Out	-
PB	4	In	Out	In	Out	-
PB	5	In	Out	In	Out	-
PB	6	In	Out	In	Out	-
PB	7	In	Out	In	Out	-
PC	0	In	Out	INTRb	INTRb	I/O
PC	1	In	Out	IBFb	OBFb/	I/O
PC	2	In	Out	STBb/	ACKb/	I/O
PC	3	In	Out	INTRa	INTRa	INTRa
PC	4	In	Out	STBa/	I/O	STBa/
PC	5	In	Out	IBFa	I/O	IBFa/
PC	6	In	Out	I/O	ACKa/	ACKa/
PC	7	In	Out	I/O	OBFa/	OBFa/

CHAPTER 5

SERVICE INFORMATION

5.1 INTRODUCTION

This chapter provides an assembly drawing, a schematic, and repair assistance instructions for the DTX350 DIO module.

5.2 ASSEMBLY DRAWING

The part locations for the DTX350 module are provided on the assembly drawing in Appendix A.

5.3 SCHEMATIC DIAGRAM

The electrical scheme of the DTX350 is provided on the schematic diagram shown in Appendix A.

5.4 SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Data Translation by contacting:

Customer Service Department
Data Translation, Inc.
100 Locke Drive
Marlboro, MA 01752
(617) 481-3700

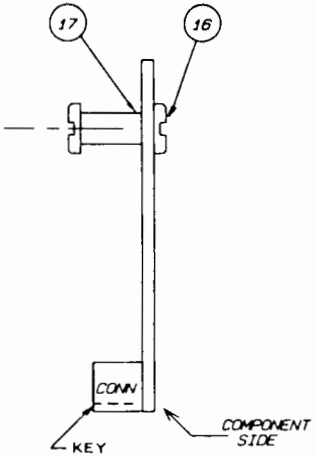
NOTE

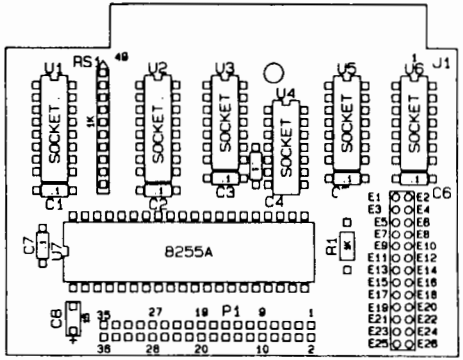
A Return Material Authorization (RMA) number must be obtained from the Data Translation Customer Service Department before a product may be returned to Data Translation for repair. Be sure to comply with the return-for-repair guidelines given in Chapter 1, Inspection and Unpacking.

APPENDIX A
DTX350 DIAGRAMS

NOTE: INSTALL JUMPER E1 TO E2

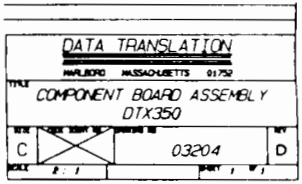
U1 AND U2 ARE 8226 INSERTED IN SOCKETS.





SILKSCREEN AND ASSEMBLY

FIGURE A-1: DTX350 DIO MODULE ASSEMBLY DRAWING



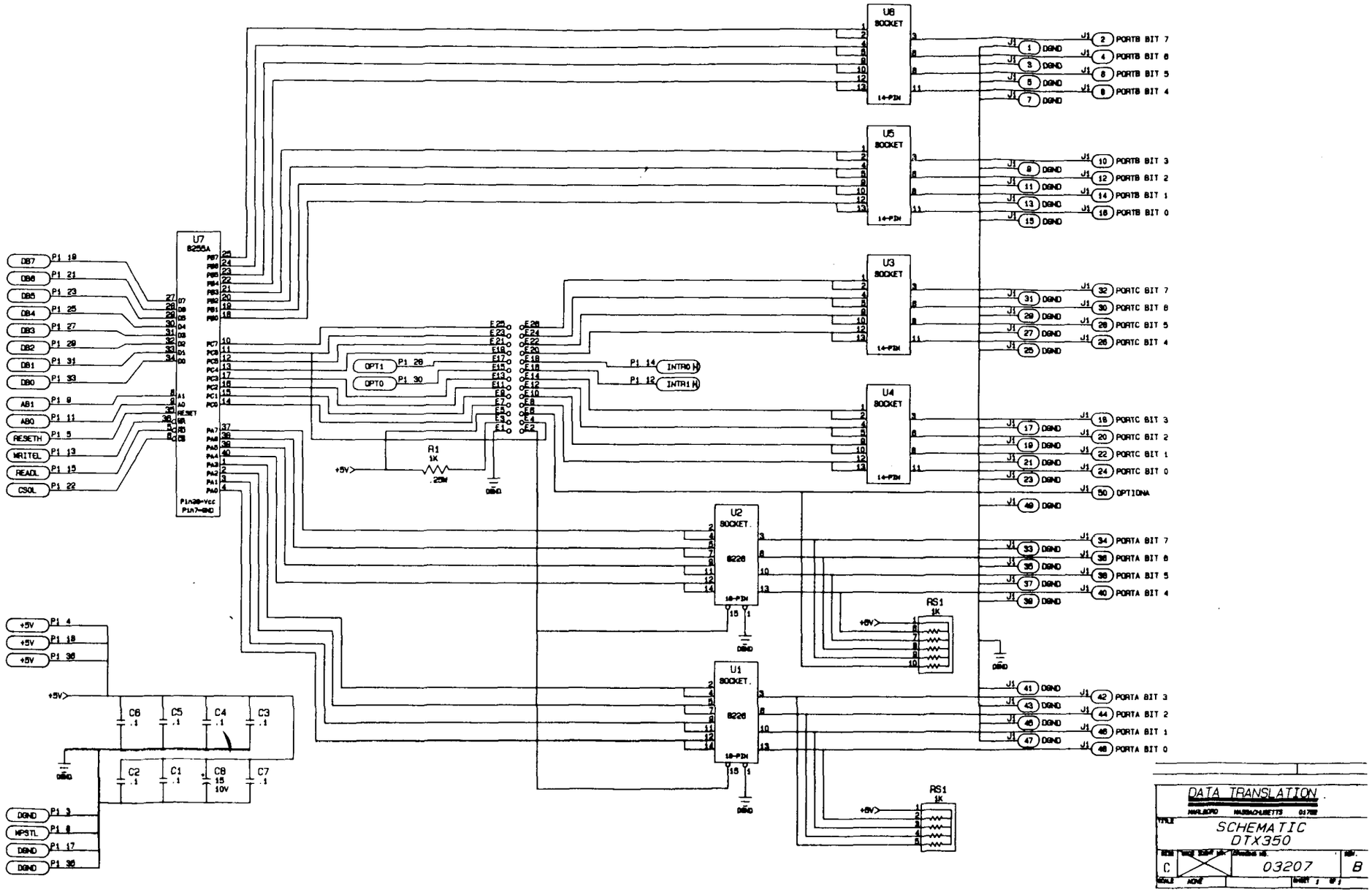


FIGURE A-2: DTX350 DIO MODULE SCHEMATIC DIAGRAM

APPENDIX B

8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE SPECIFICATIONS

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8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - —Standard Temperature Range
  - —Extended Temperature Range

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

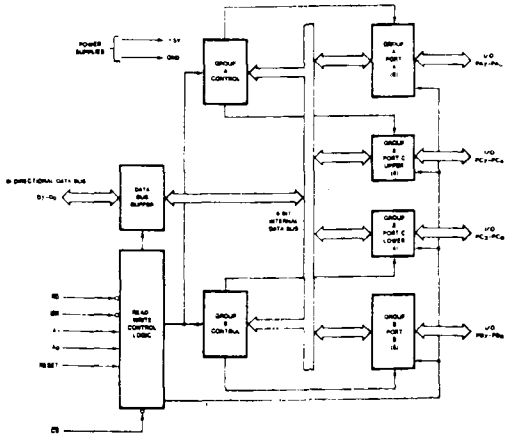


Figure 1. 8255A Block Diagram

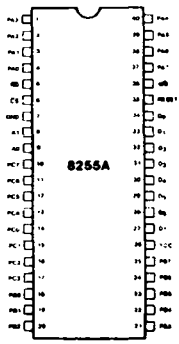


Figure 2. Pin Configuration

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8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

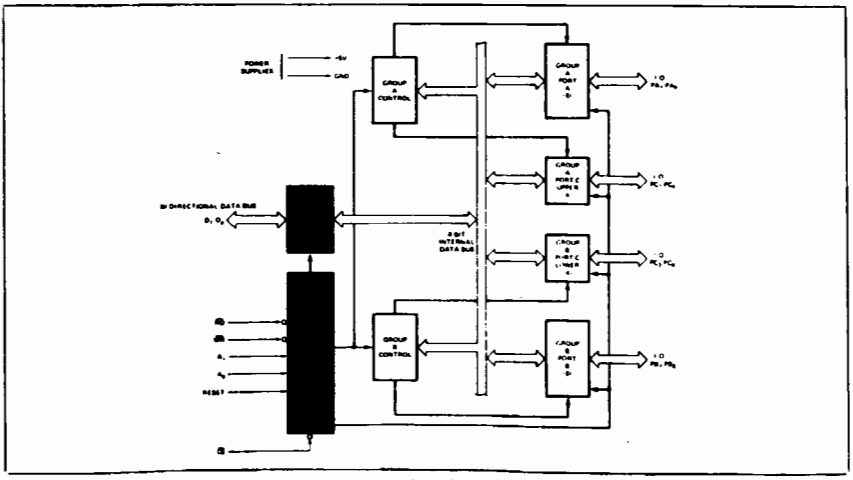


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

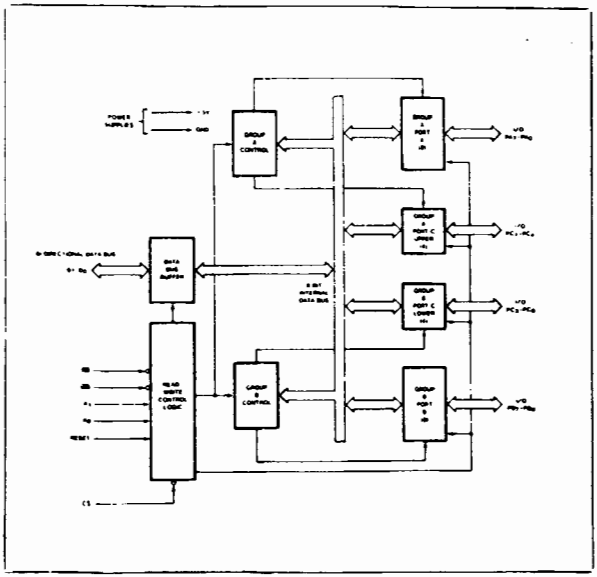
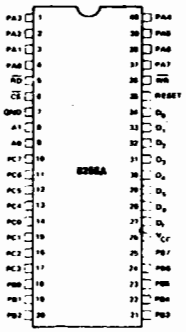


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

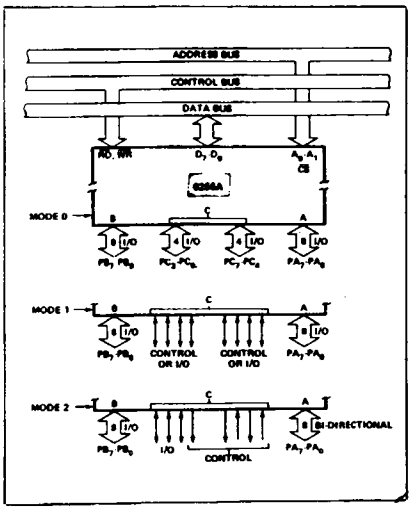


Figure 5. Basic Mode Definitions and Bus Interface

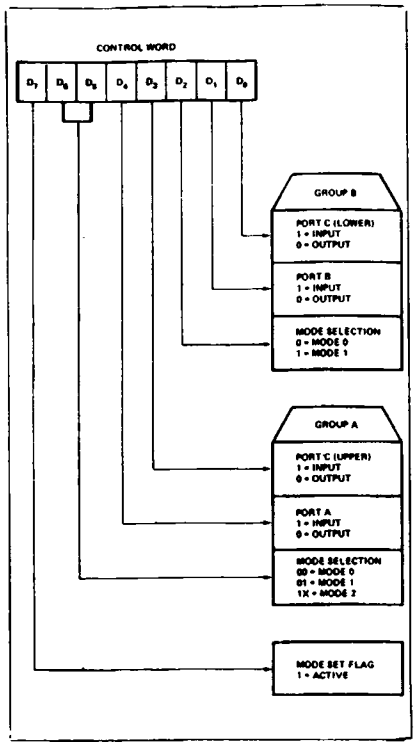


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

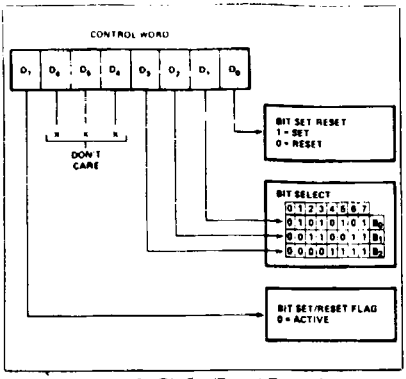


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) – INTE is SET – Interrupt enable
(BIT-RESET) – INTE is RESET – Interrupt disable

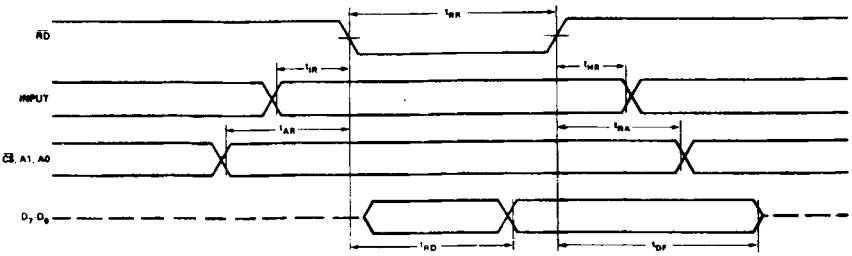
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

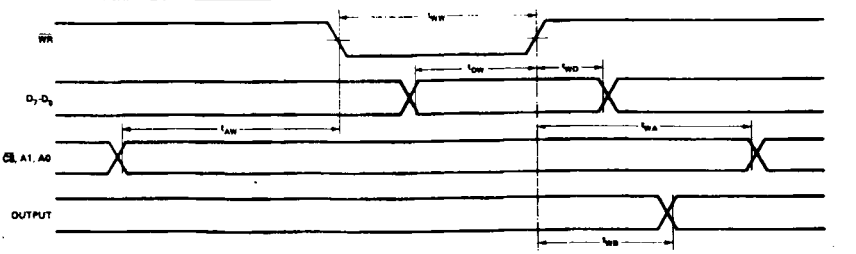
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)

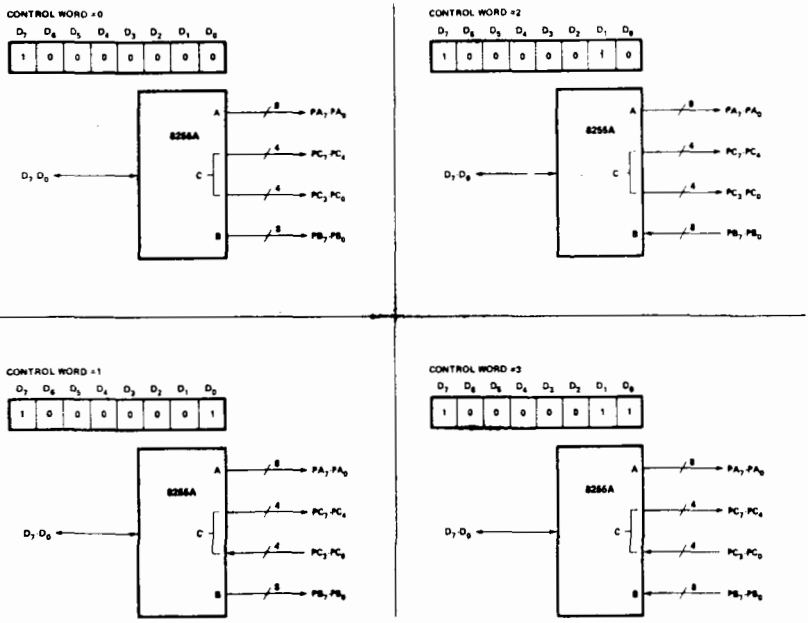


MODE 0 (Basic Output)

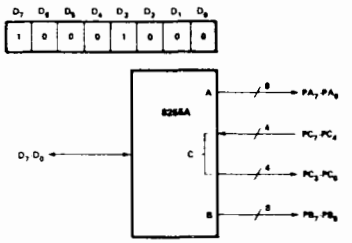
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

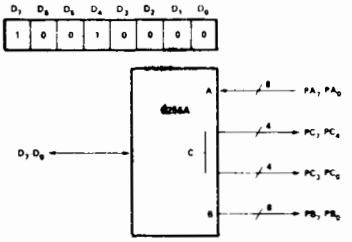
MODE 0 Configurations



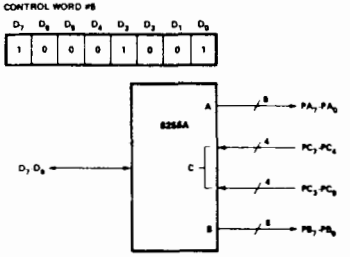
CONTROL WORD =4



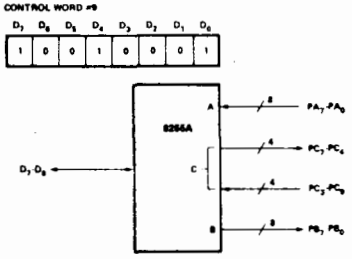
CONTROL WORD =8



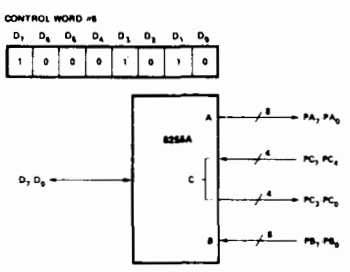
CONTROL WORD =8



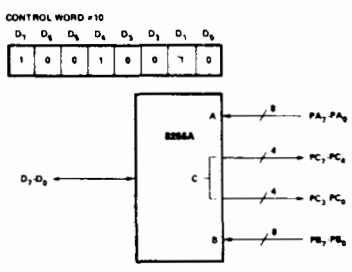
CONTROL WORD =9



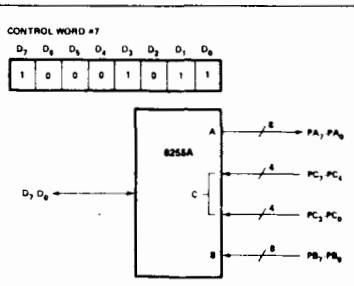
CONTROL WORD =6



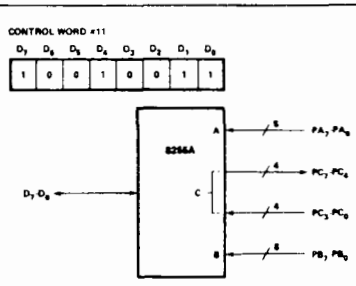
CONTROL WORD =10

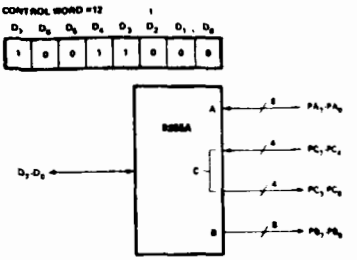


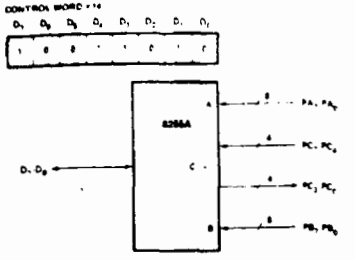
CONTROL WORD =7

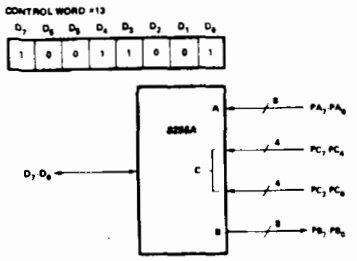


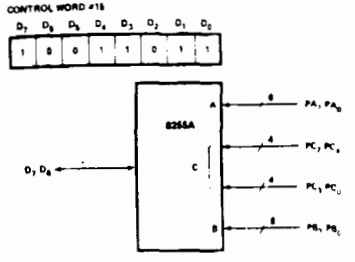
CONTROL WORD =11











Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

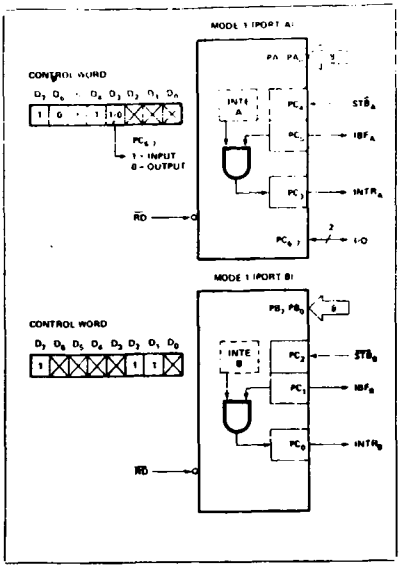


Figure 8. MODE 1 Input

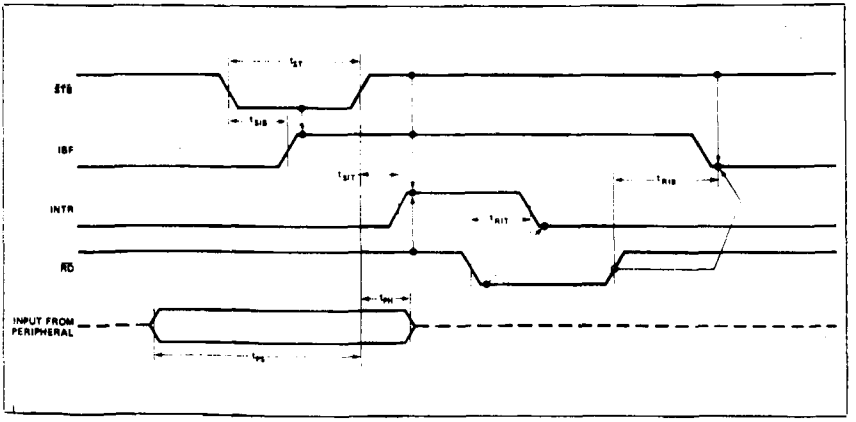


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

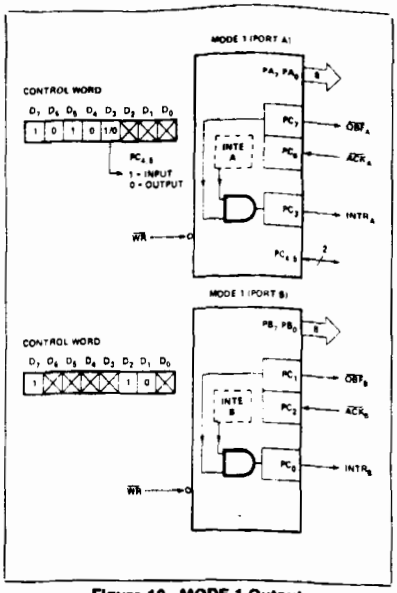


Figure 10. MODE 1 Output

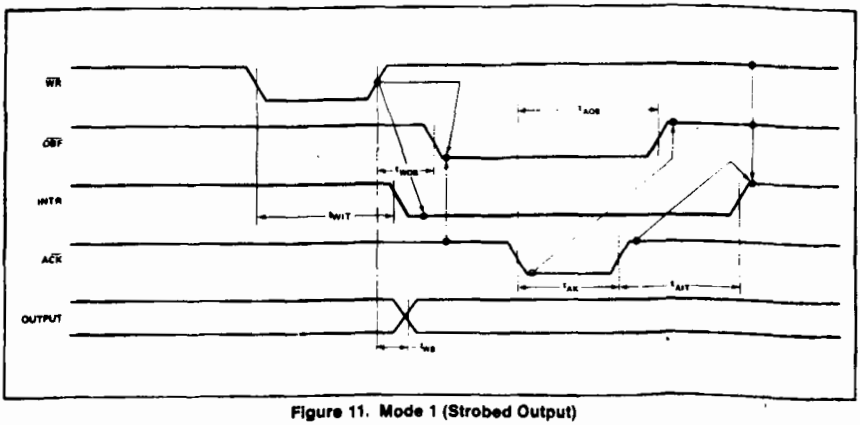


Figure 11. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

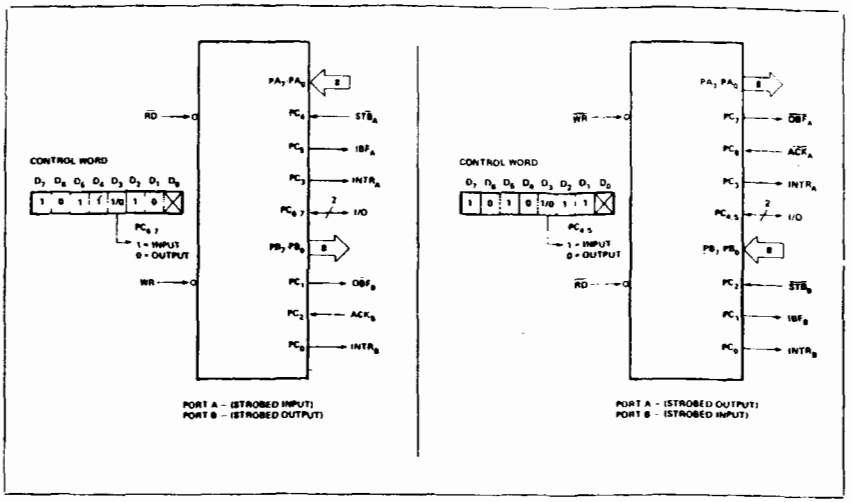


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

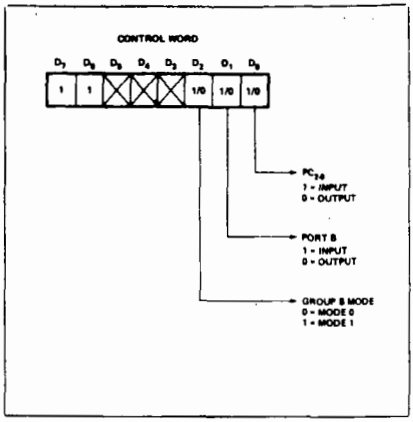


Figure 13. MODE Control Word

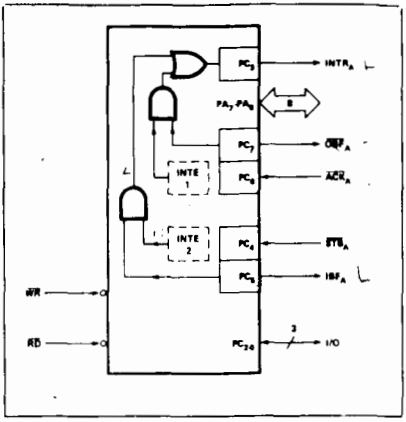


Figure 14. MODE 2

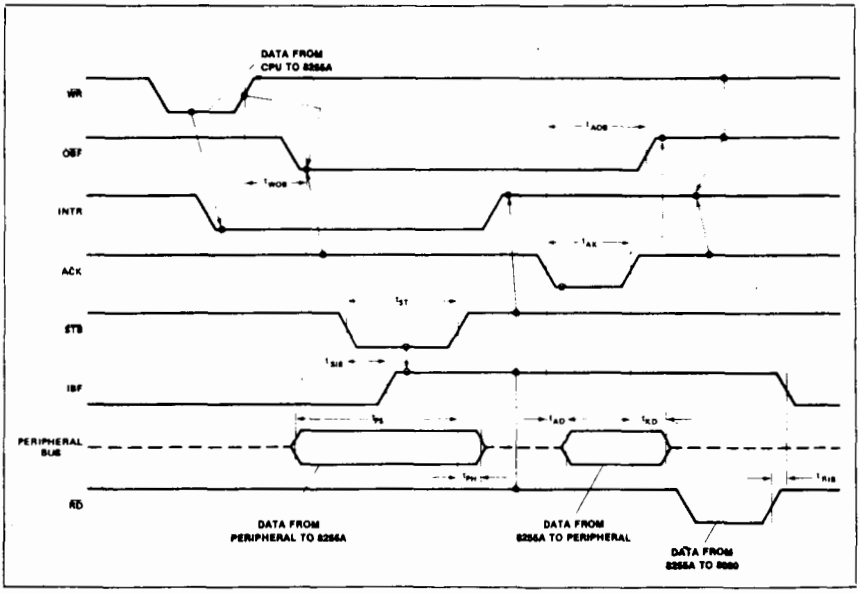


Figure 15. MODE 2 (Bidirectional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

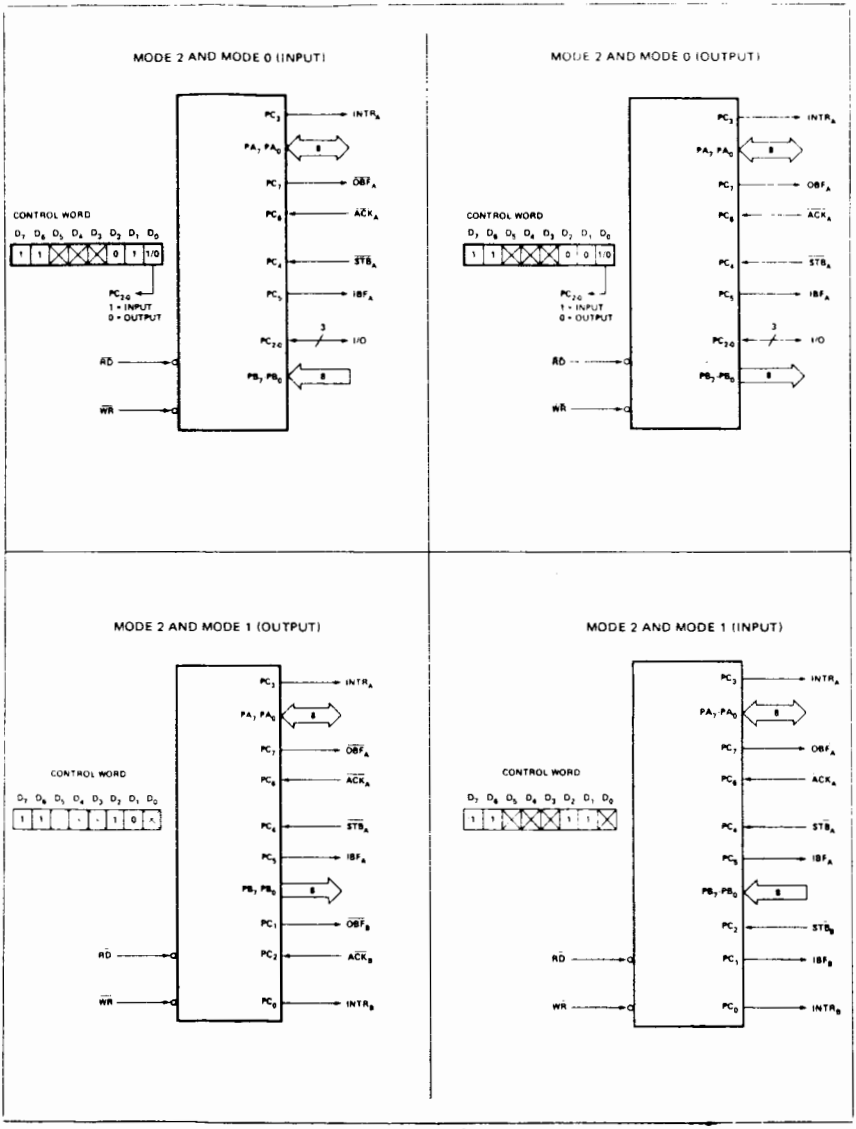


Figure 16. MODE ¼ Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	⟷	
PA_1	IN	OUT	IN	OUT	⟷	
PA_2	IN	OUT	IN	OUT	⟷	
PA_3	IN	OUT	IN	OUT	⟷	
PA_4	IN	OUT	IN	OUT	⟷	
PA_5	IN	OUT	IN	OUT	⟷	
PA_6	IN	OUT	IN	OUT	⟷	
PA_7	IN	OUT	IN	OUT	⟷	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

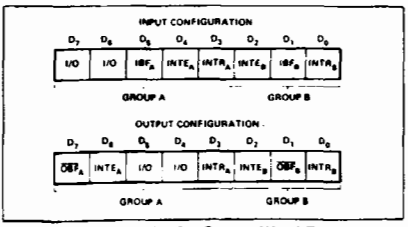


Figure 17. MODE 1 Status Word Format

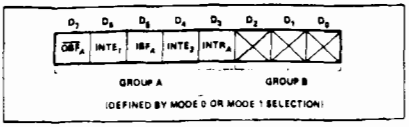


Figure 18. MODE 2 Status Word Format

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 8255A.

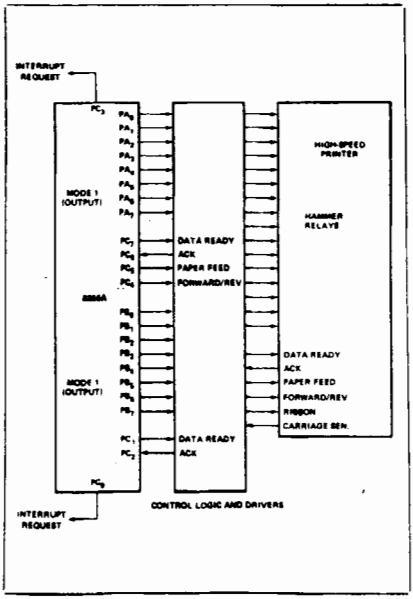


Figure 19. Printer Interface

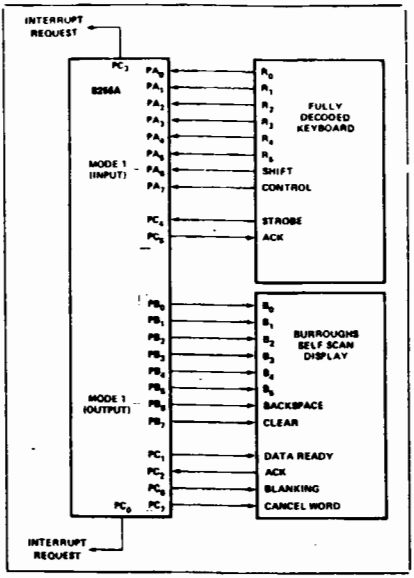


Figure 20. Keyboard and Display Interface

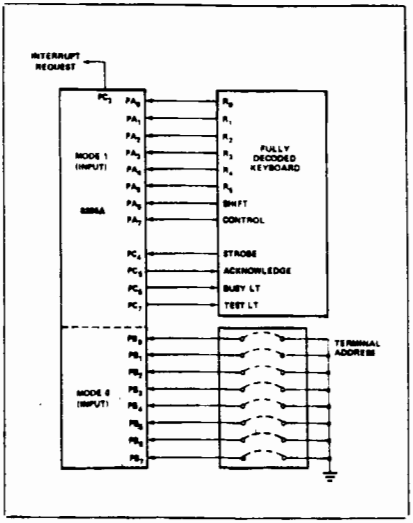


Figure 21. Keyboard and Terminal Address Interface

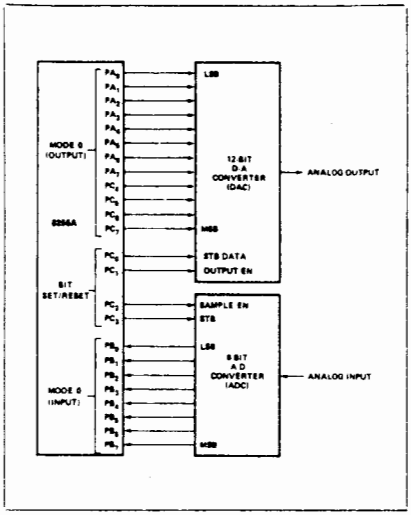


Figure 22. Digital to Analog, Analog to Digital

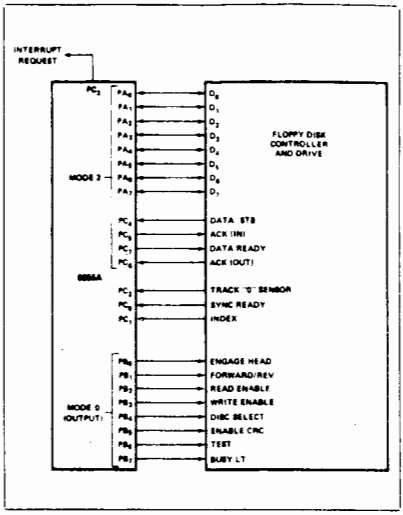


Figure 23. Basic Floppy Disk Interface

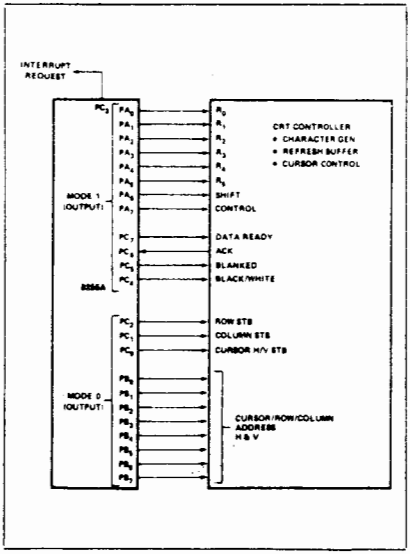


Figure 24. Basic CRT Controller Interface

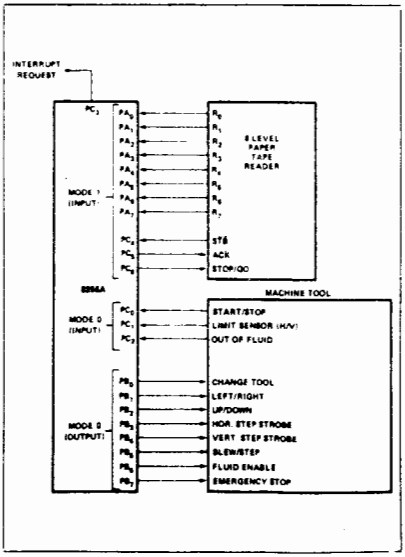


Figure 25. Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, GND = 0V)*

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45*	V	I_{OL} = 2.5mA
V_{OL} (PER)	Output Low Voltage (Peripheral Port)		0.45*	V	I_{OL} = 1.7mA
V_{OH} (DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH} (PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to .45V

NOTE:
1. Available on any 8 pins from Port B and C.

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, GND = 0V)*

Bus Parameters

READ

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

A.C. CHARACTERISTICS (Continued)

WRITE

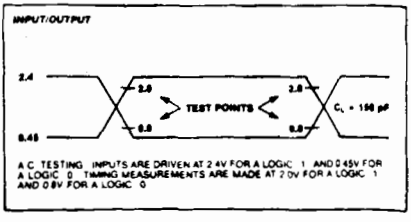
Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns

OTHER TIMINGS

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1,3]		450		450	ns

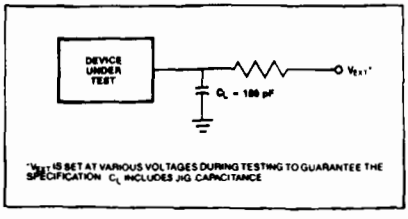
NOTES:
1. Test Conditions: C_L = 150 pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR may occur as early as $\overline{WR}\downarrow$.
* For Extended Temperature EXPRESS, use M8255A electrical parameters.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

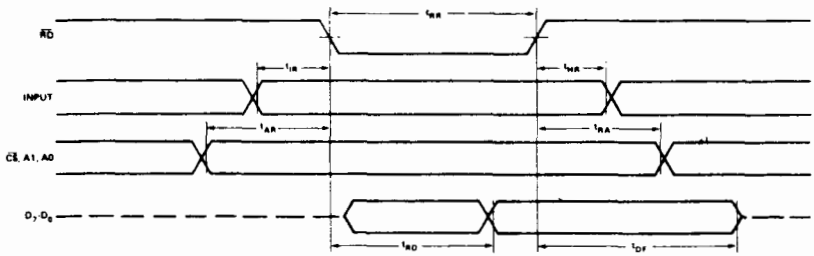
A.C. TESTING LOAD CIRCUIT



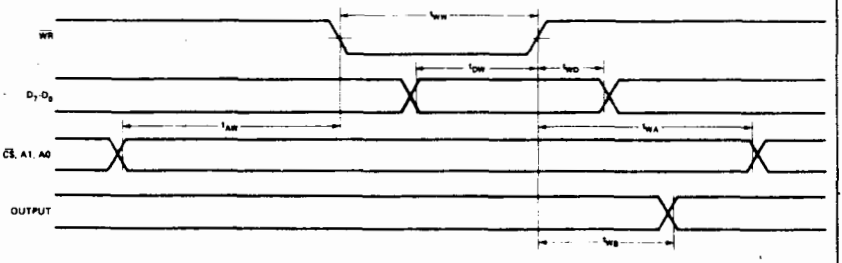
*V_{EXT} IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION. C_L INCLUDES JIG CAPACITANCE.

WAVEFORMS

MODE 0 (BASIC INPUT)

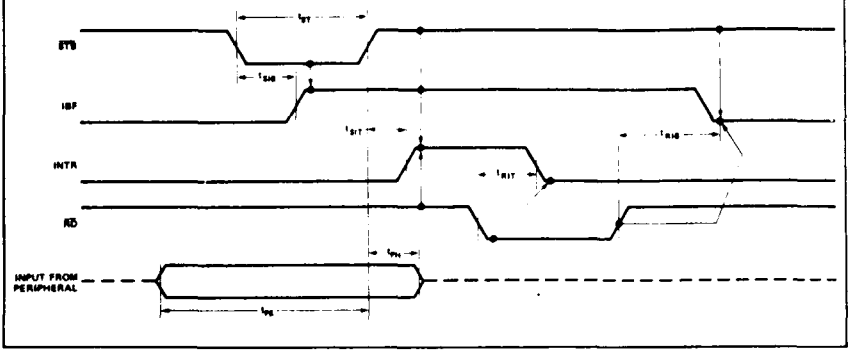


MODE 0 (BASIC OUTPUT)

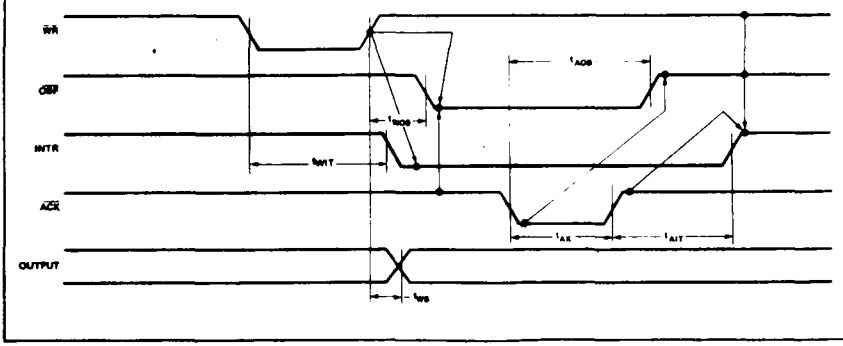


WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

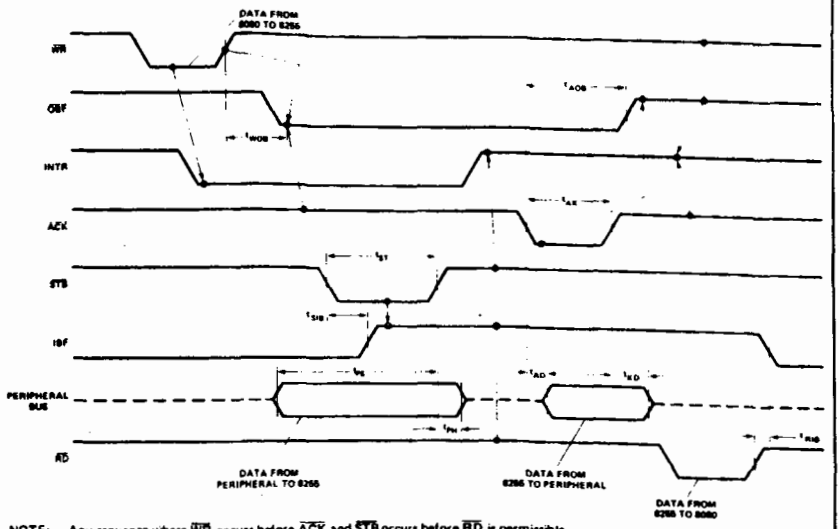


MODE 1 (STROBED OUTPUT)



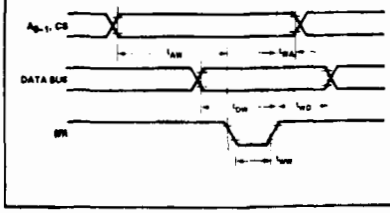
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)

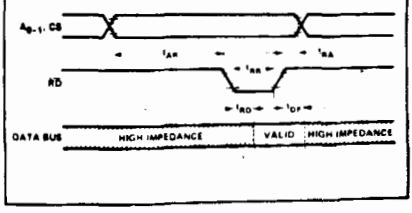


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

WRITE TIMING



READ TIMING



APPENDIX C
SAMPLE PROGRAMS

C.1 SAMPLE PROGRAMS

First initialize the DTX350 to the proper mode and select the operation for input or output from the DTX350. Verify that the DTX350 jumpers are properly configured for the mode and port desired (refer to Chapter 2).

In the following programs, a value is written into the registers of the DTX350 and then read back to check the value, which appears in decimal. A probe may be used to check the bits of the port being used.

EXAMPLE PROGRAM 1: PORT A; MODE 0 OUTPUT(LATCHED)

This sample program was written using a DT2806 host board (which has a factory-configured base address of 370H). The jumper configuration was set using only jumpers E1-E2, since just Port A was to be used.

```
10 OUT &H4F70,&H80      :REM DTX350 INITIALIZATION
20 LET ADD = &H4370     :REM ADDRESS OF PORT A
30 FOR X = 255 TO 0     :REM DECREMENT DATA
   STEP -1              :REM FROM FF TO 00
40 OUT ADD,X            :REM LOAD X INTO PORT A
50 A = INP(ADD)         :REM READ ADDRESS
                        :REM VALUE OF PORT A
60 PRINT A              :REM WRITE ADDRESS VALUE
70 NEXT X
80 END
```

EXAMPLE 2: PORT A, B, C; MODE 0 OUTPUT(LATCHED)

This sample program was written using a DT2806 board. This board used the same jumper configuration as the board in EXAMPLE 1. The DTX350 jumper configuration was changed so that Port C would be written to and read from by putting in jumpers: E7-E8, E9-E10, E11-E12, E13-E14, E19-E20, E21-E22, E23-E24, and E25-E26, in addition to the factory-configured jumpers E1-E2.

```
10 OUT &H4F70,&H80       :REM DTX350 INITIALIZATION
20 LET ADD = &H4370      :REM ADDRESS OF PORT A
30 FOR X = 1 TO 3        :REM THREE PORTS TO
                         :REM LOOP THROUGH
40 OUT ADD,&H55          :REM START CHECKERBOARD
                         :REM TEST
50 A = INP(ADD)          :REM READ ADDRESS
                         :REM VALUE OF PORT
60 PRINT A               :REM WRITE ADDRESS VALUE
70 OUT ADD,&HAA
80 B = INP(ADD)
90 PRINT B
93 ADD = ADD +H400       :REM INCREMENT TO NEXT PORT
96 NEXT X
99 END
```

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