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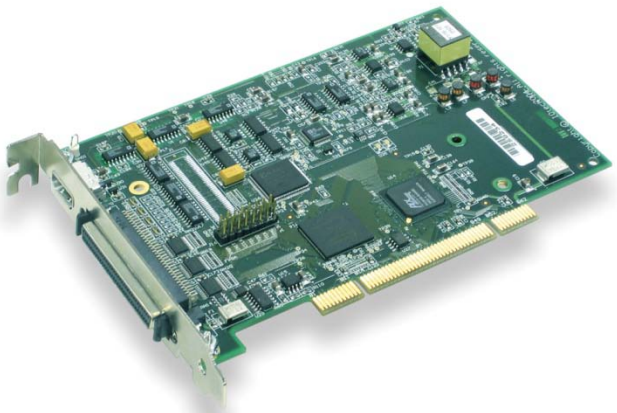
Find the *Measurement Computing / IOtech DaqBoard/3005* at our website: *Click HERE*

DaqBoard/3000 Series

Requires a 32-bit version of Windows®

Windows XP
Windows Vista (x86)

DaqBoard/3000, /3001, /3005, and /3006



PCI 16-Bit, 1-MHz Multifunction Boards

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In this manual, the book symbol always precedes the words "Reference Note." This type of note identifies the location of additional information that may prove helpful. References may be made to other chapters or other documentation.



Tips provide advice that may save time during a procedure, or help to clarify an issue. Tips may include additional reference.

Specifications and Calibration

Specifications are subject to change without notice. Significant changes will be addressed in an addendum or revision to the manual. As applicable, the hardware is calibrated to published specifications. Periodic hardware calibration is not covered under the warranty and must be performed by qualified personnel as specified in this manual. Improper calibration procedures may void the warranty.

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CAUTION
 **Using this equipment in ways other than described in this manual can cause personal injury or equipment damage. Before setting up and using your equipment, you should read *all* documentation that covers your system. Pay special attention to Warnings and Cautions.**

Note:

During software installation, Adobe® PDF versions of user manuals will automatically install onto your hard drive as a part of product support. The default location is in the **Programs** group, which can be accessed from the *Windows Desktop*. Initial navigation is as follows:

Start [on Desktop] ⇒ **All Programs** ⇒ **IOtech …**

Refer to the PDF documentation for information regarding hardware and software.

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DaqBoard /1000 2000 3000 Series Installation Guide

PCI-bus Data Acquisition Boards



Take ESD precautions!



Before you get started

Verify that you have the following items.

- DaqBoard/1000, /2000, or /3000 Series Device
- Data Acquisition CD
- Monitor: SVGA, 1024 x 768 screen resolution
- Windows 2000 and Windows XP users:
  PC with Intel™ Pentium, 1 GHz or equivalent;
  128 MB memory; 10 GB disk space
- Windows Vista users:
  PC must be *Windows Vista Premium Ready*

Step 1 - Install Software

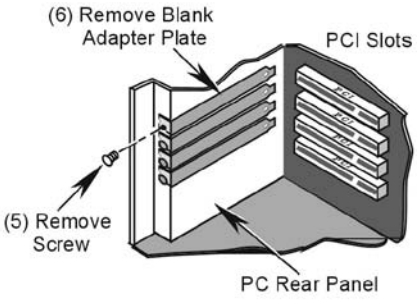
IMPORTANT: Software must be installed before installing hardware.

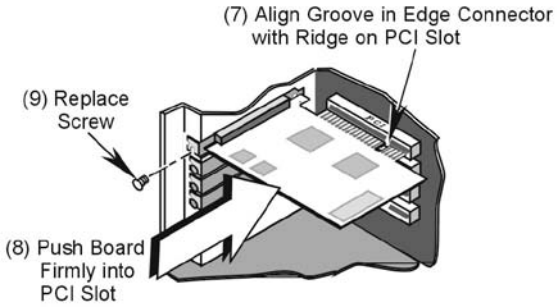
1. Remove previous version Daq drivers, if present. You can do this through Microsoft's *Add/Remove Programs* feature.
2. Insert the Data Acquisition CD into your CD-ROM drive and wait for the CD to auto-run. An *Opening Screen* will appear. As an alternative, you can download software from: www.iotech.com/ftp.html
3. After the intro-screen appears, follow the screen prompts.

Step 2 – Install Boards in available PCI Bus-slots

IMPORTANT: Bus Mastering DMA *must be* Enabled on the PCI slot [for which the board is to be installed]. Refer to your PC Owner's Manual as needed.

1. Turn **off** power to, and **UNPLUG the host PC** and externally connected equipment.
2. Remove the PC's cover. *Refer to your PC Owner's Manual as needed*.
3. Choose an available PCI bus-slot. **Lower residual noise will result by placing the board in a PCI slot which has vacant adjacent slots.**
4. Carefully remove the DaqBoard from its anti-static protective bag. If you have not already done so, write down the serial number of your board at this time.
5. Remove the screw that secures the blank adapter plate, which is associated with the PCI slot you will be using.
6. Remove the blank adapter plate.
7. Align the groove in the board's PCI edge-connector with the ridge of the desired PCI slot, and with the PC's corresponding rear-panel slot.
8. Push the board firmly into the PCI slot. The board will snap into position.
9. Secure the board by inserting the rear-panel adapter-plate screw.
10. Using the previous steps, install additional boards into available PCI bus-slots, if applicable to your application.
11. Replace the computer's cover.
12. Plug in all cords and cables that were removed in step 1.
13. Apply power to, and start up the PC.





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Step 3 – Configure Boards

1. Run the **Daq Configuration** control panel applet. Navigation from the desktop to the applet is as follows: **Start ⇒ Settings ⇒ Control Panel ⇒ DaqConfiguration** *(double-click).*
2. *Double-click* on the Device Inventory's DaqBoard icon (1K0, 2K0, or 3K0, as applicable). **ONLY IF** the board's icon is not present, perform A, B, and C, otherwise go directly to step 3.
   (A) After accessing the Daq Configuration control panel applet, click on the <Add Device> button.
   (B) Using the *Device Type's* pull-down list, select the applicable board.
   (C) Click the <OK> button. The board's Properties tab will appear. At this point, complete steps 3 through 5.
3. Enter a "**Device Name**" in the text box, or use the default, e.g., DaqBoard2K0. The Name is for identifying the specific DaqBoard, but actually refers to the PCI slot.
4. Verify that the "Device Type" shows the correct board, e.g., "DaqBoard/1000, DaqBoard/2001, etc." Note that available device types can be viewed via the pull-down list.
5. Confirm that the DaqBoard's text box shows a **Bus #, Slot #,** and **Serial Number**. If this text box is empty, use its pull-down list and select the serial number that matches the one for your board.

Step 4 – Test Hardware

Use the following steps to test the DaqBoard. Note that these steps are continued from those listed under the previous section, "Configure Boards."

1. Select the "**Test Hardware"** tab.
2. Click the "**Resource Test**" button.
3. After the test is complete, click "**OK**." System capability is now tested; and test results are displayed.

Note: If you experience difficulties, please consult your user documentation (included on your CD) before calling for technical support.

Step 5 – Connect Signals

For /1000 Series and /3000 Series boards, connection is typically made via a terminal board, such as the optional TB-100, a DBK215 module via a 68-pin SCSI connector and/or or a PDQ30 via a HDMI connector. Note that the DaqBoard/3006 has no HDMI connector and cannot be connected to a PDQ30. The user's manual, included on the Data Acquisition CD and also available on our website, contains detailed information, including specifications, pinouts, and numerous illustrations.

Note that /2000 Series boards typically make use of a DBK200 Series option for connecting signals. For detailed information regarding the DBK200 Series, refer to the *DBK Option Cards and Modules User's Manual* (p/n 457-0905). A copy is included on the Data Acquisition CD and on our website.



Reference Notes:
During software installation, Adobe PDF versions of user manuals are automatically installed onto your hard drive as a part of product support. The default location is in the **Programs** group, which can be accessed from the Windows Desktop. The documents can also be read directly from the CD. You will need Adobe Acrobat or the Acrobat Reader.

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Device Overviews 1

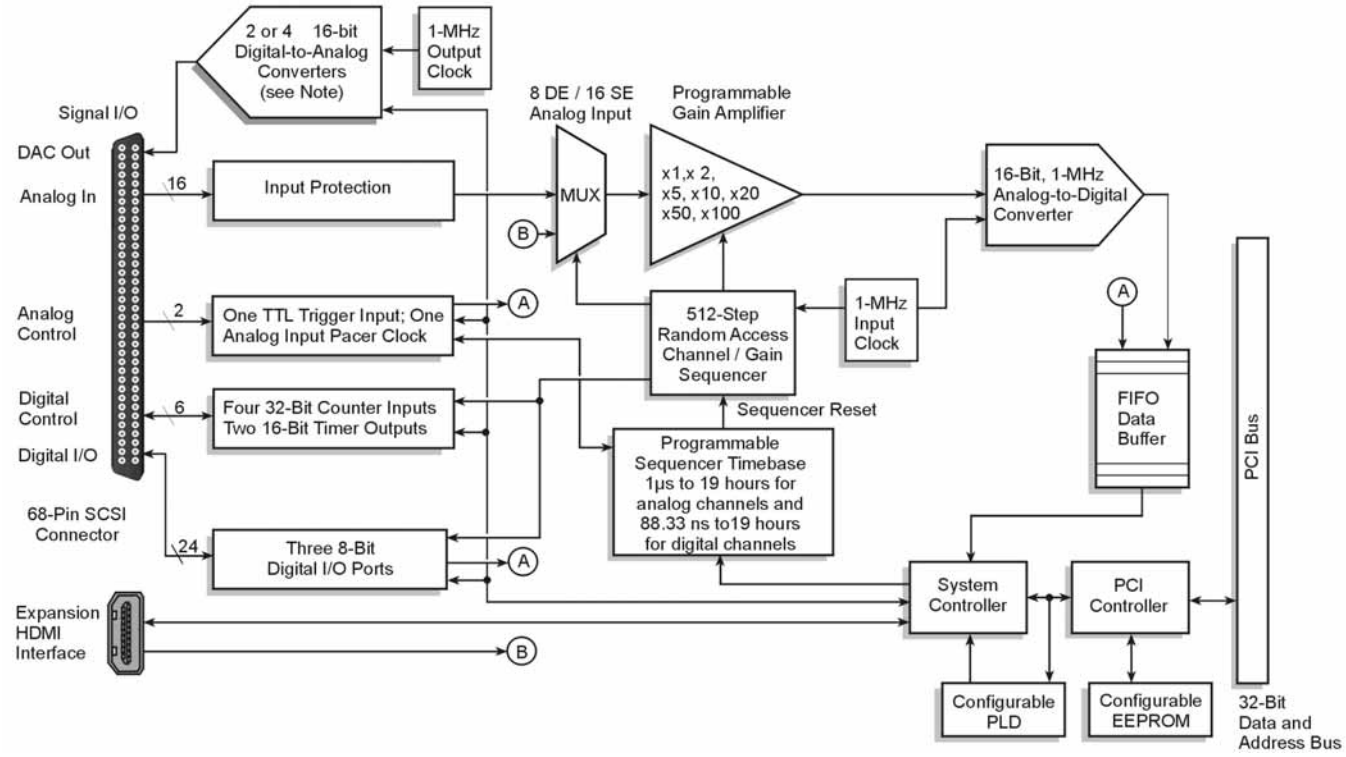
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DaqView can only be used with one DaqBoard at a time. DASYLab and LabView can be used with multiple boards. For multiple board use (via custom programming) refer to the *Using Multiple Devices* section of the *Programmer's Manual*.

Reference Note:
Programming topics are covered in the *Programmer's User Manual* (p/n 1008-0901). As a part of product support, this manual is automatically loaded onto your hard drive during software installation. The default location is the Programs group, which can be accessed through the Windows Desktop.

Reference Note:
For board details refer to Chapter 6, *Specifications*.

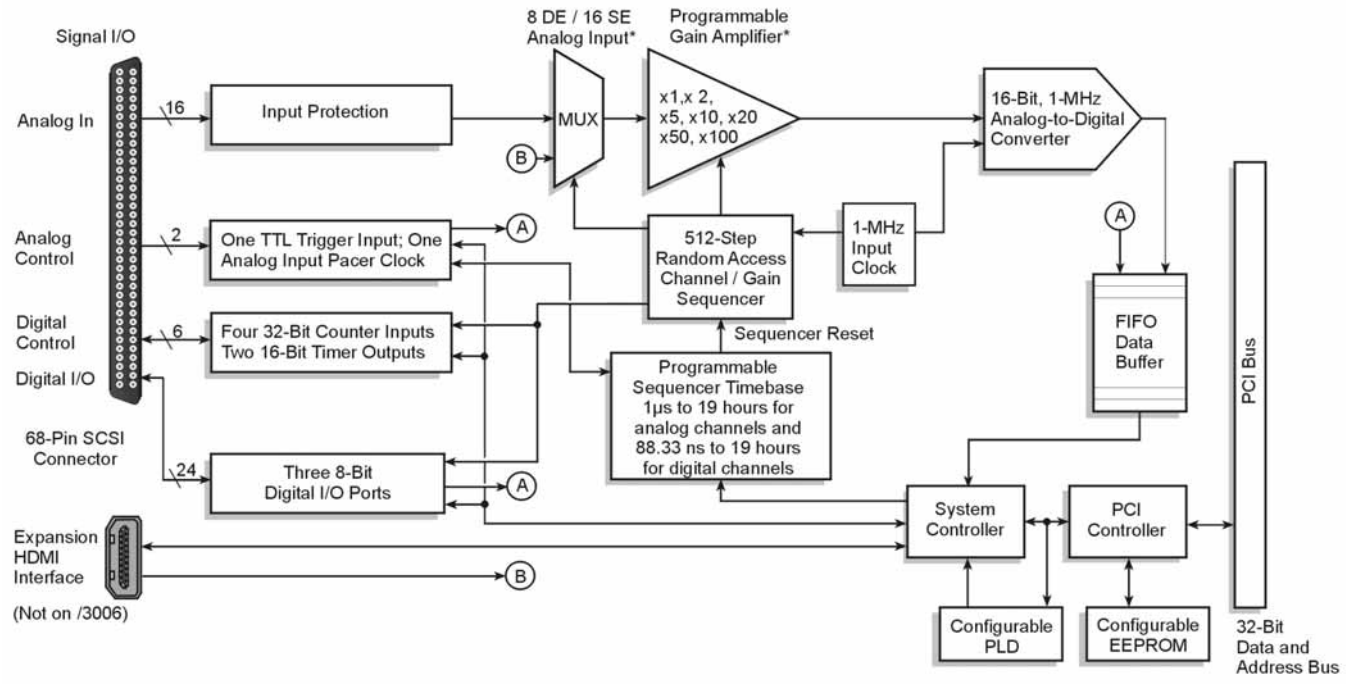
Block Diagrams



Block Diagram for DaqBoard/3000 and /3001

Note: DaqBoard/3000 has two 16-Bit Digital-to-Analog Converters.
DaqBoard/3001 has four 16-Bit Digital-to-Analog Converters.

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Block Diagram for DaqBoard/3005 and /3006

*** Note**: DaqBoard/3006 has 16 single-ended analog inputs; ±10V input range only; it has no differential input. DaqBoard/3006 has no HDMI interface.

Connections

Reference Note:
For the DaqBoard/3000 Series **installation procedure**, refer to the *DaqBoard Installation Guide (1033-0940)*. A copy of the guide is included at the beginning of this manual.

SCSI - 68 pin

All input and output signals are available at the 3000 Series board's 68-pin SCSI connector. Chapter 2 includes a pinout. A TB-100 screw-terminal board or a DBK215 BNC / screw-terminal module can be used to make all signal I/O connections. Either of these two termination options can be connected to the DaqBoard/3000 Series SCSI connector via one of the following cables.

CA-G55	68-conductor ribbon expansion cable. 3 feet.
CA-G56	68-conductor shielded expansion cable. 3 feet.
CA-G56-6	68-conductor shielded expansion cable. 6 feet.

HDMI

The HDMI connector can be used to connect a PDQ30 analog expansion module to a DaqBoard/3000 Series board. Details are provided in Chapter 2 of this manual. Cable CA-266-3 (3 ft.) [or CA-266-6 (6 ft.)] is used to connect the PDQ30 to the 3000 Series board.

The HDMI connector is not present on DaqBoard/3006.

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I/O Comparison Matrix

Product or System	Analog Input Channels	Input Ranges	Analog Output Channels	Digital I/O Channels	Counter Inputs	Timer Outputs
DaqBoard/3000	16SE / 8DE	7	2	24	4	2
DaqBoard/3001	16SE / 8DE	7	4	24	4	2
DaqBoard/3005	16SE / 8DE	7	0	24	4	2
DaqBoard/3006	16SE only	1	0	24	4	2
DaqBoard/3000 *with* PDQ30	64SE / 32DE	7	2	24	4	2
DaqBoard/3001 *with* PDQ30	64SE / 32DE	7	4	24	4	2
DaqBoard/3005 *with* PDQ30	64SE / 32DE	7	0	24	4	2

The DaqBoard/3000 Series boards feature a 16-bit/1-MHz A/D converter, 16 analog input channels [user expandable up to 64], up to four 16-bit/1-MHz analog outputs, 24 high-speed digital I/O channels, 2 timer outputs, and four 32-bit counters.

All analog I/O, digital I/O, and counter/timer I/O can operate synchronously and simultaneously, guaranteeing deterministic I/O timing amongst all signal types. The DaqBoard/3000 Series boards include a high-speed, low-latency, highly deterministic control output mode that operates independent of the PC. In this mode both digital and analog outputs can respond to analog, digital and counter inputs as fast as 2µsec.

Other Hardware Features Include:

- Encoder measurements up to 20 MHz, including Z-channel zeroing
- Frequency and Pulse-width measurements with 20.83 nsec resolution
- Timing mode: can measure the time between two counter inputs to 20.83 nsec resolution
- Self-calibration

The DaqBoard/3000 series offers up to 12-MHz scanning of all digital input lines. Digital inputs and counter inputs can be synchronously scanned [along with analog inputs] but do not affect the overall A/D rate because they use no time slot in the scanning sequencer. For example, one analog input can be scanned at the full 1-MHz A/D rate along with digital and counter input channels. The 1-MHz A/D rate is unaffected by additional digital and counter channels.

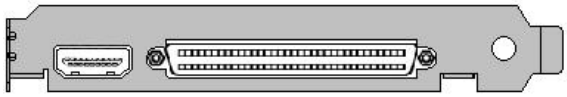
Adding analog input channels to a DaqBoard/3000 Series board is easy. An additional 48 single-ended [or 24 differential] analog input channels can be added to each board with the optional PDQ30 expansion module.* The PDQ30 connects to the Daqboard/3000 series card via an external cable. With the DaqBoard/3000's 1-MHz aggregate sample rate, users can easily add multiple analog expansion channels and still have enough bandwidth to have a per-channel sample rate in the multiple kHz range.

*DaqBoard/3006 does not support PDQ30.

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Signal I/O

One 68-pin connector provides access to the 16SE/8DE analog input channels, 24 digital I/O lines, counter/timer channels, and analog outputs (when applicable). With exception of DaqBoard/3006, a HDMI connector is also located on the orb. The HDMI provides connection for channel expansion with the PDQ30.



Orb with HDMI and 68-Pin SCSI Connectors
Note: The HDMI connector is not present on the DaqBoard/3006.

Analog Input

The DaqBoard/3000 series has a 16-bit, 1-MHz A/D coupled with 16 single-ended, or 8 differential analog inputs. Seven software programmable ranges provide inputs from ±10V to ±100 mV full scale [with exception of DaqBoard/3006 which has a fixed single-ended range of ±10V.] Each channel can be software-configured for a different range, as well as for single-ended or differential bipolar input.

Synchronous I/O

The DaqBoard/3000 series has the ability to make analog measurements and scan digital and counter inputs, while synchronously generating up to four analog outputs.

Additionally, while digital inputs and counter inputs can be synchronously scanned along with analog inputs, they do not affect the overall A/D rate because they use no time slot in the scanning sequencer. For example, one analog input can be scanned at the full 1-MHz A/D rate along with digital and counter input channels. The 1-MHz A/D rate is unaffected by the additional digital and counter channels.

Input Scanning

DaqBoard/3000 Series devices have several scanning modes to address a wide variety of applications. A 512-location scan buffer can be loaded by the user with any combination of analog input channels. All analog input channels in the scan buffer are measured sequentially at 1 µsec per channel. The user can also specify that the sequence repeat immediately, or repeat after a programmable delay from 0 to 19 hours, with 20.83 nsec resolution. For example, in the fastest mode, with a 0 delay, a single analog channel can be scanned continuously at 1 Msamples/s; two analog channels can be scanned at 500K samples/seach; 16 analog input channels can be scanned at 62.5 Ksamples/s.

The digital and counter inputs can be read in several modes. First, via software the digital inputs or counter inputs can be read *asynchronously* at anytime before, during, or after an analog input scan sequence. This software mode is not deterministic as to exactly when a digital or counter input is read relative to an analog input channel.

In either of the two synchronous modes, the digital inputs and/or counter inputs are read with deterministic time correlation to the analog inputs. In the *once-per-scan mode*, all of the enabled digital inputs and counter inputs are read during the first analog measurement of an analog input scan sequence. The advantage of this mode is that the digital and counter inputs do not consume an analog input time slot, and therefore do not reduce the available bandwidth for making analog input measurements. For example, presume all 24 bits of digital input are enabled, and all four 32-bit counters are enabled, and eight channels of analog inputs are in the scan sequence at full 1µsec/channel rate. At the beginning of each analog input scan sequence, which would be 8 µsec in total duration, all digital inputs and counter inputs will be measured and sent to the PC during the first µsec of the analog scan sequence.

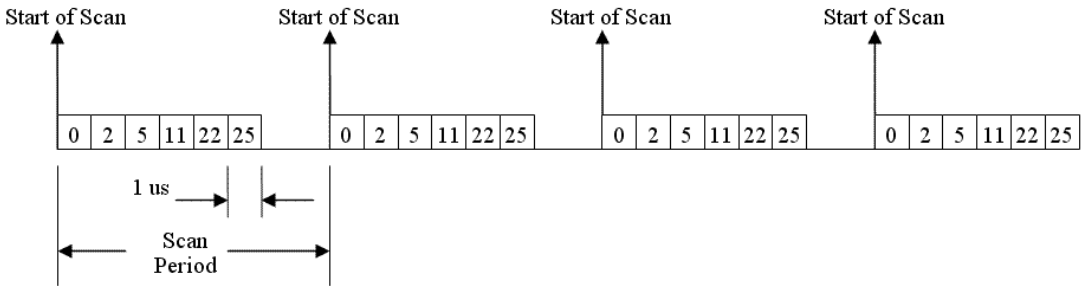
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Another synchronous mode allows digital inputs to be scanned every time an analog input channel is scanned. For example, if eight analog inputs are scanned at 1 µsec per channel continuously, and 24 bits of digital inputs are enabled, then the 24 bits of digital inputs will be scanned at 24 bits per 1 µsec. If counters are enabled in this mode, they will be scanned at once per scan, in the same manner as in the first example above.

Note: It is not necessary to read counters as often as it is to read digital inputs. This is because counters continue to count pulses regardless of whether or not they are being read by the PC.

Example 1: Analog channel scanning of voltage inputs

The figure below shows a simple acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25.) Each of these analog channels can have a different gain. The acquisition is triggered and the samples stream to the PC via DMA. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz.



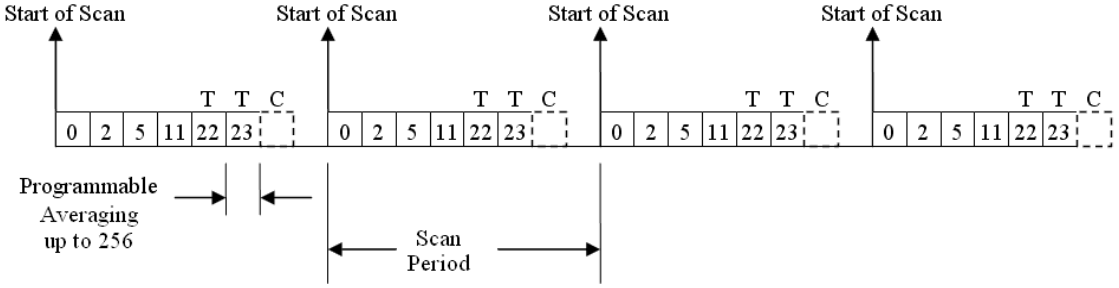
Notice that some of the analog channels in the scan group are from a PDQ30 expansion module. All analog channels are sampled at the same rate of 1us. Analog channels on the PDQ30 can also have any of the gain ranges applied.

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Example 2: Analog channel scanning of voltage and temperature inputs

The figure below shows a more complicated acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch23.) Each of these analog channels can have a different gain. Two of the channels (22 and 23) are from a PDQ30 expansion module. These two channels can be programmed to directly measure thermocouples. In this mode, oversampling is programmable up to 256 oversamples per channel in the scan group. When oversampling is applied, it is applied to all analog channels in the scan group, including temperature and voltage channels. (Digital channels are not oversampled.) If the desired number of oversamples is 256 then each analog channel in the scan group will take 256 microseconds, the returned 16-bit value represents an average of 256 consecutive 1us samples of that channel. The acquisition is triggered and 16-bit values (each representing an average of 256) stream to the PC via DMA.

Since two of the channels in the scan group are temperature channels, the acquisition engine will be required to read a cold-junction-compensation (CJC) temperature every scan. In fact, depending upon which PDQ30 channels are being used for temperature, there may be a CJC temperature required for each temperature channel in the scan. Each 4 channel terminal block of the PDQ30 shares one CJC so if all temperature channels are grouped on one (of the six) terminal blocks, then only one CJC temperature measurement will need to be made per scan. For every PDQ30 terminal block that is measuring at least one temperature channel, one additional CJC temperature measurement will be automatically added to the scan group. This increases the scan period and reduces the maximum scanning frequency.



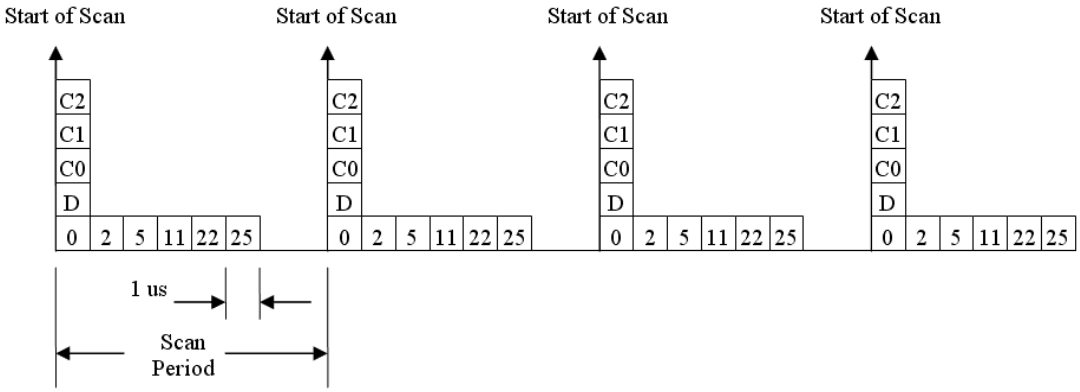
In this example, the desired number of oversamples is 256, therefore each analog channel in the scan group requires 256 microseconds to return one 16-bit value. The oversampling is also done for CJC temperature measurement channels. The minimum required scan period for this example is therefore 7 X 256 us or 1792 microseconds. The maximum scan frequency is the inverse of this number, 558 Hz.

Autozero may also be employed. This adds more channels to the scan group and further reduces the maximum scan frequency. Auto zero channels read a shorted analog input that is internal to the PDQ30. Auto zeroing reduces drift due to fluctuating ambient temperatures or ambient temperatures outside the DC specifications.

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Example 3: Analog and digital channel scanning, once per scan mode

The figure below shows a more complicated acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25) and 4 digital channels (16-bits of digital IO, 3 counter inputs.) Each of the analog channels can have a different gain and each of the counter channels can be put into a different mode (totalizing, pulsewidth, encoder, etc.) The acquisition is triggered and the samples stream to the PC via DMA. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. All of the digital channels are sampled at the start of scan and do not require additional scanning bandwidth as long as there is at least one analog channel in the scan group. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz.

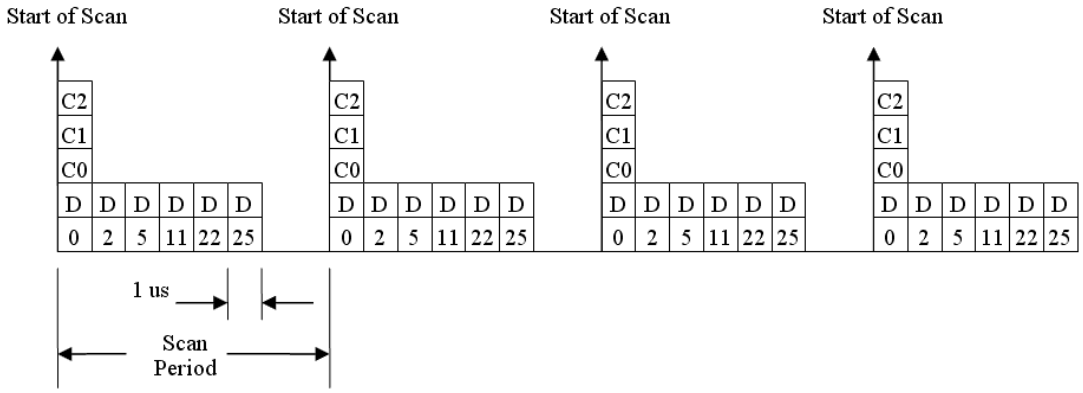


The counter channels could be returning only the lower 16-bits of count value if that is sufficient for the application. They could also be returning the full 32-bit result if necessary. Similarly, the digital input channel could be the full 24 bits if desired or only 8 bits if that is sufficient. If the 3 counter channels are all returning 32 bit values and the digital input channel is returning a 16 bit value, then 13 samples are being returned to the PC every scan period, each sample being 16-bits. 32-bit counter channels are divided into two 16-bit samples, one for the low word and the other for the high word. If the maximum scan frequency is 166,666 Hz then the data bandwidth streaming into the PC is 2.167 MSamples per second. Some slower PCs may have a problem with data bandwidths greater than 6 MSamples per second.

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Example 4: Sampling digital inputs for every analog sample in a scan group

The figure below shows another acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25) and 4 digital channels (16-bits of digital input, 3 counter inputs.) Each of the analog channels can have a different gain and each of the counter channels can be put into a different mode (totalizing, pulsewidth, encoder, etc.) The acquisition is triggered and the samples stream to the PC via DMA. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. All of the digital channels are sampled at the start of scan and do not require additional scanning bandwidth as long as there is at least one analog channel in the scan group. The 16-bits of digital input are sampled for every analog sample in the scan group. This allows up to 1MHz digital input sampling while the 1MHz analog sampling bandwidth is aggregated across many analog input channels. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz. Note that digital input channel sampling is not done during the "dead time" of the scan period where no analog sampling is being done either.



If the 3 counter channels are all returning 32 bit values and the digital input channel is returning a 16 bit value, then 18 samples are being returned to the PC every scan period, each sample being 16-bits. 32-bit counter channels are divided into two 16-bit samples, one for the low word and the other for the high word. If the maximum scan frequency is 166,666 Hz then the data bandwidth streaming into the PC is 3 MSamples per second. Some slower PCs may have a problem with data bandwidths greater than 6 MSamples per second.

Analog Input & Channel Expansion

The DaqBoard/3000 series has a 16-bit, 1-MHz A/D coupled with 16 single-ended, or 8 differential analog inputs. Seven software programmable ranges provide inputs from ±10V to ±100 mV full scale. Each channel can be software-configured for a different range, as well as for single-ended or differential bipolar input. A hybrid PGIA on the boards is guaranteed to settle to the specified accuracy while operating at the full 1 Msample/s rate.

Adding additional analog input channels to the /3000 series boards is easy with the optional PDQ30 expansion module. The PDQ30 connects to the board via cable and does not consume a PCI slot. PDQ30 adds an additional 48 single-ended or [24 differential-ended] analog inputs for a total channel capacity of 64 single-ended [or 32 differential] inputs.

Measurement speed of PDQ30 channels is the same 1 Msample/s exhibited by the /3000 board channels. The DaqBoard/3000 Series supports up to four boards per PC, effectively quadrupling the number of channels.

The PDQ30 attaches via the CA-266-3 cable to the HDMI expansion connector on the orb of the DaqBoard, with exception of the DaqBoard/3006.*

*DaqBoard/3006 has no HDMI connector and is intended for small channel applications for which expansion is not a desired option.

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Bus Mastering DMA

The DaqBoard/3000 series supports Bus Mastering DMA. Multiple DMA channels allow analog and digital/counter input data, as well as analog and digital output data to flow between the PC and the DaqBoard/3000 series without consuming valuable CPU time. The driver supplied with the DaqBoard/3000, as well as all other third-party software support such as LabVIEW®, automatically utilize Bus Mastering DMA to efficiently conduct I/O from the PC to the DaqBoard.

Triggering

Triggering can be the most critical aspect of a data acquisition application. The DaqBoard/3000 series supports a full complement of trigger modes to accommodate any measurement situation.

Hardware Analog Triggering. TheDaqBoard/3000 Series uses true analog triggering, whereby the trigger level programmed by the user sets an analog DAC, which is then compared in hardware to the analog input level on the selected channel. The result is analog trigger latency which is guaranteed to be less than1 µs. Any analog channel can be selected as the trigger channel, including built-in or PDQ30 expansion channels. The user can program both the trigger level, as well as the rising or falling edge and hysteresis.

Digital Triggering. A separate digital trigger input line is provided, allowing TTL-level triggering with latencies guaranteed to be less than 1 µs. Both the logic levels (1 or 0), as well as the rising or falling edge can be programmed for the discrete digital trigger input.

Pattern Triggering. The user can specify a 16-bit digital pattern to trigger an acquisition, including the ability to mask or ignore specific bits.

Software-Based Channel Level Triggering. This mode differs from the modes just discussed because the readings [analog, digital, or counter] are interrogated by the PC in order to detect the trigger event. Triggering can also be programmed to occur when one of the counters reaches, exceeds, or is within a programmed window.

Any of the built-in counter/totalizer channels can be programmed as a trigger source. Triggers can be detected on scanned digital input channel patterns as well. Normally software-based triggering results in long latencies from the moment a trigger condition is detected until the instant data is acquired. However, theDaqBoard/3000 Series circumvents this undesirable situation by use of pre-trigger data. Specifically, when software-based-triggering is employed, and the PC detects that a trigger condition has occurred, (which may be thousands of readings after the actual occurrence of the signal), the DaqBoard driver automatically looks back to the location in memory, to where the actual trigger-causing measurement occurred. The acquired data presented to the user begins at the point where the trigger-causing measurement occurs. The maximum latency in this mode is equal to one scan period

Stop Trigger. Any of the software trigger modes previously described, including scan count, can be used to stop an acquisition. Thus an acquisition can be programmed to begin on one event, such as a voltage level, and then can stop on another event, such as a digital pattern.

Pre-Triggering and Post-Triggering Modes. Six modes of pre-triggering and post-triggering are supported, providing a wide variety of options to accommodate any measurement requirement. When using pre-trigger, the user must use software-based triggering to initiate an acquisition. The six modes are:

- ***No pre-trigger, post-trigger stop event***. This, the simplest of modes, acquires data upon receipt of the trigger, and stops acquiring upon receipt of the stop-trigger event.
- ***Fixed pre-trigger with post-trigger stop event***. In this mode, the user specifies the number of pre-trigger readings to be acquired, after which, acquisition continues until a stop-trigger event occurs.
- ***No pre-trigger, infinite post-trigger***. No pre-trigger data is acquired in this mode. Instead, data is acquired beginning with the trigger event, and is terminated when the operator issues a command to halt the acquisition.
- ***Fixed pre-trigger with infinite post-trigger***. The user specifies the amount of pre-trigger data to acquire, after which the system continues to acquire data until the program issues a command to halt acquisition.

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- ***Variable pre-trigger with post trigger stop event***. Unlike the previous pre-trigger modes, this mode does not have to satisfy the pre-trigger number of readings before recognizing the trigger event. Thus the number of pre-trigger readings acquired is variable and dependent on the time of the trigger event relative to the start. In this mode, data continues to be acquired until the stop trigger event is detected. *Driver support only*.
- ***Variable pre-trigger with infinite post trigger***. This is similar to the mode described above, except that the acquisition is terminated upon receipt of a command from the program to halt the acquisition. *Driver support only*.

Calibration

Every range of a DaqBoard/3000 Series device is calibrated at the factory using a digital NIST traceable calibration method. This method works by storing a correction factor for each range on the unit at the time of calibration. The user can adjust the calibration of the board while it is installed in the acquisition system. This does not destroy the factory calibration supplied with the board. This is accomplished by having 3 distinct calibration tables in the DaqBoard/3000 series on-board EPROM, one which contains the factory cal, and two which are available for user calibration.

The user can select any of the three cal tables provided [factory, user or self-cal tables] by API call or from within factory-included software, DaqCal.

The user-friendly DaqCal application supports two calibration modes: Self-Cal and User-Cal.

- **Self-cal** can be performed automatically in minutes with included software and without the use of external hardware or instruments. Self-cal derives its tracebility through an on-board reference which has a stability of 0.005% per year.
- **User-cal** is for users that require traceability to international standards such as NIST. A 6-1/2 digital multimeter is required and user calibration software is included with step-by-step instructions for full calibration.

Note that a 2-year calibration period is recommended for DaqBoard/3000 Series boards.

Analog Output

DaqBoard/3000 and /3001 Only

DaqBoard/3000 has two 16-bit, 1 MHz analog output channels. DaqBoard/3001 has four such channels. The channels have an output range of -10V to +10V. Through the use of Bus Mastering DMA, each D/A output can continuously output a waveform at up to 1 MHz. This can be read from PC RAM or from a file on the hard disk. In addition, a program can asynchronously output a value to any of the D/As for non-waveform applications, presuming that the D/A is not already being used in the waveform output mode.

When used to generate waveforms, the D/As can be clocked in several different modes. Each D/A can be separately selected to be clocked from one of the following sources.

- **Asynchronous Internal Clock**. The on-board programmable clock can generate updates ranging from 1.5 Hz to 19 hours, independent of any acquisition rate.
- **Synchronous Internal Clock**. The rate of analog output update can be synchronized to the acquisition rate derived from 1 MHz to once every 19 hours.
- **Asynchronous External Clock**. A user-supplied external input clock can be used to pace the D/A, entirely independent of analog inputs.
- **Synchronous External Clock**. A user-supplied external input clock can pace both the D/A and the analog input.

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Digital Inputs and Outputs

Twenty-four TTL-level digital I/O lines are included in each of the DaqBoard/3000 Series boards. Digital I/O can be programmed in 8-bit groups as either inputs or outputs and can be scanned in several modes (see *Input Scanning*). Ports programmed as input can be part of the scan group and *scanned along with analog input channels*, or can be asynchronously accessed via the PC at any time, including when a scanned acquisition is occurring.

Two synchronous modes are supported when digital inputs are scanned along with analog inputs.

- **Scanning digital inputs at the start of each scan sequence**. In this mode the digital inputs are scanned at the start of each scan sequence, which means the rate at which they are scanned is dependent on the number of analog input channels and the delay period. For example, if 8 analog inputs were enabled with a 0 delay period, then the digital inputs in this mode would be scanned at once per 8µsec, i.e., 125 kHz.
- **Scanning digital inputs synchronously with every analog input channel**. In this synchronous mode, the enabled digital inputs are scanned synchronously with every analog input channel. So in the preceding example the digital inputs would be scanned at once per µsec, or 1 MHz. If no analog inputs were being scanned the digital inputs could be scanned at up to 12 MHz.

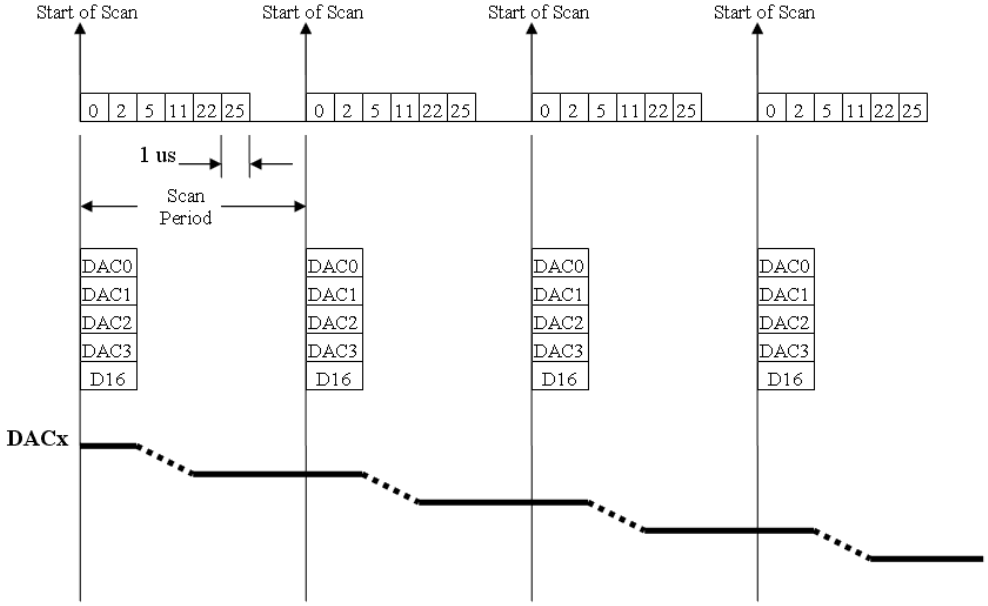
Digital Outputs and Pattern Generation

Digital outputs can be updated asynchronously at anytime before, during or after an acquisition. Two of the 8-bit ports can also be used to generate a 16-bit digital pattern at up to 12 MHz. The DaqBoard/3000 Series boards support digital pattern generation via Bus Mastering DMA. In the same manner as analog output, the digital pattern can be read from PC RAM or a file on the hard disk. Digital pattern generation is clocked in the same four modes as described with analog output.

The ultra low-latency digital output mode allows a digital output to be updated based on the level of an analog, digital or counter input. In this mode, the user associates a digital output bit with a specific input, and specifies the level of the input where the digital output changes state. The response time in this mode is dependent on the number of input channels being scanned, and can typically be in the range of 2 to 20 µsec.

Example 5: Analog channel scanning of voltage inputs and streaming analog outputs

The figure below shows a simple acquisition. The scan is programmed pre-acquisition and is made up of 6 analog channels (Ch0, Ch2, Ch5, Ch11, Ch22, Ch25.) Each of these analog channels can have a different gain. The acquisition is triggered and the samples stream to the PC via DMA. Each analog channel requires one microsecond of scan time therefore the scan period can be no shorter than 6 us for this example. The scan period can be made much longer than 6 us, up to 19 hours. The maximum scan frequency is one divided by 6us or 166,666 Hz.



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This example has all 4 DACs being updated and the 16-bits of digital IO. These updates are performed at the same time as the acquisition pacer clock (also called the scan clock.) All 4 DACs and the 16-bits of pattern digital output are updated at the beginning of each scan. Note that the DACs will actually take up to 4 us after the start of scan to settle on the updated value. This is due to the amount of time to shift the digital data out to the DACs plus the actual settling time of the digital to analog conversion.

The data for the DACs and pattern digital output comes from a PC-based buffer. The data is streamed across the PCI bus to the Daqboard/3000 via DMA.

It is possible to update the DACs and pattern digital output with the DAC pacer clock (either internally generated or externally applied.) In this case, the acquisition input scans are not synchronized to the analog outputs or pattern digital outputs. It is possible to synchronize everything (input scans, DACs, pattern digital outputs) to one clock. That clock can be either internally generated or externally applied.

Counter Inputs

Four 32-bit counters are built into the DaqBoard/3000 Series boards. Each of the four counters accepts frequency inputs up to 20 MHz. The high-speed counter channels can be configured on a per-channel basis. Possible configurations include the following modes:

- **Counter**
- **Period**
- **Pulse width**
- **Time between edges**
- **Multi-axis quadrature encoder**



Reference Note:
For detailed information regarding the various counter modes refer to Chapter 5, *Counter Input Configuration Modes*.

The counters can concurrently monitor time periods, frequencies, pulses, and other event driven incremental occurrences directly from encoders, pulse-generators, limit switches, proximity switches, and magnetic pick-ups.

As with all other inputs to the boards, the counter inputs can be read asynchronously under program control, or synchronously as part of an analog and digital scan group based on a programmable internal timer or an external clock source.

The boards support quadrature encoders with up to 2 billion pulses per revolution, 20 MHz input frequencies, and x1, x2, x4 count modes. With only A-phase and B-phase signals, 2 channels are supported. With A-phase, B-phase, and Z-index signals, 1 channel is supported.

Each input can be debounced from 500 ns to 25.5 ms (total of 16 selections) to eliminate extraneous noise or switch induced transients. Encoder input signals must be within -15V to +15V and the switching threshold is TTL (1.3V). Power is available for encoders, +5V at up to 500 mA.

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Timer Outputs

Two 16-bit timer outputs are built into every 3000 series board. Each timer is capable of generating a different square wave with a programmable frequency in the range of 16 Hz to 1 MHz.

Example 6: Timer Outputs

Timer outputs are programmable square waves. The period of the square wave can be as short as 1us or as along as 65535 us. See the table below for some examples.

Divisor	Timer Output Frequency
1	1 MHz
100	10 kHz
1000	1 kHz
10000	100 Hz
65535	15.259 Hz

There are 2 timer outputs that can generate different square waves. The timer outputs can be updated asynchronously at any time. Both timer outputs can also be updated during an acquisition as the result of setpoints applied to analog or digital inputs. See the section on pattern detection setpoints for more information and examples.

Multiple DaqBoards per PC

The features described for DaqBoard/3000 Series boards can be replicated up to four times, as up to four boards can be installed in a single host PC. The serial number on each board differentiates one from another, and a user-selected name can be assigned to each board for easy recognition within the program. When multiple boards are installed they can be operated synchronously. This is done by designating one board as the master. The other boards [slaves] are synchronized to the master by the pacer clock which is externally routed to the designated slave boards.

Software

Included with the /3000 Series is a complete set of drivers and example programs for the most popular programming languages and software packages. Driver support includes Visual Basic®, C/C++, LabVIEW®, DASYLab®, and MATLAB®. DaqCOM™ provides Windows®-basedActiveX/COM-based programming tools for Microsoft® VisualStudio® and VisualStudio.NET®. Also included with the /3000 Series is new DaqView™ software, a comprehensive Out-of-the-Box™ application that enables set-up, data logging, and real-time data viewing without existing programming skills. Optional DaqView/Pro also adds features such as direct-to-Excel® enhancements, FFT analysis, statistics, etc. DaqView software provides Out-of-the-Box™, quick and easy set up and collection of data.

Daq devices have software options capable of handling most applications. Three types of software are available:

- ready-to-use graphical programs, e.g., DaqView, DaqViewXL, and post acquisition data analysis programs such as PostView, DIAdem, and eZ-PostView
- drivers for third-party, icon-driven software such as DASYLab and LabView
- various language drivers to aid custom programming using API

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Ready-to-use programs are convenient for fill-in-the-blank applications that do not require programming for basic data acquisition and display:

- DaqView is a Windows-based program for basic set-up and data acquisition. DaqView lets you select desired channels, gains, transducer types (including thermocouples), and a host of other parameters with a click of a PC's mouse. DaqView lets you stream data to disk and display data in numerical or graphical formats. PostView is a post-acquisition waveform-display program within DaqView.
- ViewXL/Plus allows you to interface directly with Microsoft Excel to enhance data handling and display. Within Excel you have a full-featured Daq control panel and all the data display capabilities of Excel.
- Post acquisition data analysis programs, e.g., PostView, DIAdem, and eZ-PostView, typically allow you to view and edit post-acquisition data.
- The Daq Configuration control panel allows for interface configuration, testing, and troubleshooting.

Each Daq system comes with an Application Programming Interface (API). API-language drivers include C/C++ and Visual Basic. The latest software is a 32-bit version API.



Reference Notes:

- The software documents for: *DaqView*, *ViewXL*, and *Post Acquisition Data Analysis* are not included as part of the hardcopy manual, but are available in PDF version. See the PDF Note, below.
- Programming topics are covered in the *Programmer's User Manual* (1008-0901). As a part of product support, this manual is automatically loaded onto your hard drive during software installation. The default location is the Programs directory, which can be accessed through the Windows Desktop.

PDF Note: During software installation, Adobe® PDF versions of user manuals will automatically install onto your hard drive as a part of product support. The default location is in the **Programs** group, which can be accessed from the *Windows Desktop*. Refer to the PDF documentation for details regarding both hardware and software.

A copy of the Adobe Acrobat Reader® is included on your CD. The Reader provides a means of reading and printing the PDF documents. Note that hardcopy versions of the manuals can be ordered from the factory.

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Connections and Pinouts 2

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Pinout for DaqBoard/3000 Series Boards …… 2-2
TB-100 Terminal Connector Option …… 2-3
PDQ30 Analog Expansion and DBK215 Connector Options …… 2-4

CAUTION



Turn off power to all devices connected to the system before connecting cables or setting configuration jumpers and switches. Electrical shock or damage to equipment can result even under low-voltage conditions.

CAUTION



The discharge of static electricity can damage some electronic components. Semiconductor devices are especially susceptible to ESD damage. You should always handle components carefully, and you should never touch connector pins or circuit components unless you are following ESD guidelines in an appropriate ESD controlled area. Such guidelines include the use of properly grounded mats and wrist straps, ESD bags and cartons, and related procedures.

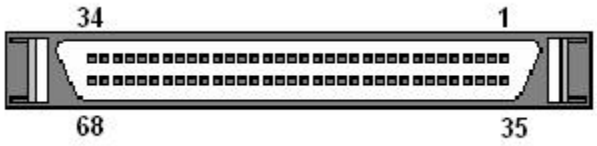
Overview

DaqBoard/3000 Series boards communicate [external from the host PC] through a 68-pin SCSI connector. A TB-100 terminal board can be used to provide convenient screw-terminal connections for all signal I/O. Instead of the TB-100 [which is an open board], a DBK215 module can be used for connectivity. The DBK215 includes 16 BNC connectors in addition to screw-terminals.

Pinouts for both the TB-100 and the DaqBoard/3000 Series boards follow. In addition, use of the optional PDQ30 analog expansion module is discussed, as is the DBK215 should refer to Appendix A.

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Pinout for DaqBoard/3000 Series Boards



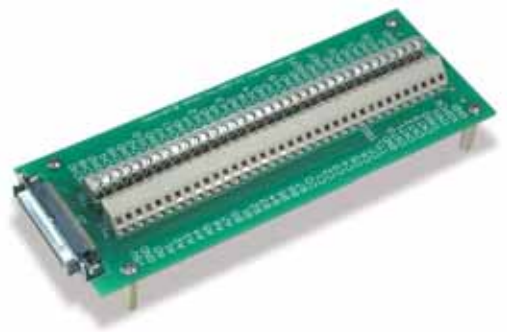
Pin numbers refer to the 68-pin SCSI female connector, located on the DaqBoard/3000.				
Function	**Pin**		**Pin**	**Function**
Analog input Channel 8	**34**		**68**	Analog input Channel 0
Analog input Channel 1	**33**		**67**	Analog Common
Analog Common	**32**		**66**	Analog input Channel 9
Analog input Channel 10	**31**		**65**	Analog input Channel 2
Analog input Channel 3	**30**		**64**	Analog Common
Analog Common	**29**		**63**	Analog input Channel 11
Analog input Channel 4	**28**		**62**	Low Level Sense Common
Analog Common	**27**		**61**	Analog input Channel 12
Analog input Channel 13	**26**		**60**	Analog input Channel 5
Analog input Channel 6	**25**		**59**	Analog Common
Analog Common	**24**		**58**	Analog input Channel 14
Analog input Channel 15	**23**		**57**	Analog input Channel 7
Analog Output 0 (**DAC0**) Note 1	**22**		**56**	Analog Output 3 (**DAC3**) Note 1
Analog Output 1 (**DAC1**) Note 1	**21**		**55**	Analog Output 2 (**DAC2**) Note 1
SELFCAL	**20**		**54**	Digital Common
Vcc (+5 VDC)	**19**		**53**	Digital Common
Digital I/O line A0	**18**		**52**	Digital I/O line A1
Digital I/O line A2	**17**		**51**	Digital I/O line A3
Digital I/O line A4	**16**		**50**	Digital I/O line A5
Digital I/O line A6	**15**		**49**	Digital I/O line A7
Digital I/O line B0	**14**		**48**	Digital I/O line B1
Digital I/O line B2	**13**		**47**	Digital I/O line B3
Digital I/O line B4	**12**		**46**	Digital I/O line B5
Digital I/O line B6	**11**		**45**	Digital I/O line B7
Digital I/O line C0	**10**		**44**	Digital I/O line C1
Digital I/O line C2	**9**		**43**	Digital I/O line C3
Digital I/O line C4	**8**		**42**	Digital I/O line C5
Digital I/O line C6	**7**		**41**	Digital I/O line C7
TTL Trigger Input	**6**		**40**	Digital Common
Counter Input CTR0	**5**		**39**	Counter Input CTR1
Counter Input CTR2	**4**		**38**	Counter Input CTR3
Timer Output 0	**3**		**37**	Timer Output 1
A/D Pacer Clock Input/Output	**2**		**36**	Digital Common
DAC Pacer Clock I/O	**1**		**35**	Digital Common

Note 1: DaqBoard/3000 includes DAC0 and DAC1
DaqBoard/3001 includes DAC0, DAC1, DAC2, and DAC3
DaqBoard/3005 has no DACs
DaqBoard/3006 has no DACs

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TB-100 Terminal Connector Option

The TB-100 Terminal Connector option can be used to connect all signal I/O lines that are associated with a DaqBoard/3000 Series device. TB-100 connects to the DaqBoard's 68-pin SCSI connector via a 68-conductor cable: p/n CA-G55, CA-G56, or CA-G56-6.



TB-100 Pinout The "Pin" column refers to the pin no. on the 68-Pin SCSI Connector.

Screw Terminals for TB2 Side		Pin		Screw Terminals for TB1 Side		Pin
+5V	Vcc (+5 VDC)	19		ACH0	Analog Input Channel 0	68
GND	Digital Common	Note 1		ACH8	Analog Input Channel 8	34
A0	Digital I/O Line A0	18		AGND	Analog Common	Note 2
A1	Digital I/O Line A1	52		ACH1	Analog Input Channel 1	33
A2	Digital I/O Line A2	17		ACH9	Analog Input Channel 9	66
A3	Digital I/O Line A3	51		AGND	Analog Common	Note 2
A4	Digital I/O Line A4	16		ACH2	Analog Input Channel 2	65
A5	Digital I/O Line A5	50		ACH10	Analog Input Channel 10	31
A6	Digital I/O Line A6	15		AGND	Analog Common	Note 2
A7	Digital I/O Line A7	49		ACH3	Analog Input Channel 3	30
B0	Digital I/O Line B0	14		ACH11	Analog Input Channel 11	63
B1	Digital I/O Line B1	48		AGND	Analog Common	Note 2
B2	Digital I/O Line B2	13		ACH4	Analog Input Channel 4	28
B3	Digital I/O Line B3	47		ACH12	Analog Input Channel 12	61
B4	Digital I/O Line B4	12		AGND	Analog Common	Note 2
B5	Digital I/O Line B5	46		ACH5	Analog Input Channel 5	60
B6	Digital I/O Line B6	11		ACH13	Analog Input Channel 13	26
B7	Digital I/O Line B7	45		AGND	Analog Common	Note 2
C0	Digital I/O Line C0	10		ACH6	Analog Input Channel 6	25
C1	Digital I/O Line C1	44		ACH14	Analog Input Channel 14	58
C2	Digital I/O Line C2	9		AGND	Analog Common	Note 2
C3	Digital I/O Line C3	43		ACH7	Analog Input Channel 7	57
C4	Digital I/O Line C4	8		ACH15	Analog Input Channel 15	23
C5	Digital I/O Line C5	42		XDAC3	Analog Output, **DAC3**	56
C6	Digital I/O Line C6	7		SGND	Low Level Sense Common	62
C7	Digital I/O Line C7	41		POSREF	+5 VDC Positive Reference	20
TTLTRG	TTL Trigger Input	6		XDAC2	Analog Output, **DAC2**	55
GND	Digital Common	Note 1		NEGREF	- 5 VDC Negative Reference	54
CNT0	Counter Input CTR0	5		AGND	Analog Common	Note 2
CNT1	Counter Input CTR1	39		XDAC0	Analog Output, **DAC0**	22
CNT2	Counter Input CTR2	4		AGND	Analog Common	Note 2
CNT3	Counter Input CTR3	38		XDAC1	Analog Output, **DAC1**	21
TMR0	Timer Output 0	3		AGND	Analog Common	Note 2
TMR1	Timer Output 1	37		XAPCR	A/D Pacer Clock I/O	2
XDPCR	DAC Pacer Clock I/O	1		GND	Digital Common	Note 1
GND	Digital Common	Note 1		EGND	Earth Ground	N/A

Note 1: Digital Common Pins on the SCSI connector are: 35, 36, and 40.

Note 2: Analog Common Pins on the SCSI connector are: 24, 27, 29, 32, 59, 64, and 67

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PDQ30 Analog Expansion and DBK215 Connector Options



PDQ30 Analog Expansion Module



DBK215 16 BNC Connector Module

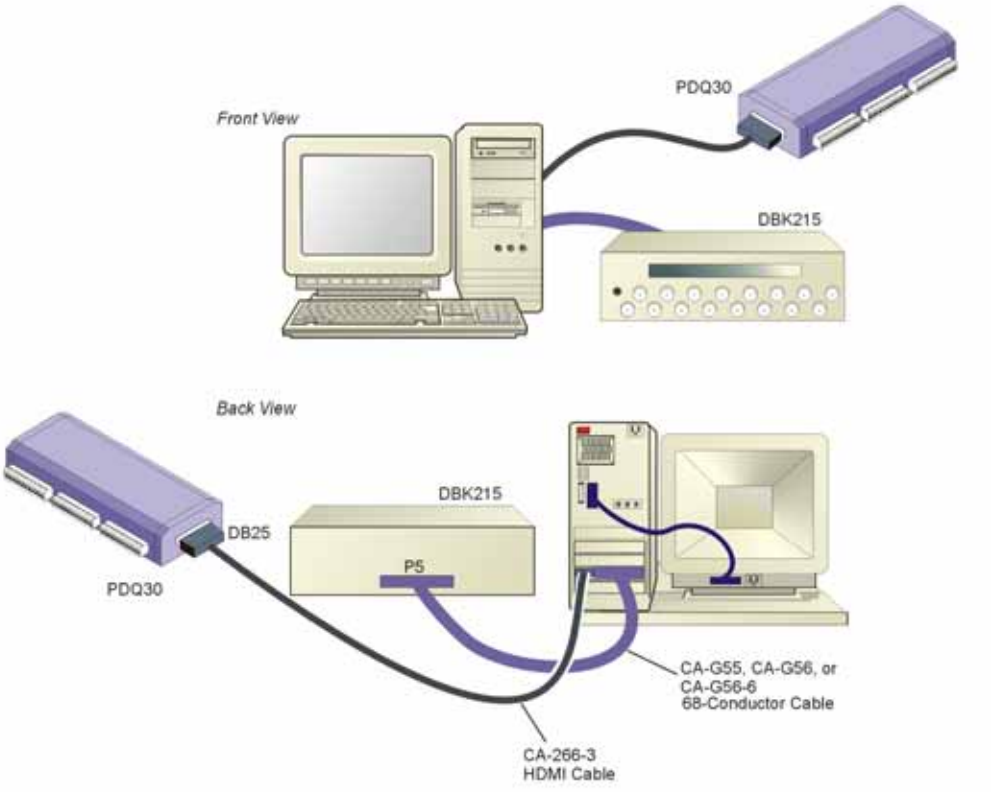
DaqBoard/3000 Series boards can connect to optional devices through either or both of the board's orb connectors.



DaqBoard/3000 Series Connector Layout*

***Note**: DaqBoard/3006 has no HDMI Connector and cannot be connected to a PDQ30.

- The HDMI connector can be used to connect a PDQ30 Analog Expansion Module to a DaqBoard/3000 Series board [other than a DaqBoard/3006]. A CA-266-3 (3-ft.) or a CA-266-6 (6-ft.) HDMI cable is used for this purpose.
- The 68-pin SCSI connector can be used to connect a TB-100 terminal option to the DaqBoard/3000 Series board via a CA-G55, CA-G56, or CA-G56-6 cable, or
- The 68-pin SCSI connector can be used to connect a DBK215 BNC/Screw-Terminal connector to the DaqBoard/3000 Series board. A CA-G55, CA-G56, or CA-G56-6 cable is used for this purpose.



DaqBoard/3000 Connected to a PDQ30 and to a DBK215
Note that a TB-100 Terminal Connector option can be used in place of the DBK215 option.

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DBK215

If you are not using a TB-100 terminal board connection option with your DaqBoard/3000 Series board you can, instead, make use of a DBK215 module. The DBK215 includes:

- BNC Access to 16 inputs or outputs (on front panel)
- on-board screw-terminal blocks*
- on-board socket locations for custom RC Filter networks*
- 68-pin SCSI connector (on rear panel)

* The top cover plate must be removed to access the terminal blocks and the RC filter network section of the DBK215's board.

The 68-pin SCSI connector (P5) connects to the DaqBoard/3000 Series board's 68-pin SCSI connector via a CA-G55, CA-G56, or CA-G56-6 cable.

The DBK215 provides BNC and screw-terminal access to all analog and digital I/O from the host data acquisition device. Related to the screw-terminals is a front panel slot for routing all I/O wiring.



Reference Notes:
The remainder of this chapter focuses on the PDQ30 Analog Expansion option. For details regarding using DaqBoard/3000 Series boards with DBK215 refer to Appendix A.

PDQ30

PDQ30 is an optional analog expansion module that, when connected to a DaqBoard/3000 series device, adds an additional 48 analog inputs. The features of the expansion channels are identical to the board's main channels, with exception that the PDQ30 channels can measure temperature when in differential mode. Refer to PDQ30 specifications sheet for channel input specifications.

With exception of DaqBoard/3006, a PDQ30 can be connected to a DaqBoard/3000 Series board via a three-foot long HDMI cable (CA-266-3) or a six-foot long cable (CA-266-6). The cable runs from the board's HDMI connector to the PDQ30's DB25 connector.

DaqBoard/3006 has no HDMI connector.

Connection Tips

CAUTION



Turn off power to the host PC and externally connected equipment prior to connecting cables or signal lines. Electric shock or damage to equipment can result even under low-voltage conditions.



Take ESD precautions (packaging, proper handling, grounded wrist strap, etc.)

Use care to avoid touching board surfaces and onboard components. Only handle boards by their edges (or ORBs, if applicable). Ensure boards do not come into contact with foreign elements such as oils, water, and industrial particulate.

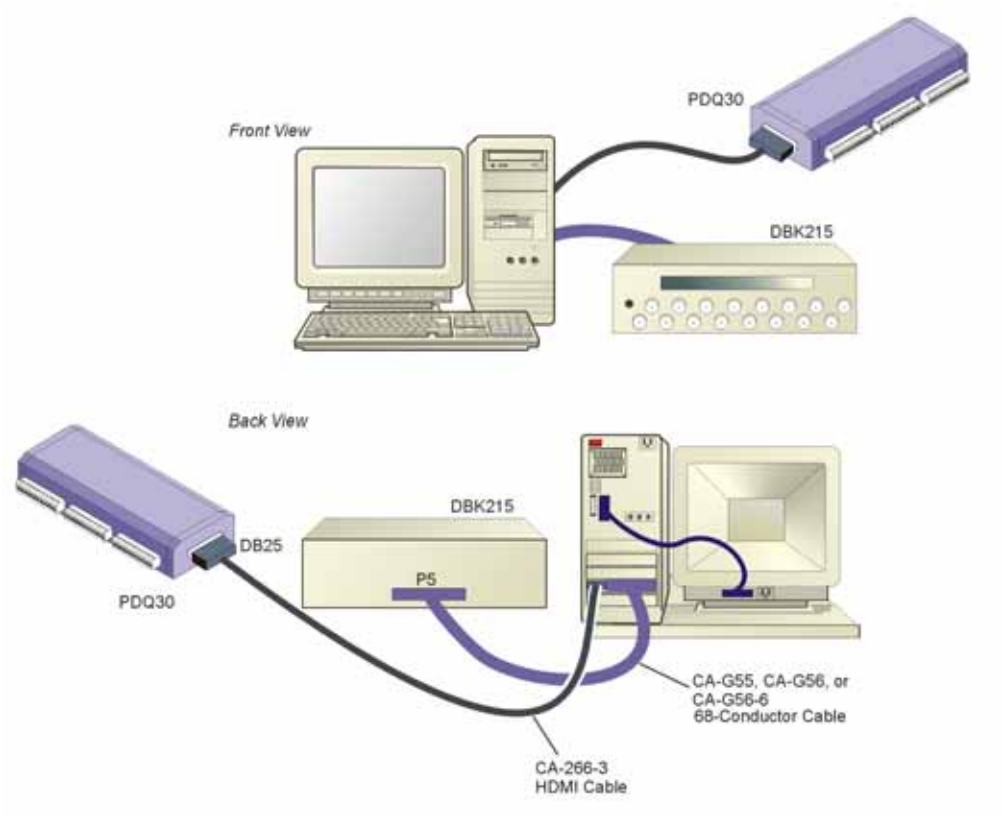
1. Ensure power is removed from all device(s) to be connected.
2. Observe ESD precautions when handling the board and making connections.
3. PDQ30's DB25 connector connects to a DaqBoard/3000 Series boards' HDMI connector via a CA-266-3 cable. The cable is 3 feet long.
4. Refer to the Declaration of Conformity in regard to meeting CE requirements.

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System Example

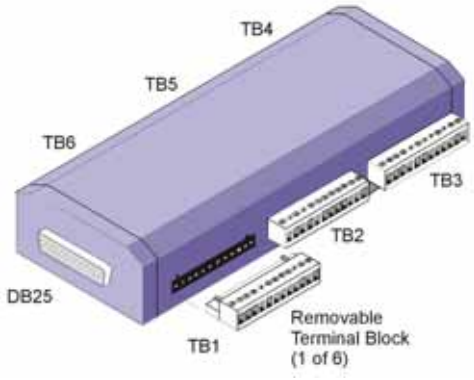
A DaqBoard/3000 Series system example which includes both a PDQ30 and a DBK215 is illustrated on page 2-4. For convenience, it has been repeated below. In regard to the PDQ30 aspect:

1) Connection from PDQ30 to DaqBoard/3000 is made via a CA-266-3 (or CA-266-6) HDMI cable.
2) PDQ30's analog input lines connect via removable screw-terminal blocks (TB1 through TB6).
3) A pinout for PDQ30 follows shortly.
4) Users of DBK215 should refer to Appendix A.
5) Instead of connecting a DBK215 to the DaqBoard/3000 series 68-pin SCSI connector, a TB-100 terminal board option can be connected. The TB-100 option is discussed on page 2-3.



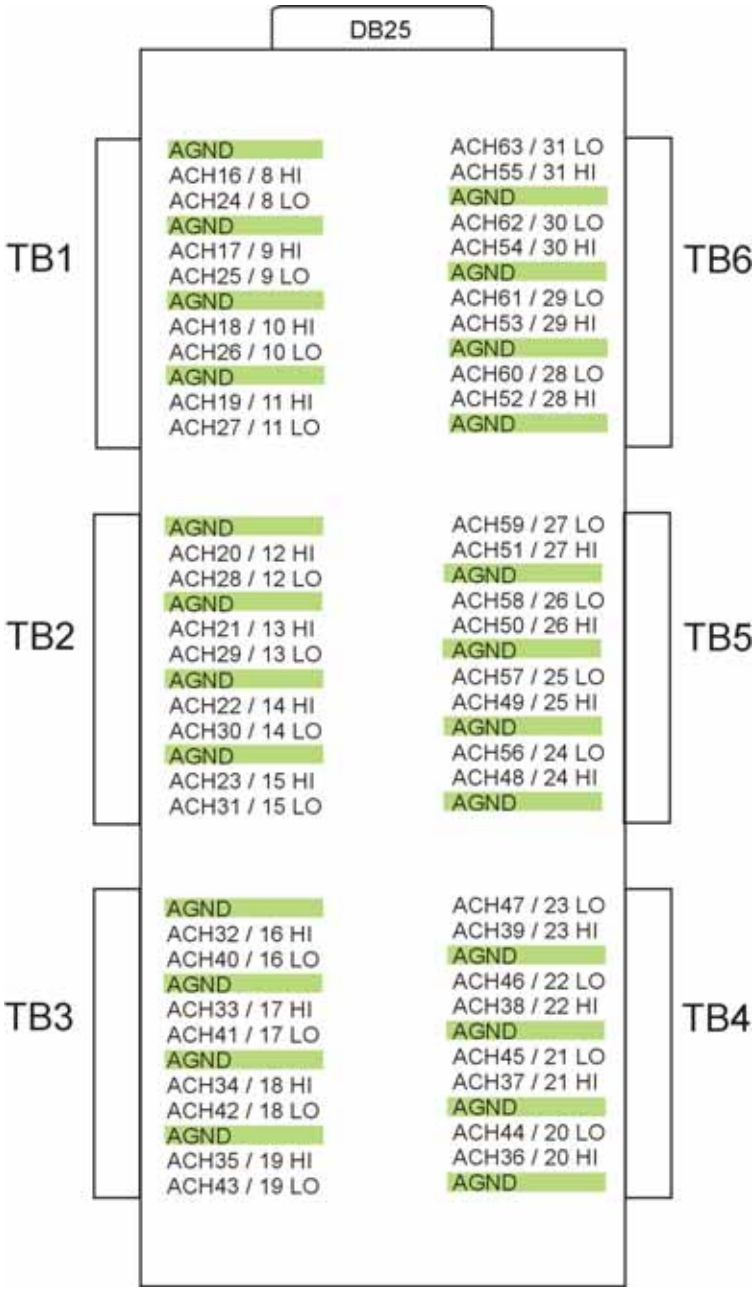
DaqBoard/3000 Connected to a PDQ30 and to a DBK215*

***Note**: The DBK215 offers screw terminal connections and BNC connections in an enclosure. If BNC connectors and an enclosure are not needed, a TB-100 Terminal Connector option can be connected to the 68-pin SCSI connector instead of the DBK215. See page 2-3 for TB-100 information. Refer to Appendix A for DBK215 information.



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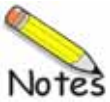
PDQ30 Terminal Block Pinouts (TB1 through TB6)



PDQ30 can measure 48 channels of voltage or 24 channels of temperature. The temperature measurement requires the use of Differential Mode.

Reference Notes:
For PDQ30 specifications, refer to chapter 6.

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CE Compliance & Noise Considerations 3

Overview …… 3-1
Safety Conditions …… 3-1
Emissions/Immunity Conditions …… 3-2
CE Rules of Thumb …… 3-2
Noise Considerations …… 3-3

Overview

CE compliant products bear the "CE" mark and include a *Declaration of Conformity* stating the particular specifications and conditions that apply. The test records and supporting documentation that validate the compliance are kept on file at the factory.

The standards are published in the *Official Journal of European Union* under direction of CENELEC (*European Committee for Electrotechnical Standardization*). The specific standards relevant to data acquisition equipment are listed on the product's *Declaration of Conformity*.

This product meets the essential requirements of applicable European directives, as amended for CE markings in accordance with the product family standard for:

- electrical equipment for measurement, control, and laboratory use
- immunity requirements for equipment used in controlled EM environments

Refer to this product's Declaration of Conformity (DoC) for any additional regulatory compliance information. To obtain the DoC for this product, visit iotech.com/CE

Safety Conditions

Users must comply with all relevant safety conditions as stated in the user's manual and in the pertinent *Declarations of Conformity*. Both the documentation and the associated hardware make use of the following Warning and Caution symbols. If you see any of these symbols on a product or in a document, carefully read the related information and be alert to the possibility of personal injury and/or equipment damage.



This WARNING symbol is used in documentation and/or on hardware to warn of possible injury or death from electrical shock under noted conditions.



This WARNING/CAUTION symbol is used to warn of possible personal injury or equipment damage under noted conditions.



This CAUTION symbol warns of possible equipment damage due to electrostatic discharge. The discharge of static electricity can damage some electronic components. Semiconductor devices are especially susceptible to ESD damage. You should always handle components carefully, and you should never touch connector pins or circuit components unless you are following ESD guidelines in an appropriate ESD-controlled area. Such guidelines include the use of properly grounded mats and wrist straps, ESD bags and cartons, and related procedures.



Unless otherwise stated our data acquisition products contain no user-serviceable parts. Only qualified personnel are to provide service to the devices.

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The specific safety conditions for CE compliance vary by product; but general safety conditions include the following bulleted items:

- The operator must observe all safety cautions and operating conditions specified in the documentation for all hardware used.
- The host computer and all connected equipment must be CE compliant.
- All power must be off to the device and externally connected equipment before internal access to the device is permitted.
- Ensure that isolation voltage ratings do not exceed documented voltage limits for power and signal inputs. All wire insulation and terminal blocks in the system must be rated for the isolation voltage in use. Voltages above 30 Vrms or ±60 VDC must not be applied if any condensation has formed on the device.
- Current and power use must not exceed specifications. Do not defeat fuses or other over-current protection.

Emissions/Immunity Conditions

The specific immunity conditions for CE compliance vary by product. General immunity conditions include the following:

- Cables must be shielded, braid-type with metal-shelled connectors. Input terminal connections are to be made with shielded wire. The shield should be connected to the chassis ground with the hardware provided.
- The host computer must be properly grounded.
- In low-level analog applications some inaccuracy is to be expected when I/O leads are exposed to RF fields or transients, as noted on the *Declaration of Conformity*, if applicable to the device.

CE Rules of Thumb

The IOtech device is CE Compliant at the time it leaves the factory and should remain in compliance as long as the conditions stated on the *Declaration of Conformity* continue to be met.

A few general rules of thumb:

- Use short cables.
- When assembling or disassembling components, take ESD precautions, including the use of grounded wrist straps.
- Ensure that the host computer is CE Compliant.
- Review the most recent *Declaration of Conformity*.
- Ensure all system components are properly grounded.

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Noise Considerations

Controlling electrical noise is imperative because it can present problems even with the best measurement equipment. Most laboratory and industrial environments suffer from multiple sources of electrical noise. For example, AC power lines, heavy equipment (particularly if turned on and off frequently), local radio stations, and electronic equipment can create noise in a multitude of frequency ranges.

Local radio stations are a source of high frequency noise, while computers and other electronic equipment can create noise in all frequency ranges. Creating a completely noise-free environment for test and measurement is seldom practical. Fortunately, simple techniques such as using shielded/twisted pair wires, filtering, and differential voltage measurement are available for controlling the noise in our measurements. Some techniques prevent noise from entering the system; other techniques remove noise from the signal.

While many techniques for controlling noise in signals provide a means of removing the noise that is already present, the preferred solution is to prevent the occurrence of noise in the signal in the first place.

The following practices, some of which are required for CE compliance, should be employed to minimize noise.

- **Make a solid earth ground connection**. Using insulated, low resistance wire, connect the chassis to solid earth ground. This practice accomplishes the following:
  (a) keeps radiated emissions low by keeping the chassis electrically quiet,
  (b) keeps potential common-mode voltages low,
  (c) improves user safety, and
  (d) provides a safe path for Electrostatic Discharge energy back to earth ground.

- **Minimize ambient EMI**. The lower the ambient EMI, the better. Sources of electromagnetic interference include solenoids, motors, computer equipment, high power distribution wiring, etc.

- **Distance cables**. Route signal cables away from Ethernet lines, Mains and other high voltage cables and equipment to minimize signal interference from radiated noise.

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Calibration 4

DaqBoard/3000 Series boards are factory-calibrated. However, if adjustments are needed they should be completed in the following order:

1. Analog Measurement Path, Offset and Gain
2. Voltage Reference
3. DAC0 Offset and Gain *
4. DAC1 Offset and Gain *
5. DAC2 Offset and Gain *
6. DAC3 Offset and Gain *

*In regard to DAC applicability:

DaqBoard/3000 – DAC0 and DAC1 apply
DaqBoard/3001 – DAC0, DAC1, DAC2, and DAC3 apply
DaqBoard/3005 – No DACs apply
DaqBoard/3006 – No DACs apply

Note: DaqBoard/3006 has one fixed range of ±10V.

A Windows-based program, DaqCal.exe, is used to calibrate Daq systems, including analog expansion cards. DaqCal.exe is used in conjunction with:

- a 6.5-digit, digital multi-meter
- an adjustable voltage calibrator
- an ambient temperature meter

To use the calibration program:

1. Launch **DaqCal**.

   Note: DaqCal is installed automatically from your data acquisition CD as a part of product support. This takes place during software installation. DaqCal's default location is the **IOtech DaqX Software** folder, in the **Programs** group.

2. When DaqCal opens you will be prompted to select your device from a list. After doing so, simply follow the illustrated on-screen instructions.



Reference Note:
We have incorporated a copy of the *DaqCal User Calibration Utility Guide* (p/n 457-0931) with this chapter. The guide includes information regarding NIST (National Institute of Standards and Technology) traceability, and equipment and setup information. Though far from all encompassing, the general guide should give you a good understanding as to how DaqCal is used.

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Calibrating DBK Expansion Options …… viii

CAUTION



Turn off power to all devices connected to the system before connecting cables or setting configuration jumpers and switches. Electrical shock or damage to equipment can result even under low-voltage conditions.

CAUTION



The discharge of static electricity can damage some electronic components. Semiconductor devices are especially susceptible to ESD damage. You should always handle components carefully, and you should never touch connector pins or circuit components unless you are following ESD guidelines in an appropriate ESD controlled area. Such guidelines include the use of properly grounded mats and wrist straps, ESD bags and cartons, and related procedures.

Overview

DaqCal is a Windows-based program used to calibrate Daq systems, for example: DaqBoards, DaqBooks, DaqScans, and DaqLabs. DaqCal can also be used to calibrate optional analog expansion cards.

Daq devices are factory-calibrated and you do not need to recalibrate the devices upon initially receiving them.

Note: Certain DBK options are self-calibrating and do not require manual calibration by the user. Such devices are disassociated from DaqCal, i.e., you cannot use DaqCal to calibrate them.

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Equipment

Refer to the appropriate block below, depending on whether you will be calibrating through a 37-pin, 68-pin, or 100-pin connector.

P1 37-PIN

If calibration signals will be passing through a 37-pin P1 connector you will need:

Required:

6.5-digit, digital multi-meter[1]
adjustable voltage calibrator[2]
ambient temperature meter

In addition, the following are recommended:

DBK11A, passive screw-terminal board
CA-37, 37 conductor ribbon cable

P4 100-PIN

If calibration signals will be passing through a 100-pin P4 connector you will need:

Required:

6.5-digit, digital multi-meter[1]
adjustable voltage calibrator[2]
ambient temperature meter

In addition, the following are recommended:

DBK11A, passive screw-terminal board*
DBK200, P4-to-DB37 adapter card*
CA-195 100-conductor ribbon cable

*Another DBK200 Series device that includes a P1 and P4 connector may be substituted.
See page iv.

P5 SCSI 68-PIN

If calibration signals will be passing through a 68-pin SCSI (P5) connector you will need:

Required:

6.5-digit, digital multi-meter[1]
adjustable voltage calibrator[2]
ambient temperature meter

In addition, the following are recommended:

TB-100, passive screw-terminal board
CA-G56 (3 ft. shielded cable) **

** One of the following cables may be substituted: CA-G55, a 3 ft. unshielded cable; or CA-G56-6, a 6 ft. shielded cable.

Certain steps in the calibration process require that you apply a signal to the device via a specific pin, or take a measurement reading from a specific pin. To make the task easier we recommend that you use a passive screw-terminal board, such as the DBK11A, TB-100, or possibly a DBK200 Series device. See the *Setup* section beginning on page iii.

[1]Agilent 34401A or better DMM.
[2]Traceability is through the DMM. The calibrator is only used as a quiet and stable voltage source.

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NIST Traceability

Calibration test equipment should be traceable through the National Institute of Standards and Technology. (NIST). Customers not familiar with traceability through that institute should contact them at traceability@nist.gov

The NIST Policy on Traceability (contained in NIST Administrative Manual, Subchapter 5.16) addresses:

- establishing traceability of measurement results
- assessing the claims of traceability made by others

Installing DaqCal

DaqCal is installed automatically from your data acquisition CD during software installation of DaqView. The default location of **DaqCal.exe** is the **IOtech DaqX** Software Program Group. The DaqX program group can be accessed through the "All Programs" feature in the Miccrosoft Windows Desktop.

Setup

Depending on your device, the setup will involve a 37-pin, 68-pin, or 100-pin connector. Although you can calibrate your Daq device directly through these connectors, it is much easier and quicker to perform the calibration via a passive screw terminal option such as a DBK213 (or DBK215 for SCSI devices), DBK11A, or TB-100. Many connection options are possible. A few are illustrated below. Connections to [or installation within] the host PC are not shown.

CAUTION



Turn off power to all devices connected to the system before connecting cables or setting configuration jumpers and switches. Electrical shock or damage to equipment can result even under low-voltage conditions.

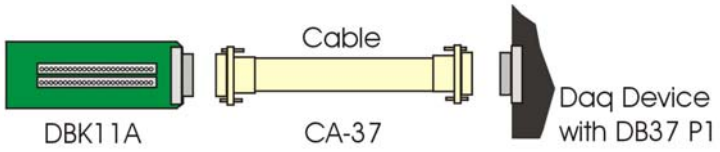
CAUTION



The discharge of static electricity can damage some electronic components. Semiconductor devices are especially susceptible to ESD damage. You should always handle components carefully, and you should never touch connector pins or circuit components unless you are following ESD guidelines in an appropriate ESD controlled area. Such guidelines include the use of properly grounded mats and wrist straps, ESD bags and cartons, and related procedures.

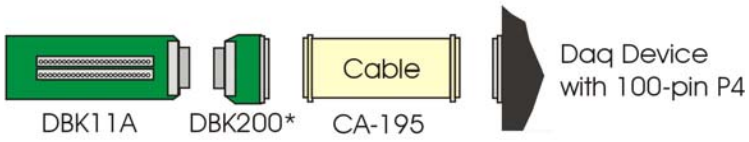
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P1 (37-pin) For DB37 P1 applications you can attach a DBK11A to the device via a CA-37 cable.

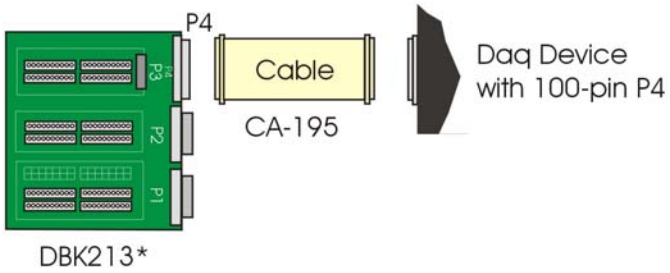


Connecting a DBK11A

P4 (100-pin) For 100-pin P4 connector applications you can use a DBK200 (or DBK201), DBK11A, and a CA-195 cable; or you could use a DBK213 and a CA-195 cable. Illustrations of these two scenarios follow.



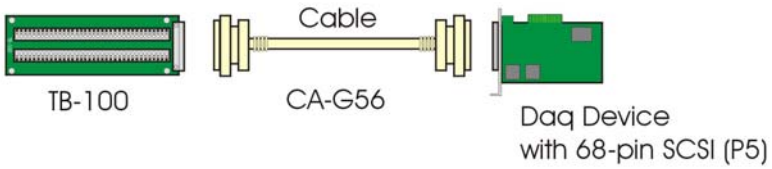
Connecting a DBK11A via a DBK200



Connecting a DBK213

* There are several DBK200 Series adaptive boards and modules available for 100-pin P4 connector applications. Refer to your hardware documentation or *DBK Options Manual* for specific information. PDF versions of documents are included on the data acquisition CD and on our web site.

P5 SCSI (68-pin)



Connecting a TB-100

For 68-pin SCSI (P5) connector applications you can use a CA-G56 cable to attach a passive TB-100 screw-terminal connector option. CA-G55 or CA-G56-6 can be substituted for the CA-G56 cable.**

Note that in place of the TB-100, a DBK215 Module could be used. Refer to your hardware documentation or DBK Options Manual for specific information. PDF versions of documents are included on the data acquisition CD and on our web site.

** CA-G56 is a 3 ft. shielded cable; CA-G55, a 3 ft. unshielded cable; CA-G56-6, a 6 ft. shielded cable.

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After you have completed the setup according to the type of device and appropriate connectivity option, launch DaqCal and follow the on-screen instructions.

What to Expect when using DaqCal

When DaqCal opens you will be prompted to select your device from a list. After doing so the application will guide you through the calibration process using simple on-screen instructions. It is important that you select the correct device as the steps required usually differ from one device to another.

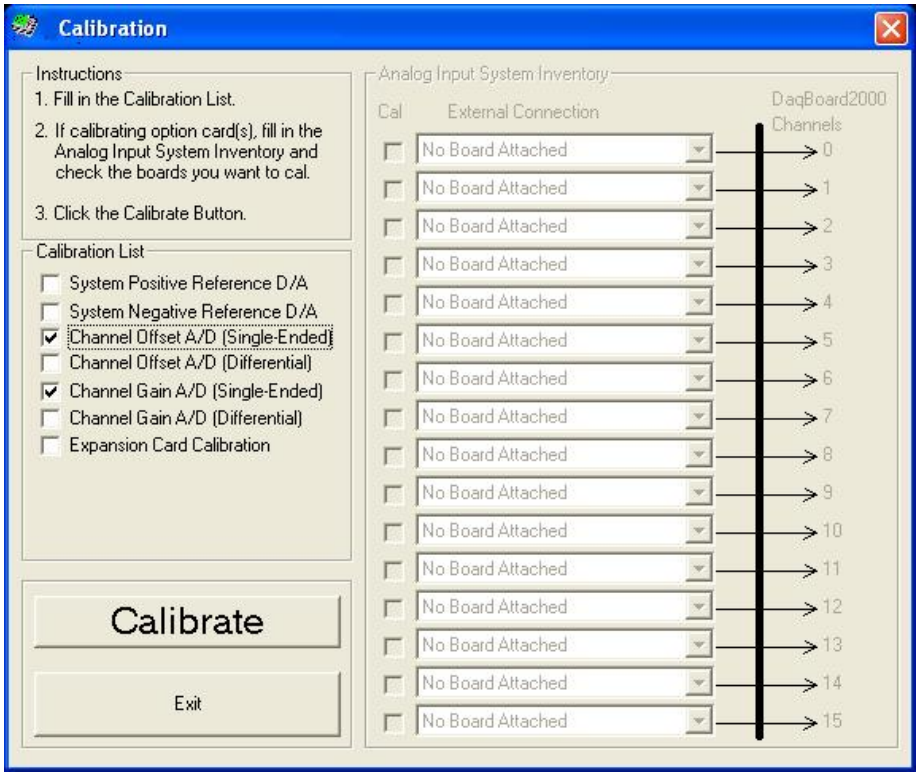
The following text and illustrations are shown for illustrative purposes only. This material is not to be substituted for actual DaqCal procedures.

After launching DaqCal, select the device to be calibrated from the device inventory list.



Selecting the Device from Device Inventory

After selecting your device, click the <OK> button. An instruction screen with a Calibration List will display. See following figure.



Initial Calibration Instruction Screen

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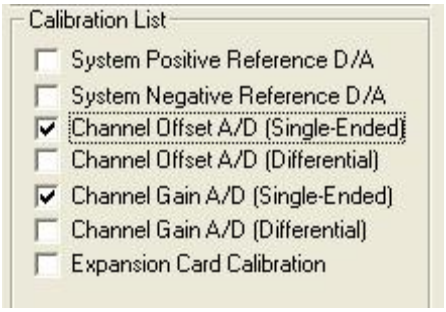
From the screen's Calibration List (right-hand figure), select the desired types of calibration. In the example shown we have selected:

- Channel Offset A/D (Single-Ended)
- Channel Gain A/D (Single-Ended)

After making the selections, click the <Calibrate> button (see preceding figure).

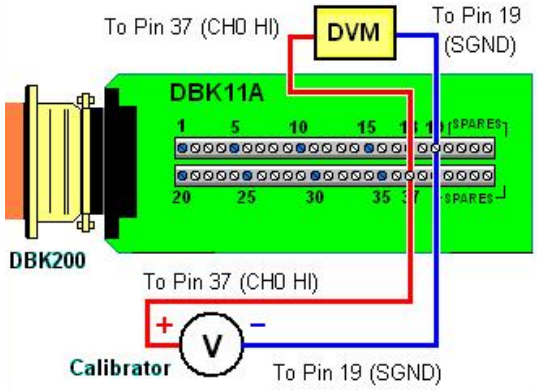


Steps specific to your device will now display.



Selecting the Desired Calibrations

Follow the on-screen instructions for your device. Note that every time you are prompted to <Go To Next Step> [and you do so] a new image and new steps will be displayed.

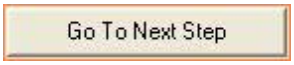


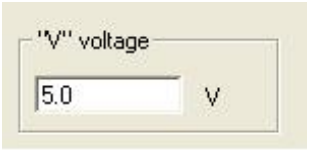
Example of an On-screen Graphic

DaqCal will prompt you to set various Calibrator voltages and to enter the Digital Voltmeter (DVM) readings into a numeric field on the screen.

DaqCal will instruct you step-by-step throughout the entire calibration.

Each completed step will result in a prompt to <Go To the Next Step>.





Enter a Voltage Value as Measured by the DVM

Note: Some calibration points may be insignificant to your application. If this is the case you can click the <Skip> button, in those instances, if desired.



Note that other buttons allow you to <Repeat Previous Step> or to return <Back to Main Window>; as indicated in the preceding button bar graphic.

In most cases the user proceeds sequentially, one step at a time; clicking the <Go To Next Step> button upon completion of each step.

DaqCal informs you when all calibration steps for your device have been completed.

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Calibrating Analog Outputs

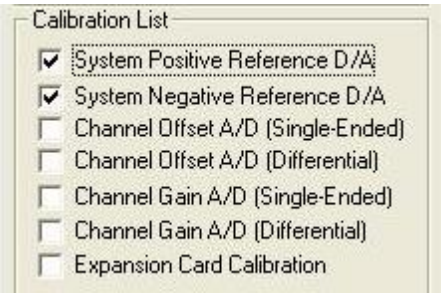
After launching DaqCal, select the device to be calibrated from the device inventory list.

After selecting your device, click the <OK> button. An instruction screen with a Calibration List will display.

From the screen's Calibration List select the desired types of calibration. For the example we have selected:

- System Positive Reference D/A
- System Negative Reference D/A

After making the selections, click the <Calibrate> button (see preceding figure). Steps specific to your Daq device will now display.



Selecting the Desired Calibrations

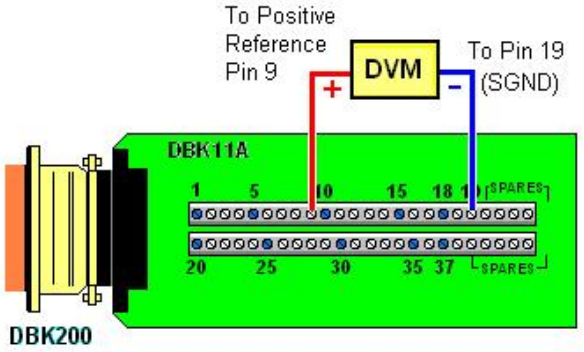
Follow the DaqCal screen prompts. You will likely see instructions similar to the following:

Connect the multi-meter positive (+) lead to Pin 9 (Positive Reference) of DBK11A.

Connect the multi-meter negative (-) lead to Pin 19 (SGND) of DBK11A.

Note: A multi-meter with a 6 ½ digit accuracy is required.

Click <Go To Next Step.>

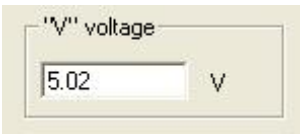


Connectivity Example from DaqCal

In continuing to follow DaqCal screen prompts you will be instructed to enter the DVM reading into the numeric field on the screen.

Click <Go To Next Step>.

This procedure is repetitive and DaqCal will instruct you step-by-step. Eventually, for example, after eight DVM voltage entries, a message similar to the following will be displayed:



Enter a Voltage Value as Measured by the DVM

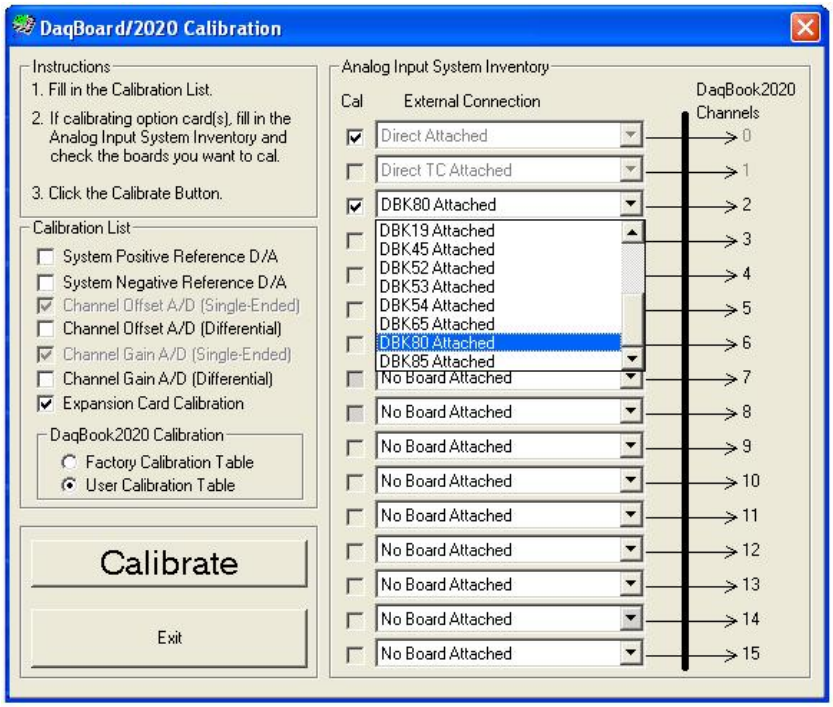
"No further steps in this section. Please click <OK> to continue."

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Calibrating DBK Expansion Options

If the primary data acquisition device (DaqBook, or DaqBoard) is out of its calibration period, calibrate that device prior to calibrating the DBK expansion option. An alternative to using DaqCal is to contact the factory or your service representative to schedule a factory calibration.

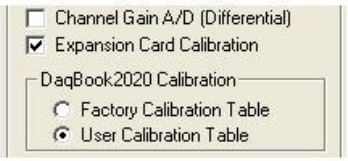
After launching DaqCal, select the device to be calibrated from the device inventory list. After selecting your device click the <OK> button. An instruction screen with a Calibration List will display.



Initial Calibration Instruction Screen

From the Calibration List, on the left side of the screen, select "Expansion Card Calibration."

A panel will appear allowing you to select one of two tables to be used as for calibration reference values. Selection is made via radio button, as indicated in the following figure.



Selecting the User Calibration Table

Select the calibration table that indicates **the most recent calibration** given to your primary data acquisition device, i.e., *User Calibration Table* or *Factory Calibration Cable*.

Note: Selecting "Factory Calibration Table" causes factory defaults to be used as reference calibration values.

After selecting the appropriate calibration table, select the DBK expansion option for the applicable channel. For example, in the first figure a DBK80 has been selected from the Analog Input channel 2 pull-down list. After selecting the DBK click the <Calibrate> button and follow the screen prompts.

Note: Certain DBK options are self-calibrating and do not require manual calibration by the user. Such devices are disassociated from DaqCal, i.e., you cannot use DaqCal to calibrate them.

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Counter Input Modes 5

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Timing Mode …… 5-13

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Each of the high-speed, 32-bit counter channels can be configured for counter, period, pulse width, time between edges, or encoder modes.

Debounce

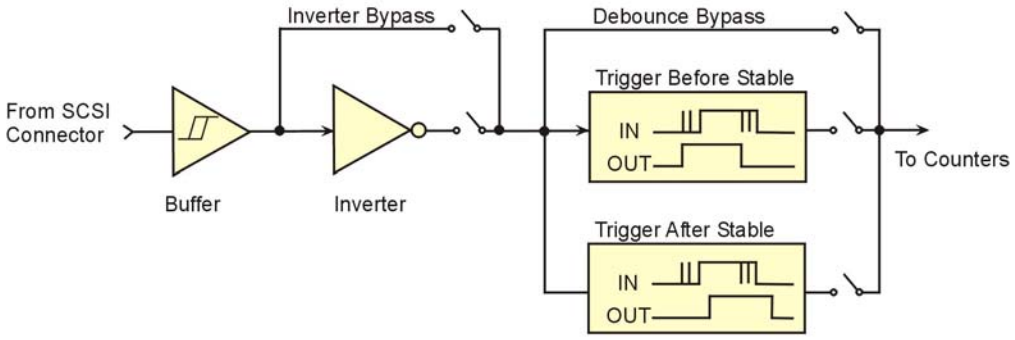
Each channel's output can be debounced with 16 programmable debounce times from 500 ns to 25.5 ms. The debounce circuitry eliminates switch-induced transients typically associated with electro-mechanical devices including relays, proximity switches, and encoders.

From the following illustration we can see that there are two debounce modes, as well as a debounce bypass. In addition, the signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is used to make the input rising-edge or falling-edge sensitive.

Edge selection is available with or without debounce. In this case the debounce time setting is ignored and the input signal goes straight from the inverter [or inverter bypass] to the counter module.

There are 16 different debounce times. In either debounce mode, the debounce time selected determines how fast the signal can change and still be recognized.

The two debounce modes are "trigger after stable" and "trigger before stable." A discussion of the two modes follows.

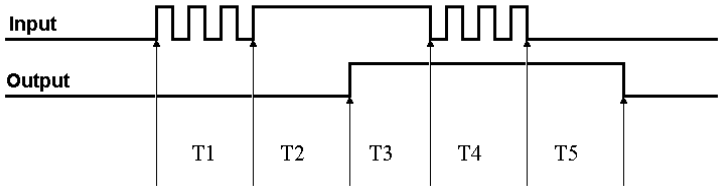


Debounce Model

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Trigger After Stable Mode

In the “Trigger After Stable” mode, the output of the debounce module will not change state until a period of stability has been achieved. This means that the input has an edge and then must be stable for a period of time equal to the debounce time.



Debounce Module – Trigger After Stable Mode

The following time periods (T1 through T5) pertain to the above drawing. In Trigger After Stable mode, the input signal to the debounce module is required to have a period of stability after an incoming edge, in order for that edge to be accepted (passed through to the counter module.) The debounce time for this example is equal to T2 and T5.

T1 – In the example above, the input signal goes high at the beginning of time period T1 but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)

T2 – At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time, therefore the output transitions high. If the Input signal never stabilized in the high state long enough, no transition would have appeared on the output and the entire disturbance on the input would have been rejected.

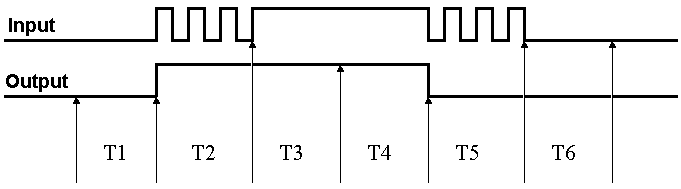
T3 – During time period T3 the input signal remained steady. No change in output is seen.

T4 – During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.

T5 – At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time, therefore the output goes low.

Trigger Before Stable Mode

In the “Trigger Before Stable” mode, the output of the debounce module immediately changes state, but will not change state again until a period of stability has passed. For this reason the mode can be used to detect glitches.



Debounce Module – Trigger Before Stable Mode

The following time periods (T1 through T6) pertain to the above drawing.

T1 – In the illustrated example, the **Input** signal is low for the debounce time (equal to T1); therefore when the input edge arrives at the end of time period T1 it is accepted and the **Output** (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.

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T2 – During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays "high" and does not change state during time period T2.

T3 – During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.

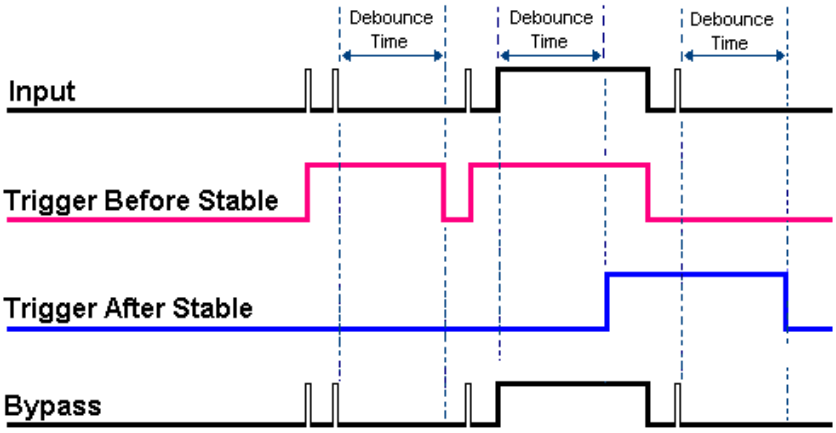
T4 – At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action [by going low].

T5 – During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.

T6 – After time period T6, the input signal has been stable for the debounce time and therefore any edge on the input after time period T6 will be immediately reflected in the output of the debounce module.

Mode Comparison

The following example shows how the two modes interpret the same input signal (which exhibits glitches). Notice that the *Trigger Before Stable* mode will recognize more glitches than the *Trigger After Stable* mode. Use the *bypass* option to achieve maximum glitch recognition.



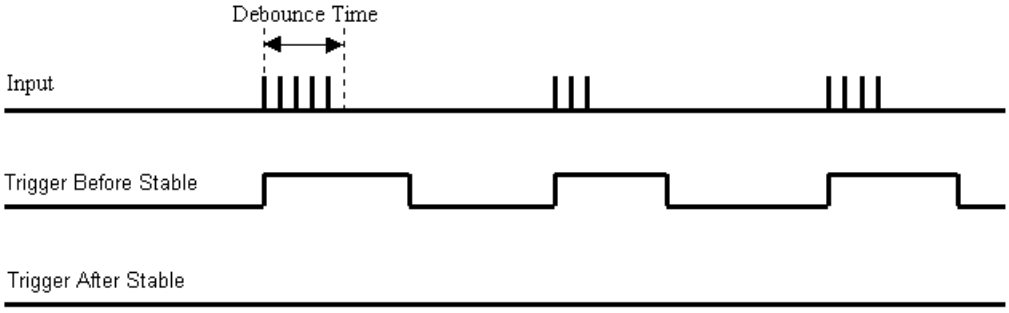
Example of Two Debounce Modes Interpreting the Same Signal

Debounce times should be set according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

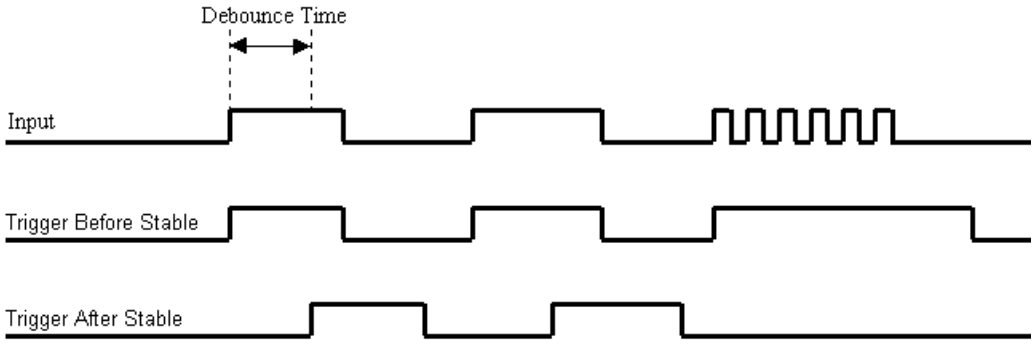
To see the effects of different debounce time settings, simply view the analog waveform along with the counter output. This can be done by connecting the source to an analog input.

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Use trigger before stable mode when the input signal has groups of glitches and each group is to be counted as one. The trigger before stable mode will recognize and count the first glitch within a group but reject the subsequent glitches within the group if the debounce time is set accordingly. The debounce time should be set to encompass one entire group of glitches as shown in the following diagram.



Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. Trigger after stable mode is used with electro-mechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving. The debounce time should be set short enough to accept the desired input pulse but longer than the period of the undesired disturbance as shown in the diagram below.



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Terms Applicable to Counter Modes

The following terms and definitions are provided as an aid to understanding counter modes.

Gating: Any counter can be gated by the mapped channel. When the mapped channel is high, the counter will be allowed to count, when the mapped channel is low, the counter will not count but hold its value.

Mapped Channel: A mapped channel is one of 4 signals that can get multiplexed into a channel's counter module. The mapped channel can participate with the channel's input signal by gating the counter, clearing the counter, etc. The 4 possible choices for the mapped channel are the 4 input signals (post debounce).

Start of Scan: The start of scan is a signal that is internal to the 3000 Series board. It signals the start of a scan group and therefore pulses once every scan period. It can be used to clear the counters and latch the counter value into the acquisition stream.

Terminal Count: This signal is generated by the counter value. There are only two possible values for the terminal count: 65,535 for a 16-bit counter (Counter Low); and 4,294,967,295 for a 32-bit counter (Counter High). The terminal count can be used to stop the counter from rolling over to zero.

Ticksize: The ticksize is a fundamental unit of time and has four possible settings: 20.83ns, 208.3ns, 2083ns, 20833ns. For measurements that require a timebase reference like period or pulsewidth, the ticksize is the basic unit of time. Ticksize is derived from the period of the 48 MHz system clock. The count value returned in the scan is the number of ticks that make up the time measurement.

Counter Options

The following mode options are available with the /3000 Series board and are detailed in the upcoming pages.
A separate block diagram has been created for each mode. Note that the **OPT** numbers relate to sections of the block diagrams.

Counter/Totalize Mode (see page 6):

OPT0: Selects *totalize* or *clear on read* mode.
OPT1: Determines if the counter is to *rollover* or "*stop at the top.*"
OPT2: Determines whether the counter is 16-bits (Counter Low); or 32-bits (Counter High).
OPT3: Determines which signal latches the counter outputs into the data stream back to the /3000 Series board. Start of scan or mapped channel.
OPT4: Allows the mapped channel to gate the counter.
OPT5: Allows the mapped channel to decrement the counter.
OPT6: Allows the mapped channel to increment the counter.

Period Mode (see page 8):

OPT[1:0]: Determines the number of periods to time, per measurement (1, 10, 100, 1000).
OPT2: Determines whether the period is to be measured with a 16-bit (Counter Low); or 32-bit (Counter High).
OPT4: Allows the mapped channel to gate the counter.
OPT6: Allows the mapped channel to be measured for periods.

Pulsewidth Mode (see page 11):

OPT2: Determines whether the pulsewidth is to be measured with a 16-bit counter (Counter Low); or a 32-bit counter (Counter High).
OPT4: Allows the mapped channel to gate the counter.
OPT6: Allows the mapped channel to be measured for pulsewidth.

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Encoder Mode (see page 15).

OPT[1:0]: Determines the encoder measurement mode: 1X, 2X, or 4X.
OPT2: Determines whether the counter is 16-bits (Counter Low); or 32-bits (Counter High).
OPT3: Determines which signal latches the counter outputs into the data stream going back to the /3000 Series board. Start of scan or mapped channel.
OPT4: Allows the mapped channel to gate the counter.
OPT5: Allows the mapped channel to clear the counter for Z reference.

Counter/Totalize Mode



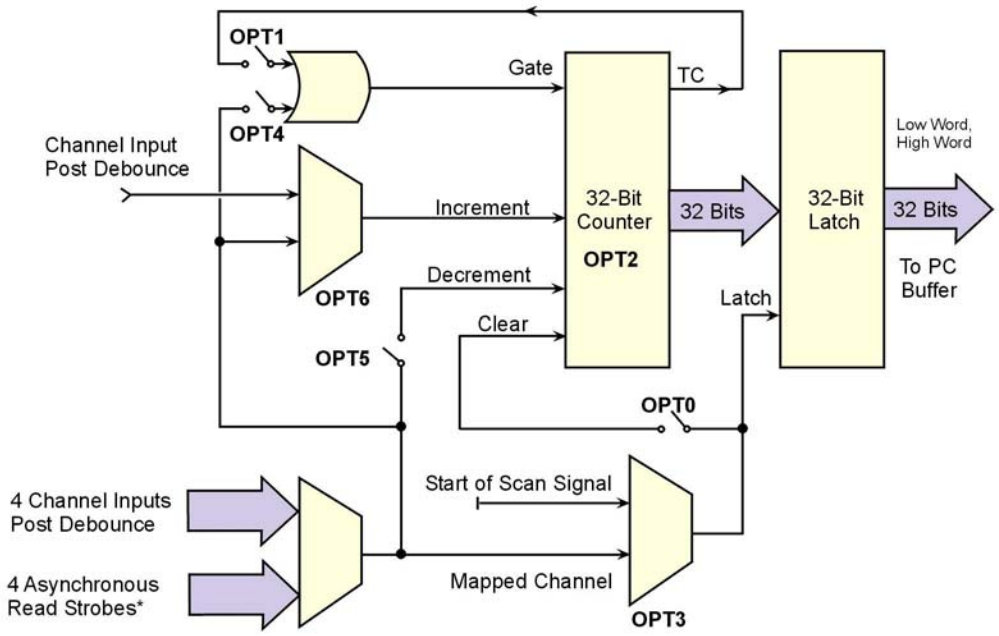
TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

The *counter mode* allows basic use of a 32-bit counter. While in this mode, the channel's input can only increment the counter upward. When used as a 16-bit counter (Counter Low), one channel can be scanned at the 12 MHz rate. When used as a 32-bit counter (Counter High), two sample times are used to return the full 32-bit result. Therefore a 32-bit counter can only be sampled at a 6 MHz maximum rate. If only the upper 16 bits of a 32-bit counter are desired then that upper word can be acquired at the 12 MHz rate.

The first scan of an acquisition always zeroes all counters. It is usual for all counter outputs to be latched at the beginning of each scan; however, there is an option to change this. A second channel, referred to as the **"mapped" channel**, can be used to latch the counter output. The mapped channel can also be used to:

- **gate the counter**
- **increment the counter**
- **decrement the counter**

The mapped channel can be any of the 4 counter input channels (post-debounce), or any of the four asynchronous read strobes. When a counter is not in the scan it can be asynchronously read with, or without, *clear on read*. The asynchronous read-signals strobe when the lower 16-bits of the counter are read by software. The software can read the counter's high 16-bits at a later time, after reading the lower 16-bits. The full 32-bit result reflects the timing of the first asynchronous read strobe.



Counter/Totalize Mode

*There is one asynchronous read strobe for each of the four counter channels.

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An explanation of the various counter options, depicted in the previous figure, follows.

COUNTER: OPT0: This selects *totalize* or *clear on read* mode.
Totalize Mode – The counter counts up and rolls over on the 16-bit (Low Counter) boundary, or on the 32-bit (High Counter) boundary. See OPT2 in regard to choosing 16-bit or 32-bit counters.
Clear On Read Mode – The counter is cleared at the beginning of every scan or synchronous read; and the final value of the counter [the value just before it was cleared] is latched and returned to the /3000 Series board.

COUNTER: OPT1: This determines if the counter is to *rollover* or "*stop at the top*."
Rollover Mode - The counter continues to count upward, rolling over on the 16-bit (Counter Low) boundary, or on the 32-bit (Counter High) boundary. See OPT2 in regard to choosing 16-bit or 32-bit counters.
Stop at the Top Mode - The counter will stop at the top of its count. The top of the count is FFFF for the 16-bit option (Counter Low), and FFFFFFFF for the 32-bit option (Counter High).

COUNTER: OPT2: Determines whether the counter is **16-bits** or **32-bits** (Counter Low, or Counter High, respectively). This only matters when the counter is using the "stop at the top" option, otherwise this option is inconsequential.

COUNTER: OPT3: Determines which signal latches the counter outputs into the data stream back to the /3000 Series board. Normally, the start of scan signal latches the counter outputs at the beginning of every scan; but an option is to have the mapped signal latch the counter outputs. This mapped-signal option allows a second signal to control the latching of the count data. This allows the user to know the exact counter value when an edge is present on another channel. This also allows the counters to be asynchronously read.

COUNTER: OPT4: Allows the **mapped channel to gate the counter** if desired. When the mapped channel is **high**, the counter is enabled. When the mapped channel is **low**, the counter is disabled (but holds the count value). The mapped channel can be any other input channel.

COUNTER: OPT5: Allows the **mapped channel to decrement the counter**. With this option the input channel [for the counter] will increment the counter. The mapped channel can be used to decrement the counter.

COUNTER: OPT6: Allows the **mapped channel to increment the counter** instead of the main channel. This option allows the counter to be used with any other input channel (post-debounce). If the channel's input is used elsewhere, for example, gating another counter, the counter for this channel does not need to go unused.

Asynchronously Reading These Counters

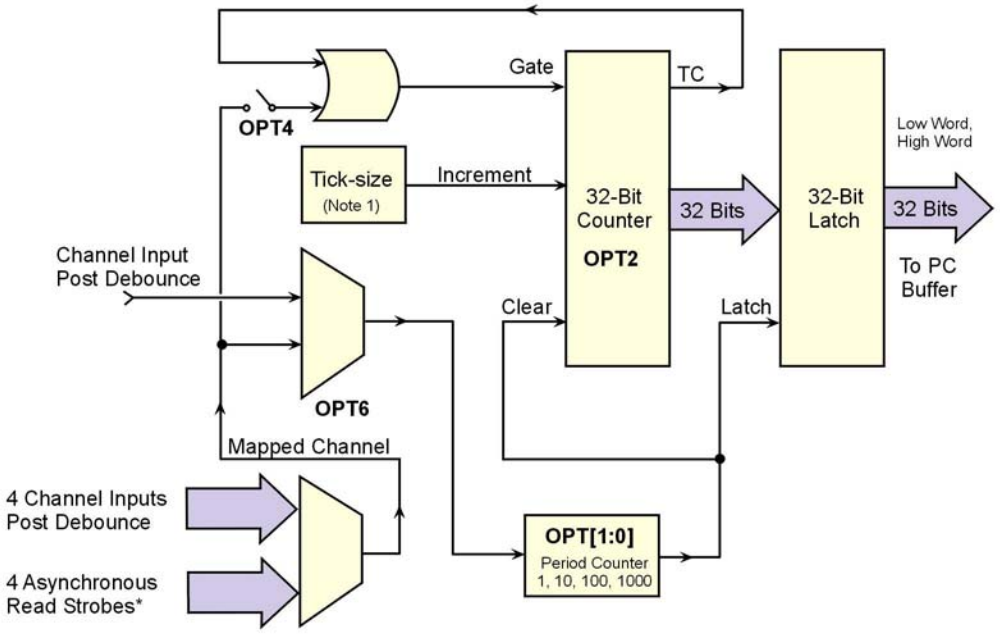
If the counter is in asynchronous mode the *clear on read* mode is available. The counter's lower 16-bit value should be read first. This will latch the full 32-bit result and clear the counter. The upper 16-bit value can be read after the lower 16-bit value. Also, counters can only be asynchronously read in modes that allow the mapped channel to latch the data, i.e., Counter and Encoder modes. However, it is possible for the user to use that read strobe as a mapped channel elsewhere, if desired. For example, the read strobe could be used to increment or decrement the counter.

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Period Mode

TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

This mode allows for period measurement of the channel input. The measurement period is the time from edge-to-edge, either both rising or both falling. Period data is latched as it becomes available and the data is logged by the /3000 Series board at the scan rate. Therefore, if the scan period is much faster than the input waveform, there will be a great deal of repetition in the period values. This repetition is due to the fact that updates take place only when another full period becomes available.



Period Mode

*There is one asynchronous read strobe for each of the four counter channels.

Note 1: Tick-sizes are: 20.83ns, 208.3ns, 2083ns, and 20833ns, derived from the 48 MHz system clock.

An example: One channel's acquired data might be: 0,0,0,0,80,80,80,80,79,79,79,79,81,81,81,81,….. This data represents the number of ticksize intervals counted during the period measurement. The first value(s) returned will be zero since the counters are cleared at the beginning of the acquisition. The data comes in sets of four since the scan period is about one-fourth as long as the input channel's period. Every time the period measurement is latched from the counter, the counter is immediately cleared and begins to count the time for the subsequent period.

If the scan period is a lot slower than the input period, the acquired data will be missing some periods. To obtain greater resolution, you can increase the scan period, or use an averaging option (see OPT[1:0]).

The data returned is interpreted as time measured in ticks. There are four timebase settings: 20.83 ns, 208.3 ns, 2083 ns, and 20833 ns. These are often referred to as tick-sizes. The /3000 Series board uses a 48 MHz, 30 ppm oscillator as a timing source. The tick sizes are derived from 1 period, 10 periods, 100 periods, or 1000 periods of the 48 MHz clock.

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PERIOD: OPT[1:0]: Determines the **number of periods to time, per measurement**. This makes it possible to *average out jitter* in the input waveform, sampling error, noise, etc. There are four options:

(1) The channel's measurement is latched every time one complete period has been observed.

(2) The channel's measurement is latched every time that 10 complete periods have been observed. The value that gets returned is equal to 10 consecutive periods of the input channel.

(3) The number returned is 100 consecutive periods.

(4) The number returned is 1000 consecutive periods.

PERIOD: OPT2: Determines whether the period is to be measured with a **16-bit** (Counter Low), or **32-bit** (Counter High) counter. Since period measurements always have the "stop at the top" option enabled, this option dictates whether the measurement has a range of 0 to 65535 ticks or 0 to 4,294,967,295 ticks.

PERIOD: OPT4: Allows the **mapped channel to gate the counter** if desired. When the mapped channel is **high**, the counter is enabled. When the mapped channel is **low**, the counter is disabled, but still holds the count value. The mapped channel can be any other input channel.

PERIOD: OPT6: This allows a mapped channel's period to be measured, instead of the input channel. The mapped channel can be any other input channel (post debounce). This option allows the counter to be used with any other input channel (post-debounce). If the channel's input is used elsewhere, for example, gating another counter, the counter for this channel does not need to go unused.

Period and Frequency Accuracy

The /3000 Series board can measure the period of any input waveform. It does this by counting the integral number of "ticks" that make up the period, the data returned will always be time measured in "ticks." The error in each data sample will come from two sources: the sampling error caused by not being able to count a partial "tick"; and the 3000 Series Board's internal timebase inaccuracy. The board's internal timebase has an absolute accuracy of 30 ppm. The sampling error will vary with input frequency, selected ticksize, and selected averaging mode. The absolute error is the "root-sum-of-squares" of the two independent error sources. For example, if the sampling error is 30 ppm and the timebase accuracy is 30 ppm, the absolute accuracy is 42 ppm.

Many times the desired accuracy is much less than what the internal timebase is capable of. Other applications will require a more accurate period measurement and the effects of sampling error will have to be averaged out leaving only the inaccuracy associated with the internal timebase. Inaccuracy due to the internal timebase cannot be averaged out.

For period and frequency measurements, percent sampling error is equal to 100%/(n+1) where n=0 to 65,535 for a 16-bit counter and n=0 to 4,294,967,295 for a 32-bit counter. For small count values, the sampling error is large and for large count values, the sampling error is small. If sampling error is to be less than 0.21%, n must be greater than 480 regardless of counter size.

Sampling error can also be reduced by averaging many samples together. Assuming the input signal is asynchronous to the board's internal timebase, sampling error can be divided by the square-root of the number of samples taken. The averaging can be done with PC-based software.

The board has the ability to measure 1, 10, 100 or 1000 periods, dividing the sampling error by 1, 10, 100, or 1000. This is done within the board circuitry and may eliminate the need for any averaging to be done in the PC. For high accuracy on high frequency inputs, multiple period measurement and PC-based averaging can be done.

The 3000 Series board has the ability to provide various frequency ranges that are based upon different ticksizes, averaging options, and counter size (16 bit or 32 bit values.) The frequency ranges are designed to fit a wide array of possible applications. Within each range, the sampling error decreases dramatically as the input period increases. The ranges will get smaller as required accuracy increases.

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Upper 16-bits of the 32-bit counter		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 1500u	20833.333	1
150u – 15m	2083.333	1
1500u – 150m	208.333	1
15m – 1500m	20.833	1
150m – 15	20.833	10
1500m – 150	20.833	100
15 – 1500	20.833	1000

Lower 16-bits of the 32-bit counter		
Range (Hz)	Ticksize (nS)	Averaging Option
1 – 100	20833.333	1
10 – 1k	2083.333	1
100 – 10k	208.333	1
1k – 100k	20.833	1
10k – 1M	20.833	10
100k – 5M	20.833	100
1M – 5M	20.833	1000

Frequency Ranges for a 16-bit value, sampling error is less than 0.21%

Each frequency range given in the previous table-set can be exceded. If the input waveform goes under-range by too much, the counter value will top out at 65535 indicating you have reached the lowest possible frequency that can be measured on that range. If the input waveform goes over range by too much, the counter will return values that are very course and have a lot of sampling error. The values returned will have a small number of counts for the period duration. If an input waveform cannot fit within one of the 16-bit ranges shown above or requires much higher accuracy, then a 32-bit range should be considered.

Full 32-bit Counter		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 100	20833.333	1
150u – 1k	2083.333	1
1.5m – 10k	208.333	1
15m – 100k	20.833	1
150m – 1M	20.833	10
1.5 – 5M	20.833	100
15 – 5M	20.833	1000

Frequency Ranges for a 32-bit Value,
Sampling Error is Less than 0.21%

The 32-bit ranges shown above are much wider than the 16-bit ranges, but also require the full 32-bit value to be returned. Since digital or counter channels do not take up any time in the scan period there is no disadvantage in reading a 32-bit counter versus a 16-bit counter. The 32-bit frequency ranges can also be exceeded with a loss of accuracy or topping out at 4,294,967,295 counts.

Some measurements will require the accuracy of an input waveform to be free of sampling error, having only the absolute accuracy of the internal timebase as the source of error. Sampling error can be averaged out to give the required result. In most cases, the 3000 Series board can perform the required averaging on the values before they are returned to the PC. The frequency ranges shown below will give a sampling error that is less than 10ppm or 1ppm.

Full 32-bit Counter **<10 ppm**		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 500m	20833.333	1
150u – 5	2083.333	1
1.5m – 50	208.333	1
15m – 500	20.833	1
150m – 5k	20.833	10
1.5 – 50k	20.833	100
15 – 500k	20.833	1000

Full 32-bit Counter **<1 ppm**		
Range (Hz)	Ticksize (nS)	Averaging Option
15u – 50m	20833.333	1
150u – 500m	2083.333	1
1.5m – 5	208.333	1
15m – 50	20.833	1
150m – 500	20.833	10
1.5 – 5k	20.833	100
15 – 50k	20.833	1000

High Accuracy Frequency Ranges for a 32-bit Value
that has little sampling error (<10ppm, <1ppm)

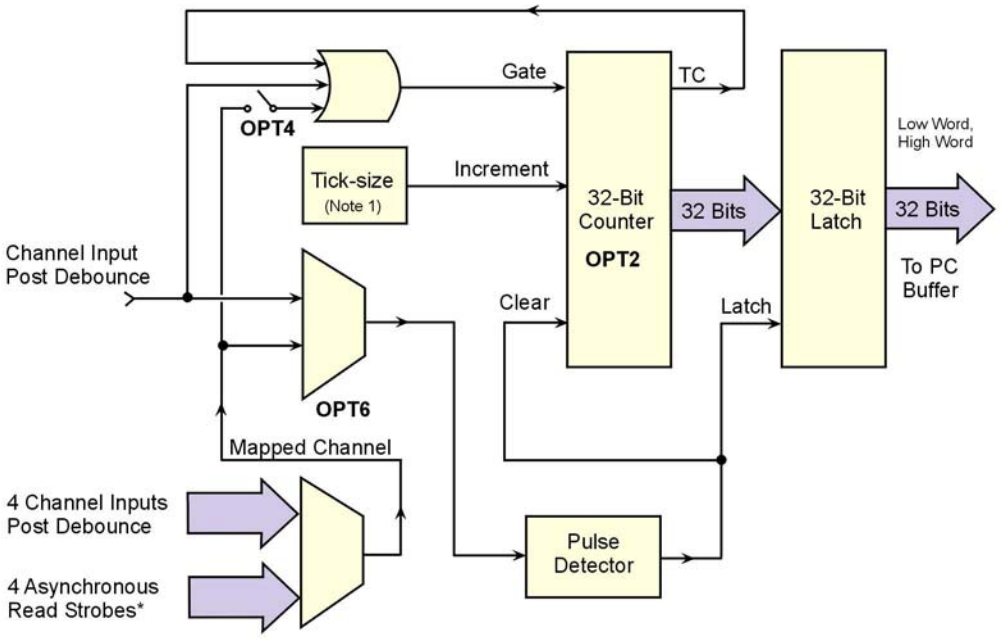
If the input frequency is required to have less than 1 ppm sampling error and is greater than 50kHz, use the 15– 50kHz, 1ppm range. The values returned will have sampling error that is greater than 1ppm but they can be averaged by the PC software to further reduce the sampling error.

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Pulsewidth Mode

TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

This mode provides a means to measure a channel's pulsewidth. The measurement is the time from the rising edge to the falling edge, or visa versa. The measurement will be either pulsewidth low, or pulsewidth high, depending upon the edge polarity set in the debounce module.
Every time the pulsewidth measurement is latched from the counter, the counter is immediately cleared and enabled to count the time for the next pulsewidth. The pulsewidth measurements are latched as they become available.



Pulsewidth Mode

*There is one asynchronous read strobe for each of the four counter channels.
Note 1: Tick-sizes are: 20.83ns, 208.3ns, 2083ns, and 20833ns, derived from the 48 MHz system clock.

An example: one channel's acquired data might be: 0,0,0,0,80,80,80,80,79,79,79,79,81,81,81,81,….
This data represents the number of ticksize intervals counted during the pulsewidth measurement. The first value(s) returned will be zero since the counters are cleared at the beginning of the acquisition. In this example the data comes in sets of four because the scan period is about one-fourth as long as the input channel's period. Every time the pulsewidth measurement is latched from the counter, the counter is immediately cleared and enabled to count time for the next pulsewidth.

If the scan period is much slower than the input period, then the acquisitions will miss some pulsewidths. Decreasing the scan period will increase the number of different pulsewidths received.

The data returned is interpreted as time measured in ticks. There are four timebase settings: 20.833 ns, 208.33 ns, 2.083 µs, and 20.83 µs. These are often referred to as tick-sizes. The 3000 Series board uses a 48 MHz, 30 ppm oscillator as a timing source.

If the input signal has a poor slew rate the pulsewidth mode will provide variant results.

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PULSEWIDTH: OPT2: Determines whether the pulsewidth is to be measured with a **16-bit** (Counter Low), or **32-bit** (counter High) counter. Since pulsewidth measurements always have the "stop at the top" option enabled, this option dictates whether the measurement has a range of 0 to 65535 ticks, or 0 to 4,294,967,295 ticks.

PULSEWIDTH: OPT4: Allows the **mapped channel to gate the counter**. When the mapped channel is **high**, the counter is enabled to count. When the mapped channel is **low**, the counter is disabled, but holds the count value. The mapped channel can be any other input channel.

PULSEWIDTH: OPT6: This allows the mapped channel's pulsewidth to be measured instead of the input channel. The mapped channel can be any other input channel (post debounce). This option allows the counter to be used with any other input channel (post-debounce). If the channel's input is used elsewhere, for example, gating another counter, the counter for this channel does not need to go unused.

Pulsewidth and Timing mode Accuracy

The 3000 Series board has the ability to measure the pulsewidth of an input and the time between any two edges on any two inputs. The time ranges are similar to those shown for period mode except that averaging is not available. The ranges given below reflect this.

Upper 16-bits of the 32-bit Counter		
Range (S)	Ticksize (nS)	Averaging Option
800 – 80000	20833.333	1
80 – 8000	2083.333	1
8 – 800	208.333	1
800m – 80	20.833	1

Lower 16-bits of the 32-bit Counter		
Range (S)	Ticksize (nS)	Averaging Option
10m – 1	20833.333	1
1m – 100m	2083.333	1
100u – 10m	208.333	1
10u – 1m	20.833	1

Pulsewidth and Time Ranges for a 16-bit Value
Sampling error is less than 0.21%

Full 32-bit Counter		
Range (S)	Ticksize (nS)	Averaging Option
10m – 80000	20833.333	1
1m – 8000	2083.333	1
100u – 800	208.333	1
10u - 80	20.833	1

Pulsewidth and Time Ranges for a 32-bit Value
Sampling error is less than 0.21%

Full 32-bit Counter <10 ppm		
Range (S)	Ticksize (nS)	Averaging Option
2 – 80000	20833.333	1
200m – 8000	2083.333	1
20m – 800	208.333	1
2m – 80	20.833	1

Full 32-bit Counter <1 ppm		
Range (S)	Ticksize (nS)	Averaging Option
20 – 80000	20833.333	1
2 – 8000	2083.333	1
200m – 800	208.333	1
20m – 80	20.833	1

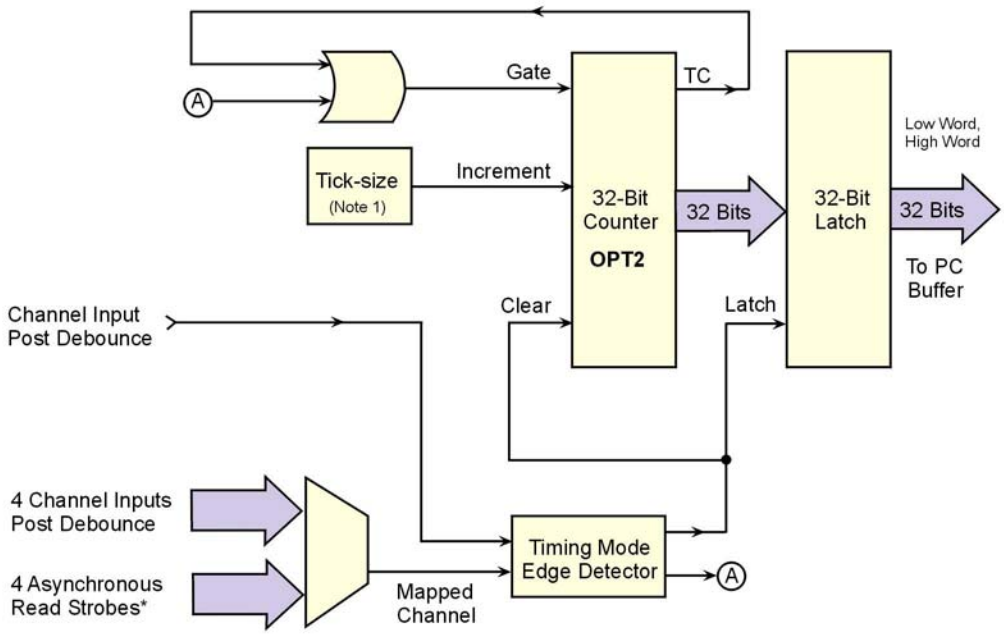
High Accuracy Pulsewidth and Time Ranges for a 32-bit Value
that has little sampling error (<10ppm, <1ppm)

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Timing Mode

TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

This mode provides a means of measuring time between two subsequent events, i.e., the edge of one channel with respect to the edge of another channel. The edge selection is done in each channel's debounce setup. Whenever the time measurement is latched from the counter, the counter is immediately cleared and enabled for accepting the subsequent time period, which starts with the next edge on the main channel.



Timing Mode

*There is one asynchronous read strobe for each of the four counter channels.

Note 1: Tick-sizes are: 20.83ns, 208.3ns, 2083ns, and 20833ns, derived from the 48 MHz system clock.

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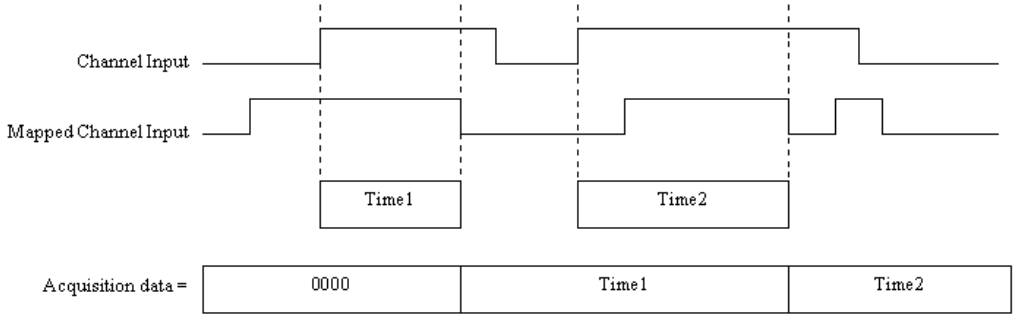
An Example of Timing Mode

The following example represents one channel in timing mode. The time desired is between the *rising edge* on the **input channel** and the *falling edge* on the **mapped channel**. Zeroes are returned, in the scan, until one complete time measurement has been taken. At that point, the value (time in ticks) is latched and logged by the /3000 Series board until the next time measurement has been completed. Rising edges on the input channel will clear the counter and falling edges on the mapped channel will latch the output of the counter at that time. If the scan period is much slower than the rate of time-frames coming [available on the two channels] then the data will miss some time-frames. The scan period can be decreased to capture more time-frames.

The data returned is interpreted as time measured in ticks. This data represents the number of ticksize intervals counted during the timing measurement. There are four timebase settings: 20.833 ns, 208.33 ns, 2.083 µs, and 20.83 µs. These are often referred to as tick-sizes. The 3000 Series board uses a 48 MHz, 30 ppm oscillator as a timing source.



If the input signal has a poor slew rate the timing mode will provide variant results, dependant upon the input switching threshold.



Example of One Channel in Timing Mode

TIMING: OPT2: This determines whether the time is to be measured with a **16-bit** (Counter Low), or **32-bit** (Counter High) counter. Since time measurements always have the "stop at the top" option enabled, this option dictates whether the measurement has a range of 0 to 65535 ticks or 0 to 4,294,967,295 ticks.

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Encoder Mode

TIP: When using a counter for a trigger source, it is a good idea to use a pre-trigger with a value of at least 1. The reason is that all counters start at zero with the initial scan; and there will be no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

Introduction

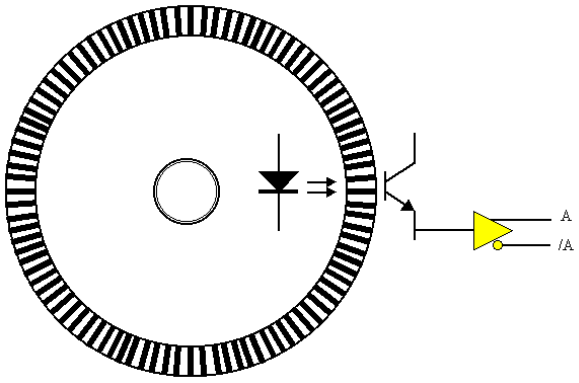
Rotary shaft encoders are frequently used with CNC equipment, metal-working machines, packaging equipment, elevators, valve control systems, and in a multitude of other applications in which rotary shafts are involved.

The *encoder mode* allows the 3000 Series board to make use of data from optical incremental quadrature encoders. When in the *encoder mode*, the board accepts *single-ended* inputs. When reading phase A, phase B, and index Z signals, the 3000 Series board provides positioning, direction, and velocity data.

The 3000 Series board can only receive input from up to two encoders.

The 3000 Series board supports quadrature encoders with a 16-bit (Counter Low), or a 32-bit (Counter High) counter, 20 MHz frequency, and x1, x2, and x4 count modes. With only phase A and phase B signals, 2 channels are supported; with phase A, phase B, and index Z signals, 1 channel is supported.

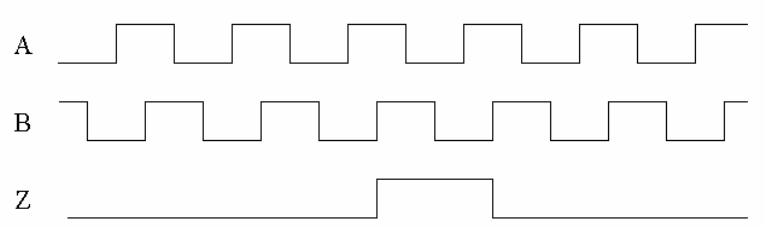
Quadrature encoders generally have 3 outputs: A, B, and Z. The A and B signals are pulse trains driven by an optical sensor inside the encoder. As the encoder shaft rotates, a laminated optical shield rotates inside the encoder. The shield has three concentric circular patterns of alternating opaque and transparent windows through which an LED will shine. There is one LED for each of the concentric circular patterns and likewise, one phototransistor. One phototransistor produces the A signal, another phototransistor produces the B signal and the last phototransistor produces the Z signal. The concentric pattern for A has 512 window pairs (or 1024, 4096, etc.)



The concentric pattern for B has the same number of window pairs as A except that the entire pattern is rotated by 1/4 of a window-pair. Thus the B signal will always be 90 degrees out of phase from the A signal. The A and B signals will pulse 512 times (or 1024, 4096, etc.) per complete rotation of the encoder.

The concentric pattern for the Z signal has only one transparent window and therefore pulses only once per complete rotation. Representative signals are shown in the following figure.

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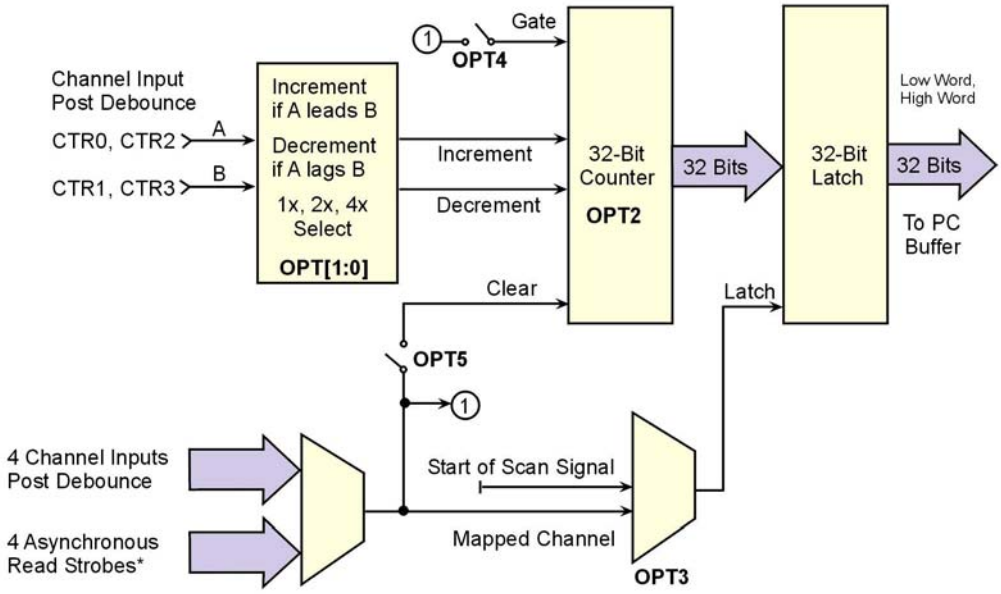


Representation of Quadrature Encoder Outputs: A, B, and Z

As the encoder rotates, the A (or B) signal is indicative of the distance the encoder has traveled. The frequency of A (or B) indicates the velocity of rotation of the encoder. If the Z signal is used to zero a counter (that is clocked by A) then that counter will give the number of pulses the encoder has rotated from its reference. The Z signal is a reference marker for the encoder. It should be noted that when the encoder is rotating clockwise (as viewed from the back), A will lead B and when the encoder is rotating counter-clockwise, A will lag B. If the counter direction control logic is such that the counter counts upward when A leads B and counts downward when A lags B, then the counter will give direction control as well as distance from the reference.

An Example of Encoder Accuracy

If there are 512 pulses on A, then the encoder position is accurate to within 360 degrees/512. Even greater accuracy can be obtained by counting not only rising edges on A but also falling edges on A, giving position accuracy to 360 degrees/1024. The ultimate accuracy is obtained by counting rising and falling edges on A and on B (since B also has 512 pulses.) This gives a position accuracy of 360 degrees/2048. These 3 different modes are known as 1X, 2X, and 4X. The 3000 Series board implements all of these modes and functions, as described in the following options.



Encoder Mode

*There is one asynchronous read strobe for each of the four counter channels.

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ENCODER: OPT[1:0]: This determines the encoder measurement mode: 1X, 2X, or 4X.

ENCODER: OPT3: This determines which signal latches the counter outputs into the data stream going back to the /3000 Series board. Normally, the start of scan signal latches the counter outputs at the beginning of every scan. The other option is to have the mapped signal latch the counter outputs. This allows the user to have another signal control the latching of the count data, so the exact value of the counter is known when an edge is present on another channel.

ENCODER: OPT4: This allows the mapped channel to gate the counter if desired. When the mapped channel is high, the counter is enabled to count, when the mapped channel is low, the counter is disabled (but holds the count value.) The mapped channel can be any other input channel.

ENCODER: OPT5: This allows the mapped channel to clear the counter if desired. OPT5 implements the Z-function [described above], allowing the encoder reference to clear the counter. The counter is cleared on the rising edge of the mapped channel.

Encoder Wiring Diagrams

You can use up to two encoders with each 3000 Series board module in your acquisition system. Each A and B signal can be made as a single-ended connection with respect to common ground.

Encoder wiring diagrams and example setup tables are included in the following pages; refer to them as needed.

For Single-ended Connections:

For single-ended applications, the connections made from the encoder to the 3000 Series board are as follows:

- Signals A, B, and Z connect to the Counter Inputs on 3000 Series board.
- Each encoder ground connects to GND.
- +5 V is available on the 68-pin SCSI connector for powering encoders.



Differential applications are not supported.



For Open-Collector Outputs: External ***pullup resistors*** can be connected to the 3000 Series board's counter input terminal blocks. A pullup resistor can be placed between any input channel and the provided +5 V power supply.

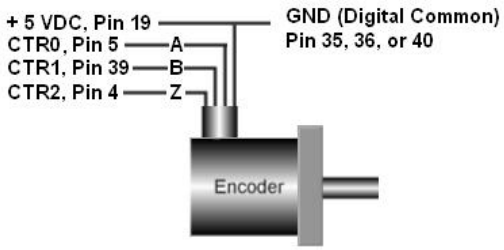
Choose a pullup resistor value based on the encoder's output drive capability and the input impedance of the 3000 Series board. Lower values of pullup resistors will cause less distortion but also cause the encoder's output driver to pull down with more current.

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Wiring for 1 Encoder

The following figure illustrates connections for one encoder to a 68-pin SCSI connector on a DaqBoard/3000 Series board.

The "A" signal must be connected to an even-numbered channel and the associated "B" signal must be connected to the next [higher] odd-numbered channel. For example, if "A" were connected to CTR0, "B" would be connected to CTR1.



Encoder Connections to pins on the SCSI Connector*

* Connections can instead, be made to the associated screw-terminals of a connected TB-100 terminal connector option.

In addition to the previous figure, the following table indicates how to connect a single encoder to a 3000 Series board. Each signal (A, B, Z) can be connected as a single-ended connection with respect to the common ground. The encoder can draw power from the 3000 Series board's +5 VDC power output (pin 19). Connect the encoder's power input to the +5V pin and connect the return to digital common (GND) on the same connector.

The programming setup given below is just a representative of possible options.

Single Encoder – Programming Example Setup		
SCSI Pin	**Connects to:**	**Example Programming Setup**
Pin 5 (CTR0)	Encoder – A	Encoder Mode, 4X option, 16-bit counter, Latch on SOS, Map channel Clears the counter, set Map channel to CTR2.
Pin 39 (CTR 1)	Encoder – B	Period Mode, 1Xperiod option, 16-bit counter, Map channel doesn't gate, Ticksize to 208.3 ns.
Pin 4 (CTR2)	Encoder – Z	Counter in Totalize mode, stop-at-the-top, 16-bit counter.

If the encoder stops rotating, but is vibrating [due to the machine it is mounted to], the debounce feature can be used to eliminate false edges. An appropriate debounce time can be chosen and applied to each encoder channel. Refer to the *Debounce Module* section on page 1 for additional information regarding debounce times.

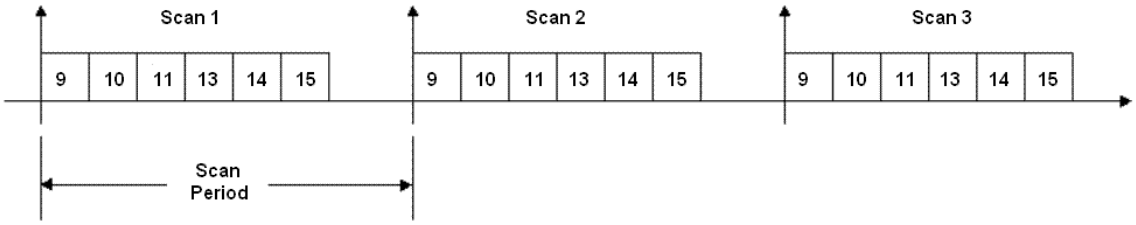
Relative position and *velocity* can be obtained from the encoder. However, during an acquisition, data that is relative to the Z-position cannot be obtained until the encoder locates the Z-reference.

During an acquisition, data that is relative to the Z-position cannot be obtained until the encoder locates the Z-reference.

Note that the number of Z-reference crossings can be tabulated. If the encoder was turning in only one direction, then the Z-reference crossings will equal the number of complete revolutions. This means that the data streaming to the PC will be *relative position*, *period = 1/velocity*, and *revolutions*.

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A typical acquisition might take 6 readings off of the 3000 Series board module as illustrated below. The user determines the scan rate and the number of scans to take.



DaqBoard/3000 Series board Acquisition of Six Readings per Scan

Note: Digital channels do not take up analog channel scan time.

In general, the output of each channel's counter is latched at the beginning of each scan period (called the *start-of-scan*.) Every time the 3000 Series board receives a *start-of-scan* signal, the counter values are latched and are available to the /3000 Series board.

The 3000 Series board clears all counter channels at the beginning of the acquisition. This means that the values returned during scan period 1 will always be zero. The values returned during scan period 2 reflect what happened during scan period 1.

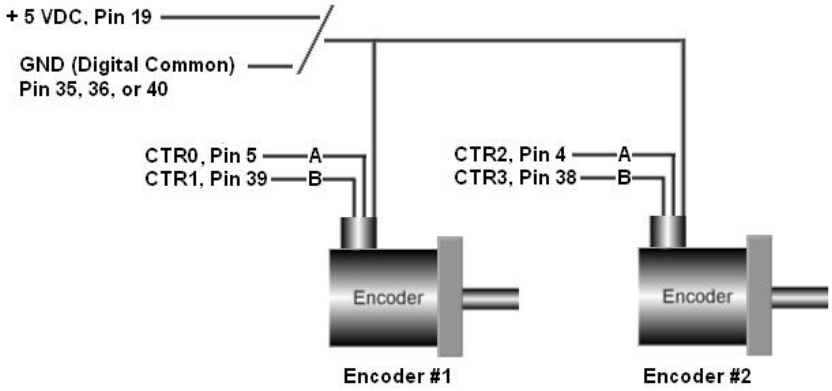


The scan period defines the timing resolution for the /3000 Series board. If you need a higher timing resolution, shorten the scan period.

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Wiring for 2 Encoders

The following figure illustrates single-ended connections for two encoders. Differential connections are not applicable.



Two Encoders Connected to pins on the SCSI Connector*

* Connections can instead, be made to the associated screw-terminals of a connected TB-100 terminal connector option.

Connect two encoders to the 3000 Series board as shown in the table below. Each signal (A, B) can be connected as a single-ended connection with respect to the common digital ground (GND). Both encoders can draw their power from the +5V power output (pin 19) on the 68-pin SCSI connector.

Connect each encoder's power input to +5V power. Connect the return to digital common (GND) on the same connector. Make sure that the current output spec is not violated. The programming setup given below is just a representative of possible options.

Two Encoders – Programming Example Setup		
SCSI Pin	**Connects to:**	**Example Programming Setup**
Pin 5 (CTR0)	Encoder #1 – A	Encoder Mode, 1X option, 16-bit counter, Latch on SOS
Pin 39 (CTR 1)	Encoder #1 – B	Period Mode, 1Xperiod option, 16-bit counter, Map channel doesn't gate, Ticksize to 20833 ns
Pin 4 (CTR2)	Encoder #2 – A	Encoder Mode, 2X option, 16-bit counter, Latch on SOS
Pin 38 (CTR3)	Encoder #2 – B	Period Mode, 1Xperiod option, 16-bit counter, Map channel doesn't gate, Ticksize to 2083.3 ns

With the encoders connected in this manner there is no relative positioning information available on encoder #1 or #2 since there is no Z signal connection for either. Therefore only distance traveled and velocity can be measured for each encoder.

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Setpoint Configuration for Output Control 6

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P2C, DAC, or Timer Update Latency …… 6-6

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Detection on an Analog Input, DAC and P2C Updates …… 6-7

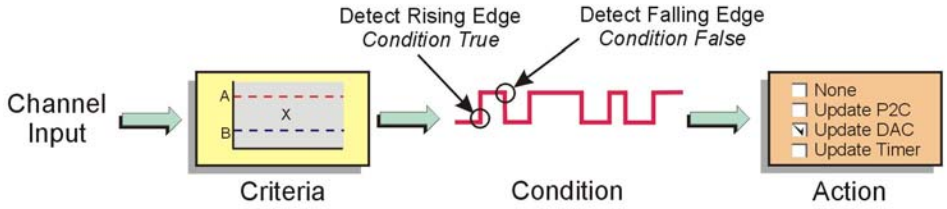
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Overview



Criteria Input Signal is Equal to X		**Action Driven by Condition**
Compare X To:	**Setpoint Definition:**	**Update Conditions:**
Limit A or Limit B	• Equal to A X = A • Below A X < A • Above B X > B *(Choose 1)*	**True Only**: If True, then Output Value 1 If False, then perform no action **True and False**: If True, then Output Value 1 If False, then Output Value 2
Window* (non-Hysterisis Mode)	• Inside B < X < A • Outside B > X; or X > A *(Choose 1)*	**True Only**: If True, then Output Value 1 If False, then perform no action **True and False**: If True, then Output Value 1 If False, then Output Value 2
Window* (Hysterisis Mode)	• Above A X > A • Below B X < B *(Both conditions are checked when in Hysterisis Mode)*	**Hysterisis Mode (Forced Update)**: If X > A is True, then Output Value 1 until X < B is True, then Output Value 2. If X < B is True, then Output Value 2 until X > A is True, then Output Value 1. This is saying: (1) If the input signal is outside the window "high", then Output Value 1 until the signal goes outside the window "low" and (2) if the signal is outside the window low, then Output Value 2 until the signal goes outside the window "high." There is no change to the detect signal while within the window.

***** Value A defines the upper limit of the Window and Value B defines the low limit.

Using Setpoints to Control Outputs

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DaqBoard/3000 Series boards include a setpoint configuration feature which allows the user to individually configure up to 16 detection setpoints associated with channels within a scan group. Each detection setpoint can be programmed in the following ways:

- **Single Point referenced** – above, below, or equal to the defined setpoint
- **Window (dual point) referenced** – inside, or outside the window
- **Window (dual point) referenced, Hysterisis Mode** – outside the window high forces Output 1; outside the window low forces Output 2

A digital detect signal is used to indicate when a signal condition is True or False, i.e., whether or not the signal has met the defined criteria. The detect signals themselves can be part of the scan group and can be measured as any other input channel; thus allowing real time data analysis during an acquisition.

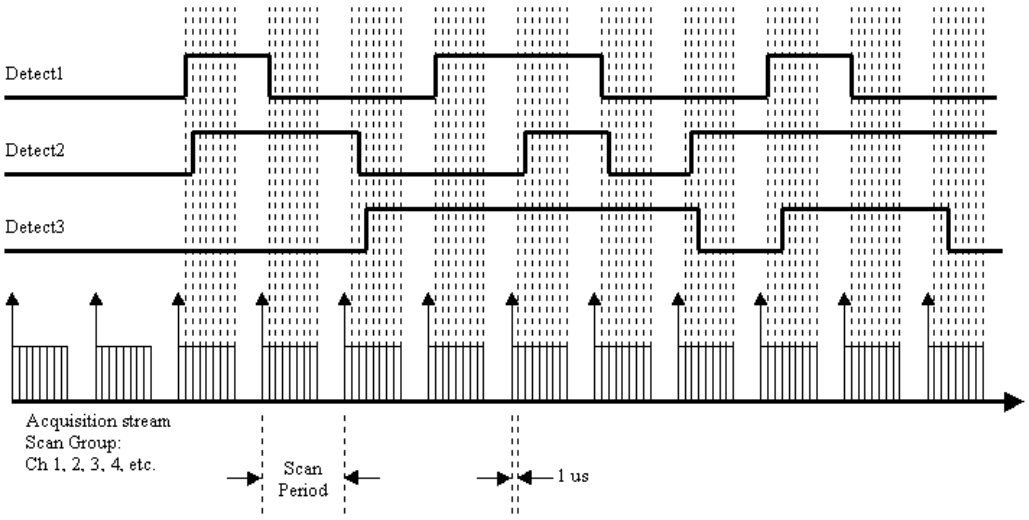
Each setpoint can update the following, allowing for real time control based on acquisition data:

- **P2C digital output port with a data byte and mask byte**
- **analog outputs (DACs)**
- **timers**

The detection module looks at the 16-bit data being returned on a given channel and generates another signal for each channel with a setpoint applied: Detect1 for Channel 1, Detect2 for Channel 2, etc. These signals serve as data markers for each channel's data. It doesn't matter whether that data is volts, counts, period, pulsewidth, timing, or encoder position.

A channel's detect signal will show a **rising edge** and will be **True** when the channel's data meets the setpoint criteria. The detect signal will show a **falling edge** and will be **False** when the channel's data does not meet the setpoint criteria.

The detect signal has the timing resolution of the scan period as seen in the diagram below. The detect signal can change no faster than the scan frequency (1/scan period.)



Example Diagram of Detection Signals for Channels 1, 2, and 3

Each channel in the scan group can have one detection setpoint. There can be no more than 16 setpoints, in total, applied to channels within a scan group.

Detection setpoints act on 16-bit data only. Since the DaqBoard/3000 Series boards have 32-bit counters, data is returned 16-bits at a time. The lower word, the higher word or both lower and higher words can be part of the scan group. Each counter input channel can have 1 detection setpoint for the counter's lower 16-bit value and 1 detection setpoint for the counter's higher 16-bit value.

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Detecting Input Values

All setpoints are programmed as part of the pre-acquisition setup, similar to setting up the analog path, debounce mode, or counter mode setup. Since each setpoint acts on 16-bit data, each has two 16-bit compare values: **Limit A** (High Limit) and **Limit B** (Low Limit). These limits define the setpoint window.

There are several possible conditions (criteria) and effectively 3 update modes, as can be seen in the following configuration summary.

Setpoint Configuration Summary

- ◊ **16-bit High Limit** Identified as "Limit A" in software
- ◊ **16-bit Low Limit** Identified as "Limit B" in software
- ◊ **Criteria:**

Inside window	Signal is below Limit A and Above Limit B
Outside window	Signal is above Limit A, or below Limit B
Greater than value	Signal is above Limit B, *Limit A is not used*
Less than value	Signal is below Limit A, *Limit B is not used*
Equal to value	Signal is equal to Limit A, *Limit B is not used.* Note that the *Equal to mode* is intended for use with counter or digital input channels [as the source channel]. See the TIP below.
Hysteresis mode	*Outside the window high* forces Output 1 until an *outside the window low* condition exists; then Output 2 is forced. Output 2 continues until an *outside the window high* condition exists. The cycle repeats as long as the acquisition is running in Hysterisis mode.

- ◊ **Update Mode:**
  Update on True Only
  Update on True and False
  None - Do not update
- ◊ **16-bit DAC value, P2C value, or Timer value when input meets criteria**
- ◊ **16-bit DAC value, P2C value, or Timer value when input does not meet criteria**
- ◊ **Type of Action:**
  None
  Update P2C (see note)
  Update DACx
  Update TImerx



By software default, P2C comes up as a digital input. If you want the P2C signal to be a digital output [in some initial state before an acquisition is started] and P2C is to be updated by set point criterion, then you must do an asynchronous write to P2C before the acquisition is started. The initial value will only be output if the asynchronous write to P2C has been performed.



When using setpoints with triggers *other than* immediate, hardware analog, or TLL, the setpoint criteria evaluation will begin immediately upon arming the acquisition.



TIP: It is recommended that the "Equal to Limit A" mode only be used with counter or digital input channels as the channel source. If similar functionality is desired for analog channels, then the "Inside Window" mode should be used.

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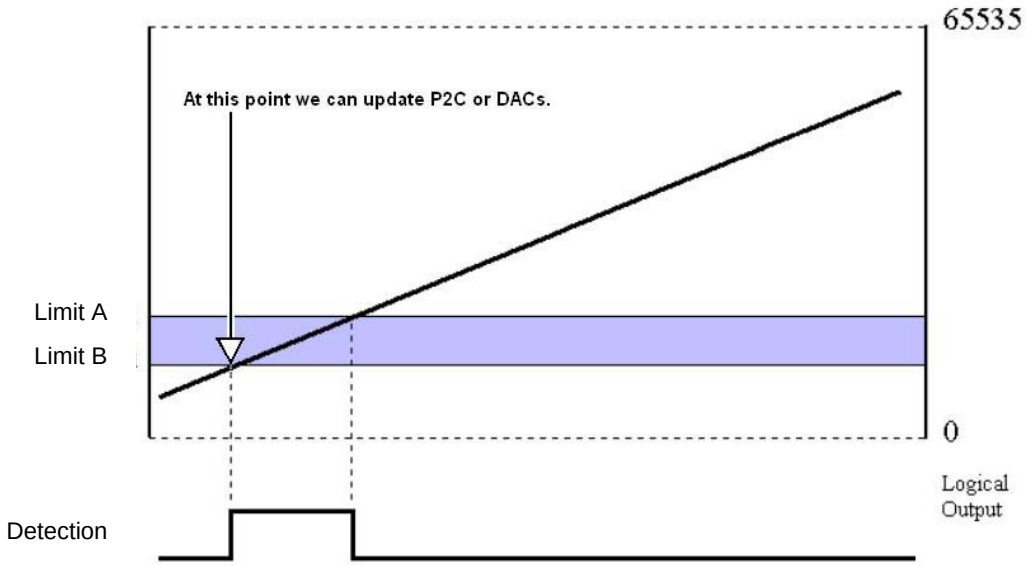
Each setpoint can be programmed with an 8-bit digital output byte and corresponding 8-bit mask byte. When the setpoint criteria has been met, the P2C digital output port can be updated with the given byte and mask. Alternately, each setpoint can be programmed with a 16-bit DAC update value, any one of the 4 DAC outputs can be updated in real time. Any setpoint can also be programmed with a timer update value.

In *hysteresis mode* each setpoint has two forced update values. Each update value can drive one DAC, one timer, or the P2C digital output port. *In hysteresis mode the outputs do not change when the input values are inside the window*. There is one update value that gets applied when the input values are less than the window and a different update value that gets applied when the input values are greater than the window.

Update on True and False uses two update values. There is one update value that gets applied when the specified criteria is met (True) and a different update value that gets applied when the specified criteria is not met (False). The update values can drive DACs, P2C, or timer outputs.

Example: Setpoint Detection on a Totalizing Counter

In the following figure Channel 1 is a counter in totalize mode. Two setpoints are used to define a point of change for Detect 1 as the counter counts upward. The detect output will be high when inside the window (greater than Limit B (the low limit) but less than Limit A (the high limit). In this case, the Channel 1 setpoint is defined for the 16 lower bits of channel 1's 32-bit value. The P2C digital output port could be updated on a True condition (the rising edge of the Detection signal). Alternately, one of the DAC output channels, or timer outputs, could be updated with a value.



Channel 1 in Totalizing Counter Mode, Inside the Window Setpoint

The detection circuit works on data that is put into the acquisition stream at the scan rate. This data is acquired according to the pre-acquisition setup (scan group, scan period, etc.) and returned to the PC. Counters are latched into the acquisition stream at the beginning of every scan. The actual counters may be counting much faster than the scan rate and therefore only every 10^{th}, 100^{th}, or n^{th} count will show up in the acquisition data. Therefore it is possible to set a small detection window on a totalizing counter channel and have the detection setpoint "stepped over" since the scan period was too long. Even though the counter value stepped into and out of the detection window, the actual values going back to the PC may not. This is true no matter what mode the counter channel is in.

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The setting of a detection window must be done with a scan period in mind. This applies to analog inputs and counter inputs. Quickly changing analog input voltages can step over a setpoint window if not sampled often enough.

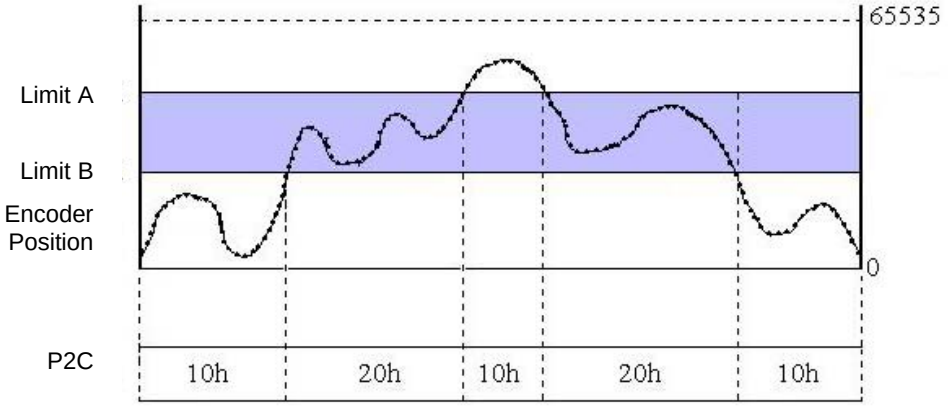
There are three possible solutions for overcoming this problem:

(1) The scan period could be shortened to give more timing resolution on the counter values or analog values

(2) The setpoint window can be widened by increasing Limit A and/or lowering Limit B.

(3) A combination of both solutions (1 and 2) could be made.

Example: Setpoint Detection on a Counter in Encoder Mode.



Example of a Counter in Encoder Mode

The figure above shows values pertaining to a Counter in Encoder Mode. The acquisition is started and 16-bit data [from the counter] streams into the PC at the scan rate. The 16-bit counter data is interpreted as the position from an encoder, which is connected to the counter inputs.

The update on *True and False* mode is being used. Thus, one value is output on P2C when the position is *outside of the window* (a value of 10h in the example); and a second value is output on P2C when the position is *inside the window* (a value of 20h in the example).

In the *True and False* mode, each setpoint has two DAC update values, two P2C update values, or 2 timer update values. One of the two values is used to update the DACs, P2C, or timers when it is *true* that the input channel meets the setpoint criteria. The second value is used to update the DACs, P2C, or timers when the condition is *false*, i.e., when the setpoint criteria is not met.



By software default, P2C comes up as a digital input. If you want the P2C signal to be a digital output [in some initial state before an acquisition is started] and P2C is to be updated by set point criterion, then you must do an asynchronous write to P2C before the acquisition is started. The initial value will only be output if the asynchronous write to P2C has been performed.

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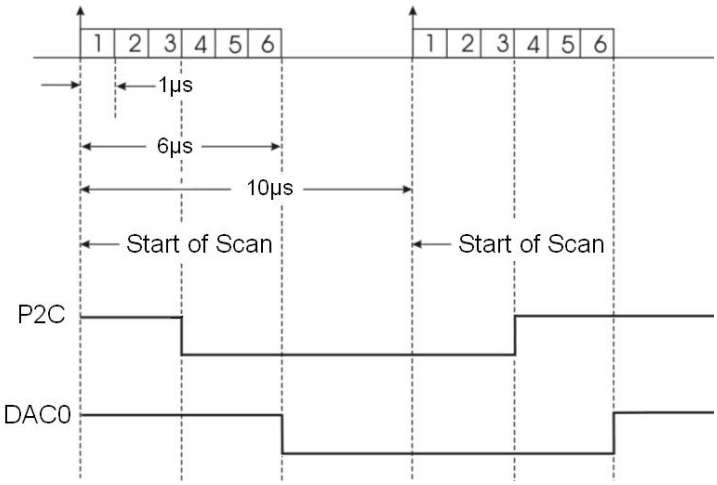
P2C, DAC, or Timer Update Latency

Setpoints allow DACs, timers, or P2C digital outputs to be updated very quickly. Exactly how fast an output can be updated is determined by the following three factors:

- **scan rate**
- **synchronous sampling mode**
- **type of output to be updated**

Example:

We set an acquisition to have a scan rate of 100 kHz. This means each scan period is 10µs. Within the scan period we will sample six analog input channels. These are shown in the following figure as Channels 1 through 6. The ADC conversion occurs at the beginning of each channel's 1µs time block.



Example of P2C or DAC Latency

If we apply a setpoint on analog input Channel 2, then that setpoint will get evaluated every 10µs with respect to the sampled data for Channel 2.

Due to the pipelined architecture of the Analog-to-Digital Converter system, the setpoint cannot be evaluated until 2µs after the ADC conversion. In the example above, the P2C digital output port can be updated no sooner than 2µs after Channel 2 has been sampled, or 3µs after the start of the scan. This 2µs delay is due to the pipelined ADC architecture. The setpoint is evaluated 2µs after the ADC conversion and then P2C can be updated immediately.

P2C digital outputs can be updated immediately upon setpoint detection. This is not the case for analog outputs, as these incur another 3µs delay. This is due to the shifting of the digital data out to the D/A converter which takes 1µs, plus the actual conversion time of the D/A converter, i.e., another 2µs (worst case). Going back to the above example, if the setpoint for analog input Channel 2 required a DAC update it would occur 5µs after the ADC conversion for Channel 2, or 6µs after the start of the scan.



When using setpoints to control any of the DAC outputs, increased latencies may occur if attempting to stream data to DACs or pattern digital output at the same time. The increased latency can be as long as the period of the DAC pacer clock. For these reasons, avoid streaming outputs on any DAC or pattern digital output when using setpoints to control DACs.

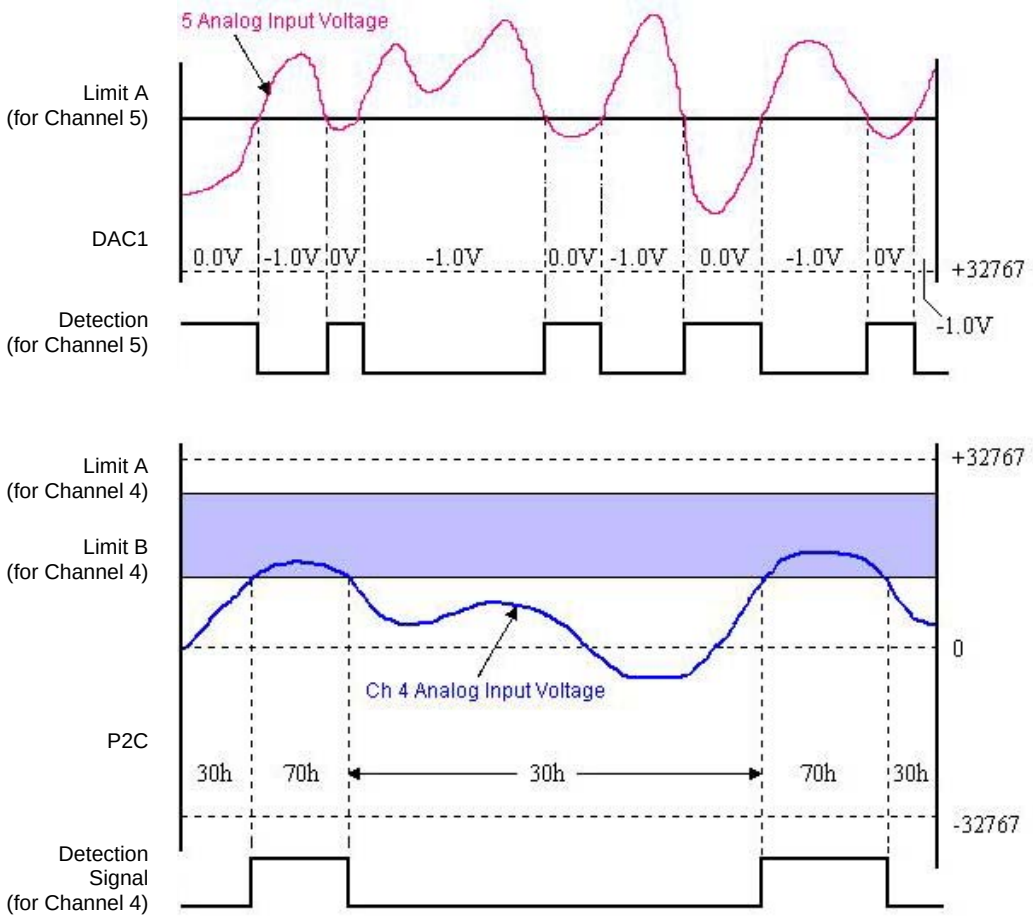
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Detection on an Analog Input, DAC and P2C Updates

Update Mode: Update on True and False
Criteria: Ch 5 example: Below Limit; Ch 4 example: Inside Window

In this example Channel 5 has been programmed with reference to one setpoint [Limit A], defining a low limit; and Channel 4 has been programmed with reference to two setpoints [Limits A and B] which define a window for that channel.

Channel	Condition	State of Detect Signal	Action
5	Below Limit A (for Channel 5)	True	When Channel 5 analog input voltage is below the limit A, update DAC1 with Output Value 0.0V.
		False	When the above stated condition is false, update DAC1 with the Output Value of *minus* 1.0V.
4	Within Window (Between Limit A and Limit B) for Channel 4	True	When Channel 4 analog input voltage is within the window, update P2C with 70h.
		False	When the above stated condition is false (Channel 4 analog input voltage is outside the window) update P2C with 30h.



Analog Inputs with Setpoints Update on True and False

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In the example [upper portion of the preceding figure], the setpoint placed on analog Channel 5 updated DAC1 with 0.0V. The update occurred when Channel 5's input was less than the setpoint (Limit A). When the value of Channel 5's input was above setpoint Limit A, the condition of <A was false and DAC1 was then updated with *minus*1.0V.

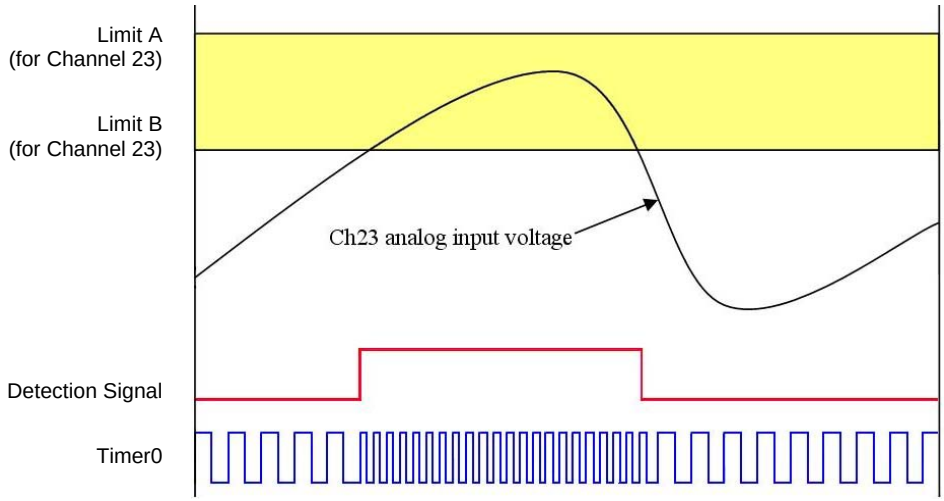
Control outputs can be programmed on each setpoint. Detection for Channel 4 could be used to update the P2C digital output port with one value (70h in the example) when the analog input voltage is within the shaded region and a different value when the analog input voltage is outside the shaded region (30h in the example).

Detection on an Analog Input, Timer Output Updates

Update Mode: Update on True and False
Criteria Used: Inside Window

The figure below shows how a setpoint can be used to update a timer output. Channel 23 is an analog input channel. It could be any analog input channel but in this example it happens to be on a PDQ30 expansion module. A setpoint is applied using *Update on True and False*, with a criteria of *inside-the-window*, where the signal value is inside the window when simultaneously less than Limit A but greater than Limit B.

Whenever the Channel 23 analog input voltage is inside the setpoint window (condition True), timer0 will be updated with one value; and whenever the Channel 23 analog input voltage is outside the setpoint window (condition False) timer0 will be updated with a second output value.



Updating a Timer Output
Update on True and False

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Using the Hysterisis Function

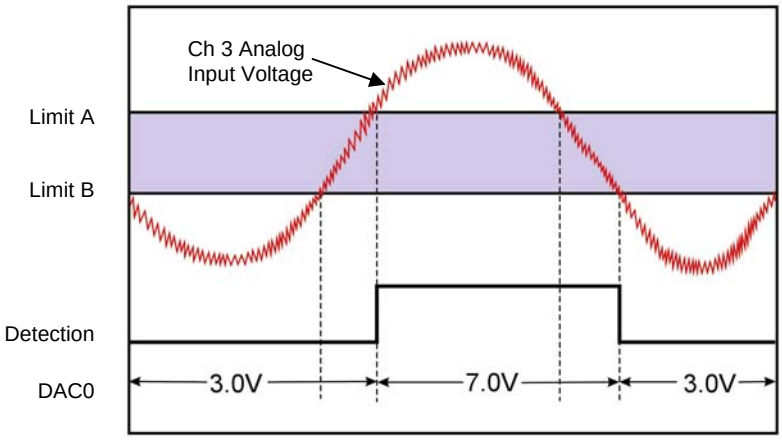
Update Mode: N/A, the Hysterisis option has a forced update built into the function
Criteria Used: window criteria for *above* and *below* the set limits

The figure below shows analog input Channel 3 with a setpoint which defines two 16-bit limits, Limit A (High) and Limit B (Low). These are being applied in the hysteresis mode and DAC Channel 0 will be accordingly.

In this example Channel 3's analog input voltage is being used to update DAC0 as follows:

- ***When outside the window, low*** (below Limit B) DAC0 is updated with 3.0V. This update will remain in effect until the analog input voltage goes above Limit A.
- ***When outside the window, high*** (above Limit A) DAC0 is updated with 7.0V. This update will remain in effect until the analog input signal falls below Limit B. At that time we are again outside the limit "low" and the update process repeats itself.

Hysteresis mode can also be done with P2C digital output port, or a timer output, instead of a DAC.



Channel 3 in Hysterisis Mode

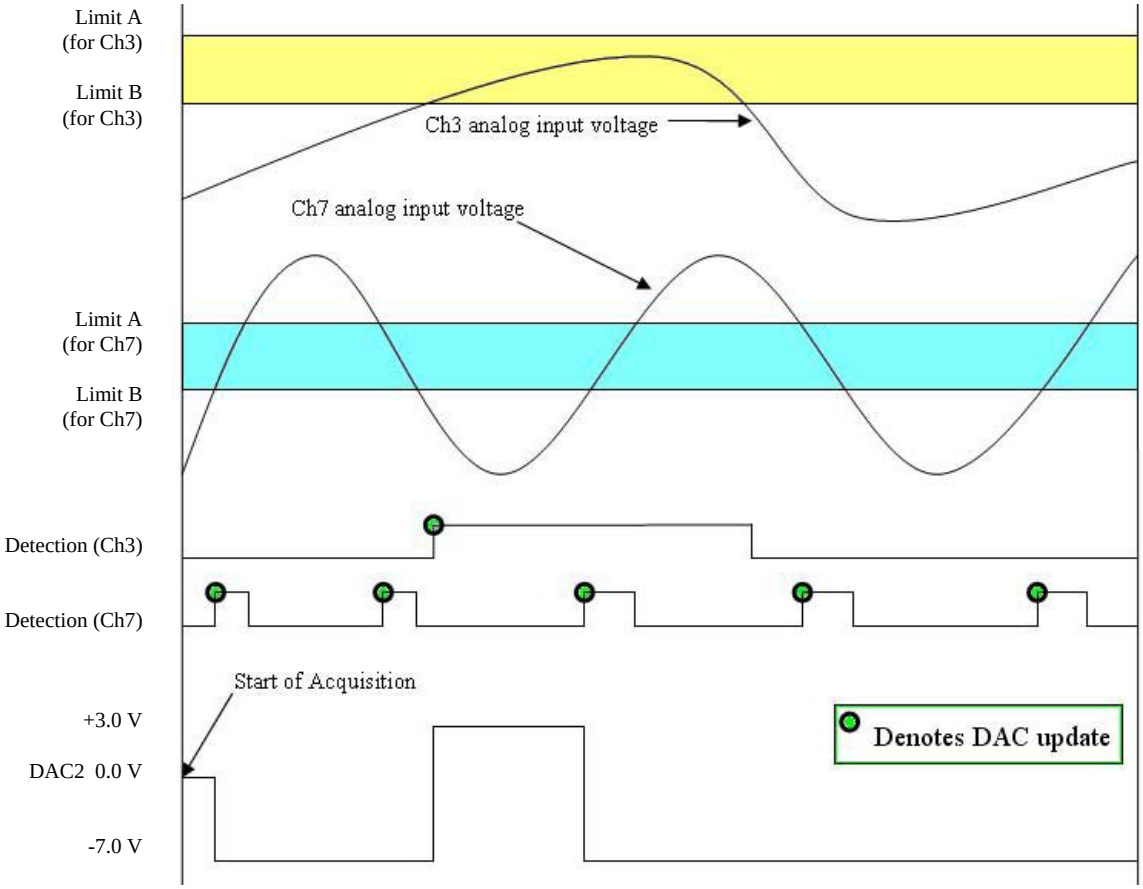
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Using Multiple Inputs to Control One DAC Output

Update Mode: Rising Edge, for each of 2 channels
Criteria Used: Inside Window, for each of 2 channels

The figure below shows how multiple inputs can update one output. In the following figure the DAC2 analog output is being updated. Analog input Channel 3 has an *inside-the-window* setpoint applied. Whenever Channel 3's input goes inside the programmed window, DAC2 will be updated with 3.0V.

Analog input Channel 7 also has an *inside-the-window* setpoint applied. Whenever Channel 7's input goes inside the programmed window, DAC2 will be updated with *minus* 7.0V.



Using Two Criteria to Control an Output*

* The update *on True Only* mode was selected and therefore the updates for DAC2 will only occur when the criteria is met. However, in the above figure we see that there are 2 setpoints acting on one DAC. We can also see that the two criteria can be met simultaneously. When both criteria are *True* at the same time, the DAC2 voltage will be associated with the criteria that has been most recently met.

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The Setpoint Status Register

Regardless of which software application you are using with a DaqBoard/3000 Series device, a setpoint status register can be used to check the current state of the 16 possible setpoints. In the register, Setpoint 0 is the least significant bit and Setpoint 15 is the most significant bit. Each setpoint is assigned a value of 0 or 1. 0 indicates that the setpoint criteria is not met, i.e., the condition is false. 1 indicates that the criteria has been met, i.e., the condition is true.

In the following example, the criteria for setpoints 0, 1, and 4 is satisfied (True); but the criteria for the other 13 setpoints has not been met.

Setpoint #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
True (1) False (0)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
	<<< Most Significant Bit															Least Significant Bit >>>

From the above table we have 10011 binary, or 19 decimal, derived as follows:

Setpoint 0, having a True state, shows “1;” giving us decimal “1.”

Setpoint 1, having a True state, shows “1;” giving us decimal “2.”

Setpoint 4, having a True state, shows “1;” giving us decimal “16.”

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DaqBoard/3000 Series Specifications

I/O Comparison Matrix

Product or System	Analog Input Channels	Input Ranges	Analog Output Channels	Digital I/O Channels	Counter Inputs	Timer Outputs
DaqBoard/3000	16SE / 8DE	7	2	24	4	2
DaqBoard/3001	16SE / 8DE	7	4	24	4	2
DaqBoard/3005	16SE / 8DE	7	0	24	4	2
DaqBoard/3006	16SE only	1	0	24	4	2
DaqBoard/3000 *with* PDQ30	64SE / 32DE	7	2	24	4	2
DaqBoard/3001 *with* PDQ30	64SE / 32DE	7	4	24	4	2
DaqBoard/3005 *with* PDQ30	64SE / 32DE	7	0	24	4	2

General Specifications

Power consumption (per board): 3 W
Operating temperature: 0 to +60°C
PCI Bus: PCI r 2.2 compliant, universal 3.3V to 5V signaling support
Storage temperature: -40 to +80°C
Relative Humidity: 0 to 95% non-condensing
Vibration: MIL STD 810E Category 1 and 10
Signal I/O Connector: 68-pin standard "SCSI type III" female connector
Dimensions: 165 mm W x 15 mm D x 108 mm H (6.5" x 0.6" x 4.2")
Weight: 160 g (0.35 lbs)

Analog Inputs

Channels: 16 single-ended or 8 differential. Programmable on a per-channel basis as single-ended or differential.[=]
Expansion: An additional 48 analog inputs per board via optional PDQ30 module. Expansion channel features are identical to those of the board main channels.[=]
Expansion Connector: HDMI Connector[=]
Expansion Cable: HDMI cable: CA-266-3 (3 ft.), or CA-266-6 (6 ft.)
Over-Voltage Protection: ±30V
Ranges: Software or sequencer selectable on a per-channel basis.
±10V, ±5V, ±2V, ±1V, ±0.5V, ±0.2V, ±0.1V [=]
Input Impedance: 10MΩ single-ended; 20MΩ differential
Total Harmonic Distortion: -80 db, typical for ±10V range, 1 kHz fundamental
Signal to Noise and Distortion: 72 db, typical for ±10V range, 1 kHz fundamental
Bias Current: 40pA typical (0°C to 35°C)
Crosstalk: -67 db typical DC to 10 kHz
Common Mode Rejection: -70 dB typical DC to 1 kHz

[=] Except DaqBoard/3006, which is limited to 16 single-ended analog inputs with a fixed range of ±10V. OEMs can contact the factory for other range configurations.

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Maximum Usable Input Voltage + Common Mode Voltage	
Ranges	Maximum (CMV + V_{in})
5, 10V	10.5V
0.1, 0.2, 0.5, 1, 2V	6.0V

A/D Specifications

Type: Successive approximation

Resolution: 16 bit

Maximum Sample Rate: 1 MHz

Nonlinearity (Integral): ±2 LSB maximum

Nonlinearity (Differential): ±1 LSB maximum

Input Sequencer

Analog, digital and counter inputs can be scanned synchronously based on either an internal programmable timer, or an external clock source. Analog and digital outputs can be synchronized to either of these clocks.

Scan Clock Sources: 2

Note: The maximum scan clock rate is the inverse of the minimum scan period. The minimum scan period is equal to 1µs times the number of analog channels. If a scan contains only digital channels then the minimum scan period is 83 ns times the number of digital channels.

1. **Internal, programmable**
   Analog Channels from 1 µs to 19 hours in 20.83 ns steps
   Digital Channels and Counters from 83.33 ns to 19 hours in 20.83 ns steps

2. **External, TTL level input**
   Analog Channels down to 1 µs minimum
   Digital Channels and Counters down to 83.33 ns minimum

Programmable Parameters per Scan: Channel (random order), gain

Depth: 512 location

On-board Channel-to-Channel Scan Rate:

Analog: 1 MHz maximum
Digital: 12 MHz if no analog channels are enabled, 1 MHz with analog channels enabled

Voltage Range*	Accuracy ±(% Reading + % Range) 23ºC ± 10°C, 1 year	Temperature Coefficient ± (ppm of Reading + ppm Range)/ºC 0ºC to 13°C and 33ºC to 60ºC	Noise** (cts RMS)
-10V to 10V (/3006)	0.040% + 0.010%	14 + 8	2.0
-10V to 10V	0.031% + 0.008%	14 + 8	1.5
-5V to 5V	0.031% + 0.009%	14 + 9	2.0
-2V to 2V	0.031% + 0.010%	14 + 10	1.6
-1V to 1V	0.031% + 0.012%	14 + 12	2.5
-500 mV to 500 mV	0.031% + 0.018%	14 + 18	4.0
-200 mV to 200 mV	0.036% + 0.012%	14 + 12	5.0
-100 mV to 100 mV	0.042% + 0.018%	14 + 18	9.0

* Specifications assume differential input single-channel scan, 1-MHz scan rate, unfiltered, CMV=0.0V, 30 minute warm-up, exclusive of noise. DaqBoard/3006 is single-ended only.

** Noise reflects 10,000 samples at 1-MHz, typical, differential short, CA-G56. DaqBoard/3006 is single-ended only.

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External Acquisition Scan Clock Input

Maximum rate: 1.0 MHz

Clock Signal Range: Logical zero 0V to 0.8V; Logical one 2.4V to 5.0V; protected to ±15V

Minimum pulse width: 50 ns high, 50 ns low

Triggering

Trigger Sources: 6, individually selectable for starting and stopping an acquisition. Stop acquisition can occur on a different channel than start acquisition; stop acquisition can be triggered via modes 2, 4, 5, or 6 described below.

1. **Single-Channel Analog Hardware Trigger**: Any analog input channel can be software programmed as the analog trigger channel, including any of the analog expansion channels.
   Input Signal Range: -10 to +10V max
   Trigger Level: Programmable; 12-bit resolution
   Hysteresis: Programmable; 12-bit resolution
   Latency: 350 ns typical, 1.3 µs max
   Accuracy: ±0.5% of reading, ±2 mV offset
   Noise: 2 mV RMS

2. **Single-Channel Analog Software Trigger**: Any analog input channel, including any of the analog expansion channels, can be selected as the software trigger channel. If the trigger channel involves a calculation, such as temperature, then the driver automatically compensates for the delay required to obtain the reading, resulting in a maximum latency of one scan period.
   Input Signal Range: Anywhere within the range of the selected trigger channel
   Trigger Level: Programmable; 16-bit resolution, including “window triggering”
   Latency: One scan period max

3. **Single-Channel Digital Trigger**: A separate digital input is provided for digital triggering.
   Input Signal Range: -15V to +15V
   Trigger Level: TTL
   Minimum Pulse Width: 50 ns high; 50 ns low
   Latency: 100 ns typical, 1.1 µs max

4. **Digital Pattern Triggering**: 8 or 16-bit pattern triggering on any of the digital input ports. Programmable for trigger on equal, above, below, or within/outside of a window. Individual bits can be masked for “don’t care” condition.
   Latency: One scan period max

5. **Counter/Totalizer Triggering**: Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, above, below, or within/outside of a window.
   Latency: One scan period max

6. **Software Triggering**: Trigger can be initiated under program control.

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Analog Outputs **Applicable to DaqBoard/3000 and /3001 only**

Analog output channels are updated synchronously relative to scanned inputs, and clocked from either an internal onboard clock, or an external clock source. Analog outputs can also be updated asynchronously, independent of any other scanning in the system. Bus mastering DMA provides CPU and system-independent data transfers, ensuring accurate outputs that are irrespective of other system activities. Streaming from disk or memory is supported, allowing continuous, nearly-infinite length, waveform outputs (limited only by available PC system resources).

Channels:

DaqBoard/3000: 2 DAC channels (DAC0, DAC1)
DaqBoard/3001: 4 DAC channels (DAC0, DAC1, DAC2, DAC3)

Resolution: 16 bits

Data Buffer: PC based memory

Output Voltage Range: ±10V

Output Current: ±10 mA

Offset Error: ±0.0045V maximum

Digital Feedthrough: <10 mV when updated

DAC Analog Glitch: <12 mV typical at major carry

Gain Error: ±0.01%

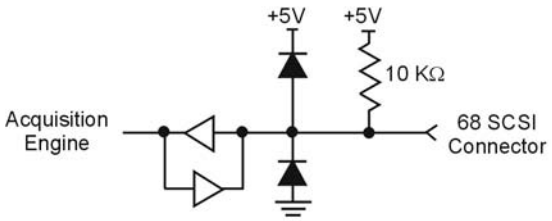
Update Rate: 1 MHz maximum, 19 hours minimum (no minimum with external clock); resolution: 20.83 ns

Settling Time: 2 μs to rated accuracy

Clock Sources: 4 programmable

1. Onboard D/A clock, independent of scanning input clock
2. Onboard scanning input clock
3. External D/A input clock, independent of external scanning input clock
4. External scanning input clock

Digital I/O



One Digital I/O Channel, Typical

Channels: 24

Ports: 3 x 8-bit. Each port is programmable as input or output.

Input Scanning Modes: 2 programmable

1. Asynchronous, under program control at any time relative to input scanning
2. Synchronous with input scanning

Input Characteristics: 10K Ω pull up to +5V, 20 pF to common

Input Protection: ±15 kV ESD clamp diodes parallel

Input Levels:

Low: 0 to 0.8V
High: +2.0V to +5.0V

Output Levels:

Low: < 0.8V
High: >2.0V

Sampling/Update Rate: 12 MHz maximum

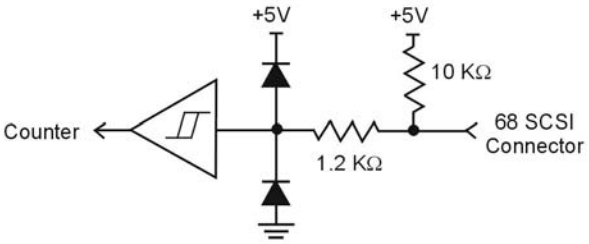
Output Characteristics: Output 12 mA per pin, 200 mA total continuous (per bank of 24 outputs)

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Pattern Generation Output

Two of the 8-bit ports can be configured for 16-bit pattern generation. The pattern can be updated synchronously with an acquisition at up to 12 MHz.

Counters



One Counter Channel, Typical

Each of the four high-speed, 32-bit counter channels can be configured for counter, period, pulse width, time between edges, or multi-axis quadrature encoder modes. Counter inputs can be scanned synchronously along with analog and digital scanned inputs, based on an internal programmable timer, or an external clock source.

Channels: 4 x 32-bit

Input Frequency: 20 MHz maximum

Input Signal Range: -5V to +10V

Input Characteristics: 10 kΩ pull-up, ±15 kV ESD protection

Trigger Level: TTL

Minimum pulse width: 25 ns high, 25 ns low

Debounce Times: 16 selections from 500 ns to 25.5 ms. Positive or negative edge sensitive. Glitch detect mode or debounce mode.

Time Base Accuracy: 30 ppm (0º to 50ºC)

Five Programmable Modes: Counter, Period, Pulsewidth, Timing, Encoder

1. Counter Mode Options: Totalize, Clear on Read, Rollover, Stop at all Fs, 16-bit or 32-bit, any other channel can gate or decrement the counter

2. Period Mode Options: Measure x1, x10, x100, or x1000 periods, 16-bit or 32-bit, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the period measurement

3. Pulsewidth Mode Options: 16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the pulsewidth measurement

4. Timing Mode Options: 16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs)

5. Encoder Mode Options: x1, x2, x4 options, 16-bit or 32-bit values, Z-channel clearing of the counter, any other channel can gate the counter

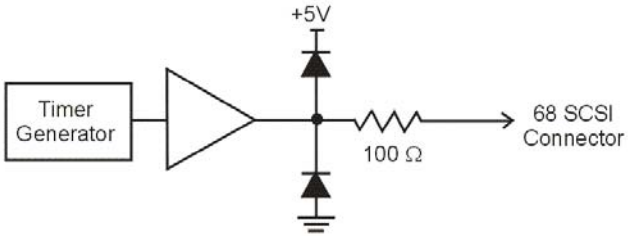
Power Available for Encoders: 5V @ 500 mA max

Multi-axis Quadrature Encoder Inputs:

- o 1 channel with A (phase), B (phase), and Z (index)
- o 2 channel with A (phase) and B (phase)
- o x1, x2, and x4 count modes
- o Single-ended TTL

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Frequency/Pulse Generators



One Timer Channel, Typical

Channels: 2 x 16-bit
Output Waveform: Square wave
Output Rate: 1 MHz base rate divided by 1 to 65535 (programmable)
High Level Output Voltage: 2.0V minimum @ -1.0 mA, 2.9V minimum @ -400 µA
Low Level Output Voltage: 0.4V maximum @ 400 µA

Software

DaqViewXL/Plus	DaqView add-on for seamless execution with Microsoft Excel's tool palette
DaqView/Pro	DaqView add-on includes all of the features of DaqViewXL/Plus, plus frequency-domain analysis
DASYLab	Icon-based data acquisition, graphics, control, and analysis software

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PDQ30 Specifications

General

Operating Temperature: -30˚ to +70˚C
Storage Temperature: -40˚ to +80˚C
Power Consumption: 400 mW (max)
Warm up: 30 minutes to rated specifications
Relative Humidity: 0 to 95%, non-condensing
Vibration: MIL STD 810E, category 1 and 10
Communications Connector: 25 pin DSUB
Signal I/O Connector: Six removable screw terminal blocks (12 connections each)
Dimensions: 269mm W x 92mm D x 45 mm H: (10.6" x 3.6" x 1.6")
Weight: 400g (0.88 lbs)

Analog Inputs

Channels: 48 single-ended inputs; 24 channels differential inputs
Voltage Measurement Speed: 1µs per channel
Temperature Measurement Speed: programmable from 100µs to 20ms per channel
Ranges: ±10V, ±5V, ±2V, ±1V, ±500mV, ±200mV, ±100mV, universal thermocouple.
Software or sequencer selectable on a per-channel basis
Total Harmonic Distortion: -80dB typical for ±10V range, 1 kHz fundamental
Signal to Noise and Distortion: 72dB typical for ±10V range, 1 kHz fundamental
Input Impedance: 10M Ohm (single-ended); 20M Ohm (differential)
Bias Current: 40 pA typical (0 to 35°C)
Crosstalk: -67 db typical DC to 10 kHz
Over-Voltage Protection: ±20V

Voltage Range*	Accuracy ±(% Reading + % Range) 23ºC ± 10°C, 1 year	Temperature Coefficient ± (ppm of Reading + ppm Range)/ºC 0ºC to 13°C and 33ºC to 60ºC	Noise** (cts RMS)
-10V to 10V	0.031% + 0.008%	14 + 8	2
-5V to 5V	0.031% + 0.009%	14 + 9	2
-2V to 2V	0.031% + 0.010%	14 + 10	2
-1V to 1V	0.031% + 0.012%	14 + 12	3
-500 mV to 500 mV	0.031% + 0.018%	14 + 18	5
-200 mV to 200 mV	0.036% + 0.012%	14 + 12	9
-100 mV to 100 mV	0.042% + 0.018%	14 + 18	17

* Specifications assume differential input signal channel scan, 1-MHz scan rate, unfiltered, CMV=0.0V, 30 minute warm-up, DaqBoard/3000
** Noise reflects 10,000 samples at 1-MHz, typical, differential short

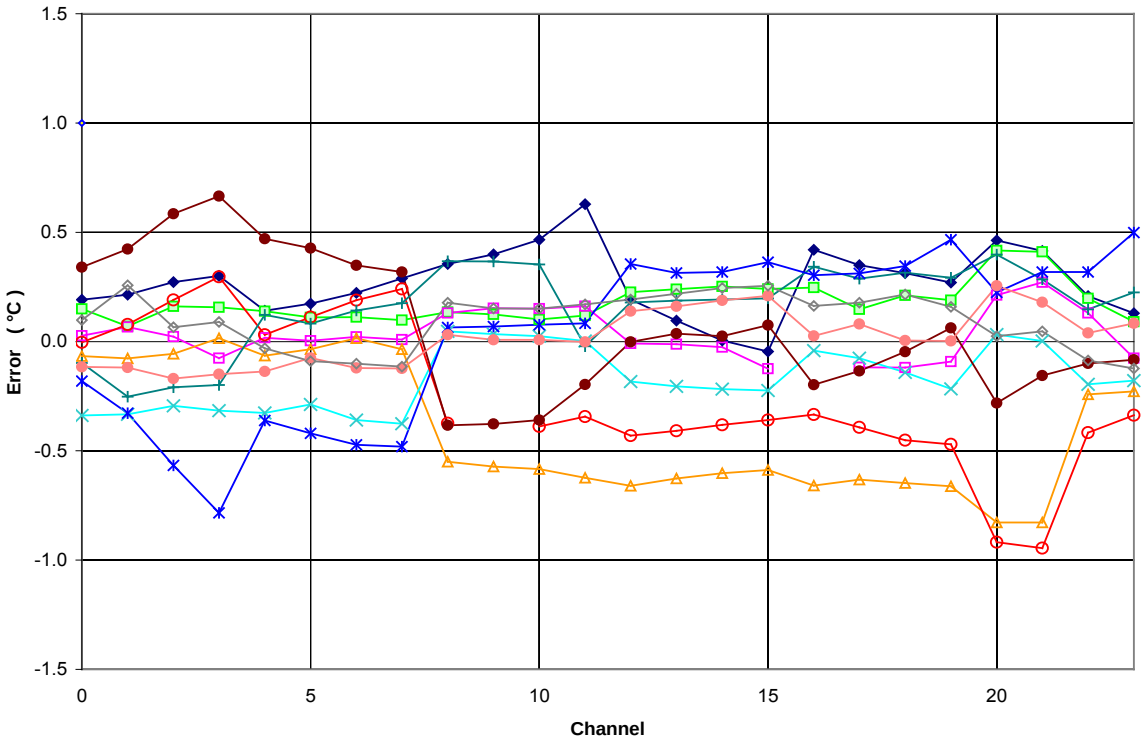
TC Types and Accuracy[1]			
TC	Temp Range (°C)	Accuracy (±°C)	Noise (±°C)
J	-200 to +760	1.1	0.2
K	-200 to +1200	1.2	0.2
T	-200 to +400	1.1	0.2
E	-270 to +650	1.0	0.2
R	-50 to +1768	2.5	0.2
S	-50 to +1768	2.6	0.2
B	+50 to +1780	3.3	0.2
N	-270 to +1300	1.5	0.2

[1] Assumes 256 average mode applied, CMV=0.0V, 30 minute warm-up, and 25ºC ambient temperature. Excludes thermocouple errors.

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PDQ30 Type T Thermocouple

Typical Performance of 12 PDQ30 Units; 0°C (Note 1)



Note 1: Assumes 16384 oversampling applied, CMV = 0.0V, 60 minute warm-up, still environment, and 25°C ambient temperature. Excludes thermocouple error. TC_{IN} = 0.0 °C

Accessories and Cables

Termination Board (TB-100): Termination board with screw terminals for access to DaqBoard/3000 Series I/O. The terminal board connects to the DaqBoard's 68-pin connector via a CA-G55, CA-56, or CA-56-6 cable.

Rack Mount Kit (Rack3): Kit for mounting the TB-100 termination board to a rack.

DBK215 Termination Module: Includes 16 BNC connectors and internal screw-terminals. DBK215 connects to the DaqBoard's 68-pin connector via a CA-G55, CA-56, or CA-56-6 cable.

PDQ30 Analog Input Expansion Module: Adds 48 SE [or 24 DE] channels to a DaqBoard/3000 Series board. Characteristics of the expansion channels are identical to those of the onboard channels. PDQ30 connects to the 3000 Series board via HDMI cable CA-266-3, or CA-266-6. *PDQ30 cannot be connected to a DaqBoard/3006.*

CA-G55: 68-conductor ribbon expansion cable. Can be used to connect a DaqBoard/3000 Series board to a TB-100 or DBK215. Cable length: 3 ft.

CA-G56: 68-conductor shielded expansion cable. Can be used to connect a DaqBoard/3000 Series board to a TB-100 or DBK215. Cable length: 3 ft.

CA-G56-6: 68-conductor shielded expansion cable. Can be used to connect a DaqBoard/3000 Series board to a TB-100 or DBK215. Cable length: 6 ft.

CA-266-3: HDMI cable. Can be used to connect a PDQ30 expansion module to a DaqBoard/3000 Series board. Cable length: 3 ft. *PDQ30 cannot be connected to a DaqBoard/3006.*

CA-266-6: HDMI cable. Can be used to connect a PDQ30 expansion module to a DaqBoard/3000 Series board. Cable length: 6 ft. *PDQ30 cannot be connected to a DaqBoard/3006.*

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Appendix A — DBK215 16-Connector BNC Connection Module

With 68-Pin SCSI Adaptability for Analog I/O, Digital I/O, & Pulse/Frequency

Overview …… 1
Block Diagram …… 2
Connection Tips…… 3
System Examples …… 4
Using the Screw-Terminal Blocks …… 5
Adding RC Filter Networks …… 11
Specifications …… 13



DBK215 Front Panel
Upper Slot for Terminal Board Wiring Pass-Through
Lower section of 16 BNC Connectors

The DBK215 module is compatible with the following products:

- DaqBoard/500 Series • DaqBoard/1000 Series • DaqBoard/3000 Series

Overview



DBK215 Rear Panel
Includes a 68-pin SCSI connector designated as P5.

The DBK215 module includes:

- BNC Access to 16 inputs or outputs (on front panel)
- on-board screw-terminal blocks*
- on-board socket locations for custom RC Filter networks*
- 68-pin SCSI connector (on rear panel)

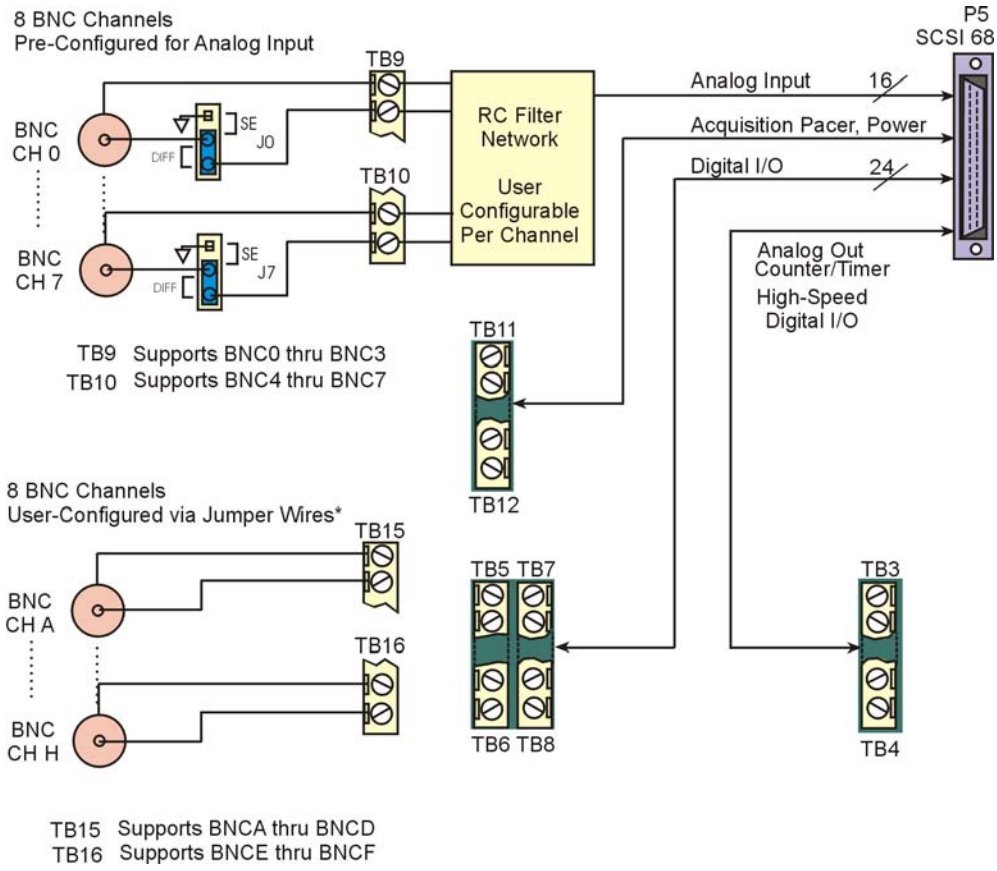
* The top cover plate must be removed to access the terminal blocks and the RC filter network section of the board.

DBK215's SCSI connector (P5) connects to a second 68-pin SCSI connector on a DaqBoard/500 Series, DaqBoard/1000 Series, or DaqBoard/3000 Series board. Connection is made via a CA-G55, CA-G56, or CA-G56-6 cable. Cable descriptions are provided on page A-2.

The DBK215 provides BNC and screw-terminal access to all analog and digital I/O from the host data acquisition device. Related to the screw-terminals is a front panel slot for routing all I/O wiring.

Reference Note:
DBK215 is intended for DaqBoard/500 Series, /1000 Series, and /3000 Series applications. Refer to the associated documentation as needed. For information concerning similar16 channel BNC connectivity/interface boards, designed for use with other products, refer to the DBK213 and DBK214 sections of the DBK Options manual (p/n 457-0905).

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DBK215 Block Diagram

* Accessory Kit p/n 1139-0800 includes jumper wires and a screw driver.

Note that the 68-pin SCSI (P5) connector typically connects to a SCSI connector via a CA-G55, CA-G56, or CA-G56-6 cable.

- CA-G55 is a 3-foot long cable.
- CA-G56 is a 3-foot long shielded cable.
- CA-G56-6 is a 6-foot long shielded cable.

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Connection Tips

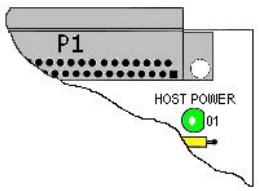
CAUTION

Turn off power to the host PC and externally connected equipment prior to connecting cables or signal lines to DBKs. Electric shock or damage to equipment can result even under low-voltage conditions.

Take ESD precautions (packaging, proper handling, grounded wrist strap, etc.)

Use care to avoid touching board surfaces and onboard components. Only handle boards by their edges (or ORBs, if applicable). Ensure boards do not come into contact with foreign elements such as oils, water, and industrial particulate.

1. Ensure power is removed from all device(s) to be connected.
2. As soon as the DBK215 cover is removed, verify that the Host Power LED is "Off." See figure at right for location.
3. Observe ESD precautions when handling the board and making connections.
4. You do not need to remove the cover unless you need to access a terminal block, customize an RC filter network, or set a BNC channel to Single-Ended mode or to Differential mode (via Jumpers J0 through J7). Information regarding these tasks follows shortly.

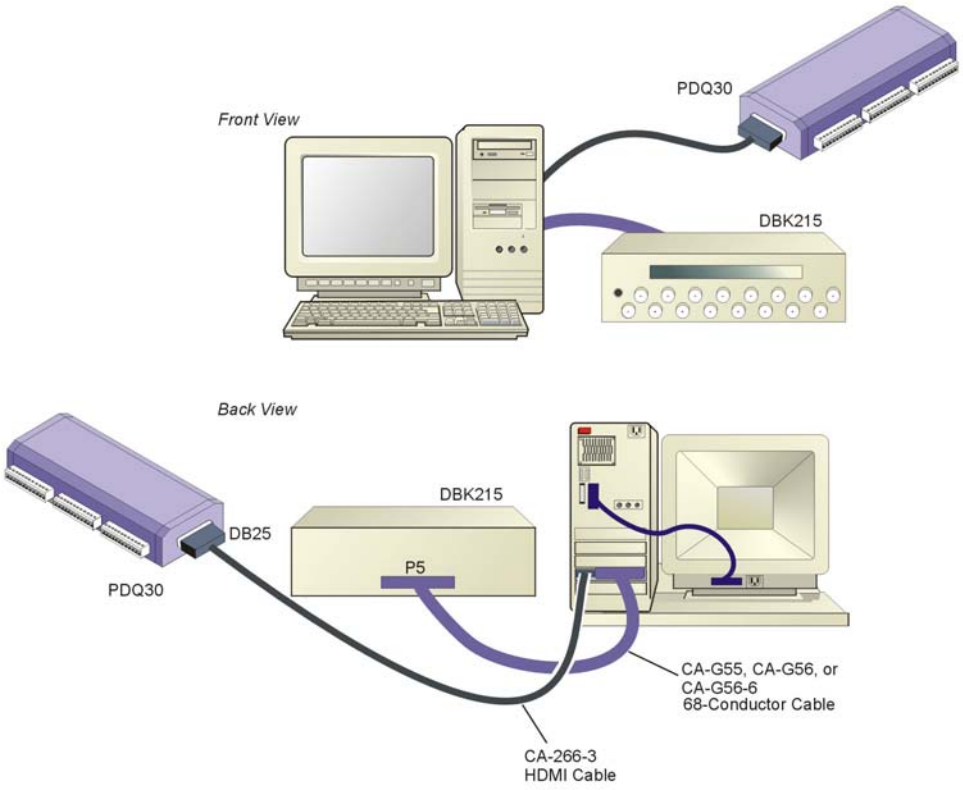


Location of DBK215's Host Power LED

5. DBK215's 68-pin SCSI (P5) connector typically connects to a board's SCSI connector via a CA-G55, CA-G56, or CA-G56-6 cable.
   - CA-G55 is a 3-foot long cable.
   - CA-G56 is a 3-foot long shielded cable.
   - CA-G56-6 is a 6-foot long shielded cable.
6. Refer to the separate CE Cable Kit instructions that are included with the associated CE cable kit. Refer to the Declaration of Conformity in regard to meeting CE requirements.

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System Example



DBK215 and PDQ30 Connection to a DaqBoard/3000 Series Board

Notes regarding the above system example:

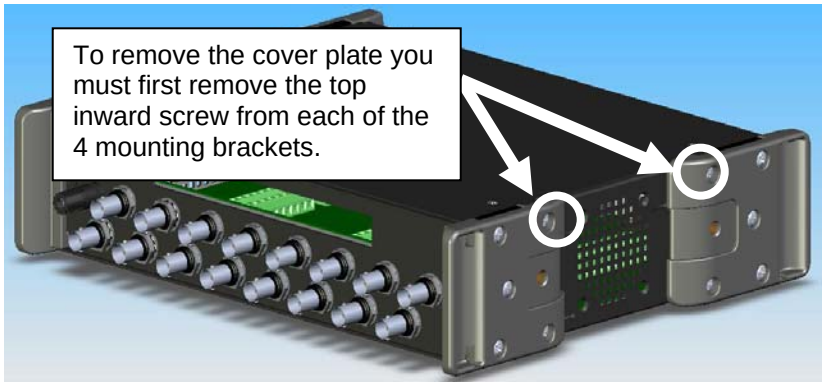
1) Any of three 68-conductor SCSI ribbon cables can be used to connect the DBK215 to the board's SCSI..
   - o CA-G55 is a 3-foot long cable.
   - o CA-G56 is a 3-foot long shielded cable.
   - o CA-G56-6 is a 6-foot long shielded cable.
2) Signal lines connect to the DBK215's front panel BNC connectors or to the internal screw-terminal board.
3) When signal lines are connected to the DBK215's terminal blocks (instead of the BNC connectors) the wires are routed out through the upper slot of the front panel.
4) The PDQ30 analog input expansion module can be connected to a /3000 Series board's HDMI connector. It does not apply to DaqBoard/500 Series or /1000 Series boards.

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Using the Screw-Terminal Blocks

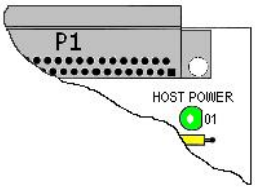
You must remove the DBK215 module's cover plate to access the screw terminal blocks. This is described in steps 1 and 2 below.

1. Remove the top inward screws from each of the 4 mounting brackets. See following figure.



The Cover Plate is Secured by 4 Srews [2 Screws per-side]

2. After the 4 screws have been removed, carefully remove the cover plate.
3. As soon as the DBK215 cover is removed, verify that the Host Power LED is "Off." See following figure for location.



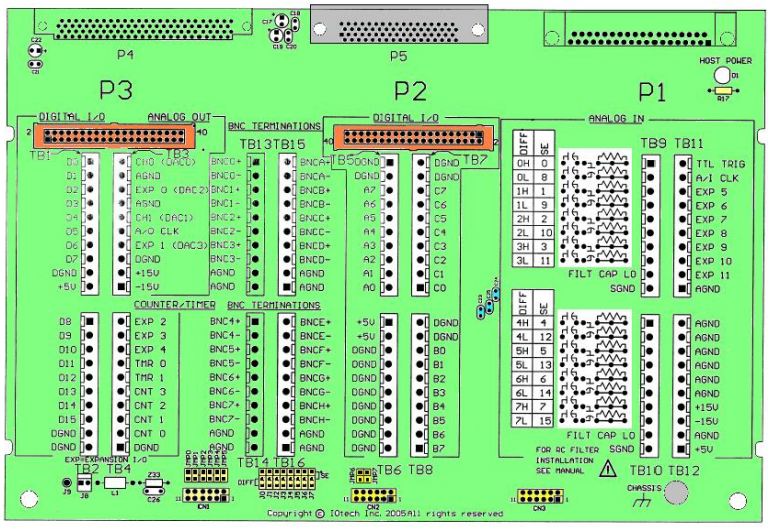
Host Power LED Location

4. Make the wiring connections to the terminals. Refer to the board's silkscreen and to the pin correlations on the next few pages.
5. Tighten the terminal block screws snug; but do not over-tighten.
6. After all terminal connections are made and verified correct, return the cover to the unit and secure in place with the 4 screws removed earlier. Tighten snug, but do not over-tighten.

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In general, the following *terminal block-to-signal* relationships apply:

DBK215 Terminal Blocks	Used for . . .	Alternative
TB9 TB10	ANALOG INPUT	BNC 0 thru 7
TB11 TB12	ANALOG INPUT	N/A
TB5 TB6 TB7 TB8	DIGITAL I/O	N/A
TB13** TB14**	ANALOG INPUT BNC Channels 0 thru 7**	TB9,TB10
TB15 TB16 (Note 1)	USER CONFIGURABLEB NC Channels A thru H	(See Note 1)
TB1 TB2	-- Not Used---	N/A
TB3 TB4	PULSE/ FREQUENCY ANALOG OUTPUT	N/A



DBK215 Board

* P4 is used for connecting to DaqBoard/2000 Series devices.

** TB13 and TB14 are "virtual" terminal blocks which are routed in the printed circuit board to TB9 and TB10. The TB13 and TB14 silk-screened locations on the DBK215 board do not have physical screw terminal blocks.

Note 1: TB15 and TB16 are used for optional user-configured BNC connectors A through H. These connectors can be configured on a per-channel basis as Analog [Input or Output], Digital I/O, or Counter/Timer. When BNC A through H are used, the user must route wires from the "BNC routing terminal blocks" (TB15 and TB16) to the appropriate functional TB termination points.

Accessory Wire Kit, p/n 1139-0800 includes jumper wires and a screwdriver.

The following pages correlate the DBK215 terminal block connectors with the 68-pin SCSI connector.

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Analog I/O Correlation to 68-pin SCSI

Also see “Correlation to BNC Terminations (TB13 and TB14) on page DBK215-10.”

TB9		Pin Number and Description	
DIFF	SE		
0H	0	68	CH 0 IN (Single-Ended Mode) / CH 0 HI IN (Differential Mode)
0L	8	34	CH 8 IN (Single-Ended Mode) / CH 0 LO IN (Differential Mode)
1H	1	33	CH 1 IN (Single-Ended Mode) / CH 1 HI IN (Differential Mode)
1L	9	66	CH 9 IN (Single-Ended Mode) / CH 1 LO IN (Differential Mode)
2H	2	65	CH 2 IN (Single-Ended Mode) / CH 2 HI IN (Differential Mode)
2L	10	31	CH 10 IN (Single-Ended Mode) / CH 2 LO IN (Differential Mode)
3H	3	30	CH 3 IN (Single-Ended Mode) / CH 3 HI IN (Differential Mode)
3L	11	63	CH 11 IN (Single-Ended Mode) / CH 3 LO IN (Differential Mode)
FILT CAP LO		**N/A**	For RC filter networks install a wire jumper between the relevant FILT CAP LO and AGND. Note that there is no association between FILT CAP LO and P4.
SGND		62	Signal Ground, Sense Common; reference ground, not for general use.



P1 – TB9
(Note 2)

TB10		Pin Number and Description	
DIFF	SE		
4H	4	28	CH 4 IN (Single-Ended Mode) / CH 4 HI IN (Differential Mode)
4L	12	61	CH 12 IN (Single-Ended Mode) / CH 4 LO IN (Differential Mode)
5H	5	60	CH 5 IN (Single-Ended Mode) / CH 5 HI IN (Differential Mode)
5L	13	26	CH 13 IN (Single-Ended Mode) / CH 5 LO IN (Differential Mode)
6H	6	25	CH 6 IN (Single-Ended Mode) / CH 6 HI IN (Differential Mode)
6L	14	58	CH 14 IN (Single-Ended Mode) / CH 6 LO IN (Differential Mode)
7H	7	57	CH 7 IN (Single-Ended Mode) / CH 7 HI IN (Differential Mode)
7L	15	23	CH 15 IN (Single-Ended Mode) / CH 7 LO IN (Differential Mode)
FILT CAP LO		**N/A**	For RC filter networks install a wire jumper between the relevant FILT CAP LO and AGND.
SGND		62	Signal Ground, Sense Common; reference ground, not for general use.



P1 – TB10
(Note 2)

TB11		
TTL TRIG	6	TTL Trigger, Digital IN, External TTL Trigger Input
A/I CLK	2	A/I Clock, External ADC Pacer Clock Input/ Internal ADC Pacer Clock Output
EXP 5	**N/A**	Expansion 5. Digital OUT, external GAIN select bit 1
EXP 6	**N/A**	Expansion 6. Digital OUT, external GAIN select bit 0
EXP 7	**N/A**	Expansion 7. Digital OUT, external ADDRESS, select bit 3
EXP 8	**N/A**	Expansion 8. Digital OUT, external ADDRESS, select bit 2
EXP 9	**N/A**	Expansion 9. Digital OUT, external ADDRESS, select bit 1
EXP 10	**N/A**	Expansion 10. Digital OUT, external ADDRESS, select bit 0
EXP 11	**N/A**	Expansion 11. Simultaneous Sample and Hold (SSH)
AGND	*	Analog Ground, Common



P1 – TB11

TB12		
AGND	*	Analog Ground, Common
AGND	*	Analog Ground, Common
AGND	*	Analog Ground, Common
AGND	*	Analog Ground, Common
AGND	*	Analog Ground, Common
AGND	*	Analog Ground, Common
+ 15 V	**N/A**	Expansion, +15 V Power
- 15 V	**N/A**	Expansion, -15 V Power
AGND	*	Common Ground
+ 5 V	19	Expansion, +5 V Power



P1 – TB12

*The following SCSI Pins connect to Analog Common: 24, 27, 29, 32, 55, 56, 59, 64, and 67.

Note 2: For TB9 and TB10, the filter network portion of the silkscreen is not shown. Instead, the DIFF and SE channel identifiers have been moved next to the screws for ease in identification.

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Digital I/O Correlation to 68-pin SCSI

TB5	Pin Number and Description	
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
A7	49	Digital I/O: Port A, Bit 7
A6	15	Digital I/O: Port A, Bit 6
A5	50	Digital I/O: Port A, Bit 5
A4	16	Digital I/O: Port A, Bit 4
A3	51	Digital I/O: Port A, Bit 3
A2	17	Digital I/O: Port A, Bit 2
A1	52	Digital I/O: Port A, Bit 1
A0	18	Digital I/O: Port A, Bit 0



P2 – TB5

TB6	Pin Number and Description	
+5 V	19	Expansion +5 V Power
+5 V	19	Expansion +5 V Power
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common



P2 – TB6

TB7	Pin Number and Description	
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
C7	41	Digital I/O: Port C, Bit 7
C6	7	Digital I/O: Port C, Bit 6
C5	42	Digital I/O: Port C, Bit 5
C4	8	Digital I/O: Port C, Bit 4
C3	43	Digital I/O: Port C, Bit 3
C2	9	Digital I/O: Port C, Bit 2
C1	44	Digital I/O: Port C, Bit 1
C0	10	Digital I/O: Port C, Bit 0



P2 – TB7

TB8	Pin Number and Description	
DGND	**	Digital Ground, Common
DGND	**	Digital Ground, Common
B0	14	Digital I/O: Port B, Bit 0
B1	48	Digital I/O: Port B, Bit 1
B2	13	Digital I/O: Port B, Bit 2
B3	47	Digital I/O: Port B, Bit 3
B4	12	Digital I/O: Port B, Bit 4
B5	46	Digital I/O: Port B, Bit 5
B6	11	Digital I/O: Port B, Bit 6
B7	45	Digital I/O: Port B, Bit 7



P2 – TB8

* The following SCSI Pins connect to Analog Common: 24, 27, 29, 32, 55, 56, 59, 64, and 67.
** The following SCSI Pins connect to Digital Common: 35, 36, 40, and 53.

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Pulse/Frequency Correlation to 68-pin SCSI

TB1	Pin Number and Description		
D0	N/A	P3 Digital Port Bit 0	
D1	N/A	P3 Digital Port Bit 1	
D2	N/A	P3 Digital Port Bit 2	
D3	N/A	P3 Digital Port Bit 3	**TB1 is NOT USED**
D4	N/A	P3 Digital Port Bit 4	
D5	N/A	P3 Digital Port Bit 5	
D6	N/A	P3 Digital Port Bit 6	
D7	N/A	P3 Digital Port Bit 7	
DGND	N/A	Digital Ground, Common	
+5V	N/A	Expansion, +5 Volt Power	



P3 – TB1 (not used)

TB2	Pin Number and Description		
D8	N/A	P3 Digital Port Bit 8	
D9	N/A	P3 Digital Port Bit 9	
D10	N/A	P3 Digital Port Bit 10	
D11	N/A	P3 Digital Port Bit 11	**TB2 is NOT USED**
D12	N/A	P3 Digital Port Bit 12	
D13	N/A	P3 Digital Port Bit 13	
D14	N/A	P3 Digital Port Bit 14	
D15	N/A	P3 Digital Port Bit 15	
DGND	N/A	Digital Ground, Common	
DGND	N/A	Digital Ground, Common	



P3 – TB2 (not used)

TB3	Pin Number and Description	
CH0 (DAC0)	22	Analog Out; Analog DAC 0 Output
AGND	*	Analog Ground, Common; intended for use with DACs
EXP 0 (DAC2)	N/A	Analog Out; Analog DAC 2 Output
AGND	*	Analog Ground, Common; intended for use with DACs
CH1 (DAC1)	21	Analog Out; Analog DAC 1 Output
A/O CLK	1	Analog Out Clock; External DAC Pacer Clock Input/ Internal DAC Pacer Clock Output
EXP 1 (DAC3)	N/A	Analog Out; Analog DAC 3 Output
DGND	**	Digital Ground, Common
+15 V	N/A	Expansion, + 15 VDC
-15 V	N/A	Expansion, -15 VDC



P3 – TB3

TB4	Pin Number and Description	
EXP 2	N/A	Reserved
EXP 3	N/A	Reserved
EXP 4	N/A	Reserved
TMR 0	3	P3 Timer 0 Output
TMR 1	37	P3, Timer 1 Output
CNT 3	38	P3 Counter 3 Input
CNT 2	4	P3 Counter 2 Input
CNT 1	39	P3 Counter 1 Input
CNT0	5	P3 Counter 0 Input
DGND	**	Digital Ground, Common



P3 – TB4

* The following SCSI Pins connect to Analog Common: 24, 27, 29, 32, 55, 56, 59, 64, and 67.
** The following SCSI Pins connect to Digital Common: 35, 36, 40, and 53.

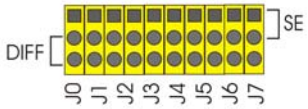
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Correlation to Analog Input BNC Terminations – BNC 0 through BNC 7

"Virtual" Terminal Blocks TB13 and TB14 for ANALOG INPUT connect to TB9 and TB10 through the printed circuit board.

TB13 ("Virtual" Terminal Block)			68-Pin SCSI Connector, Pin Number and Description		
BNC CH	**DIFF**	**SE**	**Pin**	**SE** = Single Ended ; **DIFF** = Differential	**Jumper Used**
BNC0+	0H	0	68	CH 0 IN (SE) / CH 0 HI IN (DIFF)	J0
BNC0-	0L	8	34	CH 8 IN (SE) / CH 0 LO IN (DIFF)	
BNC1+	1H	1	33	CH 1 IN (SE) / CH 1 HI IN (DIFF)	J1
BNC1-	1L	9	66	CH 9 IN (SE) / CH 1 LO IN (DIFF)	
BNC2+	2H	2	65	CH 2 IN (SE) / CH 2 HI IN (DIFF)	J2
BNC2-	2L	10	31	CH 10 IN (SE) / CH 2 LO IN (DIFF)	
BNC3+	3H	3	30	CH 3 IN (SE) / CH 3 HI IN (DIFF)	J3
BNC0+	3L	11	63	CH 11 IN (SE) / CH 3 LO IN (D DIFF)	
AGND	N/A	N/A	*	Analog Ground	N/A
AGND	N/A	N/A	*	Analog Ground	N/A

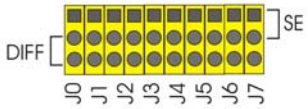
TB13 does not physically exist on DBK215. A silkscreen of TB13 is present as a visual aid to signal routing and configuration.



A header located beneath TB14 and TB16 is used to set the BNC channels to Single-Ended or to Differential. Simply place channel's 2-pin jumper in the appropriate position (SE or DIFF).

TB14 ("Virtual" Terminal Block)			68-Pin SCSI Connector, Pin Number and Description		
BNC CH	**DIFF**	**SE**	**Pin**	**SE** = Single Ended ; **DIFF** = Differential	**Jumper Used**
BNC4+	4H	4	28	CH 4 IN (SE) / CH 4 HI IN (DIFF)	J4
BNC4-	4L	12	61	CH 12 IN (SE) / CH 4 LO IN (DIFF)	
BNC5+	5H	5	60	CH 5 IN (SE) / CH 5 HI IN (DIFF)	J5
BNC5-	5L	13	26	CH 13 IN (SE) / CH 5 LO IN (DIFF)	
BNC6+	6H	6	25	CH 6 IN (SE) / CH 6 HI IN (DIFF)	J6
BNC6-	6L	14	58	CH 14 IN (SE) / CH 6 LO IN (DIFF)	
BNC7+	7H	7	57	CH 7 IN (SE) / CH 7 HI IN (DIFF)	J7
BNC7+	7L	15	23	CH 15 IN (SE) / CH 7 LO IN (DIFF)	
AGND	N/A	N/A	*	Analog Ground	N/A
AGND	N/A	N/A	*	Analog Ground	N/A

TB14 does not physically exist on DBK215. A silkscreen of TB14 is present as a visual aid to signal routing and configuration.



A header located beneath TB14 and TB16 is used to set the BNC channels to Single-Ended or to Differential. Simply place channel's 2-pin jumper in the appropriate position (SE or DIFF).

Correlation to Custom BNC Terminations – BNC A through BNC H

Pertains to Terminal Blocks TB15 and TB16 for Custom Configuration on a per-channel basis.

TB15 ("Routing" Terminal Block)	
BNC CH	**Description**
BNCA+	BNC channels A through D are configured on a per-channel basis by the user. TB15 is a routing terminal block used to connect BNCs (A thru D) to the desired signals, which are selected via a second DBK215 terminal block. For example: a user could run a wire from BNCA+ to TB4 screw terminal "TMR0" and BNCA- to TB4 DGND to create a BNC timer connection. Accessory Wire Kit, p/n 1139-0800 includes jumper wires and a screwdriver.
BNCA-	
BNCB+	
BNCB-	
BNCC+	
BNCC-	
BNCD+	
BNCD+	
AGND	Analog Ground *
AGND	Analog Ground *



TB15

TB16 ("Routing" Terminal Block)	
BNC CH	**Description**
BNCA+	BNC channels E through H are configured on a per-channel basis by the user. TB16 is a routing terminal block used to connect BNCs (E thru H) to the desired signals, which are selected via a second DBK215 terminal block. Customizing is as described for BNCA through BNCD above. Accessory Wire Kit, p/n 1139-0800 includes jumper wires and a screwdriver.
BNCA-	
BNCB+	
BNCB-	
BNCC+	
BNCC-	
BNCD+	
BNCD+	
AGND	Analog Ground *
AGND	Analog Ground *



TB16

* The following SCSI Pins connect to Analog Common: 24, 27, 29, 32, 55, 56, 59, 64, and 67.

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Adding Resistor/Capacitor Filter Networks

WARNING

Disconnect the DBK215 from power and signal sources prior to installing capacitors or resistors.

CAUTION

Ensure wire strands do not short power supply connections to any terminal potential. Failure to do so could result in damage to equipment.

Do not exceed maximum allowable inputs (as listed in product specifications). There should never be more than 30 V with reference to analog ground (AGND) or earth ground.

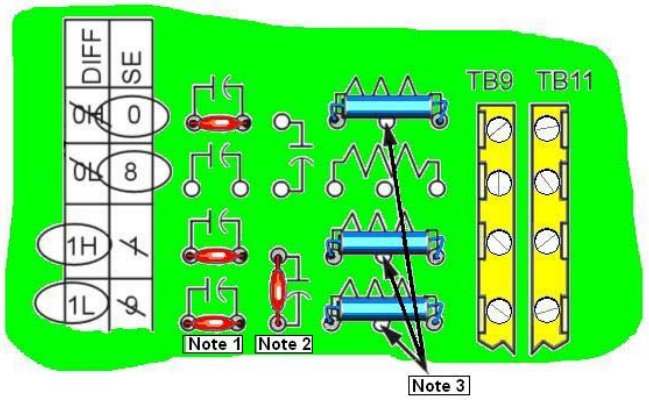
You must provide strain-relief (lead slack) to all leads leaving the module. Use tie-wraps [not included] to secure strain-relief.

Always connect the CHASSIS terminal to earth ground. This will maximize static protection.

If a channel is not associated with a DBK expansion option you can install a customized RC filter network to improve the signal-to noise ratio, assuming that an unacceptable level of noise exists. DBK215's internal board includes silk-screened sockets for installing RC filter networks. The following table contains values that are typical for RC filter network components.

Typical One-Pole Low Pass Filter Values for DBK215			
R	**C**	**f**	**f**
Ohms	**µF**	**Hertz (-3dB)**	**kHz (-3dB)**
510	1	312	0.31
510	0.47	664	0.66
510	0.22	1419	1.42
510	0.1	3122	3.12
510	0.047	6643	6.64
510	0.022	14192	14.19
510	0.01	31223	31.22
510	0.0047	66431	66.43
470	0.0033	102666	102.67

Do not use RC filters in conjunction with additional DBK expansion accessories.



An Example of Customer-Installed Capacitors and Filters for RC Networks

In this example Channels 0 and 8 are shown as *Single-Ended*. Channel 1 is *Differential*, i.e., using 1H and 1L (channel High and Low).

The following three notes pertain to the above figure.

Note 1: The 3 horizontal capacitors [as oriented in the illustration] are optional filter capacitors.

Note 2: The vertical capacitor [as oriented in the illustration] is an optional isolation capacitor used for the reduction of *Differential* noise. Such capacitor placement is <u>not</u> used in *Single-Ended* applications.

Note 3: If installing filter resistors, carefully drill out the indicated centers with a 1/16 inch drill-bit. Otherwise the resistor will be short-circuited.

Prior to installing RC components, review the previous Warning and Caution statements, then read over the following information regarding resistors and capacitors.

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- **Do not use RC filters in conjunction with additional DBK expansion accessories.**
- **Prior to installing a resistor to the filter network you must drill a 1/16" hole through the center pinhole [beneath the board's silkscreen resistor symbol] as indicated in the preceding figure. Failure to do so will short-circuit the resistor.**
- **Do not drill holes on the board for channels, unless those channels are to receive a filter network (see preceding statement).**
- **Resistors should be ¼ watt, film-type with up to 5% tolerance. Do not use wire-wound resistor types.**
- **A resistor value of 510 Ω is recommended. Do not exceed 510 Ω.**
- **Capacitors used are to be of the film dielectric type (e.g., polycarbonate or NPO ceramic), above 0.001 µF.**
- **RECOMMENDED: For reduction of both *Common Mode Noise* and *Differential Mode Noise*, use one capacitor between Channel High and AGND; and use a second capacitor between Channel Low and AGND.**
- **For reduction of *Differential Noise* [when no reduction of *Common Mode Noise* is needed] position a capacitor across the respective Channel High and Channel Low.**
- **When in Differential Mode, using capacitors between Channel High, Channel Low, and AGND may cause a slight degradation of *wideband Common Mode rejection*.**
- **When making a RC filter network, always install a wire jumper between the relevant FILT CAP LO and AGND. FILT CAP LO terminals are located on TB9 and TB10.**

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Specifications for DBK215

Operating Environment:

Temperature: -30°C to 70°C
Relative Humidity: 95% RH, non-condensing

Connectors:

P5: 68-Pin SCSI
Screw Terminals: 14 banks of 10-connector blocks
Wire Size: 12 TO 28 AWG

Dimensions:

285 mm W x 220 mm D x 45 mm H (11" x 8.5" x 2.7")

Weight:

1.36 kg (3 lbs)

Cables and Accessories:

Item Description	Part Number
Rack Mount Kit, p/n	RackDBK4
68-conductor expansion cables; mate with P5 (SCSI, 68-pin) connectors:	
3 ft., non-shielded	CA-G55
3 ft., shielded	CA-G56
6 ft., shielded	CA-G56-6
Accessory Wire Kit Includes jumper wires and a screwdriver.	1139-0800

Specifications subject to change without notice.

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An Important Note Regarding Hardware Analog Level Trigger and Comparator Change State

Issue:

When the starting out analog input voltage is near the trigger level, and you are performing a rising [or falling] hardware analog level trigger, it is possible that the analog level comparator will have already tripped, i.e., to have tripped before the sweep was enabled. If this is the case, the circuit will wait for the comparator to change state. However, since the comparator has already changed state, the circuit will not see the transition.

Solution:

(1) Set the analog level trigger to the desired threshold.

(2) Apply an analog input signal that is *more than* 2.5% of the full-scale range *away from the desired threshold*. This ensures that the comparator is in the proper state at the beginning of the acquisition.

(3) Bring the analog input signal toward the desired threshold. When the input signal is at the threshold (± some tolerance) the sweep will be triggered.

(4) Before re-arming the trigger, again move the analog input signal to a level that is more than 2.5% of the full-scale range *away from* the desired threshold.

Example:

- an engineer is using the ±2V full-scale range (gain = 5)
- he desires to trigger at +1V on the rising edge
- he sets the analog input voltage to an initial start-value which is less than +0.9V (1V – (2V * 2 * 2.5%)).

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Appendix C Signal Modes and System Noise

Signal Modes …… C-1
Connecting Thermocouples via PDQ30…… C-2
Shielding …… C-3
TC Common Mode …… C-3
Cold Junction Compensation Techniques …… C-4
System Noise …… C-5
Averaging …… C-5
Analog Filtering …… C-5
Input and Source Impedance …… C-5
Crosstalk …… C-5
Floating Differential Inputs …… C-6
Oversampling and Line Cycle Rejection …… C-6

Signal Modes

DaqBoard/3000 Series boards can make use of single-ended mode, or differential modes. Mode selection is made in software.

Single-ended mode refers to a mode, or circuit set-up, in which a voltage is measured between one signal line and common ground voltage (Analog Common, or A_{COM}). The advantage of a single-ended *non-differential* mode [over differential mode] is that it provides for a higher channel count, for example: 16 channels instead of 8.

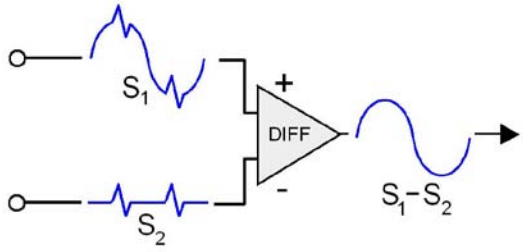


In DaqBoard/3000 Series applications, thermocouples should never be connected *single-ended*. Doing so can result in noise and false readings.

Differential mode refers to a mode, or circuit set-up, in which a voltage is measured between two signal lines. The measured differential voltage is used for a single channel. An advantage of using differential inputs is that they reduce signal errors and the induction of noise resulting from ground current. The following illustration is an example of how noise is reduced, or canceled-out, when using the differential mode.

In the schematic, voltage signal S_2 is subtracted from signal S_1, resulting in the output signal shown. Noise spikes with *the same polarity, phase, and magnitude in each input signal* cancel out—resulting in a clean differential signal (S_1 - S_2).

In the schematic, signals S_1 and S_2 are shown in-phase; however, even if these signals were out of phase, the noise in each (indicated by jagged lines) would still have the same magnitude, phase, and polarity. For that reason, they would still cancel out.



Noise Reduction in Differential Mode



Differential signal hookups do not provide isolation or any kind of circuit protection.

Resolution: An analog-to-digital converter (ADC) converts an analog voltage to a digital number. The digital number represents the input voltage in discrete steps with finite resolution. ADC resolution is determined by the number of bits that represent the digital number. An *n*-bit ADC has a resolution of 1 part in 2^n. Thus, 12-bit and 16-bit resolutions are as follows:

- 12-bit resolution: 1 part in 4096 (2^{12}), corresponding to 2.44 mV in a 10 V range.
- 16-bit resolution: 1 part in 65,536 (2^{16}), corresponding to 0.153 mV in a 10 V range.

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Connecting Thermocouples via PDQ30

DaqBoard/3000 Series boards can use *single-ended* or *differential modes to* measure voltage input; or use *differential mode* to measure temperature (if a PDQ30 is used). You can, of course, mix signal types, for example have some channels connected to thermocouples and others connected to voltage signals.



In PDQ30 applications, thermocouples must be connected *differentially*. Failure to do so will result in false readings.

PDQ30 modules do not have open thermocouple detection.

Differential connection is made as follows:

(a) the red TC wire connects to the channel's Low (L) connector.
(b) the other color TC wire connects to the channel's High (H) connector.

Thermocouple wire is standardized, color-coded, and polarized, as noted in the following table.

Thermocouple Standards				
T/C Type	(+) Lead to Channel High		(-) Lead to Channel Low	
J	White		Red	
K	Yellow		Red	
T	Blue		Red	
E	Violet		Red	
N28	Orange		Red	
N14	Orange		Red	
S	Black		Red	
R	Black		Red	
B	Gray		Red	

Thermocouples output very small voltages and long thermocouple leads can pickup a large amount of noise. If desired, noise reduction can be achieved through the use of shielded thermocouples and/or averaging.



You can minimize the effect of noise by employing one or more of the following practices. Using all three is best.

(1) Use shielded thermocouples *(see Shielding, page C-3)*

(2) Average readings *(see Averaging, page C-4)*

(3) Route thermocouple wires away from others. Wires adjacent or close to TC wires may introduce noise into the TC wires. For example, you should never route TC wires in a conduit that is being used for mains or motor drive power. Such practices could introduce a great deal of signal noise.

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Shielding

Using shielded TC wire with the shield connected to analog common will result in further noise reduction. You can connect the shield of a shielded thermocouple to one of the analog commons. When this connection is made the shield at the other end of the thermocouple is to be left unconnected. Refer to Chapter 2 for connection options and pinouts.

If a thermocouple shield is connected to the PDQ30, leave the shield unconnected at the other end of the thermocouple. Connecting the shield to common at both ends will result in a ground loop.

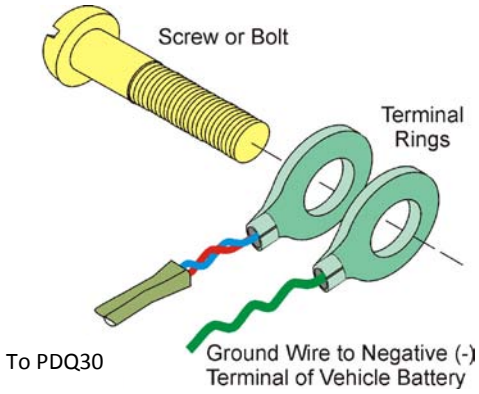
TC Common Mode

The maximum common-mode voltage for a PDQ30 is ±10 volts. Common-mode voltage is the DC or AC voltage signal that is applied equally to both sides of a differential input. Since thermocouples are measured using the 100 mV range, their maximum common mode voltage is ±6.0 volts.

If a thermocouple is connected directly to an engine component in a motor vehicle, at a potential that is over the maximum common-mode voltage, then very noisy or incorrect readings will be seen. Thermocouple connections that are made directly to an alternator or engine block may also result in high noise. Two methods of reducing noise are:

(a) Run a ground line from the screw (or bolt), as indicated in the first figure.

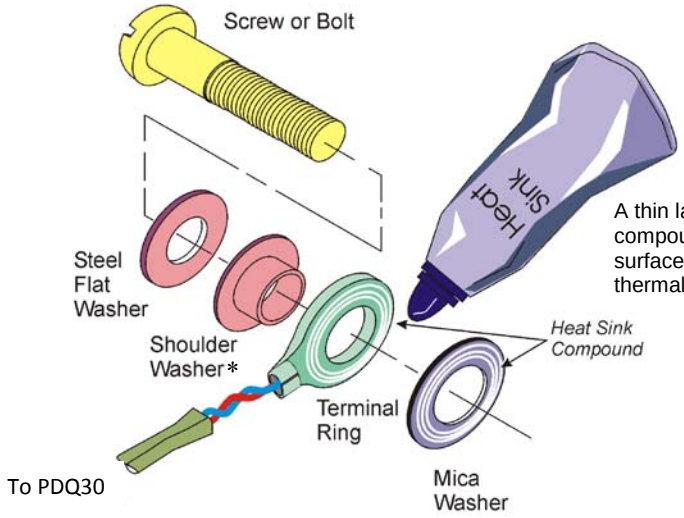
(b) Isolate the thermocouple leads with a set of washers, one of which is electrically insulating (such as mica), as indicated in the second figure.



Running a Ground Wire to the Battery's Negative Terminal

The length of the insulating shoulder washer's hub must not exceed the combined thickness of the terminal ring and mica washer.

* The insulating shoulder washer is non-metallic. It is made of insulating material, such as plastic.



A thin layer of heat-sink compound on the indicated surfaces will improve thermal conductivity.

Using a Washer Set and Heat Sink to Isolate the Thermocouple

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Cold Junction Compensation Techniques (PDQ30)

The PDQ30 can measure up to 24 channels of temperature. The units employ thermistors to measure the junction temperature (at the terminal block) for each thermocouple connection. These thermistors are inside the unit, just behind the mating terminal block connector on the internal circuit board. The actual junction is outside the unit and therefore there is some amount of error in the thermistor's ability to measure the actual junction temperature.

Software compensates for the thermal error between the CJC thermistor temperature and the actual junction temperature at the terminal block. The units are profiled under controlled conditions (still air, 25C, 60 minute warm-up, lying on a flat surface) and the thermal error is measured on a per channel basis. This is done for the PDQ30. The per-channel CJC temperature offsets are then stored inside the unit in non-volatile memory, along with the calibration constants.



Tips for Making Accurate Temperature Measurements (using PDQ30)

- Use as much oversampling as possible (See *Oversampling and Line Cycle Rejection, page C-6*).
- Apply Line Cycle Noise Reduction (See *Oversampling and Line Cycle Rejection, page C-6*).
- Make sure the PDQ30 has been warmed up for at least 60 minutes, including thermocouple wires. This allows the unit to thermally stabilize so the CJC thermistors can accurately measure the junction at the terminal block.
- Make sure the PDQ30's surrounding environment is thermally stabilized and ideally around 20°C to 30°C. If the PDQ30's ambient temperature is changing due to a local heating or cooling source, then the TC junction temperature may be changing and the CJC thermistor will have a larger error.
- Use small diameter thermocouple wire that is "instrument grade." Small diameter thermocouple wire will have less effect on the thermocouple junction at the terminal block, as less heat will be transferred from the ambient environment to the junction.
- Make sure the PDQ30 is mounted on a flat surface.
- If the PDQ30 will have a sustained ambient operating environment outside of the 20°C to 30°C range, consider autozero mode as a way to reduce the effects of offset drift. Performing a Y=MX+B adjustment at a desired ambient temperature can also be done. Make sure the unit has stabilized for at least 60 minutes.
- Be careful to avoid loading down the digital outputs or DAC outputs too heavily (>1 mA). Heavy load-down will cause significant heat generation inside the unit and increase the CJC thermistor error.

System Noise

Laboratory and industrial environments often have multiple sources of electrical noise. An AC power line is a source of 50/60 Hz noise. Heavy equipment (air conditioners, elevators, pumps, etc.) can be a source of noise, particularly when turned on and off. Local radio stations are a source of high-frequency noise, and computers and other electronic equipment can create noise in a multitude of frequency ranges. Thus, an absolute noise-free environment for data acquisition is not realistic. Fortunately, noise-reduction techniques such as averaging, filtering, differential voltage measurement and shielding are available to reduce noise to an acceptable level.

Averaging

Certain acquisition programs apply *averaging* after several samples have been collected. Depending on the nature of the noise, averaging can reduce noise by the square root of the number of averaged samples. Although averaging can be effective, it suffers from several drawbacks. Noise in measurements only decreases as the square root of the number of measurements—reducing RMS noise significantly may require many samples. Thus, averaging is suited to low-speed applications that can provide many samples.

Note: Only random noise is reduced or eliminated by averaging. Averaging does not reduce or eliminate periodic signals. Refer to the section, *Oversampling and Line Cycle Rejection (page C-6)*.

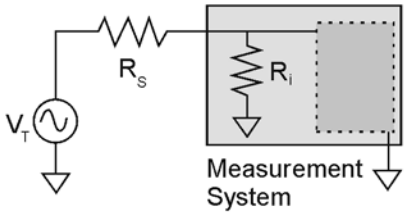
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Analog Filtering

A filter is an analog circuit element that attenuates an incoming signal according to its frequency. A low-pass filter attenuates frequencies above the cutoff frequency. Conversely, a high-pass filter attenuates frequencies below the cutoff. As frequency increases beyond the cutoff point, the attenuation of a single-pole, low-pass filter increases slowly. Multi-pole filters provide greater attenuation beyond the cutoff frequency but may introduce phase (time delay) problems that could affect some applications.

Input and Source Impedance

As illustrated in the following figure, input impedance (R_i) of a measurement system combines with the transducer's source impedance (R_s) forming a voltage divider. This divider distorts the voltage being read. The actual voltage read is represented by the equation: $\mathbf{V_{ADC} = V_T \times R_i / (R_s + R_i)}$



With input impedance (R_i) of 10 MΩ, which is a realistic value for many measurement systems, a low source impedance (R_s) of less than 100Ω usually presents no problem. Signals from sources with impedance greater than 100Ω should have appropriate signal conditioning.

Crosstalk

Crosstalk is a type of noise related to source impedance and capacitance, in which signals from one channel leak into an adjacent channel, resulting in interference or signal distortion. The impact of source impedance and stray capacitance can be estimated by using the following equation.

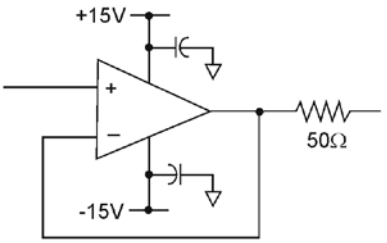
T = RC

Where **T** is the time constant, **R** is the source impedance, and **C** is the stray capacitance.

High source (transducer) impedance can be a problem in multiplexed A/D systems. When using more than 1 channel, the channel input signals are multiplexed into the A/D. The multiplexer samples one channel and then switches to the next channel. A high-impedance input interacts with the multiplexer's stray capacitance and causes crosstalk and inaccuracies in the A/D sample.

A solution to high source impedance in relation to multiplexers involves the use of buffers. The term buffer has several meanings; but in this case, *buffer* refers to an operational amplifier having high input impedance but very low output impedance. Placing such a buffer on each channel (between the transducer and the multiplexer) prevents the multiplexer's stray capacitance from combining with the high input impedance. This use of a buffer also stops transient signals from propagating backwards from the multiplexer to the transducer.

An example of a buffer is illustrated by the simple op-amp schematic at the right. The op-amp should have a bandwidth between 8MHz and 50MHz, even if the signal being measured is DC. This allows the op-amp to recover quickly from the DaqBoard's input multiplexer charge injection.



Note that characteristics of the op-amp (offset voltage, bias current, etc.) should be chosen with serious consideration for the signal being measured.

DaqBoard/3000 Series boards and PDQ30 units do not have a buffer for each analog input channel, due to power restrictions. Crosstalk is particularly troublesome when measuring high amplitude signals (+/-10V) along with low level signals (+/- 100mV.) All PDQ30 temperature measurements are low level signals that use the +/- 100mV range.

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If an acquisition's scan group includes both high level signals and low level signals, here are some tips on how to reduce the amount of crosstalk.

- Use as much oversampling as possible.
- Within the scan group, group high level signals together, group low level signals together
- Place a shorted channel in the scan group between the high level signals and the low level signals. The shorted channel should have the same gain as the last high level signal. This may allow for a faster scan rate with less oversampling.

Floating Differential Inputs

The DaqBook/3000 series and DaqBoard/3000 series products have fully differential input capability. However, they are *not intended for use as floating differential inputs*.

The low input of the differential pair is intended to remotely sense a signal that has a low resistance path to analog ground (variously referred to as ANALOG COMMON and AGND). Although a resistive path of up to 50kΩ may be acceptable, a lower resistive path is preferable.

The ideal ground connection is one that is made directly to analog common. But connections to mains-powered computer grounds have also functioned well.

Oversampling and Line Cycle Rejection

DaqBoard/3000 Series boards and PDQ30 units allow for oversampling and line cycle rejection. When the units are put into oversampling mode, noise is reduced and ambient 60Hz or 50Hz pick up can be rejected. When enabled, oversampling is adjustable from 2 to 16384. As the amount of oversampling increases, the noise present in the readings decreases. Line cycle rejection is just another mode of oversampling where 16384; 8192; 4096; etc. consecutive samples are averaged over one line cycle of 50Hz or 60Hz.

When oversampling is employed it is done for all analog channels in the scan group: voltage, temperature (PDQ30 only), CJC (PDQ30 only), and autozero. Digital channels are not oversampled. Increasing the amount of oversampling will drastically decrease the maximum allowable scan rate. During acquisitions, the system controller reads each of the channel entries in the scan list and measures each channel according to the desired channel number and gain. If oversampling is enabled, the acquisition engine reads each of the channel entries in the scan list and takes multiple consecutive measurements without changing the channel or gain. All consecutive 16-bit measurements are averaged and then returned to the software.

In the case of line cycle rejection, the acquisition engine adjusts the conversion time of the ADC slightly so that 16384; 8192; 4096; etc. samples will fit inside one line cycle of 50 Hz (20ms) or 60Hz (16.666ms.)

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Glossary

Acquisition — A collection of scans acquired at a specified rate as controlled by the sequencer.

Analog — A signal of varying voltage or current that communicates data.

Analog-to-Digital Converter (ADC) — A circuit or device that converts analog values into digital values, such as binary bits, for use in digital computer processing.

API — Application Program Interface. The interface program within the Daq system's driver that includes function calls specific to Daq hardware and can be used with user-written programs (several languages supported).

Bipolar — A range of analog signals with positive and negative values (e.g., -5 to +5 V); see *unipolar*.

Buffer — *Buffer* refers to a circuit or device that allows a signal to pass through it, while providing isolation, or another function, without altering the signal. *Buffer* usually refers to:

(a) A device or circuit that allows for the temporary storage of data during data transfers. Such storage can compensate for differences in data flow rates. In a FIFO (First In - First Out) buffer, the data that is stored first is also the first data to leave the buffer.

(b) A follower stage used to drive a number of gates without overloading the preceding stage.

(c) An amplifier which accepts high source impedance input and results in low source impedance output (effectively, an impedance buffer).

Buffer Amplifier — An amplifier used primarily to match two different impedance points, and isolate one stage from a succeeding stage in order to prevent an undesirable interaction between the two stages. (Also see, *Buffer*).

Channel — In reference to Daq devices, *channel* simply refers to a single *input*, or *output* entity.

In a broader sense, an *input channel* is a signal path between the transducer at the point of measurement and the data acquisition system. A channel can go through various stages (buffers, multiplexers, or signal conditioning amplifiers and filters). Input channels are periodically sampled for readings.

An *output channel* from a device can be digital or analog. Outputs can vary in a programmed way in response to an input channel signal.

Common mode — Common mode pertains to signals that are identical in amplitude and duration; also can be used in reference to signal components.

Common mode voltage — Common mode voltage refers to a voltage magnitude (referenced to a common point) that is shared by two or more signals. *Example*: referenced to common, Signal 1 is +5 VDC and Signal 2 is +6 VDC. The common mode voltage for the two signals is +5.5 VDC [(5 + 6)/2].

Crosstalk — An undesired transfer of signals between systems or system components. Crosstalk causes signal interference, more commonly referred to as *noise*.

Digital — A digital signal is one of discrete value, in contrast to a varying signal. Combinations of binary digits (0s and 1s) represent digital data.

Digital-to-Analog Converter (DAC) — A circuit or device that converts digital values (binary bits), into analog signals.

DIP switch — A DIP switch is a group of miniature switches in a small *Dual In-line Package* (DIP). Typically, users set these switches to configure their particular application.

Differential mode — The differential mode measures a voltage between 2 signal lines for a single channel. (Also see *single-ended mode*).

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Differential mode voltage	Differential mode voltage refers to a voltage difference between two signals that are referenced to a common point. Example: Signal 1 is +5 VDC referenced to common. Signal 2 is +6 VDC referenced to common. If the +5 VDC signal is used as the reference, the differential mode voltage is +1 VDC (+ 6 VDC - +5 VDC = +1 VDC). If the +6 VDC signal is used as the reference, the differential mode voltage is -1 VDC (+ 5 VDC - +6 VDC = -1 VDC).
ESD	Electrostatic discharge (ESD) is the transfer of an electrostatic charge between bodies having different electrostatic potentials. This transfer occurs during direct contact of the bodies, or when induced by an electrostatic field. ESD energy can damage an integrated circuit (IC).
Excitation	Some transducers [e.g. strain gages, thermistors, and resistance temperature detectors (RTDs)] require a known voltage or current. Typically, the variation of this signal through the transducer corresponds to the condition measured.
Gain	The degree to which an input signal is amplified (or attenuated) to allow greater accuracy and resolution; can be expressed as ×n or ±dB.
Isolation	The arrangement or operation of a circuit so that signals from another circuit or device do not affect the *isolated* circuit. In reference to Daq devices, *isolation* usually refers to a separation of the direct link between the signal source and the analog-to-digital converter (ADC). Isolation is necessary when measuring high common-mode voltage.
Linearization	Some transducers produce a voltage in linear proportion to the condition measured. Other transducers (e.g., thermocouples) have a nonlinear response. To convert nonlinear signals into accurate readings requires software to calibrate several points in the range used and then interpolate values between these points.
Multiplexer (MUX)	A device that collects signals from several inputs and outputs them on a single channel.
Range	For the purposes of calculating accuracy, range is equal to the full dynamic input voltage. For example, the full-scale range is 20V for the -10 to +10V range.
Sample (reading)	The value of a signal on a channel at an instant in time. When triggered, the ADC reads the channel and converts the sampled value into a 12- or 16-bit value.
Scan	A series of measurements across a pre-selected sequence of channels.
Sequencer	A programmable device that manages channels and channel-specific settings.
Simultaneous Sample-and-Hold	An operation that gathers samples from multiple channels at the same instant and holds these values until all are sequentially converted to digital values.
Single-ended mode	The single-ended mode measures a voltage between a signal line and a common reference that may be shared with other channels. (Also see *differential mode*).
Trigger	An event to start a scan or mark an instant during an acquisition. The event can be defined in various ways; e.g., a TTL signal, a specified voltage level in a monitored channel, a button manually or mechanically engaged, a software command, etc. Some applications may use pre- and post-triggers to gather data around an instant or based on signal counts.
TTL	Transistor-Transistor Logic (TTL) is a circuit in which a multiple-emitter transistor has replaced the multiple diode cluster (of the diode-transistor logic circuit); typically used to communicate logic signals at 5 V.
Unipolar	A range of analog signals that is always zero or positive (e.g., 0 to 10 V). Evaluating a signal in the right range (unipolar or bipolar) allows greater resolution by using the full-range of the corresponding digital value. See *bipolar.*

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