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PCI-DAS6034, PCI-DAS6035, and PCI-DAS6036

Specifications



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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog inputs

A/D converter	Successive approximation type, min 200 kS/s conversion rate.
Resolution	16 bits, 1-in-65536
Number of channels	16 single ended /8 differential, software selectable
Input ranges	±10 V, ±5 V, ±500 mV, ±50 mV, software selectable
A/D pacing	Internal counter – ASIC. Software selectable time base: ▪ Internal 40 MHz, 50 ppm stability ▪ External source via AUXIN<5:0>, Software selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software selectable option, burst rate = 5 µS.
A/D gate sources	External digital: A/D GATE
A/D gating modes	External digital: Programmable, active high or active low, level or edge
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.
ADC pacer out	Available at user connector: A/D PACER OUT
RAM buffer size	8 K samples
Data transfer	DMA
	Programmed I/O
DMA modes	Demand or non-demand using scatter gather.
Configuration memory (see Note 1)	Up to 8 K elements in the queue. Programmable channel, gain, and offset.
Streaming-to-disk rate	200 kS/s, system dependent

Note 1: Mixing high gains (±500 mV, ±50 mV) with low gains (±10 V, ±5 V) within the channel-gain queue is not supported.

Accuracy

200 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of factory calibration temperature. Calibrator test source high side tied to channel 0 high and low side tied to channel 0 low. Low-level ground is tied to channel 0 low at the user connector.

Table 1. Absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±10.2 LSB
±5 V	±10.9 LSB
±500 mV	±19.7 LSB
±50 mV	±40.6 LSB

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Table 2. Absolute accuracy components specifications - all values are (±)

Range	% of Reading	Offset (µV)	Averaged Noise + Quantization (µV)[1]	Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
±10 V	0.0239	531	180	0.001	3.10
±5 V	0.0262	274	85	0.001	1.67
±500 mV	0.0467	54	12.3	0.001	0.30
±50 mV	0.0685	21.2	6.54	0.001	0.062

[1] Averaged measurements assume averaging of 100 single-channel readings.

Each PCI-DAS6034, PCI-DAS6035, and PCI-DAS6036 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 1.

Table 3. Differential non-linearity specifications

All ranges	±0.5 LSB typ	±1.0 LSB max

System throughput

Condition	Calibration Coefficients	ADC Rate (max)
1. Single channel, single input range	Per specified range	200 kS/s
2. Multiple channel, single input range	Per specified range	200 kS/s
3. Single channel, multiple input ranges	Default to value for cbAInScan() range parameter	200 kS/s

Note 2: For conditions 1-2 above, specified accuracy is maintained at rated throughput. Condition 3 applies a calibration coefficient which corresponds to the range value selected in `cbAInScan()`. This coefficient remains unchanged throughout the scan. Increased settling times may occur during gain-switching operations.

Settling time

Settling time is defined as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at the specified rate. A –FS DC signal is presented to channel 1; a +FS DC signal is presented to channel 0.

Condition	Range	Accuracy	
		±0.0031% (±2.0 LSB)	±0.0062% (±4.0 LSB)
Same range to same range	±10 V	5 µS max	*
	±5 V	5 µS max	*
	±500 mV	5 µS typ	*
	±50 mV	*	5 µS typ

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Parametrics

Max working voltage (signal + common-mode)	±11 V
CMRR @ 60 Hz	±10 V range: 85 dB
	±5 V range: 85 dB
	±500 mV range: 93 dB
	±50 mV range: 93 dB
Small signal bandwidth, all ranges	*413 kHz*
Input coupling	*DC*
Input impedance	*100 GOhm in normal operation.*
	2 kOhm typ in powered off or overload condition.
Input bias current	*±200 pA*
Input offset current	*±100 pA*
Absolute maximum input voltage	*±25 V powered on, ±15 V powered off.* *Protected inputs:* ▪ *CH<15:0> IN* ▪ *AISENSE*
Crosstalk	Adjacent channels: -75 dB
	All other channels: -90 dB

Noise performance

Table 4 summarizes the noise performance for the PCI-DAS6036/6035/6034. Noise distribution is determined by gathering 50 K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel-sampling rate. This specification applies to both single-ended and differential modes of operation.

Table 4. Analog input noise performance specifications

Range	Typical Counts	LSBrms
±10 V	7	0.7
±5 V	7	0.7
±500 mV	11	1.1
±50 mV	45	5.6

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Analog outputs (PCI-DAS6036 & PCI-DAS6035 only)

	PCI-DAS6035	**PCI-DAS6036**
D/A converter type	Double-buffered, multiplying	Double-buffered, multiplying
Resolution	12-bits, 1-in-4096	16 bits, 1-in-65536
Number of channels	2 voltage output	2 voltage output
Voltage range	±10 V	±10 V
Monotonicity	*12-bits, guaranteed monotonic*	*16-bits, guaranteed monotonic*
DNL	*±1 LSB max*	*±1 LSB max*
Slew rate	10 V/µs min	15 V/µs min
Settling time (full scale step)	10 µs to ±0.5 LSB accuracy	5 µs to ±1.0 LSB accuracy
Noise	200 µVrms, DC to 1 MHz BW	110 uVrms, DC to 400 kHz BW
Glitch energy	*24 mV @ 2 µS duration, mid-scale.*	*10 mV @ 1 µS duration, mid-scale*
Current drive	±5 mA	±5 mA
Output short-circuit duration	*Indefinite @ 25 mA*	*Indefinite @ 25 mA*
Output coupling	*DC*	*DC*
Output impedance	0.1 ohms max	0.1 ohms max
Power up and reset	DACs cleared to 0 volts ±200 mV max	DACs cleared to 0 volts ±21 mV max

Table 5. Analog output absolute accuracy specifications

Product	**Range**	**Absolute Accuracy**
PCI-DAS6035	±10 V	±1.7 LSB
PCI-DAS6036	±10 V	±7.9 LSB

Table 6. Absolute Accuracy Components

Product	**Range**	**% of Reading**	**Offset (mV)**	**Temp Drift (%/DegC)**	**Absolute Accuracy at FS (mV)**
PCI-DAS6035	±10 V	±0.022	±5.93	±0.0005	±8.127
PCI-DAS6036	±10 V	±0.013	±1.10	±0.0005	±2.417

Each PCI-DAS6035 and PCI-DAS6036 is tested at the factory to assure the board's overall error does not exceed the absolute accuracy specification listed in Table 5.

Table 7. Relative accuracy specifications

Product	**Range**	**Relative Accuracy**	
PCI-DAS6035	±10 V	±0.3 LSB, typical	±0.5 LSB, max
PCI-DAS6036	±10 V	-	±2.0 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

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Analog output pacing and triggering

DAC pacing (software programmable)	Internal counter – ASIC. Selectable time base: ▪ Internal 40 MHz, 50 ppm stability. ▪ External source via AUXIN<5:0>, software selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate source (software programmable)	External digital: D/A START TRIGGER
	Software gated
DAC gating modes	External digital: Programmable, active high or active low, level or edge
DAC trigger sources	External digital: D/A START TRIGGER
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge.
DAC pacer out	Available at user connector: D/A PACER OUT
RAM buffer size	16 K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously, software Selectable.
DMA modes	Demand or non-demand using scatter gather.
Waveform generation throughput	10 kS/s max per channel, 2 channels simultaneous

Analog input / output calibration

Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	*DC Level: 10.000 V± 5 mv. Actual measured values stored in EEPROM.*
	Tempco: 5 ppm/°C max, 2 ppm/°C typical
	Long-term stability: 15 ppm, T = 1000 hrs, non-cumulative
Calibration interval	1 year

Digital input / output

Digital type	Discrete, 5V/TTL compatible
Number of I/O	8
Configuration	8 bits, independently programmable for input or output. All pins pulled up to +5 V via 47 K resistors (default). Positions available for pull-down to ground. Hardware selectable via solder gap.
Input high voltage	2.0 V min, 7.0 V absolute max
Input low voltage	0.8 V max, –0.5 V absolute min
Output high voltage (IOH = -32 mA)	3.80 V min, 4.20V typ
Output low voltage (IOL = 32 mA)	0.55 V max, 0.22 V typ
Data transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

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Interrupts

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9080
ADC interrupt sources (software programmable)	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE: Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL: Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE: Interrupt is generated after each conversion completes.
	DAQ_EOSCAN: Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ: Interrupt is generated after each interval delay during multi-channel scans.
DAC interrupt sources (software programmable)	DAC_ACTIVE: Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE: Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY: Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL: Interrupt is generated when the DAC high channel output is updated.

Counters

User counter type	82C54
Number of channels	2
Resolution	16-bits
Compatibility	5V/TTL
CTRn base clock source (software selectable)	Internal 10 MHz, internal 100 KHz, or external connector (CTRn CLK)
Internal 10 MHz clock source stability	50 ppm
Counter n gate	Available at connector (CTRn GATE)
Counter n output	Available at connector (CTRn OUT)
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*15 ns min*
Low pulse width (clock input)	*25 ns min*
Gate width high	*25 ns min*
Gate width low	*25 ns min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*

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Configurable AUXIN<5:0>, AUXOUT<2:0> external trigger/clocks

The PCI-DAS6036/6035/6034 provides nine user-configurable trigger/clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

AUXIN<5:0> sources (software selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer timebase
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer timebase
AUXOUT<2:0> sources (software selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan.
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK:	CTR1 clock source
	D/A UPDATE:	D/A update pulse
	CTR2 CLK:	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	D/A START TRIGGER:	DAC Start Trigger Out
Default selections:	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D PACER GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK
Compatibility	5V/TTL	
Edge-sensitive polarity	Rising/falling, software selectable	
Level-sensitive polarity	Active high/active low, software selectable	
Minimum input pulse width	37.5ns	

DAQ-Sync inter-board triggers/clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

DAQ-Sync Signals:	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

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Power consumption

+5 V	0.9 A typical, 1.1 A max. Does not include power consumed through the I/O connector.
+5 V available at I/O connector	1 A max, protected with a resettable fuse

Environmental

Operating temperature range	0 to 55 °C
Storage temperature range	-20 to 70 °C
Humidity	0 to 90% non-condensing

Mechanical

Card dimensions	PCI half card: 174.4 mm (L) x 100.6 mm (W) x 11.65 mm (H)

DAQ-Sync connector and pin out

Connector type	14-pin right-angle 100 mil box header
Compatible cable	MCC p/n: CDS-14-x, 14-pin ribbon cable. x = number of boards (2 - 5)

Pin	Signal Name
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

Main connector and pin out

Connector type	Shielded SCSI 100 D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2 or 3 meters
Compatible accessory products (with the C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P (PCI-DAS6036/6035 only) BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with the C100MMS-x cable)	SCB-100

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8-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN HI	52	n/c
3	CH0 IN LO	53	n/c
4	CH1 IN HI	54	n/c
5	CH1 IN LO	55	n/c
6	CH2 IN HI	56	n/c
7	CH2 IN LO	57	n/c
8	CH3 IN HI	58	n/c
9	CH3 IN LO	59	n/c
10	CH4 IN HI	60	n/c
11	CH4 IN LO	61	n/c
12	CH5 IN HI	62	n/c
13	CH5 IN LO	63	n/c
14	CH6 IN HI	64	n/c
15	CH6 IN LO	65	n/c
16	CH7 IN HI	66	n/c
17	CH7 IN LO	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND*	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = n/c on PCI-DAS6034

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16-channel single-ended mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN	52	n/c
3	CH8 IN	53	n/c
4	CH1 IN	54	n/c
5	CH9 IN	55	n/c
6	CH2 IN	56	n/c
7	CH10 IN	57	n/c
8	CH3 IN	58	n/c
9	CH11 IN	59	n/c
10	CH4 IN	60	n/c
11	CH12 IN	61	n/c
12	CH5 IN	62	n/c
13	CH13 IN	63	n/c
14	CH6 IN	64	n/c
15	CH14 IN	65	n/c
16	CH7 IN	66	n/c
17	CH15 IN	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND*	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = n/c on PCI-DAS6034

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