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PCI-DAS64/M1/16

Specifications



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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	Sub-ranging sampling ADC
Resolution	16 bits
Number of channels	32 differential or 64 single-ended, software selectable
Input ranges (software programmable)	±5 V, ±2.5 V, ±1.25 V, ±0.625 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
Polarity	Unipolar/bipolar, software selectable
A/D pacing (software programmable)	▪ Internal counter – ASIC ▪ External source (A/D external pacer). The total number of sample clocks must be at least 5 greater than the total number of samples desired. This is required to accommodate the pipelined architecture of the ADC. ▪ Software polled
Burst mode	Software selectable option. Valid for a fixed input range only. Burst rate = 1 µS.
A/D gate sources	▪ External digital (A/D pacer gate) ▪ External analog (analog trigger in)
A/D gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window. Trigger levels set by DAC0 and/or DAC1.
A/D trigger sources	▪ External digital (A/D start trigger in and A/D stop trigger in) ▪ External analog (Analog Trigger In)
A/D triggering modes	▪ External digital: Software-configurable for rising or falling edge. ▪ External analog: Software-configurable for positive or negative slope. Trigger levels set by DAC0 and/or DAC1. ▪ Pre-/post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. Compatible with both digital and analog trigger options.
Data transfer	▪ From 8 k RAM buffer via DMA (demand or non-demand mode) using scatter gather. ▪ Programmed I/O
Configuration memory	*8 K words*
Channel/gain queue	Up to 8 K elements. Programmable channel, gain, and offset.
A/D conversion time	*1 µS*
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.

System throughput

Table 2. System throughput specifications

Condition	Calibration coefficients	Max ADC rate
1. Single channel, single input range.	Per specified range	1.0 MS/s
2. Multiple-channel, single-input range: ±5 V, ±2.5 V, ±1.25 V, 0 to 5 V, 0 to 2.5 V	Per specified range	1.0 MS/s
3. Multiple channel, single input range: ±0.625 V, 0 to 1.25 V	Per specified range	750 kS/s
4. Single channel, multiple input ranges.	Default to value for `cbAInScan()` range	500 kS/s
5. Multiple channels, multiple ranges. All samples in unipolar *or* bipolar bode.	Default to value for `cbAInScan()` range	500 kS/s
6. Multiple channels, multiple ranges. All samples in unipolar *and/or* bipolar bode.	Default to value for `cbAInScan()` range	500 kS/s
7. Multiple-channel, switching unipolar/bipolar mode, single-input range.	Default to value for `cbAInScan()` range	750 kS/s

Note 1: For conditions 1-3, specified accuracy is maintained at rated throughput. Conditions 4-7 apply calibration coefficients which correspond to the range value selected in `cbAInScan()`. These coefficients remain unchanged throughout the scan. Errors of up to 25 counts may be incurred when switching gains while in bipolar or unipolar mode only (conditions 4 and 5). Errors of up to 500 counts may be incurred when mixing unipolar/bipolar modes (conditions 6 and 7).

Accuracy

A 100 kS/s sampling rate, single-channel operation and a 60-minute warm-up. Accuracies are listed for operational temperatures within ±2ºC of internal calibration temperature. Calibrator test source high side tied to channel 0 and low side tied to low-level ground at the user connector

Table 3. Analog input — absolute accuracy specifications

Range	Absolute accuracy
±5.000 V	±6.0 LSB
±2.500 V	±8.0 LSB
±1.250 V	±8.0 LSB
±0.625 V	±10.0 LSB
0 V to +5.000 V	±8.0 LSB
0 V to +2.500 V	±11.0 LSB
0 V to +1.250 V	±13.0 LSB

Table 4. Analog input — typical accuracy specifications

Range	Typical accuracy
±5.000 V	±5.5 LSB
±2.500 V	±7.5 LSB
±1.250 V	±7.5 LSB
±0.625 V	±9.5 LSB
0 V to +5.000 V	±7.5 LSB
0 V to +2.500 V	±10.5 LSB
0 V to +1.250 V	±12.5 LSB

Each PCI-DAS64/M1/16 is tested at the factory to assure the board's overall error does not exceed accuracy limits shown in Table 3.

Typical accuracy is derived directly from the various component typical errors. The information in Table 4 assumes that each of the errors contributes in the same direction.

Table 5. Analog input — accuracy components specifications

Range	Gain error	Offset error	DLE	ILE
±5.000 V	±3.0 max, ±2.0 typ	±3.0 max, ±2.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±2.500 V	±3.0 max, ±2.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±1.250 V	±3.0 max, ±2.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±0.625 V	±5.0 max, ±4.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to + 5.000 V	±4.0 max, ±3.0 typ	±4.0 max, ±3.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to + 2.500 V	±6.0 max, ±5.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to + 1.250 V	±6.0 max, ±5.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ

As shown in Table 5, total board error is a combination of *gain*, *offset*, *differential linearity error* (DLE), and *integral linearity error* (ILE). The theoretical worst-case error of the board can be calculated by summing these component errors. Worst-case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full-scale 100 Hz triangle wave is input on channel 1, and channel 0 is tied to analog ground at the 100-pin user connector. Table 6 summarizes the influence of channel 1 on channel 0 with the effects of noise removed. The residue on channel 0 is described in LSBs.

Table 6. Crosstalk specifications

Range	Crosstalk (LSB $_{pk-pk}$)	Per channel rate (kS/s)	ADC rate (kS/s)
±5.000 V	15	500	1000
±2.500 V	15	500	1000
±1.250 V	20	500	1000
±0.625 V	8	375	750
0 V to +5.000 V	15	500	1000
0 V to +2.500 V	20	500	1000
0 V to +1.250 V	8	375	750

Table 7. Analog input drift specifications

Analog input full-scale gain drift	+0.3 LSB/°C typical
Analog input zero drift	+2.1 LSB/°C typical
Overall analog input drift	±2.4 LSB/°C typical
Common mode range	±5 V
CMRR @ 60Hz	-90 dB
Input leakage current	*2.3 nA*
Input impedance	*10 x 10*^{11} Ω
Absolute maximum input voltage	*±15 V*
Warm-up time	60 minutes

Noise performance

Table 8 summarizes the worst case noise performance for the PCI-DAS64/M1/16. Noise distribution is determined by gathering 50 K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel sampling rate. Specification applies to both single-ended and differential modes of operation.

Table 8. Noise performance specifications

Range	±2 counts	±1 count	MaxCounts	LSBrms (Note 2)
± 5.000 V	60%	40%	22	3.3
± 2.500 V	60%	40%	24	3.6
± 1.250 V	60%	40%	26	3.9
± 0.625 V	45%	30%	32	4.8
0 to +5.000 V	60%	40%	24	3.6
0 to +2.500 V	60%	40%	26	3.9
0 to +1.250 V	45%	30%	32	4.8

Note 2: RMS noise is defined as the peak-to-peak bin spread divided by 6.6.

Analog output

Table 9. Analog output specifications

Resolution	*16-bits*
Number of channels	*2*
Voltage range	±5 V
Monotonicity	*Guaranteed monotonic over temperature*
Analog output zero drift	±1.6 LSB/°C
Overall analog output drift	±4.0 LSB/°C
Slew rate	2.5 V/µs
Settling time	FS step to .0008%: 6µs max, all ranges
Current drive	±15 mA
Output short-circuit duration	*Indefinite @25 mA*
Output coupling	*DC*
Output impedance	0.1 Ω
Power up and reset	DACs cleared to 0 V±75 mV max

Accuracy

Table 10. Analog output — absolute accuracy specifications

Range	Absolute accuracy
± 5 V	±16.0 LSB

Table 11 Analog output — accuracy components specifications

Range	Gain error (LSB)	Offset error (LSB)	DLE (LSB)	ILE (LSB)
±5.0 V	±10.0 max	±5.0 max	±1.0 max	±1.0 max

Each PCI-DAS64/M1/16 is tested at the factory to assure the board's overall error does not exceed the absolute accuracy limits listed in Table 10.

Analog output pacing and triggering

Table 12. Analog output pacing and triggering specifications

D/A pacing (software-programmable)	Internal counter – ASIC
	External source (D/A external pacer)
	Software paced
D/A gate sources (software-programmable)	External digital (external D/A trigger/pacer gate)
	External analog (analog trigger in)
D/A gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Software-configurable for above or below reference. Gating levels are set by DAC0 or DAC1.
D/A trigger sources	External digital (external D/A trigger/pacer gate)
	Software triggered
D/A triggering modes	External digital: Software-configurable for rising or falling edge.
Data transfer	From 16 k RAM buffer via DMA (demand or non-demand mode) using scatter gather.
	Programmed I/O
	100 kS/s max per channel

Digital input/output

Table 13. Digital I/O specifications

Digital type (main connector)	Output: 74LS175
	Input: 74LS244
Configuration	Four inputs, four outputs (DIN0 through DIN3; DOUT0 to DOUT3)
Output high voltage (IOH = -0.4 mA)	*2.7 V min*
Output low voltage (IOL = 8 mA)	*0.5 V max*
Input high voltage	*2.0 V min, 7 volts absolute max*
Input low voltage	*0.8 V max, –0.5 volts absolute min*
Digital type (digital I/O connector)	82C55
Number of I/O	24 (FIRSTPORTA Bit 0 through FIRSTPORTC Bit 7)
Configuration	2 banks of 8 and 2 banks of 4, or
	3 banks of 8 or
	2 banks of 8 with handshake
Input high voltage	*2.0 V min, 5.5 V absolute max*
Input low voltage	*0.8 V max, –0.5 V absolute min*
Output high voltage (IOH = -2.5 mA)	*3.0 V min*
Output low voltage (IOL = 2.5 mA)	*0.4 V max*
Power-up / reset state	Input mode (high impedance)
SSH output	TTL compatible output, HOLD is asserted from start of the conversion for Channel 0 through conversion of the last channel in the scan. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT (default) or D/A PACER OUT.
SSH polarity	HOLD high (default) or HOLD low, software selectable

Interrupts

Table 14. Interrupt specifications

Interrupts	PCI INTA# - Mapped to IRQ*n* via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC interrupt	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.
DAC interrupt sources (software-programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.
	DAC_RETRANSMIT:	Interrupt is generated when the end of a waveform sequence has occurred in retransmit mode.
External interrupt	Interrupt is generated via edge-sensitive transition on the External Interrupt pin. Rising/falling edge polarity software selectable.	

Counters

Table 15. Counter specifications

User counter type	82C54
Configuration	One down counter, 16-bits. Counters 2 and 3 not used.
Counter 1 source	External, from connector (CTR1 CLK)
Counter 1 gate	Available at connector (CTR1 GATE).
Counter 1 output	Available at connector (CTR1 OUT).
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*30 nS min*
Low pulse width (clock input)	*50 nS min*
Gate width high	*50 nS min*
Gate width low	*50 nS min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*

Pacer

Table 16. Pacer specifications

ADC pacer type	ASIC
Configuration	One down counter, 24 bits (1 scan interval, 1 sample interval)
ADC pacer source	40 MHz internal source
ADC pacer gate	Internally controlled by software/hardware trigger.
ADC pacer out	ADC pacer clock, available at user connector (A/D PACER OUT)
DAC pacer type	ASIC
Configuration	One down counter, 24 bits (1 scan interval, 1 sample interval)
DAC pacer source	40 MHz or 100 kHz internal source. Software-selectable.
DAC pacer gate	Internally controlled by software/hardware trigger.
DAC pacer out	DAC pacer clock. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT (default) or D/A PACER OUT.
Internal pacer crystal oscillator	40 MHz
Frequency accuracy	50 ppm

Power consumption

Table 17. Power specifications

+5 V	2.9 A typical, 3.3 A max
+12 V	10 mA max.

Environmental

Table 18. Environmental specifications

Operating temperature range	0 to 50 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

Mechanical

Table 19. Mechanical specifications

Card dimensions	315 mm (L) x 100.6 mm (W) x 16 mm (H)

Main connector and pin out

Table 20. Main connector and pinout specifications

Parameter	**Specification**
Connector type	Shielded SCSI 100-pin D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet.
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters.
Compatible accessory products using the C100HD50-x cable	CIO-MINI50 (two required) SCB-50
Compatible accessory products using the C100MMS-x cable	CIO-TERM100 SCB-100

Differential mode pin out

Table 21. 32-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	GND	51	GND
2	CTR1 OUT	52	EXTERNAL INTERRUPT
3	CTR1 CLK	53	A/D EXTERNAL PACER
4	CTR1 GATE	54	A/D STOP TRIGGER IN
5	DOUT3	55	A/D START TRIGGER IN
6	DOUT2	56	ANALOG TRIGGER IN
7	DOUT1	57	A/D PACER GATE
8	DOUT0	58	A/D PACER OUT
9	DIN3	59	SSH OUT / D/A PACER OUT
10	DIN2	60	EXTERNAL D/A TRIGGER/PACER GATE
11	DIN1	61	D/A EXTERNAL PACER
12	DIN0	62	PC +5 V
13	GND	63	D/A OUT 1
14	-12 V	64	D/A GND 1
15	GND	65	D/A OUT 0
16	+12 V	66	D/A GND 0
17	CH31 IN LO	67	CH31 IN HI
18	CH30 IN LO	68	CH30 IN HI
19	CH29 IN LO	69	CH29 IN HI
20	CH28 IN LO	70	CH28 IN HI
21	CH27 IN LO	71	CH27 IN HI
22	CH26 IN LO	72	CH26 IN HI
23	CH25 IN LO	73	CH25 IN HI
24	CH24 IN LO	74	CH24 IN HI
25	CH23 IN LO	75	CH23 IN HI
26	CH22 IN LO	76	CH22 IN HI
27	CH21 IN LO	77	CH21 IN HI
28	CH20 IN LO	78	CH20 IN HI
29	CH19 IN LO	79	CH19 IN HI
30	CH18 IN LO	80	CH18 IN HI
31	CH17 IN LO	81	CH17 IN HI
32	CH16 IN LO	82	CH16 IN HI
33	LLGND	83	LLGND
34	CH15 IN LO	84	CH15 IN HI
35	CH14 IN LO	85	CH14 IN HI
36	CH13 IN LO	86	CH13 IN HI
37	CH12 IN LO	87	CH12 IN HI
38	CH11 IN LO	88	CH11 IN HI
39	CH10 IN LO	89	CH10 IN HI
40	CH9 IN LO	90	CH9 IN HI
41	CH8 IN LO	91	CH8 IN HI
42	CH7 IN LO	92	CH7 IN HI
43	CH6 IN LO	93	CH6 IN HI
44	CH5 IN LO	94	CH5 IN HI
45	CH4 IN LO	95	CH4 IN HI
46	CH3 IN LO	96	CH3 IN HI
47	CH2 IN LO	97	CH2 IN HI
48	CH1 IN LO	98	CH1 IN HI
49	CH0 IN LO	99	CH0 IN HI
50	GND	100	LLGND

Single-ended mode pin out

Table 22. 64-channel single-ended mode pin out

Pin	Signal name	Pin	Signal name
1	GND	51	GND
2	CTR1 OUT	52	EXTERNAL INTERRUPT
3	CTR1 CLK	53	A/D EXTERNAL PACER
4	CTR1 GATE	54	A/D STOP TRIGGER IN
5	DOUT3	55	A/D START TRIGGER IN
6	DOUT2	56	ANALOG TRIGGER IN
7	DOUT1	57	A/D PACER GATE
8	DOUT0	58	A/D PACER OUT
9	DIN3	59	SSH OUT / D/A PACER OUT
10	DIN2	60	EXTERNAL D/A TRIGGER/PACER GATE
11	DIN1	61	D/A EXTERNAL PACER
12	DIN0	62	PC +5 V
13	GND	63	D/A OUT 1
14	-12 V	64	D/A GND 1
15	GND	65	D/A OUT 0
16	+12 V	66	D/A GND 0
17	CH63 IN	67	CH31 IN
18	CH62 IN	68	CH30 IN
19	CH61 IN	69	CH29 IN
20	CH60 IN	70	CH28 IN
21	CH59 IN	71	CH27 IN
22	CH58 IN	72	CH26 IN
23	CH57 IN	73	CH25 IN
24	CH56 IN	74	CH24 IN
25	CH55 IN	75	CH23 IN
26	CH54 IN	76	CH22 IN
27	CH53 IN	77	CH21 IN
28	CH52 IN	78	CH20 IN
29	CH51 IN	79	CH19 IN
30	CH50 IN	80	CH18 IN
31	CH49 IN	81	CH17 IN
32	CH48 IN	82	CH16 IN
33	LLGND	83	LLGND
34	CH47 IN	84	CH15 IN
35	CH46 IN	85	CH14 IN
36	CH45 IN	86	CH13 IN
37	CH44 IN	87	CH12 IN
38	CH43 IN	88	CH11 IN
39	CH42 IN	89	CH10 IN
40	CH41 IN	90	CH9 IN
41	CH40 IN	91	CH8 IN
42	CH39 IN	92	CH7 IN
43	CH38 IN	93	CH6 IN
44	CH37 IN	94	CH5 IN
45	CH36 IN	95	CH4 IN
46	CH35 IN	96	CH3 IN
47	CH34 IN	97	CH2 IN
48	CH33 IN	98	CH1 IN
49	CH32 IN	99	CH0 IN
50	GND	100	LLGND

Digital input/output connector and pin out

Table 23. Digital I/O connector specifications

Connector type	40-pin header
Connector compatibility	Translates to standard CIO-DIO24 type using BP40-37
Compatible cable	C40FF-2
Compatible accessory products	CIO-MINI40

Table 24. Digital I/O connector pin out

Pin	Signal name	Pin	Signal name
1	NC	2	PC +5 V
3	NC	4	DIG GND
5	FIRSTPORTB Bit 7	6	FIRSTPORTC Bit 7
7	FIRSTPORTB Bit 6	8	FIRSTPORTC Bit 6
9	FIRSTPORTB Bit 5	10	FIRSTPORTC Bit 5
11	FIRSTPORTB Bit 4	12	FIRSTPORTC Bit 4
13	FIRSTPORTB Bit 3	14	FIRSTPORTC Bit 3
15	FIRSTPORTB Bit 2	16	FIRSTPORTC Bit 2
17	FIRSTPORTB Bit 1	18	FIRSTPORTC Bit 1
19	FIRSTPORTB Bit 0	20	FIRSTPORTC Bit 0
21	DIG GND	22	FIRSTPORTA Bit 7
23	NC	24	FIRSTPORTA Bit 6
25	DIG GND	26	FIRSTPORTA Bit 5
27	NC	28	FIRSTPORTA Bit 4
29	DIG GND	30	FIRSTPORTA Bit 3
31	NC	32	FIRSTPORTA Bit 2
33	DIG GND	34	FIRSTPORTA Bit 1
35	PC +5 V	36	FIRSTPORTA Bit 0
37	DIG GND	38	NC
39	NC	40	NC

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