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PCI-DAS1602/12

Specifications



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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	ADS7800
Resolution	12 bits
Number of channels	16 single ended / 8 differential, software selectable
Input ranges (SW programmable)	Bipolar: ±10 V, ±5 V, ±2.5 V, ±1.25 V Unipolar: 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
Polarity	Unipolar/Bipolar, software selectable
A/D pacing (SW programmable)	Internal counter
	External source (A/D External Pacer)
	Software polled
Burst mode	Software selectable option, burst rate = 3 µS.
A/D trigger sources	External digital (A/D External Trigger)
	External analog (Analog Trigger In)
A/D triggering modes	External digital: Software configurable for: ▪ edge (triggered) ▪ level-activated (gated). Programmable polarity (rising/falling edge trigger, high/low gate).
	External analog: Software-configurable for: ▪ Positive or negative slope. ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window Trigger levels set by DAC0 and/or DAC1, 4.88 mV resolution.
	Unlimited pre- and post-trigger samples. Total # of samples must be > 512. Compatible with both digital and analog trigger options.
Data transfer	From 1024 sample FIFO via REPINSW
	Programmed I/O
A/D conversion time	*3.0 µS max*
Throughput	330 kS/s min
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.

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Accuracy

330 kHz sampling rate, single channel operation and a 60-minute warm-up. Accuracies are listed for operational temperatures within ±2 ºC of internal calibration temperature. Calibrator test source high side tied to Channel 0 High, and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2. Absolute accuracy specifications

Range	Absolute Accuracy (LSB)	Absolute Accuracy (mV)
±10 V	±2.5 LSB	±12.2
±5 V	±2.5 LSB	±6.10
±2.5 V	±2.5 LSB	±3.05
±1.25 V	±2.5 LSB	±1.53
0 V to +10 V	±2.5 LSB	±6.10
0 V to +5 V	±2.5 LSB	±3.05
0 V to +2.5 V	±2.5 LSB	±1.53
0 V to +1.25 V	±2.5 LSB	±0.76

Table 3. Accuracy components (errors in LSBs)

Range	Gain Error	Offset Error	DLE	ILE
±10 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max
±5 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max
±2.5 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max
±1.25 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max
0 to +10 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max
0 to +5 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max
0 to +2.5 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max
0 to +1.25 V	±1.0 max	±1.0 max	±0.75 max	±1.5 max

Each PCI-DAS1602/12 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2.

As shown in Table 3, total board error is a combination of gain, offset, differential linearity error (DLE) and integral linearity error (ILE). The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

Table 4. Analog input drift specifications

ADC full-scale gain drift	±6 ppm/°C
ADC zero drift	±6 ppm/°C
No missing codes guaranteed	12 bits
Common mode range	±10 V
CMRR @ 60 Hz	-70 dB typ
Input impedance	*10 MOhm min*
Input leakage current	*200 nA max*
Absolute maximum input voltage	*±35 V power on or off*
Warm-up time	60 minutes

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Noise performance

Table 5 summarizes the noise performance for the PCI-DAS1602/12. Noise distribution is determined by gathering 50 K samples @ 330 kHz with inputs tied to ground at the user connector.

Table 5. Noise performance specifications

Range	% within ±2 counts	% within ±1 count	MaxCounts	LSBrms*
±10 V	100%	100%	3	0.45
±5 V	100%	100%	3	0.45
±2.5 V	100%	100%	3	0.45
±1.25 V	100%	100%	5	0.76
0 to +10 V	100%	100%	3	0.45
0 to +5 V	100%	100%	3	0.45
0 to +2.5 V	100%	100%	3	0.45
0 to +1.25 V	100%	100%	5	0.76

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6.

Analog output

Table 6. Analog output specifications

A/D converter type	*AD7945BR multiplying type*
Resolution	*12-bits*
Number of channels	*2*
Voltage ranges	±10 V, ±5 V, 0 to 5 V, 0 to 10 V. Each independently programmable
Monotonicity	*Guaranteed monotonic over temperature*
Overall analog output drift	▪ ±0.02 LSB/°C
Slew rate	▪ ±10 V Range: 15 V/µs ▪ ±5 V Range: 10 V/µs ▪ 0 to 10 V Range: 7.5V/µs ▪ 0 to 5 V Range: 5 V/µs
Settling time	20 V step to 0.012%: 4 µs max
Current drive	±5 mA
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 ohms
Power up and reset	DACs cleared to 0 volts ±200 mV max

Accuracy

Table 7. Absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±3.0 LSB
±5 V	±3.0 LSB
0 V to +10 V	±3.0 LSB
0 V to +5 V	±3.0 LSB

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Table 8. Accuracy components (errors in LSBs)

Range	Gain Error (LSB)	Offset Error (LSB)	DLE (LSB)	ILE (LSB)
±10 V	±2.0 max	±0.1 max	±1.0 max	±1.0 max
±5 V	±2.0 max	±0.2 max	±1.0 max	±1.0 max
0 to +10 V	±2.0 max	±0.2 max	±1.0 max	±1.0 max
0 to +5 V	±2.0 max	±0.4 max	±1.0 max	±1.0 max

Each PCI-DAS1602/12 is tested at the factory to assure the board's overall error does not exceed ±3.0 LSB.

Total board error is a combination of gain, offset, integral linearity and differential linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction. Although an examination of the chart and a summation of the maximum theoretical errors shows that the board could theoretically exhibit a ±4.4 LSB error, our testing assures this error is never realized in a board that we ship.

Analog output pacing and triggering

Table 9. Analog output pacing and triggering specifications

D/A pacing (SW programmable)	Internal counter
	External source (D/A EXTERNAL PACER)
	Software paced
D/A trigger Modes	External digital (EXTERNAL D/A PACER GATE)
	Software triggered
Data transfer	From 1024 sample FIFO via REPOUTSW mode. Data interleaved for dual analog output mode.
	Programmed I/O
	Update DACs individually or simultaneously (SW selectable)
Throughput	250 KHz max per channel, 2 channels simultaneous

Digital input/output

Table 10. Digital input/output specifications

Digital type	82C55
Number of I/O	24 (FIRSTPORTA Bit 0 through FIRSTPORTC Bit 7)
Configuration	2 banks of 8 and 2 banks of 4 or
	3 banks of 8 or
	2 banks of 8 with handshake
Input high voltage	*2.0 V min, 5.5 V absolute max*
Input low voltage	*0.8 V max, –0.5 V absolute min*
Output high voltage (IOH = -2.5 mA)	*3.0 V min*
Output low voltage (IOL = 2.5 mA)	*0.4 V max*
Power-up / reset state	Input mode (high impedance)

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Interrupts

Table 11. Interrupt specifications

Interrupt	INTA# - mapped to IRQ*n* via PCI BIOS at boot-time
PCI Interrupt enable	Programmable
Interrupt sources	▪ External (rising TTL edge event) ▪ Residual sample counter ▪ A/D end of conversion ▪ A/D end of channel scan ▪ A/D FIFO-not-empty ▪ A/D FIFO-half-full ▪ D/A FIFO-not-empty ▪ D/A FIFO-half-full

Counters

Table 12. Counter specifications

Counter type	82C54	
Configuration	Two 82C54 devices. 3 down counters per 82C54, 16 bits each	
Counter 1 — ADC residual sample counter	Source:	ADC Clock
	Gate:	Programmable source
	Output:	End-of-Acquisition interrupt source
Counter 2 — ADC pacer lower divider	Source:	Internal 10 MHz
	Gate:	Tied to counter 3 gate, programmable source.
	Output:	Chained to counter 3 clock
Counter 3 — ADC pacer upper divider	Source:	Counter 2 output
	Gate:	Tied to counter 2 gate, programmable source
	Output:	ADC Pacer clock (if software selected), available at user connector
Counter 4 — Pre-trigger mode	Source:	ADC Clock
	Gate:	A/D External Trigger
	Output:	End-of-Acquisition interrupt source
Counter 4 — Non pre-trigger mode	Source:	User input at 100-pin connector (CLK 4) or internal 10 MHz (software selectable)
	Gate:	User input at 100-pin connector (GATE 4)
	Output:	Available at 100-pin connector (OUT 4)
Counter 5 — DAC pacer lower divider	Source:	Internal 10 MHz
	Gate:	Tied to counter 6 gate, programmable source.
	Output:	Chained to counter 6 clock
Counter 6 — DAC pacer upper divider	Source:	Counter 5 output
	Gate:	Tied to Counter 5 gate, programmable source.
	Output:	DAC Pacer clock, available at user connector (D/A INTERNAL PACER OUTPUT)
Gate width high	*50 ns min*	
Gate width low	*50 ns min*	
Input high	*2.0 volts min, 5.5 volts absolute max*	
Input low	*0.8 volts max, -0.5 volts absolute min*	
Output high	*3.0 volts min @ -2.5 mA*	
Output low	*0.4 volts max @ 2.5 mA*	
Crystal oscillator frequency	10 MHz	

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Power consumption

Table 13. Power consumption specifications

+5 V	1.2 A typical, 1.5 A max
+12 V	30 mA max

Environmental

Table 14. Environmental specifications

Operating temperature range	0 to 70°C
Storage temperature range	-40 to 100°C
Humidity	0 to 95% non-condensing

Mechanical

Table 15. Mechanical specifications

Card dimensions	PCI half card: 174.4 mm (L) x 100.6 mm (W) x 11.65 mm (H)

Main connector and pin out

Table 16. Main connector specifications

Connector type	100-pin high-density Robinson-Nugent.
Compatible cables	C100FF-x
Compatible accessory products	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50 SSR-RACK24 (DADP-5037 adaptor required) SSR-RACK08 (DADP-5037 with TN-MC78M05CT adaptor required) CIO-ERB24 (DADP-5037 adaptor required) CIO-ERB08 (DADP-5037 adaptor required) CIO-SERB08 (DADP-5037 adaptor required)

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Table 17. 8-channel differential mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH0 LO	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH1 LO	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH2 LO	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH3 LO	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH4 LO	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH5 LO	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH6 LO	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH7 LO	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	N/C
31	N/C	81	N/C
32	N/C	82	N/C
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	N/C
36	D/A OUT 0	86	N/C
37	D/A GND 1	87	N/C
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12 V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12 V
43	ANALOG TRIGGER IN	93	N/C
44	D/A EXTERNAL PACER IN	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	D/A INTERNAL PACER OUTPUT
47	N/C	97	EXTERNAL D/A PACER GATE
48	PC +5 V	98	N/C
49	SSH OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

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Table 18. 16-channel single-ended mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH8 HI	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH9 HI	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH10 HI	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH11 HI	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH12 HI	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH13 HI	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH14 HI	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH15 HI	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	N/C
31	N/C	81	N/C
32	N/C	82	N/C
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	N/C
36	D/A OUT 0	86	N/C
37	D/A GND 1	87	N/C
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12 V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12 V
43	ANALOG TRIGGER IN	93	N/C
44	D/A EXTERNAL PACER IN	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	D/A INTERNAL PACER OUTPUT
47	N/C	97	EXTERNAL D/A PACER GATE
48	PC +5 V	98	N/C
49	SSH OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

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