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PCIM-DDA06/16

ANALOG OUTPUT
&
DIGITAL I/O BOARD

User's Manual



Revision 3
October, 2000

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1.0 INTRODUCTION

The PCIM-DDA06/16 has six channels of analog output and 24 bits of digital input/output. Analog outputs are from AD660 DACs with each output buffered by an OP27. Digital I/O is done with an 82C55.

The analog outputs are controlled by writing a digital control word as two bytes to the DAC's control register. The control register is double-buffered so the DAC's output is not updated until both bytes (first low byte, then high byte) have been written to the DAC control when the simultaneous transfer jumper is in the default UPDATE position.

The analog outputs can also be set for simultaneous transfer by selecting the XFER position on the jumper marked UPDATE/XFER.

When a DAC pair is set for simultaneous transfer, writing new digital values to the DAC's control register does not cause an update of the DAC's voltage output. Update of the output occurs only after a READ of a board address (any address BADR3 + 0 through BADR3 + B).

In this way, the PCIM-DDA06/16 can be set to hold new values until all channels are loaded, then update all six channels simultaneously. This is a very useful feature for multi-axis motor control.

The PCIM-DDA06/16 digital I/O lines are a direct interface to an 82C55. The 82C55 is a CMOS chip with TTL level inputs and outputs. The 8255 can source or sink about 2.5 mA. This is enough to switch other TTL or similar inputs, but is inadequate to drive relays, LEDs or solid state relays without additional buffering.

The PCIM-DDA06/16 digital I/O is controlled by programming the 8255's mode register. There are three possible modes. The most commonly used mode is Mode 0, simple input and output.

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2.0 SOFTWARE INSTALLATION

Before you open your computer and install the board, install the *Insta*Cal installation, calibration and test utility included with your board. If you have ordered the Universal Library, *Insta*Cal may be installed from that disk set rather than the *Insta*Cal disk set. Refer to the *Extended Software Installation* manual for *Insta*Cal installation instructions.

If your PCI board requires manual configuration of switches or jumpers, detailed information regarding these settings can be found below. After configuring your board (if required), install it in your computer as detailed in the Hardware Installation section below and run *Insta*Cal. Once you have restarted your computer and run *Insta*Cal, use *Insta*Cal to verify your installation and switch settings.

3.0 HARDWARE INSTALLATION

The PCIM-DDA06/16 has six banks of five switches for setting the gain for each DAC, and one simultaneous transfer jumper. These switches may require setting before installing the board in your computer. This manual and the installation program (InstaCal) included with the board describes how these switches are set. In addition, each analog channel has gain and offset potentiometers for calibrating the channel if necessary.

The PCIM-DDA06/16 is configured at the factory with the following hardware settings:

Simultaneous Update Jumper Position	In the UPDATE position. Single channel update.
ANALOG OUTPUT RANGE	±5V

Leave the switches as they were set at the factory or refer to this manual to change the settings.

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3.1 SIMULTANEOUS TRANSFER JUMPER

The analog outputs can be configured so that new output data are held until all DACs have been loaded with their new digital data. Then, as a group, the data for each DAC is simultaneously transferred and the DAC voltage outputs are updated when any of the addresses BADR3 + 0 to BADR3 + B are read.

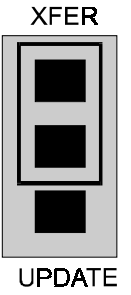


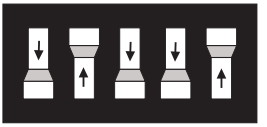
Figure 3-1. Simultaneous Transfer Jumper

Figure 3-1 shows the jumper block set for simultaneous transfer.

3.2 ANALOG OUTPUT RANGE SWITCH

The analog output voltage range of each channel can be set with a five-position DIP switch. The switches are located on the board directly above the DACs and are labeled S6 through S1.

Set the switches for an individual channel as shown in Figure 3-2.



Range	1	2	3	4	5
+/- 10V	D	U	D	U	D
+/- 5V	D	U	D	D	U (shown)
0 to 10V	U	D	U	U	D
0 to 5V	U	D	U	D	U

DAC OUTPUT RANGE SWITCH - ONE per DAC

Figure 3-2. DAC Output Range Switch

To set a channel to a particular range, read the switch positions as U (up) or D (down) from left to right in the row beside the range you desire.

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3.3 INSTALLING BOARD IN THE COMPUTER

1. Turn the power off.

2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

3. Locate an empty PCI expansion slot in your computer.

4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the card.

3.4 CABLING TO THE PCIM-DDA06/16

The PCIM-DDA06/16 connector is accessible through the PC/AT expansion bracket. The connector is a standard 37-pin male connector. A mating female connector or C37FF-# cable can be purchased from us.

Several cabling, screw termination, and signal conditioning options are available including:

DFCON-37	D-connector, D-shell and termination pins to construct your own cable.
C37FF-#	2-foot (and longer) ribbon cable with 37-pin D-type female connectors.
C37FFS-#	5-foot and 10-foot shielded round cable with molded ends housing 37-pin female connectors.
CIO-MINI37	Simple, 40-position 4”x4” screw terminal board.
SCB-37	A metal enclosure housing two CIO-MINI37 screw terminal boards
CIO-TERMINAL	Full featured 4”x16” screw terminal board with prototyping and interface circuitry.
SSR-RACK24	24-position Solid State Relay mounting and interface board.
ISO-RACK08	8-position Isolated Analog Module mounting and interface board.
ENC-MINI37	Enclosure for the MINI37.
ENC-17-3	Enclosure for larger external accessory boards.

3.5 SIGNAL CONNECTION

The analog outputs of the PCIM-DDA06/16 are two-wire hook-ups. A signal, labeled D/A # OUT on the connector diagram below, and a Low Level ground (LLGND). Always use analog ground as the ground reference for all analog hook-ups.

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Possible analog output ranges are:

Bipolar Ranges	±10V	±5V
and		
Unipolar Ranges	0 to 10V	0 to 5V

All the digital inputs and outputs are TTL level.

3.6 CONNECTOR DIAGRAM

The connector is a 37-pin D-type connector accessible from the rear of the PC through the expansion backplate (Figure 3-3). The connector accepts female 37-pin D-type connectors, such the C37FF-2, a two-foot cable with two female connectors.

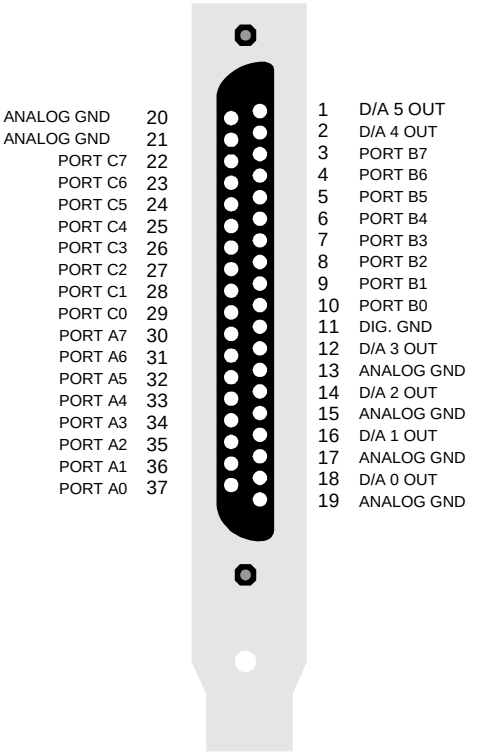


Figure 3-3. 37-Pin Connector (P2) Pin Out

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4.0 CALIBRATION

A calibration option is supplied with InstaCal. If desired, run CALIBRATE and check the calibration of the board. This step may not be necessary since the board was calibrated at the factory.

5.0 ARCHITECTURE & REGISTERS

5.1 BOARD ARCHITECTURE

The board consists of two functional sections: analog output and digital I/O (see Figure 5-1 below). The digital I/O section consists of a single 82C55, a 24-line digital I/O chip. The analog output section consists of six identical circuits, each consisting of a DAC, an OP27 output buffer, and a gain range control switch. Each of the analog outputs can be individually controlled,or all six can be simultaneously controlled.

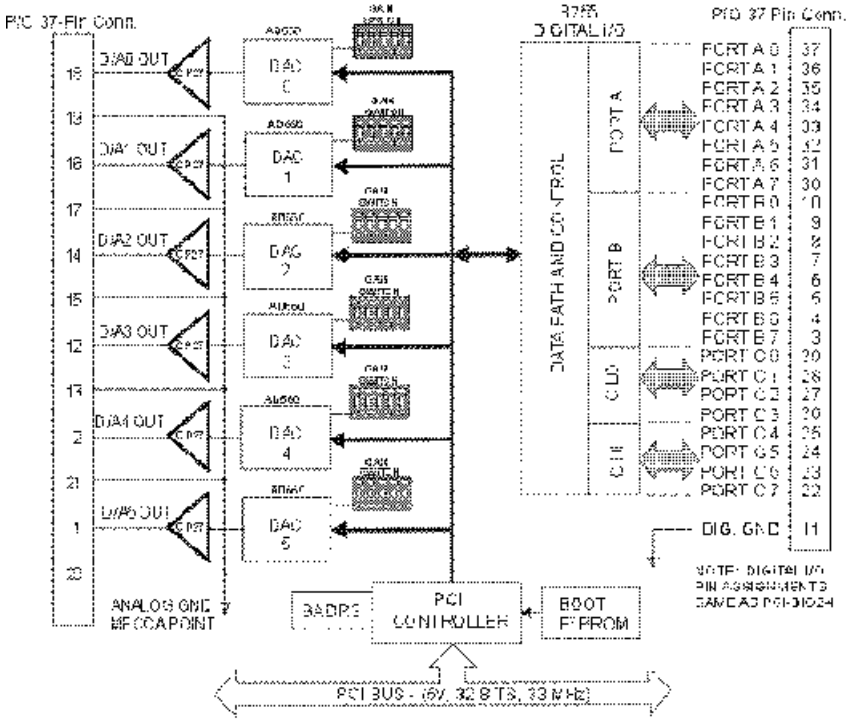


Figure 5-1. PCIM-DDA06/16 Block Diagram

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5.2 CONTROL & DATA REGISTERS

The PCIM-DDA06/16 has 12 analog output registers. There are two registers for each analog output channel, one for the lower eight bits and one for the upper eight bits. An additional four addresses are used for 82C55 data (3) and control (1) registers. The board uses 16 I/O addresses in all. The registers and their function are listed on Table 5-2, following.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

Register manipulation is best left to experienced programmers as most of the PCIM-DDA06/16 possible functions are implemented in the Universal Library.

The register descriptions all follow the format below:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

The numbers on the top row are the bit positions within the byte and the numbers and symbols in the bottom row name the function associated with each bit.

To write to or read from a register in decimal or hex, the following weights apply:

Table 5-1. Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. The registers and their function are listed on Table 5-2, following. Each register has eight bits which can either be a byte of data or eight separate read/write functions.

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Table 5-2. Board Registers

ADDRESS	WRITE FUNCTION	READ FUNCTION
BADR3 + 0	D/A 0 Least Significant Byte	Initiate simultaneous transfer
BADR3 + 1	D/A 0 Most Significant Byte	Initiate simultaneous transfer
BADR3 + 2	D/A 1 Least Significant Byte	Initiate simultaneous transfer
BADR3 + 3	D/A 1 Most Significant Byte	Initiate simultaneous transfer
BADR3 + 4	D/A 2 Least Significant Byte	Initiate simultaneous transfer
BADR3 + 5	D/A 2 Most Significant Byte	Initiate simultaneous transfer
BADR3 + 6	D/A 3 Least Significant Byte	Initiate simultaneous transfer
BADR3 + 7	D/A 3 Most Significant Byte	Initiate simultaneous transfer
BADR3 + 8	D/A 4 Least Significant Byte	Initiate simultaneous transfer
BADR3 + 9	D/A 4 Most Significant Byte	Initiate simultaneous transfer
BADR3 + 10	D/A 5 Least Significant Byte	Initiate simultaneous transfer
BADR3 + 11	D/A 5 Most Significant Byte	Initiate simultaneous transfer
BADR3 + 12	Port A Outputs	Port A Inputs
BADR3 + 13	Port B Outputs	Port B Inputs
BADR3 + 14	Port C Outputs	Port C Inputs
BADR3 + 15	Configure 8255	None

5.3 ANALOG OUTPUT REGISTERS

D/A 0 Least Significant 8 Bits
BADR3+ 0

7	6	5	4	3	2	1	0
D9	D10	D11	D12	D13	D14	D15	D16 (LSB)

D/A 0 Most Significant 8 Bits
BADR3 + 1

7	6	5	4	3	2	1	0
D1 (MSB)	D2	D3	D4	D5	D6	D7	D8

Writing data to the LSB loads that data into the D/A load register but does not update the D/A output. Writing data to the MSB both loads the upper eight bits of the 16-bit word and updates the output of the D/A (unless the simultaneous transfer jumper is set to XFER).

The function and bit layout of the remaining ten registers BADR3+2 to BADR3+11 (D/A 1 to D/A 5) is identical to that shown above.

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5.4 DIGITAL I/O REGISTERS

PORT A DATA
BADR3 + 12

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORT B DATA
BADR3 + 13

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B can be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes, individual bits are used.
Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BADR3 + 14

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Port C can be used as one eight-bit port of either input or output, or it can be split into two four-bit ports which can be either input or output. The notation for the upper four-bit port is CH3 to CH0, and for the lower, CL3 to CL0. Although it can be split, every read or write to port C carries eight bits of data so unwanted data must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS
In 8255 mode 0 configuration, ports configured for output hold the output data written to them. This output byte can be read back by reading the specific port configured as an output.

INPUT PORTS
In 8255 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed. Transitions are not latched.

For information on Mode 1 (strobed I/O) and Mode 2 (bi-directional strobed I/O), refer to the manufacturer's 8255 data sheet.

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8255 CONTROL REGISTER
BADR3 + 15

7	6	5	4	3	2	1	0
MS	M3	M2	A	CH	M1	B	CL
	Group A				Group B		

The 8255 can be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (Mode 1) or Bi-Directional Bus (Mode 2).

When the PC is powered up or RESET, the 8255 is reset. This places all 24 lines in Input Mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 8255 for other modes, the following control code byte must be assembled into one eight-bit byte.

MS = Mode Set. 1 = mode set active

Table 5-3. 82C55 Mode Control Coding

MS	**M3**	**M2**	**Group A Function**
1	0	0	Mode 0 Input / Output
1	0	1	Mode 1 Strobed Input / Output
1	1	X	Mode 2 Bi-Directional Bus

If all ports are to be used for either all inputs or for all outputs, the A, B, CH, and CL set the bits set as in Table 5-4 below.

Table 5-4. Coding for All inputs or All Outputs

A	B	CL	CH	I/O Function
1	1	1	1	All Inputs
0	0	0	0	All Outputs

NOTE:
M1 = 0 is mode 0 for group B. Input/Output
M1 = 1 is mode 1 for group B. Strobed Input/Output

The Ports A, B, C-High (CH) and C-Low (CL) can be independently programmed to be either inputs or outputs (Table 5-5).

The two groups of ports, group A and group B, can be independently programmed in one of several modes. Since the most commonly used mode is Mode 0, Input/Output, the codes for programming 8255 I/O ports in Mode 0 are listed in Table 5-5.

Refer to Table 5-5 for ports A, B, CH, and CL mode 0 configuration.

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Table 5-5. Mode 0 - Port I/O Configuration

A	CH	B	CL	D4	D3	D1	D0	HEX	DEC
OUT	OUT	OUT	OUT	0	0	0	0	80	128
OUT	OUT	OUT	IN	0	0	0	1	81	129
OUT	OUT	IN	OUT	0	0	1	0	82	130
OUT	OUT	IN	IN	0	0	1	1	83	131
OUT	IN	OUT	OUT	0	1	0	0	88	136
OUT	IN	OUT	IN	0	1	0	1	89	137
OUT	IN	IN	OUT	0	1	1	0	8A	138
OUT	IN	IN	IN	0	1	1	1	8B	139
IN	OUT	OUT	OUT	1	0	0	0	90	144
IN	OUT	OUT	IN	1	0	0	1	91	145
IN	OUT	IN	OUT	1	0	1	0	92	146
IN	OUT	IN	IN	1	0	1	1	93	147
IN	IN	OUT	OUT	1	1	0	0	98	152
IN	IN	OUT	IN	1	1	0	1	99	153
IN	IN	IN	OUT	1	1	1	0	9A	154
IN	IN	IN	IN	1	1	1	1	9B	155

Note: D7 is always 1;
D6, D5 and D2 are always 0.

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6.0 SPECIFICATIONS

Typical for 25°C unless otherwise specified.

Analog Output

D/A converter type	AD660BR
Resolution	16 bits
Number of channels	6
Voltage Ranges	±10, ±5, 0 to 10, 0 to 5. Ranges are switch-selectable
D/A pacing	Software paced
Throughput	System-dependent. Using the Universal Library programmed output function (cbAout) in a loop, in Visual Basic, a typical update rate of 150 kHz (+/- 70 ns jitter) can be expected. The rate was measured on a 500 MHz Pentium III-based PC.
Data transfer	Programmed I/O

Accuracy

Absolute Accuracy	±2.0 LSB max
Typical Accuracy	±1.0 LSB max

Accuracy Components

Gain Error	Adjustable by potentiometer to 0
Offset Error	Adjustable by potentiometer to 0
Integral Linearity Error	±1.0 LSB max, ±0.5 LSB typ
Differential Linearity	±1.0 LSB max, ±0.5 LSB typ

Each PCIM-DDA06/16 is tested at the factory to assure the board's overall error does not exceed ±2.0 LSB.
Total board error is a combination of Gain, Offset, Integral Linearity and Differential Linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Typical accuracy is derived directly from the various component typical errors. This typical, maximum error calculation for the PCIM-DDA06/16 yields ±1.0 LSB.

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Worst Case Analog Output Drift

Range	*Gain Drift (LSB/°C)*	*Offset Drift (LSB/°C)*	*Overall Drift (LSB/°C)*
±10.0V	1.0	0.3	1.3
±5.00V	4.0	0.3	4.3
0 to 10.0V	1.9	0.3	2.2
0 to 5.0V	6.0	0.3	6.3

Monotonicity	15 bits guaranteed over temperature
Slew rate	1.7V/µs minimum, 2.4V/µS typical.
Current Drive	±5 mA min
Output short-circuit duration	Indefinite
Power-on Reset Voltage	0V±15mV
Miscellaneous	Double-buffered output latches Update DACs individually or simultaneously (jumper-selectable)

Digital Input / Output

Digital Type	One 82C55
Number of I/O	24
Configuration:	• 2 banks of 8 and 2 banks of 4 or, • 3 banks of 8 or, • 2 banks of 8 with handshake
Output High	3.0 volts min @ –2.5 mA
Output Low	0.4 volts max @ 2.5 mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)

Power Consumption

+5V supply	965 mA typical, 1206 mA maximum

Environmental

Operating Temperature Range	0 to 70°C
Storage Temperature Range	–40 to 100°C
Humidity	0 to 95% non-condensing

Mechanical

Card dimensions	PCI half card: 174.4mm(L) x 100.6mm(W) x11.65mm(H)

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For Your Notes.

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EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

PCIM-DDA06/16	Analog Output and Digital I/O Card
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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