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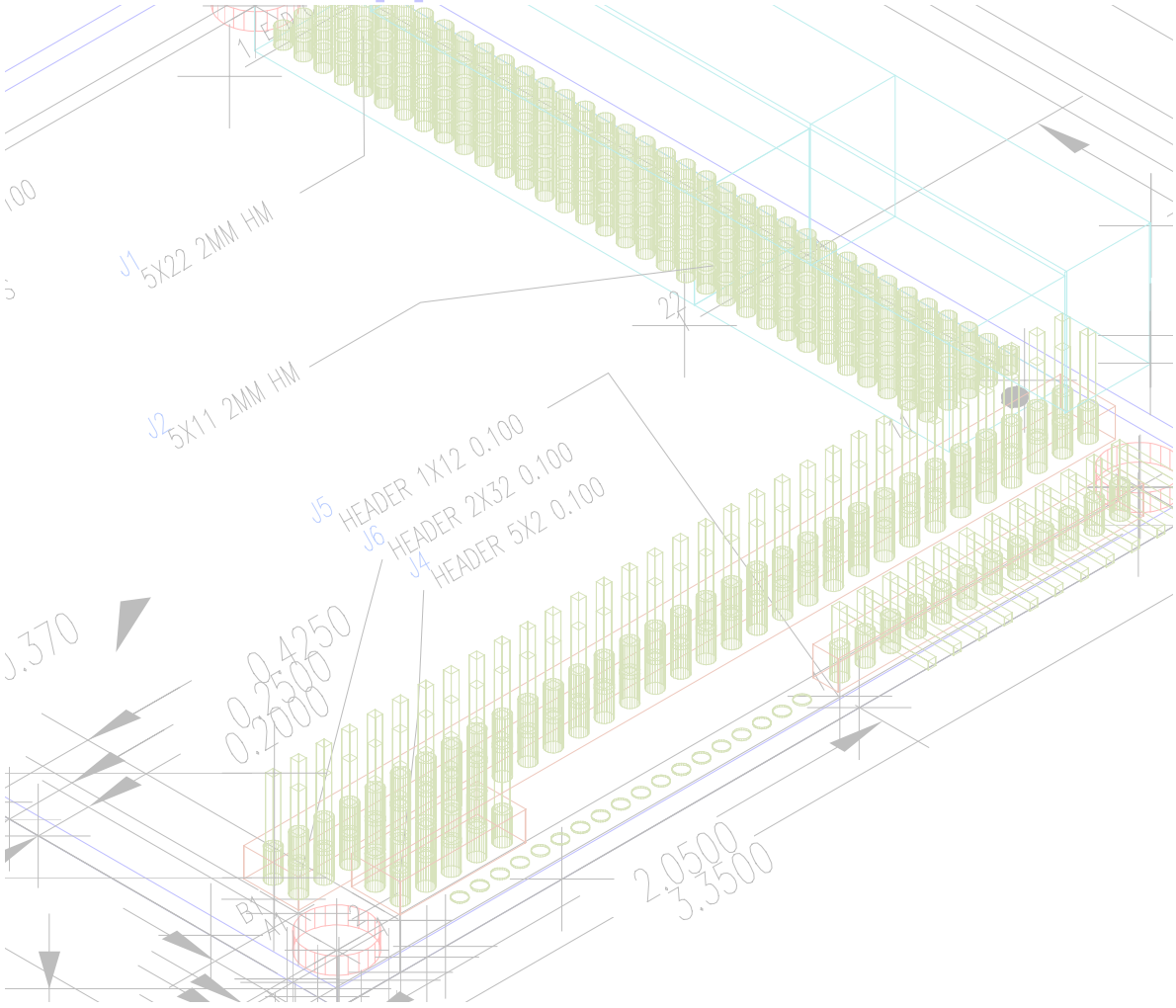
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megatel

PC/II+dx

Embedded Modular Computer for PC/104 Applications



Technical Reference Manual

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PC/II+dx

Embedded Modular Computer for PC/104 Applications

megatel 104Family



The ***PC/II+dx*** board is a rugged updated PC/104 compliant single board computer with all of the features that made us famous. This board is available with a broad set of options that can be mixed in any combination to maximize price and performance. On-board options include DX4 or DX5 processors, Super VGA & LCD output, Ethernet, 2 to 8 MB of soldered-down flash, 4 to 32 MB of soldered-down DRAM or 16 to 64 MB of soldered-down SDRAM, 32 to 64 MB of socketed SDRAM, IDE and SCSI. Many other options and base features are packed into this tiny board, all of which are combined into a small rugged package with low power consumption.

Features

- megatel PC/II+dx Board with Intel DX4 Write-Back Processor, or AMD DX4 Processor, or AMD DX5 Processor, and with National and ACC MICRO super I/O
- Supports 33 MHz FSB and choice of CPU Clocks including 66, 100 and 133 MHz
- 32 MB of DRAM, or 64 MB of SDRAM soldered down memory
- 3.3V SDRAM SODIMM memory socket option supports up to 64 MB of user option memory
- 16-Bit PC/104 Bus
- 165-Pin Mass I/O Interface uses H.M. 2mm IEC Connector System
- Crystal CS8900 Ethernet 10Base-T and AUI Controller & Filters with on-chip RAM buffers, and on-board Configuration EEPROM and LEDs, and Header
- ATA/IDE Hard drive interface
- AT compatible Keyboard and PS/2-Style mouse
- ADAPTEC Fast SCSI-2 Interface
- Chips & Tech 65550 CRT and Flat Panel Controller supports CRT and Flat Panels on a 3.3v or 5v interface
- Quad 16550 Serial Channels support full RS-232 communications
- Parallel Port ECP/EPP (1284 style)
- Floppy Interface, Watchdog, Advanced Y2K Real-Time Clock and all basic AT peripherals
- 256 KB Flash Bios (soldered) for Megatel Custom 100% AT compatible bios and option bios modules
- Flash Disk Disk-on-Chip Socket (up to 144+ MB)
- Linux, QNX, DOS, Windows

To Contact Us: Megatel Computer Corporation, 125 Wendell Ave, Weston, ON M9N 3K9, Canada
Tel:+1 416 245-2953 Fax:+1 416 245-6505 Toll Free: 1-888-SMALL-PC
Website: http://www.megatel.ca Email: sales@megatel.ca

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Electrical Specifications updated	20
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REVISION MT001807b 1999/08/24	
Release Version for PC/II+dx v1.32 board	
REVISION MT001810a 1999/06/19	
Preliminary Release Version for PC/II+dx v1.33 board	
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1 Introduction

Thank you for your interest in the Megatel PC/II+dx Cpu board, one of the PC/104 Family Cpu boards from Megatel Computer Corporation. In this document, you will find specifications for the functional, electrical, physical and operating characteristics of the PC/II+dx Cpu board. Please feel free to contact Megatel or one of its distributors or agents if you require more information.

While complete details of the functionality of the various peripheral and computer sections of this board can be best found in the datasheets referenced in this document, we have attempted to include the practical information to make this document as useful as possible to you.

We have included in this document all of the useful reference material, quick specifications, board settings and electrical specifications. The functional specifications begin in section 6, in topical order, including an introductory parts list and layout diagrams. We conclude this document with resource maps, connector pinouts and signals, peripheral attachment options (QTBs), ordering and servicing information. Physical board specifications are placed at the end of the document.

Your comments and suggestions on this document are always welcome, and may be sent to the megatel email address on page 3.

1.1 PC/II+dx Overview

PC/II+dx is a PC/104 compliant Single-Board Computer, adhering to form factor and electrical interface specifications, including bottom height requirements using basic features of the board. As a member of the "Megatel 104Family", this board is also interchangeable with other members of the family to provide the feature set and performance range you require. The Megatel 104Family of boards utilize the same physical and electrical interfaces and, in addition to PC/104 compatibility, the Megatel 104Family use the same connector placement and Mass I-O connector pinouts.

The PC/II+dx provides on-board 8-Bit or 16-Bit PC/104 bus connectors to allow direct drop-in compatibility with existing and new PC/104 designs. PC/II+dx contains an Intel or AMD 486DX4 100 MHz processor with integrated write-back L1 cache that operates at 100 MHz or 66 MHz, or an AMD 486DX5 133 MHz processor that operates at 133 MHz or 100 MHz. The local 32-Bit processor bus operates at 33 MHz. An Auctor ACCMicro 2089 Chipset provides an ISA Bus bridge, a DRAM memory controller, and a set of standard AT I/O peripherals. The board supports soldered-down main memory, either DRAM (4 MB to 32 MB) or SDRAM (16 MB to 64 MB) memory, and as an option, a 144-Pin SODIMM socket can be populated to support an additional 32 MB or 64 MB of SDRAM memory. An onboard CPLD supports the basic functionality of the board, including a full SDRAM memory controller for those configurations which are populated with SDRAM memory.

PC/II+dx also contains an on-board Flash Bios and a 100% AT compatible bios. The board contains soldered-down flash array with 2, 4 or 8 MB capacity. In addition, the board contains a socket for Disk-on-Chip to support 2 to 144 MB of M-Systems Flash Disk memory.

A rich complement of peripheral controllers and interfaces in included. Full video is provided by the Chips & Tech 65550 controller, supporting simultaneous CRT and a wide variety of 3.3v or 5v 24-Bit flat panels. SCSI is provided by the Adaptec AIC6360 controller, supporting a fast SCSI-2 bus interface. IDE, Keyboard, PS/2-style mouse, and Floppy are provided by the ACC Micro 2089 bus controller. Up to 4 Serial ports are provided by both the ACC Micro 2089 controller and a National 97338 Super I/O, and the board also contains RS232 transceivers for all standard RS232 signals.

All peripheral I/O, including Video CRT, 24-Bit Flat Panel, Keyboard, Mouse, SCSI, IDE, 4 Serial and Parallel ports are pulled to a Mass I/O Connector on the board. The Ethernet is provided separately on a standard 2X5 pin header. A 12-pin +5V power header is provided to supply the single +5V rail to the board

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and the +5V rail is either regulated to +3.3V on the board, or supplied by an optional 5-pin +3.3V power header.

Compared to conventional PC/104 Cpu boards, the PC/II+dx provides a very high density solution at a very low cost. The board is offered in its base configuration that consists of minimal memory, system controller and CPU. Any combination of peripherals can be populated at your option to meet your price/performance requirements.

2 Reference Documents

2.1 Datasheets

ACC Micro	ACC2089 Enhanced Super Chip, Databook, 1997
Adaptec	AIC-6360 Data Book PC-AT to SCSI Host Adapter,
AMD	Enhanced Am486®DX Microprocessor Family, 20736 Rev B Amendment/0, Mar 1997
AMP Incorporated	Catalog 65911, AMP Z-PACK™ 2mm HM Hard Metric Connector System, Sep 1997
Analog Devices	EMI/EMC Compliant ±15 kV ESD Protected RS-232 Line Drivers/Receivers (ADM211E), 1996
Chips and Technologies	65550 (HiQV32™) High Performance Multi-Media Flat Panel / CRT GUI Accelerator, Revision 1.5, Dec 1997 65550 HiQVideo Series Mode Support, 020089-004 (AN89.4), Revision 1.4, Feb 1996
Crystal Semiconductor Corp	CS8900 Highly Integrated Ethernet Controller, DS150PP2, Dec 95
Dallas Semiconductor	DS1706S 3.3V and 5.0V MicroMonitor, Feb 1998
Dallas Semiconductor	DS1685 Real Time Clock, Mar 1998
Intel	Embedded Write-Back Enhanced IntelDX4™ Processor, 272771-002, Dec 1997
Intel	Embedded Intel486™ Processor Family Developer's Manual, 273021
Intel	Embedded Intel486™ Processor Hardware Reference Manual, 273025
Intel	Intel486 Microprocessor Family Programmer's Reference Manual, 240486
Intel	INTEL® StrataFlash™ Memory Technology 32 and 64 Mbits (28F640J5), 290606-006, Jul 1998
Micron Technology, Inc.	Small-Outline SDRAM Module (MT4LSDT464H/864H), ZM13.p65, Apr 1998
National Semiconductor	PC97338 ACPI 1.0 and PC97 Compliant Super I/O, Apr 1998
Valor Electronics Inc.	ST7010 10Base-T Transformer Datasheet, Rev C
Valor Electronics Inc.	Ethernet AUI Transformers (ST7033) Datasheet, E/AUI105-01, Nov 1995

2.2 Reference Standards

PC/104 Consortium	PC/104 specification – Revision 2.3 – June 1996
Annabooks	AT Bus Design IEEE P996-Compatible, Edward Solari
IEEE	P996.1 Standard for Compact Embedded-PC Modules

2.3 Other References

Microsoft Press	The Programmer's PC Sourcebook, Thom Hogan

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3 Specification Summary

3.1 PC/II+dx Board Specifications

Board Form Factor: 3.775 x 3.550 inch, PC/104 compliant
Board Type: FR4
Basic Board Requires: Central Processing Unit
Minimum Memory – Soldered, 4 MB
Minimum Connectors – +5V Power

Architecture: PC/AT
Central Processing Unit: 486DX4 RISC-Core Processor – Intel or AMD
INTEL DX4:
- 66 MHz and 100 MHz core speed
- 33 MHz local bus speed
- 3.3V core and 5V tolerant I/O
- 32-Bit RISC technology core
- Pipelined execution
- Integrated Floating-Point unit
- Integrated Write-Back or Write-Through Cache

AMD DX4 and DX5:
- 100 MHz and 133 MHz core speed
- 33 MHz local bus speed
- 3.3V core and 5V tolerant I/O
- 105.6 million bytes/second burst bus
- 0.35-u CMOS-process technology
- Integrated Floating-Point unit
- Integrated Write-Back or Write-Through Cache

Cache Memory: 16K of integrated on-chip Cache Memory (L1)
Unified organization, uses modified MESI protocol
High performance write-back and write-through (user options)

DMA: (7) Channels, 128 MB addressing

Timer/Counters: AT-compatible (8254 type) timers
PC Speaker Output: Available on Mass I/O connector
Memory Bus: 32-Bit Data bus
Address Bus: 32-Bit Address bus

Power Monitoring: Dual 5% monitor – 5V rail and on-board 3.3V
Reset hold time – 130 ms minimum, 200 ms typical
Transient voltage immunity

Manual Reset: Available on Mass I/O Connector
Debounced, generates minimum of 130ms reset on Low to High
Initiated by pulling Manual Reset signal line Low, then High

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Memory: DRAM (soldered) or SDRAM (soldered and socketed) memory
Minimum System Memory 4 MB (soldered DRAM)
Maximum System Memory 128 MB (soldered and socketed SDRAM)
DRAM – EDO, 60 ns typical
SDRAM – 66 MHz (10 ns) typical

Memory Options – DRAM: 4, 8, 16 or 32 MB

Memory Options – SDRAM: 16, 32 or 64 MB; optional SODIMM 144-Pin socket

SODIMM Socket Provided: 144-Pin – compatible to BERG 61872-32844 (Right angle)
SODIMM Module Supported: One of following modules can be installed in SODIMM Socket:
32 MB user-supplied Module – compatible to
MICRON MT4LSDT464HG-662D1
64 MB user-supplied Module – compatible to
MICRON MT4LSDT864HG-662D1

Keyboard: AT-style Keyboard supported
Mouse: PS/2-style Mouse supported

Printer/Parallel Port: Bi-directional ECP/EPP-style Parallel Port supported

Serial/RS232 Ports: (1) to (4) 16C550-compatible Serial Ports
16-byte FIFOs
Full EIA-RS232E and CCITT V.28 Transceivers included
Output swing ±9V with all Transmitter Outputs
loaded with 3K ohms to Ground

Video CRT & Flat Panel: Intel (Chips and Technologies) HiQ 65550 GUI Accelerator
On-board 2 MB of 60 ns Video EDO DRAM, 512Kx32
Complete Analog CRT Video Interface
Complete 24-Bit Flat Panel Interface
Supports optional +5V or +3.3V interface to panels & CRTs
Monochrome (64 gray scale) or color
Hi-Res Passive STN, Active Matrix TFT/MIM LCD, EL
Simultaneous CRT / Flat Panel operation supported
Local bus interface – 32-Bit
64-bit Graphics Accelerator engine (BitBLT), H/W cursor
VGA register set compatibility
Supports panels from popular manufacturers
such as Sharp, Optrex, Toshiba, Hitachi, Fujitsu, Samsung, NEC, Sanyo and others
Intel (Chips and Technologies) drivers included

ATA/IDE Bus: (2) IDE hard drive devices supported

SCSI Bus: Adaptec AIC6360 Fast SCSI-2 Controller
(7) SCSI-2 devices
Adaptec SCSI BIOS included
Adaptec Drivers also supported
Bootable from either SCSI or IDE drive
Simultaneous use of both SCSI and IDE

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Flash Array: Soldered Flash EEPROM – 2, 4 or 8 MB
Coexistence support for both Flash Array and Flash Disk

Flash Disk: Socket for user-supplied solid-state disk (32 Pin DIP)
Supports M-System Disk-on-Chip®
(up to 144 MB or greater of flash disk memory module, user-populated)
Coexistence support for both Flash Array and Flash Disk

Ethernet: Crystal CS8900 High-performance 10Base-T and AUI controller option
IEEE 802.3 compliant MAC engine, full duplex operation
On-chip RAM buffers – for Transmit & Receive frames
AUI port for 10Base-2, 10Base-5 and 10Base-F
10Base-T filters included
10Base-T and AUI isolation transformers are included
10Base-T port has automatic polarity detection and correction
Auto negotiation function
LED for inbound/outbound frames to/from local controller included
LED for either valid 10Base-T link present, or other general function

Floppy Disk: Integrated Floppy Disk Controller
(2) 3.5" floppy disk drives supported
IBM System 34 double density format (MFM)
Sony EMCA format compatible
Standard transfer rates – 500 Kb/sec, 300 Kb/sec and 250 Kb/sec

Real-Time Clock, Alarm: Dallas-Certified DS1685 – Y2K Real-Time Clock Controller
Periodic Interrupt Generator – settable to period: 122 us to 500 ms
Alarm Interrupt Generator – settable to any time of day in 24 hour period
242-byte NVRAM included
12 or 24 hour format
Daylight savings time support
Unique 48-Bit Serial Number can be used for customer application

Watchdog: Dallas DS1706 Watchdog Timer/Monitor
Defaults at power-on time to software-disabled state
Hardware timer expiry issues system RESET
Software enable/disable/strobe is supported
Minimum strobe rate while enabled – 1 strobe/second
Hardware enable/disable jumper option

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Connectors:

Power Connectors –
(1) standard 1x12 right-angle header (+5V) - required
(1) standard 1x5 straight header (+3.3V) - optional
PC/104 Connectors –
(1) 2x32 and (1) 2x20 pin and socket header
stack-through and non stack-through
board stacking or other arrangements are customer specified
Ethernet Header –
(1) 2x10 right-angle header or customer specified
Mass I/O Connectors –
(1) 5x22 and (1) 5x11 IEC 2mm HM, or customer specified
total of 5x33 2mm grid
AMP Z-PACK 2mm HM Connector System
Type B22 and C
Support all variations –
straight and right-angle
male and female
Support top mounting (bottom by request)
Support 2mm headers on request (including board stacking headers)
IEC917 and IEC1076-4-101 compliant
All connectors except for the +5V Power header are optional

Sockets:

(1) 32-Pin DIP Socket for Flash Disk compatible to M-System MD2200

Peripheral I/O Signals:

Mass I/O Connector and Ethernet Header Signal Pins
Ethernet 10Base-T – 4
Ethernet AUI – 6
Ethernet LEDs – 2 (on-board dual LEDs)
Floppy Disk Bus – 15
IDE/ATA Bus – 28
Keyboard – 2
Mouse – 2
Parallel I/O – 17
PC/104 8-Bit Bus – 64
PC/104 16-bit Bus Extension – 40
Reset Switch – 1
SCSI – 18
Serial COM1 – 8
Serial COM2 – 8
Serial COM3 – 8
Serial COM4 – 8
Speaker Output – 1
Video Analog (CRT) – 5
Video Panel Interface (24-bit) – 32
Power & Ground

Supply Voltage:

Single supply at +5V 5%, or Dual supplies at +5V 5% and +3.3V 5%
When single supply, on-board regulator supplies +3.3V
On-board power monitor for both 5V and 3.3V rails is provided

Supply Power Rating:

Depends upon ordered options

Supply Regulation:

+5V and +3.3V Supplies require regulation to within 5%

+5V Max Rise Time:

(+3V to +5V) required within 100 ms

Storage Temperature:

-50C to +125C, battery excluded

Operating Temperature:

Commerical 0C to +70C standard
Industrial -20C to +85C available on request

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	Industrial -40C to +85C available on request
Operating Software:	DOS, Windows, Windows 95, Windows NT4.0
Application Software:	x86 compatible
Bios Software:	256 KB Flash EEPROM for Bios Bios write protection (hardware) Intel (Chips & Technologies) 65550 VGA Driver BIOS included AT compatible BIOS and Architecture

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3.2 PC/II+dx Board Block Diagram

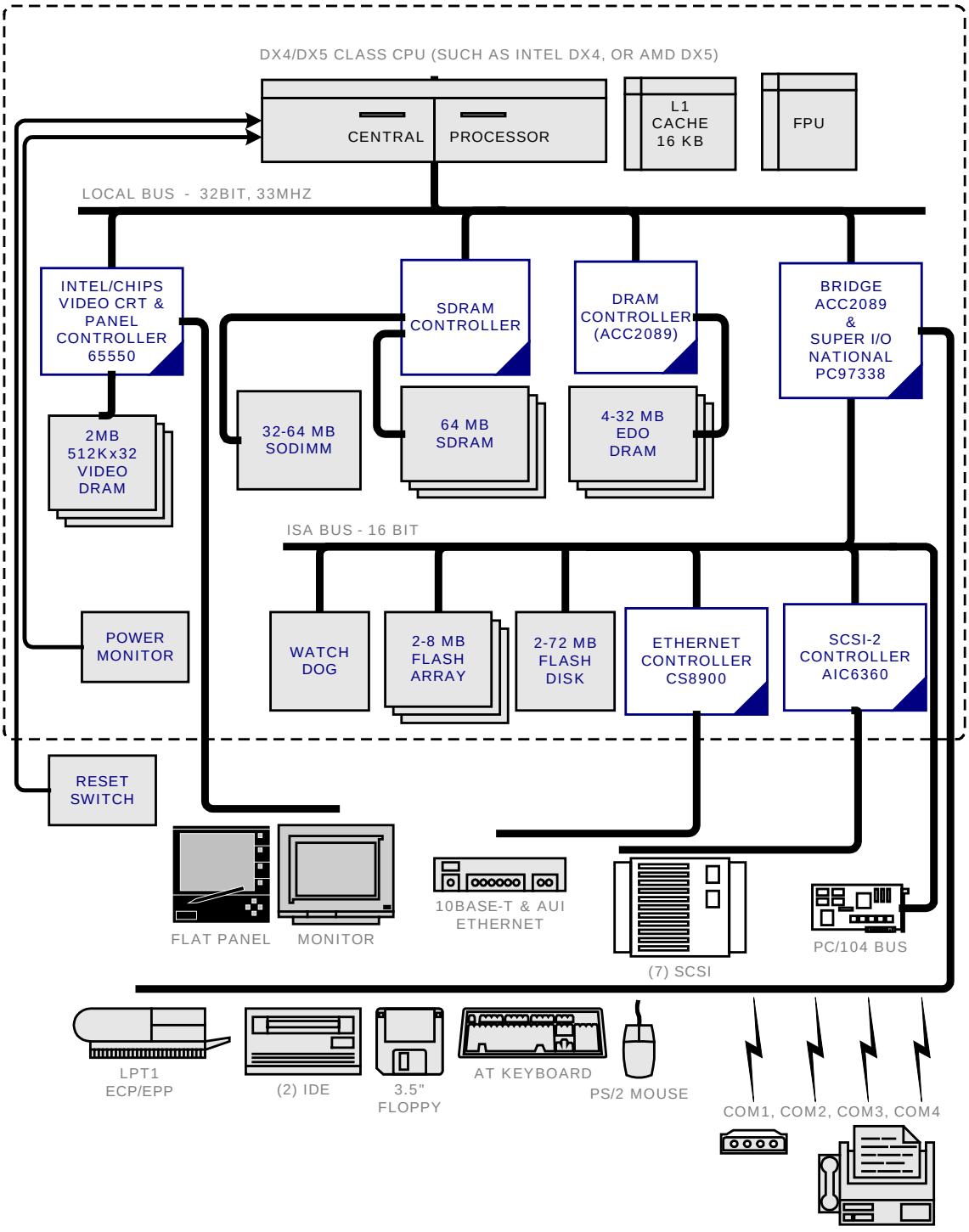


Figure 1 PC/II+dx Block Diagram (v1.33)

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4 Settings

4.1 Jumper Settings - User

Refer to the PC/II+dx Component Placement diagram. All jumpers are on the TOP side of the board.

Table 1 Jumper Settings - User

JUMPER	SETTING	SELECTED OPTION	COMMENT
JP01	open	Watchdog disabled	(default)
	closed	Watchdog enabled	This option can be ordered; please refer to section 10, "Ordering Information", on page 90. The watchdog controller and its internal functionality will always operate, whether or not this jumper is installed. However, the system will ONLY be forced into reset state at the time of a watchdog timer expiry if the watchdog is enabled, the timer has expired and this jumper is INSTALLED.
JP02	open	Normal operation	(default)
	closed	Reset RTC CMOS memory	This function is required to be enabled by the BIOS. Before closing (installing) this jumper, VCC5 and VCC3 Power may be present or not present. When the jumper is installed and the function has been enabled by the BIOS, the contents of the RTC NV SRAM User memory (242 bytes used for system configuration) is cleared. The jumper is required to be removed before power is applied (if power is applied when the jumper is installed, remove the jumper and then cycle the power to restore operation). On reboot, default configuration parameters are restored by the BIOS.

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4.2 Jumper Settings - Set by Manufacturing

Refer to the PC/II+dx Component Placement diagram. All jumpers are on the TOP side of the board.

Table 2 Jumper Settings - Manufacturing

JUMPER	SETTING	SELECTED OPTION	COMMENT
JP03	open	External bios	Used by Megatel manufacturing only
	closed	Normal operation	(default) Jumper must be present for normal operation.
JP04	open	Normal operation	(default)
	closed	Program bios	Used by Megatel manufacturing only

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5 Electrical Specifications

The PC/II+dx operates on a single +5V ± 5% supply, or on dual supplies of +5V ±5% and +3.3V ±5%. When a single +5V supply is used, the PC/II+dx board is shipped with an on-board regulator which generates the +3.3V. An on-board dual voltage monitors is used.

The +5V Power Header (J007) is shipped on all boards; an optional +3.3V Power Header (J009) can also be ordered. When both +5V and +3.3V are supplied from an external source to the board, the on-board regulated +3.3V power supply is eliminated from the board.

The PC/II+dx board sources +5V to the PC/104 bus, and can source a small amount of +5V and +3.3V to an optional transition board (QTB board series).

5.1 Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Power Supply (+5V)	Digital	VCC5	-0.3	6.0	V
Power Supply Current	(Except Peripherals)	ICC5		5000	mA
Ambient Temperature	**(Note 1)**	TA	-55	+125	°C
Storage Temperature	**(Note 1)**	TS	-65	+150	°C
Maximum Current to QTB	(+5v Through Mass I/O)	VM5		3000	mA
	(+3.3v Through Mass I/O)	VM3		50	mA

Warning: ***Operation at or beyond these limits may result in permanent damage to the board or to components attached to the board. Always operate the board at the Recommended Operating Conditions, see below.***

Note 1. ***Temperature is given for a board for which power is NOT applied and a Battery is NOT included onboard. If the board contains a lithium battery, then the absolute temperature board ratings must be modified to meet the more restrictive ratings for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board.***

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5.2 Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
Power Supply	Digital	VCC5	4.75	5.0	5.25	V
		VCC3	3.14	3.3	3.46	V
Power Supply Rise Time	+3.0V to +5.0V	VCC5S			100	ms
Operating Ambient Temperature	**(Note 1)**	TA	0		70	°C
Storage Ambient Temperature	**(Note 1)**	TS	-55		+125	°C
Humidity	(Untested)	HA	10		90	% RH

Note 1. ***Temperature is given for a board for which power IS applied, but a Battery is NOT included. If the board contains a lithium battery, then the absolute temperature board ratings must be modified to meet the more restrictive ratings for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board.***

5.3 DC Characteristics

Over Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units	NOTE
Power Supply	(digital)	VCC5	4.75	5.0	5.25	V	
		VCC3	3.15	3.3	3.45	V	
Power Supply Current		ICC5	1	2.5	5	A	
Power (+5V External, +3.3V External)	Intel DX4 Freq 66MHz FSB 33Mhz	PDD5		2.0		W	***1***
		PDD3		2.8		W	***1***

Note 1. ***Dual Supply Configuration. INTEL DX4 CPU operating at specified core frequency and specified local bus frequency, 16 MB of EDO DRAM installed, 2 MB Soldered Flash installed, SCSI installed, Ethernet installed, IDE installed, and with Video installed and an attached VGA CRT. Both +5V and +3.3V are externally supplied to board.***

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5.4 Voltage Monitor

An on-board micro voltage monitor is included in the PC/II+dx board. The Dallas Semiconductor DS1706S device provides both a watchdog function and a dual-voltage monitor function. The outputs of the device are directed to the system reset bus, RST and RST#, to provide a system reset at the time of a persistent power exception. The on-board +3.3V supply rail is monitored at minus 5% by the primary voltage monitor, and the +5V supply is monitored by the IN input voltage sense monitor, using a precision bridge to step the +5V down to the Input Trip Point (1.25V).

Over Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
+5V Supply Voltage		VCC5	4.75	5.0	5.25	V
+3.3V Supply Voltage	External Supply	VCC3	3.15	3.3	3.45	V
IN Input Trip Point		VTP	1.20	1.25	1.30	V
VCC5 Trip Point DS1706	NOTE 1	VCC5TP	4.05	4.29	4.53	V
VCC3 Trip Point DS1706	(primary)	VCC3TP	2.85	2.93	3.00	V
Reset Active Time		TRST	130	205	285	ms
VCC Detect to RST and RST#		TRFP	130	204	285	ms
PBRST# Stable Low to RST and RST#		TDLY			250	ms
VIN Detect to NMI#		TIPD		5	8	us

NOTES

1) The +5V supply to the board MUST be externally regulated to produce +5.0V on the board; and if +3.3V is externally supplied, the external supply must be externally regulated to produce +3.3V on the board.

5.5 Bus Drive Current

The PC/104 bus drive current is specified by the PC/104 Specification, Version 1.3, listed in section 2.2. The PC/II+dx board complies to this standard.

Most PC/104 bus signals have a reduced bus drive requirement of 4 mA. The 4 exceptions are open collector driven signals, which must drive 330-ohm pullup resistors defined by the P996 specification.

The following signals must be driven with devices capable of providing 20 mA sink current:

MEMCS16#, IOCS16#, MASTER# and ENDXFR#.

All other signals may be driven with devices capable of providing 4 mA sink current.

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6 Functional Specifications

6.1 Board Component List

The major components on the PC/II+dx board are contained in the following table. See Notes.

Table 3 Board Component List

REF	QTY	DESCRIPTION [1]	PART [2]	VENDOR
BAT1	1	BATTERY – 3.0V Lithium		
D002	1	LED – Ethernet Local Activity		
F001	1	TRANSFORMER – Isolation, Ethernet 10Base-T	ST7010	PULSE/VALOR
F002	1	TRANSFORMER – Isolation, Ethernet AUI	ST7033	PULSE/VALOR
J001	1	CONNECTOR – PC104AB, 2X32 .100 inch (Specified by User)		
J002	1	CONNECTOR – PC104CD, 2X20 .100 inch (Specified by User)		
J003	1	CONNECTOR – MASSIO, 5x11 HM 2mm (Specified by User)	106012-1 100161-1 100159-1 106775-1	AMP
J004	1	CONNECTOR – MASSIO, 5x22 HM 2mm (Specified by User)	352131-1 188836-1 352132-1 352268-1	AMP
J005	1	CONNECTOR – ETHERNET, 2X5 .100 Header		
J007	1	CONNECTOR – +5V POWER, 1x12 .100 Right-Angle Pin Header	22-05-2121	MOLEX
J008	1	HEADER – CPU FAN +5V & GND – 1x2 1.25 mm	53057-0210	MOLEX
J009	1	HEADER – +3.3V POWER, 1X5 .100 Straight Header		
JP01,JP02 JP03,JP04	4	JUMPER #1,#2,#3,#4 – 1x2 – 2 mm		
U001	1	BRIDGE & I-O / DRAM Controller	ACC2089	ACCMICRO
U002,U003 U006,U007	4	DRAM – EDO, 2 or 8 MB Memory, 50 ns typical	4LC1M16E5 4LC4M16R6	MICRON
U008	1	LOGIC – Gate		
U009	1	LOGIC – Bus Logic	2016	
U010	1	REGULATOR – Linear Voltage Regulator (+3.3V)		
U011	1	MONITOR – Power Monitor & Watchdog Controller	DS1706	DALLAS
U012	1	MODULE – 32 MB or 64 MB 66MHz 3.3V SDRAM SODIMM Module and SOCKET – SODIMM 144-Pin, for 32 MB or 64 MB 3.3V SDRAM Memory Module	MT4LSDT464 HG-662D1 or MT8LSDT864 HG-662D1	MICRON
U013	1	PROCESSOR – Processor, 100/66 MHz or 133/100 MHz	AM486DX4 FX80486DX4 AM486DX5	AMD INTEL AMD
U014,U015 U017,U018	4	SDRAM – 8 MB or 16 MB Memory, 66 MHz typical	48LC4M16A2 48LC8M16A2	MICRON
U016	1	CPLD		ALTERA
U019	1	Bus Switch		IDT
U021	1	FLASH ROM – ARRAY, 16 Mbit or 32 Mbit or 64 Mbit Flash	28F160 28F320 28F640	INTEL
U025	1	FLASH ROM – BIOS, 2Mbit (256 KB) Flash	29EE020	SST

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REF	QTY	DESCRIPTION [1]	PART [2]	VENDOR
U028,U029 U031,U032	4	TRANSCEIVER – RS232 High-KV Transceivers	ADM211E	ANALOG
U030	1	SUPER I/O controller for Legacy I/O	PC97338	NATIONAL
U033	1	SCSI – SCSI-2 Controller	AIC6360	ADAPTEC
U034	1	ETHERNET – Ethernet Controller	CS8900	CRYSTAL
U035	1	ETHERNET – Configuration EEPROM	93C46	
U036	1	VIDEO – Video CRT/Flat Panel Controller	65550	INTEL/CHIPS
U037	1	DRAM – VIDEO, EDO, 2MB Memory, 512Kx32		
U038	1	LOGIC – Gate		
U039	1	LOGIC – Gate		
U040	1	SOCKET – DIP 32, for M-Systems Disk-on-Chip Flash Disk		
U041	1	CLOCK – Clock Generator (System)		
U042	1	LOGIC – Gate		
U043	1	RTC – Real-Time Clock	DS1685	DALLAS
U044	1	LOGIC – Inverter		
U045	1	LOGIC – Bus Switch		
U047	1	LOGIC – Bus Switch		
U048	1	CLOCK – Clock Generator (Memory)		
U049	1	LOGIC – Inverter		
U050	1	LOGIC – Bus Switch		

NOTES

[1] For component specifications, refer to the applicable data sheets from the component respective manufacturer.

[2] All part numbers are generic, and boards may be shipped with alternatively-sourced parts which are functionally equivalent. If substitution of parts is required by Megatel, Megatel will make every attempt to provide a functionally equivalent parts, and Megatel reserves the right to change any component on the board (for example, if a component becomes obsolete, a second source part may be substituted). Please contact your distributor or agent, or contact Megatel directly if you have specific component requirements.

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6.2 Component Placement – Top Side

The following diagram shows the components on the top (component) side of the PC/II+dx board.

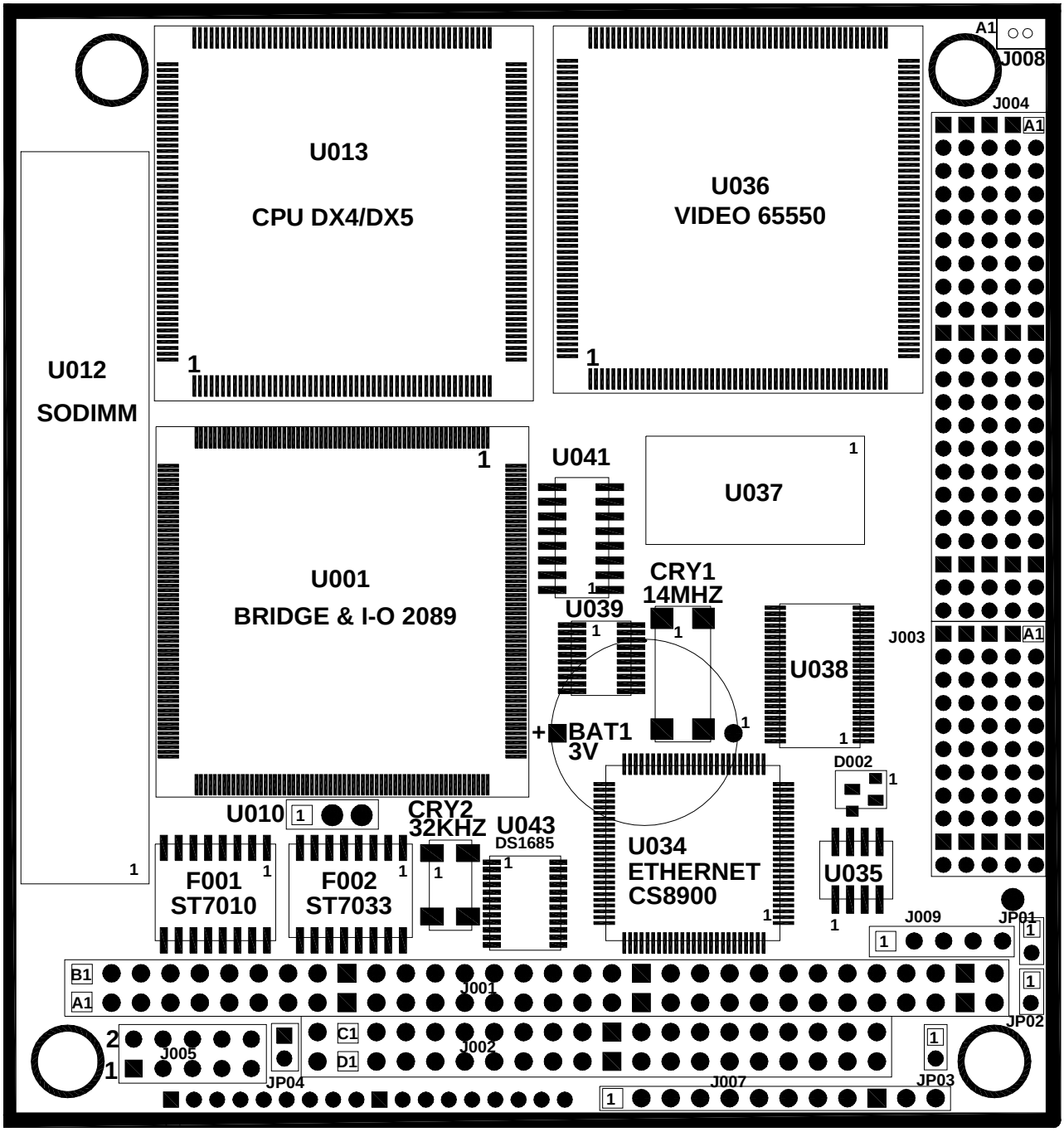


Figure 2 Component Placement – Top Side (v1.33)

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6.3 Component Placement – Bottom Side

The following diagram shows the components on the bottom (solder) side of the PC/II+dx board.

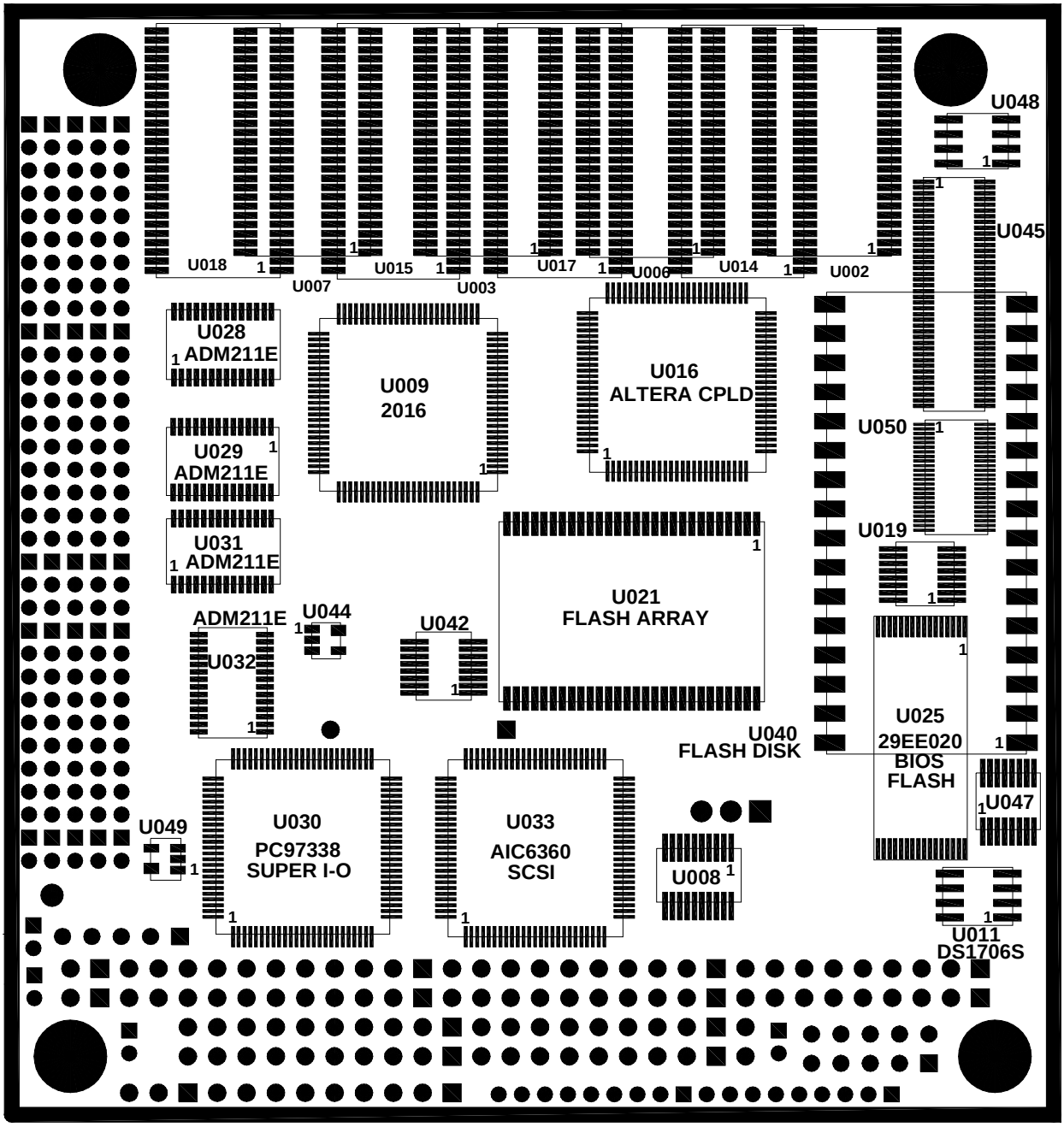


Figure 3 Component Placement – Bottom Side (v1.33)

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6.4 Cpu Processor

PC/II+dx is shipped with a user-selected Intel DX4 or AMD 486DX4/DX5 Processor installed.

Code	Processor	Freq	Ratio	Rating
1	**Intel DX4 100 MHz**	**100 MHz**	**3:1**	**Commercial**
2	**AMD DX4 100 MHz**	**100 MHz**	**3:1**	**Commercial**
3	**AMD DX5 133 MHz**	**133 MHz**	**4:1**	**Commercial**
4	**Intel DX4 66 MHz**	**66 MHz**	**3:1**	**Commercial**

The PC/II+dx can be shipped with a commercial processor – an AMD 486 DX5 133 MHz processor, an Intel 100 MHz 486 processor, an AMD 100 MHz 486 processor, or an Intel 66 MHz 486 processor. An industrial processor is also available. All standard operating software such as Linux, QNX, DOS, Windows, Windows 95/98 are supported.

The 486 DX4/DX5 processor is a full 32-bit pipelined RISC Core, with integrated Floating-Point and Write-Back or Write-Through Cached memory. It provides a high level of performance combined with a low cost base and a rich set of features and Industry Standard 486/386 Compatibility.

All DX4 and DX5 processors support host local bus speeds at 33 MHz, providing burst I/O transfers in excess of 100 Million Bytes/second. Core frequencies of DX4 processors are 66 MHz or 100 MHz, and of DX5 processors are 100 MHz or 133 MHz. Performance is greatly enhanced by the inclusion of Enhanced bus mode which provides the capability to support Write-back caching. Either Write-back or write-through caching is a selectable option. All processors implement 16K cache on-chip to provide very fast memory access for both frequent memory accesses to code and/or data. The cache is controlled using a modified MESI protocol, and the cache is implemented as a 'unified' cache to maximize hit ratios when code-to-data ratios are skewed.

The 486DX family processors support all x86 operating modes, including real mode, native protected mode and virtual mode, and support the full x86 instruction sets, register sets, memory management and I/O management functions. Many frequently-executed instructions take 1 cycle, and pipe-lined architecture allows multiple instructions to execute concurrently. An integrated on-chip floating-point unit supports the full Intel floating-point instruction set and data type set and provides high data rates.

All peripheral controllers are provided on-board as standard options. Any mix of options can be ordered, which results in a board with the exact price/performance you require.

6.5 Bus, DRAM Memory, Peripheral Controller

PC/II+dx is shipped with a highly-integrated ACC Micro ACC2089 controller. This controller implements the PC/104 (ISA) bus control functionality by bridging the local bus to the PC/1104 bus. It also supports a full memory controller function, and provides standard AT architectural functions. A set of integrated peripheral I/O controllers is also provided.

A description of the various functions of this controller are found in summary form in the corresponding sections of this document. For more detailed specifications, please refer to the ACC2089 datasheet found in the section 2, "Reference Documents" on page 11 of this document.

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6.6 Cache Description

Performance is greatly enhanced by the inclusion in the DX4 and DX5 of Enhanced bus mode which provides the capability to support Write-back caching. Either Write-back or Write-Through caching is an order option. All processors implement 16K cache on-chip to provide very fast memory access for both frequent memory accesses to code and/or data. The cache is controlled using a modified MESI protocol, and the cache is implemented as a 'unified' cache to maximize hit ratios when code-to-data ratios are skewed.

6.6.1 Write-through (WT)

Writes and reads to and from system memory are cached. Reads come from cache lines on cache hits; read misses cause cache fills. Speculative reads are allowed. All writes are written to a cache line (when possible) and through to system memory. When writing through to memory, invalid cache lines are never filled, and valid cache lines are either filled or invalidated. This type of cache-control is appropriate for frame buffers. Write-Through is required when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. It enforces coherency between caches in the processors and system memory.

6.6.2 Write-back (WB)

Writes and reads to and from system memory are cached. Reads come from cache lines on cache hits; read misses cause cache fills. Speculative reads are allowed. Write misses cause cache line fills (in the P6 family processors), and writes are performed entirely in the cache, when possible. The write-back memory type reduces bus traffic by eliminating many unnecessary writes to system memory. Writes to a cache line are not immediately forwarded to system memory; instead, they are accumulated in the cache. The modified cache lines are written to system memory later, when a write-back operation is performed. Write-back operations are triggered when cache lines need to be de-allocated, such as when new cache lines are being allocated in a cache that is already full. They also are triggered by the mechanisms used to maintain cache consistency. This type of cache-control provides the best performance, but it requires that all devices that access system memory on the system bus be able to snoop memory accesses to insure system memory and cache coherency.

If you are unsure of which option to order, contact your representative or Megatel Engineering. Write-back provides the best performance, but requires (a) all system bus devices to use bus snooping, and (b) no real-time semaphoric coherency problems exist in your applications. Write-through will always be acceptable for all bus devices and applications.

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6.7 Connectors

The following connectors are available (by option, except for J007 which is required):

- J001 – PC/104 Connectors AB – 2 x 32 Header (.100 inch pitch)
- J002 – PC/104 Connectors CD – 2 x 20 Header (.100 inch pitch)
- J003 – Mass I/O Connector – 5 x 11 (2-mm HM pitch)
- J004 – Mass I/O Connector – 5 x 22 (2-mm HM pitch)
- J005 – Ethernet Connector – 2 x 5 (.100 inch pitch)
- J007 – +5V Power Header – 1 x 12 (.100 inch pitch)
- J008 – Fan Connector – 1 x 2 (1.25mm pitch)
- J009 – +3.3V Power Header – 1 x 5 (.100 inch pitch)
- SODIMM – 144-pin SDRAM 3.3V

Table 4 Sample Connector Option Part Numbers

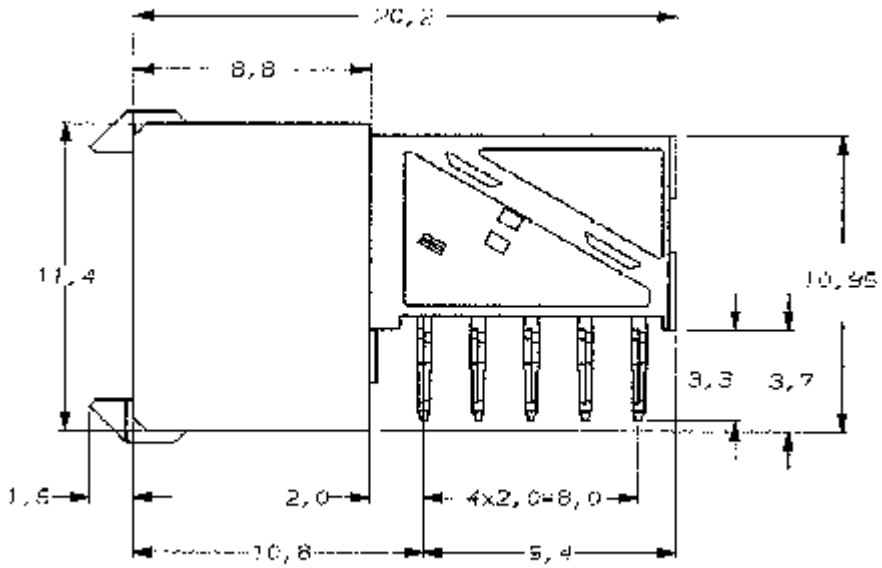
REF	PINS	VENDOR	SAMPLE PART NUMBER	DESCRIPTION
J001	64	SAMTEC	ESQ-132-12-G-D ESQ-132-14-G-D EW-32-09-G-D-xxx	2X32 .100 INCH S-RECEPTACLE NON-STK/THRU 2X32 .100 INCH S-RECEPTACLE STK/THRU 2X32 .100 INCH S-PLUG STK/THRU BOARD STACKER
J002	40	SAMTEC	ESQ-120-12-G-D ESQ-120-14-G-D EW-20-09-G-D-xxx	2X20 .100 INCH S-RECEPTACLE NON-STK/THRU 2X20 .100 INCH S-RECEPTACLE STK/THRU 2X20 .100 INCH S-PLUG STK/THRU BOARD STACKER
J003	110	AMP AMP AMP AMP SAMTEC SAMTEC	188836-1 352268-1 352131-1 352132-1 ESQT-122-03-G-Q ESQT-122-03-G-S	H.M. 2MM 5X22 TYPE B22 RA-RECEPTACLE H.M. 2MM 5X22 TYPE B22 S-RECEPTACLE H.M. 2MM 5X22 TYPE B22 RA-PLUG H.M. 2MM 5X22 TYPE B22 S-PLUG H.M. 2MM 4X22 HEADER S-RECEPTACLE H.M. 2MM 1X22 HEADER S-RECEPTACLE
J004	55	AMP AMP AMP AMP SAMTEC SAMTEC	100161-1 106775-1 106012-1 100159-1 ESQT-111-03-G-Q ESQT-111-03-G-S	H.M. 2MM 5X11 TYPE C RA-RECEPTACLE H.M. 2MM 5X11 TYPE C S-RECEPTACLE H.M. 2MM 5X11 TYPE C RA-PLUG H.M. 2MM 5X11 TYPE C S-PLUG H.M. 2MM 4X11 HEADER S-RECEPTACLE H.M. 2MM 1X11 HEADER S-RECEPTACLE
J005	10	SPECIALTY SAMTEC HARWIN	2HT05R05-4433 EW-05-09-G-D-xxx M20-998-05-08	2x5 .100 INCH R/A 2x5 .100 INCH BOARD STACKER 2x5 .100 INCH ROW POST
J007	12	MOLEX	22-05-2121	1x12 .100 INCH HEADER
J008	2	MOLEX		1x2 1.25mm
J009	5			1X5 .100 INCH VERTICAL PIN HEADER

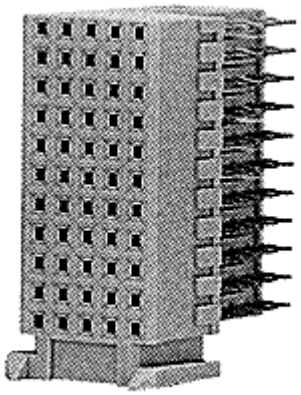
NOTES
(1) Connectors J001,J002 are specified by the PC/104 Specification version 2.3.
(2 To interface J002,J004 to the megatel side-by-side I/O board (QTB), PC/II+dx boards are normally shipped with the two right-angle female connectors, AMP 188836-1 and AMP 100161-1 or equivalent, which mate with the two right-angle male connectors on the QTB, AMP 352131-1 and AMP 106012-1 or equivalent. The straight versions may be special-ordered. for vertical board-stacking applications, you may also order HM 2mm stacking headers.
(3) All connector part numbers are sample values; equivalent connectors may also be used.
(4) J008 mates with Molex 51021.

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6.7.1 AMP Connector (Right-Angle Receptacle) Dimensions

The following diagram and picture is representative of the AMP Z-PACK 5X11 (TYPE C) connector, one of two similar connectors used on the PC/II+dx Mass I/O Interface, and were provided by AMP. Please refer to the AMP Z-PACK HM 2MM catalog for more information.





6.8 CPLD

PC/II+dx contains a CPLD device to provide miscellaneous logic that allows the PC/II+dx to function as an AT-compatible Cpu board.

6.9 Ethernet Controller

PC/II+dx contains an optional, highly-integrated LAN Ethernet Interface, that is used in networking applications. This option includes the single-chip Crystal CS8900 controller, a configuration EEPROM, isolation transformers for either 10Base-T and/or AUI, depending upon the option ordered, and an on-board Ethernet header (J005).

PC/II+dx pulls the Attachment Unit Interface (AUI) port signals and the 10Base-T twisted-pair port signals to a 10-Pin (2x5 on 0.100" [2,54 mm] spacing). When connected to the megatel Ethernet Paddle Board (an accessory board product), the AUI port signals are pulled to a DB15 connector and the 10Base-T port signals are pulled to an RJ-45 connector. Alternatively, these signals can be accessed through the same connectors on standard QTB accessory transition boards which mate with the Mass I/O connector and Ethernet header. Please refer to the section 8.3, "J005 – Ethernet Connector", on page 83 of this document for a description of the Ethernet header pins.

The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully IEEE 802.3 AUI interface, while the 10Base-T interface also fully complies to IEEE 802.3.

The CS8900 controller contains an IEEE 802.3 MAC engine that operates in the I/O memory space. It contains an on-chip RAM for buffering receive & transmit frames, and supports full duplex operation, a 10BASE-T port with analog filters & automatic polarity correction, and an AUI port. Programmable transmit features include automatic re-transmission on collision, and automatic padding and CRC generation. Programmable receive features include Automatic-switch between DMA & on-chip memory, early interrupts for frame preprocessing, and automatic rejection of erroneous packets. An on-board configuration EEPROM is provided for jumper-less configuration, and on-board transformers for each interface are provided. The CS8900 supports I/O transfers at up to 10 Megabits/sec. Depending upon which media is active, the AUI or 10Base-T interface is automatically enabled. This automatic selection can be overridden by software configuration.

Drivers for most operating systems, including DOS, Windows and NT, are available.

For detailed specifications of the Ethernet Controller and Interface, please refer to the datasheets for the Ethernet Controller and Isolation Transformers, found in section 2, "Reference Documents" on page 11 of this document.

For a pinout of the Ethernet header, see section 8.3.

For interrupt and DMA assignments, see sections 7.3 and 7.4.

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6.10 Flash ROM – BIOS

The standard ROM on the PC/II+dx is a 2Mbit (256K Byte) flash EEPROM. This EEPROM contains the system BIOS and all option BIOS modules, including the SVGA BIOS, the SCSI BIOS and other bios modules required to interface to on-board peripherals. All PC/II+dx boards are shipped with a flash BIOS.

BIOS code is shadowed in system memory located between C0000h and FFFFFh. The system BIOS code occupies the top segment of real mode memory (F0000h to FFFFFh). Option ROM BIOS modules are shadowed into the region C0000h to DFFFFh. Option BIOS modules will be loaded depending upon the configuration of the PC/II+dx board.

The following tables describe the drivers that are available for use with the PC/II+dx board. Both drivers and optional ROM BIOS modules are listed. Please contact Megatel if you have specific requirements, and to receive the driver information, or visit our web site.

Table 5 ETHERNET Drivers & Utilities

DRIVER NAME	REVISION
Netware ODI DOS Client	2.62
Netware ODI OS/2 Client	2.59
Netware ODI Server Driver	2.60
OS/2 NDIS2 Driver	2.68
DOS NDIS2 Driver	2.68
Windows NT/95 NDIS3 Driver	3.20
Windows for Workgroup NDIS3 Driver	2.57
Packet Driver	2.55
Setup utility	2.66

Table 6 VIDEO Drivers & BIOS Options

DRIVER NAME	REVISION
HiQVideo Driver for Win NT 3.5x	1.1.5
HiQVideo Driver for Win 95	1.2.6
Display Driver for Windows 3.x	1.3.2
Display Driver for OS/2	2.2.7
HiQVideo VGA BIOS	2.0.0

Table 7 FLASH Array BIOS Option

DRIVER NAME	REVISION
Datalight CardTrick (as Optional ROM)	3.01.13

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6.11 Flash Array – User

PC/II+dx contains an optional 2MB, 4MB or 8MB of Flash Array. PC/II+dx uses Intel® StrataFlash™ or FlashFile™ high-density symmetrically-blocked architecture flash memory. Flash Array parts are soldered on the circuit board. The flash array is supported by the Datalight Cardtrick BIOS driver.

All required programming voltages are provided on-board.

6.12 Flash Disk – M-Systems Disk-on-Chip

PC/II+dx contains an optional 32-Pin DIP socket that can be user-populated with a M-Systems Disk-on-Chip® 2000 flash disk. The socket is bottom-mounted on the PC/II+dx circuit board.

The Disk-on-Chip® product provides standalone or expansion Flash Disk memory in sizes ranging from 2 to 144 MB.

Both the DiskOnChip® 2000 and Flash Array can be used together on the same board.

For more detailed information on Disk-on-Chip® products, please contact M-Systems..

6.13 Floppy Disk Interface

PC/II+dx contains a Floppy Disk Drive Interface controller as part of the basic board, provided by the ACC Micro ACC2089. Floppy disk interface signals are pulled to the Mass I/O Connector.

The controller supports one (1) or two (2) 3.5" floppy disk drives. It is compatible with IBM System 34 double density format (MFM), and Sony EMCA format. Address decoding is compatible with the IBM PC drive system. Both DMA and non-DMA modes are supported. Standard 500, 250 and 300 Kb/Sec transfer rates are supported.

The Floppy Disk controller uses Interrupt Request IRQ6, and DMA channel DRQ2.

The floppy disk interface can be multiplexed to the parallel port pins for external floppy disk drive support. This function is enabled by setting Register BEh, Bit 2, to one.

For more detailed information about the Floppy Disk Interface, please refer to the ACC2089 datasheet, found in section 2, "Reference Documents" on page 11 of this document.

For a description of the Floppy drive interface signals, see section 8.2.8.

6.14 ISA bus

Please refer to PC/104 Bus, section 6.17.

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6.15 Memory

The PC/II+dx board is manufactured to contain either SDRAM-type memory or DRAM-type memory. The type of memory, which can't be mixed on the same board, and the amount of memory are selected by option. DRAM devices are normally EDO 60 ns parts, while SDRAM devices are normally 66 MHz parts.

The amount and type of soldered and socketed memory on a given board is automatically detected by the BIOS – there are no memory jumpers to configure.

The valid combinations of populated & socketed memory by total memory given in the following table.

Table 8 Total System Memory Options

TOTAL	SOLDERED EDO DRAM [1]		SOLDERED SDRAM [1]		SODIMM SDRAM [2]
MEM	MEM	DEVICES & ORG	MEM	DEVICES x ORG	MEM
4 MB	4 MB	2 of 1Mx16			
8 MB	8 MB	4 of 1Mx16			
16 MB	16 MB	2 of 4Mx16			
16 MB			16 MB	2 of 4Mx16	
32 MB	32 MB	4 of 4Mx16			
32 MB			32 MB	4 of 4Mx16	
64 MB			64 MB	4 of 8Mx16	
64 MB			32 MB	4 of 4Mx16	32 MB
96 MB			32 MB	4 of 4Mx16	64 MB
96 MB			64 MB	4 of 8Mx16	32 MB
128 MB			64 MB	4 of 8Mx16	64 MB

NOTES
[1] Either DRAM or SDRAM may be populated, but not both on the same board.
[2] SODIMM SDRAM may be used only when two banks (4 parts) of soldered SDRAM is present on the same board.

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6.15.1 Memory – EDO DRAM

There are 4 population sites on the board for one or two banks of soldered-down EDO DRAM. Either 1Mx16 or 4Mx16 parts are installed. The options are as follows:

Table 9 EDO DRAM Memory Options

TOTAL	DEVICES x ORGANIZATION
4 MB	2 x 1Mx16
8 MB	4 x 1Mx16
16 MB	2 x 4Mx16
32 MB	4 x 4Mx16

6.15.2 Memory – SDRAM

There are 4 population sites on the board for one or two banks of soldered-down SDRAM. Either 4Mx16 or 8Mx16 parts are installed, providing amounts of 16, 32 or 64 MB. The options are as follows:

Table 10 SDRAM Memory Options

TOTAL	DEVICES x ORGANIZATION
16 MB	2 x 1Mx16
32 MB	4 x 1Mx16
64 MB	4 x 4Mx16

6.15.3 Memory – SODIMM SDRAM

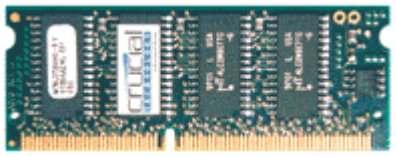
For PC/II+dx boards ordered with an SODIMM 144-Pin socket, a single SODIMM SDRAM module can be installed to increase the base SDRAM memory by an additional 32 or 64 MB, for a total system memory maximum of up to 128 MB. Two banks or soldered SDRAM (either 4 parts of 1Mx16 or 4Mx16 are required to be populated when an SODIMM socket is ordered). The options are as follows:

Table 11 SODIMM SDRAM Memory Options

TOTAL SODIMM SDRAM	DEVICES x ORGANIZATION
32 MB	1 x 32-MB SDRAM SODIMM MODULE
64 MB	1 x 64-MB SDRAM SODIMM MODULE

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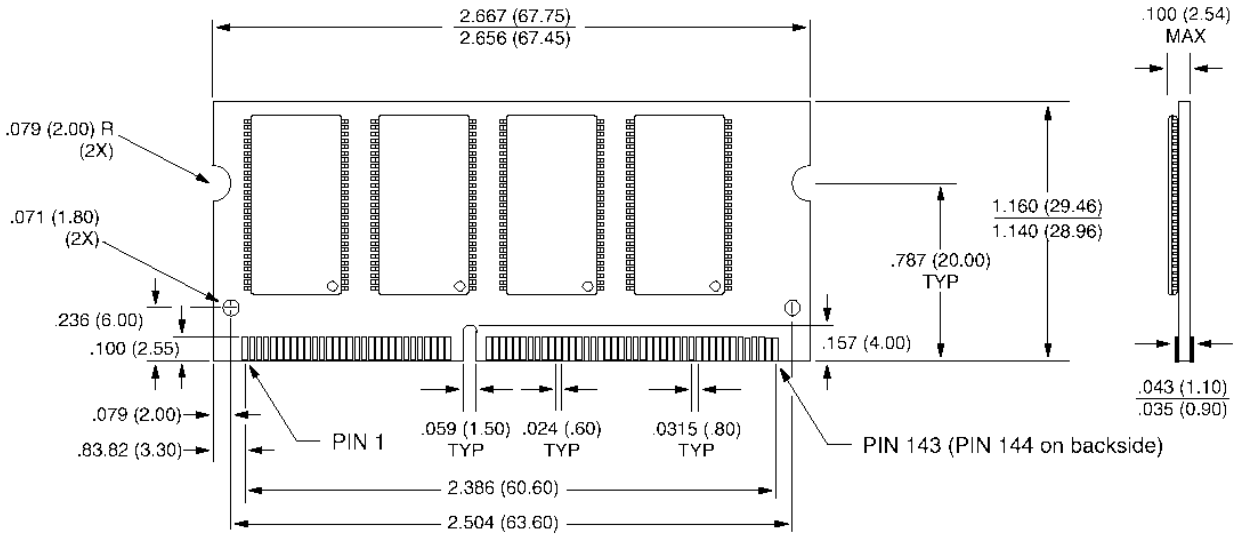
The photograph below illustrates a typical SODIMM 144-Pin module from CRUCIAL Technology (a Division of MICRON), and measures approximately 2.625" x 1".

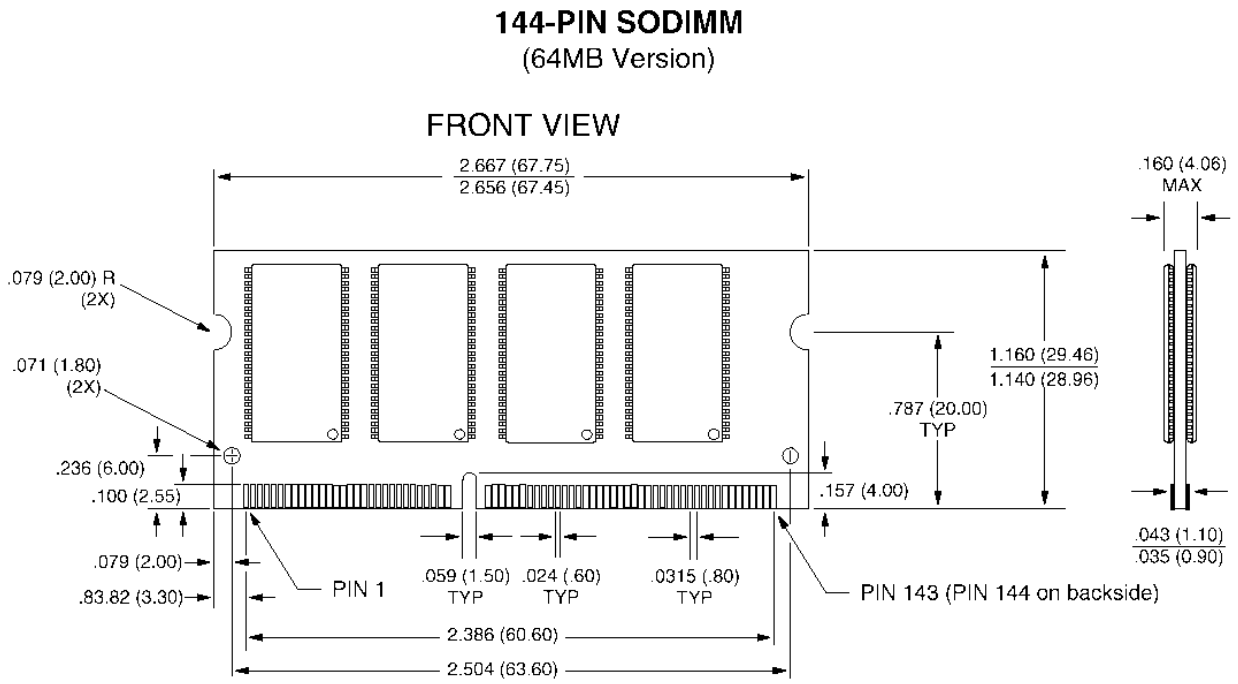


The following two diagrams indicate representative physical dimensions that apply to MICRON 32 MB and 64 MB SODIMM SDRAM modules, and were provided by MICRON. Please refer to the MICRON SODIMM SDRAM module documentation for the most recent accurate information.

144-PIN SODIMM
(32MB Version)

FRONT VIEW





6.16 Parallel Port

PC/II+dx supports a single Parallel Port controller that is integrated in the ACC2089 super I/O. The parallel port is a basic feature of PC/II+dx. It is pulled to the Mass I/O Connector.

The parallel port interface supports a standard selectable ECP/EPP/BPP/SPP mode. It is software configurable – there are no jumpers required. The parallel port supports standard Centronics-type printers, standard PS/2-type Bi-directional devices, and Enhanced Parallel Port (EPP 1.9) and Extended Capabilities Port (ECP) protocols.

A 16-byte FIFO is included in the interface, used by EPP and ECP modes. Run-Length Compression (RLE) is also supported. Both DMA and PIO transfers are supported.

For detailed parallel port specifications, please refer to the datasheets for the ACC2089, section 2.1.

For pinout and signal information, see section 8.2.14.

6.17 PC/104 Bus Interface

Please refer to the documents, "PC/104 specification – Revision 2.3 – June 1996" and "P996.1 Standard or Compact Embedded-PC Modules", listed in section 2.2.

The PC/104 bus can be software-configured to operate at one of the following clock speeds:

Table 12 Pinout – ISA 8-bit Bus J902 (Rows A and B) – 2 X 32 .100" Header

PC/104 (ISA) BUS CLOCK SPEED	CONFIGURATION VALUE (NOTE 1)
3.33 MHz	10000
4.16 MHz	10101
5.53 MHz	10001
6.66 MHz	10010
7.71 MHz	0XXXX
8.00 MHz (default speed set by BIOS)	11XXX
8.32 MHz	10111
11.11 MHz	10011
16.66 MHz	10100
16.66 MHz	10110

NOTES
[1] Binary format. This value is written to the 2089 register 0x05 (bits 4:0). 'X' = don't care value.

For Bus Drive Current requirements, please also refer to section 5.5.
For pinout information, see section 8.1.

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6.18 Real-Time Clock

The PC/II+dx contains an optional Real-Time Clock (RTC), a Dallas Semiconductor DS1685. This clock is a full-function part, and is certified as Year-2000 compliant by Dallas. The RTC uses a 32.768 KHz crystal and a 3.0V Lithium battery. The battery is soldered onto the circuit board and is part of the RTC option.

Information contained in the following sub-sections is present in summary form. For more detailed information about the Real-Time Clock, please refer to the DS1685 datasheet found in section 2, "Reference Documents" on page 11 of this document.

6.18.1 Features of the Real-Time Clock

- 242 Bytes battery backed up NVRAM
- RAM Clear input
- Low battery current (500 nA)
- Leap Year to year 2100 provides Year 2000 compliance
- Century byte with Automatic Rollover provides Year 2000 compliance
- 24 0r 12 Hour Format
- Programmable Alarm, Settable at Any Time hh:mm:ss, with Interrupt
- Programmable Timer, Settable to Periods Ranging from 122 uSec to 500 mSec
- Daylight Savings Time Support
- Unique 48-Bit Silicon Laser-Written Serial Number, Can be used by Customer Applications

The PC/II+dx is factory-shipped with the Real-Time Clock set to the correct time and date for the North-American EST (Eastern Standard Time) time zone. The software for the Real-Time Clock is included in the system BIOS for boards containing the Real-Time Clock option.

The Lithium battery is rated for 125 mAh (typical) in an operating range of -20C to +70C. Discharge current is 500 nA, and storage temperature is -40C to +60C.

6.18.2 Setting Time and Date

The DOS clock is updated automatically by the Real-Time Clock upon Boot-Up. Should you change the time or date in DOS, the PC/II+dx will conversely update the Real-Time Clock hardware time and date. The PC/II+dx uses standard DOS instructions to change the time and date. If you are using standard DOS, and if the time and date are displayed at boot time, you may at that point change the time and date if desired. Standard DOS commands to change the TIME and DATE can also be used.

Time and date are also settable in Windows and Windows NT4.0; please refer to the operating system documentation for details.

6.18.3 Using the Real-Time Clock NVRAM

The BIOS utilizes the battery backed up NVRAM to store its configuration information which it needs to access at boot time and at other times. Besides the time and data information contained in the Real-Time Clock hardware, the BIOS stores information about the Video preferences, floppy disk drive configuration, and panel information.

A total of 114 Bytes of RAM in bank 0, and 128 Bytes of RAM in bank 1 are supported (total of 242 Bytes of RAM).

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6.18.4 Real-Time Clock Interrupt 1Ah

The BIOS supports AT compatible real-time clock functions using software interrupt 1Ah. In addition, the PC/II+dx BIOS supports the following functions using the software interrupt 1Ah, which provide read and write access to bank 0 and bank 1 SRAM memory in the real-time clock, and read access to the unique serial number encoded in the real-time clock chip.

1. FUNCTION 0FFh – WRITE AND READ BANK-0 SRAM

This function writes a byte to RTC SRAM Bank 0, or reads a byte from RTC SRAM Bank 0.

```
MOV   AH,0FFh
MOV   DL,<RTC bank 0 register number>
MOV   DH,<Direction>                    Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                        Bit 1-7 = Unused
MOV   AL,<8-Bit Value to be Written>    Used if DH.0 = 0, Unused if DH.0 = 1
INT   1Ah
-- returns here with
      /FX.CF = 1 (Error)
      /FX.CF = 0 (No Error)
            /AH = Destroyed
            /AL = value read from RTC or written to RTC>
```

2. FUNCTION 0FBh – WRITE AND READ BANK-1 EXTENDED SRAM

This function writes a byte to RTC Bank 1 Extended SRAM, or reads a byte from RTC Bank 1 Extended SRAM.

```
MOV   AH,0FBh
MOV   DL,<RTC bank 1 register number>   0 - 7Fh
MOV   DH,<Direction>                    Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                        Bit 1-7 = Unused
MOV   AL,<8-Bit Value to be Written>    Used if DH.0 = 0, Unused if DH.0 = 1
INT   1Ah
-- returns here with
      /FX.CF = 1 (Error)
      /FX.CF = 0 (No Error)
            /AH = Destroyed
            /AL = value read from RTC or written to RTC>
```

3. FUNCTION 0FCh – READ RTC SERIAL NUMBER

This functions reads the silicon serial number that is embedded in the RTC chip. Each RTC chip is manufactured to contain a unique serial number.

```
MOV   AH,0FCh
LES   DI,<pointer to seven-byte buffer that will receive the serial number field>
INT   1Ah
-- returns here with
      /FX.CF = 1 (Error)
      /FX.CF = 0 (No Error)
            /[ES:DI+0] = Silicon Serial Number Byte 1 through Byte 6
            /[ES;DI+6] = Silicon Serial Number CRC byte
```

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6.18.5 Real-Time Clock Memory Map

Table 13 Real-Time Clock Memory Map

RTC Offset	Bank 0		Bank 1	
	Description	Access	Description	Access
00	Seconds	R(bits 0–7), W(bits 0–6)	Seconds	R(bits 0–7), W(bits 0–6)
01	Seconds Alarm	RW	Seconds Alarm	RW
02	Minutes	RW	Minutes	RW
03	Minutes Alarm	RW	Minutes Alarm	RW
04	Hours	RW	Hours	RW
05	Hours Alarm	RW	Hours Alarm	RW
06	Day of the Week	RW	Day of the Week	RW
07	Day of the Month	RW	Day of the Month	RW
08	Month	RW	Month	RW
09	Year	RW	Year	RW
0A	Register A	R(bits 0–7), W(bits 0–6)	Register A	R(bits 0–7), W(bits 0–6)
0B	Register B	RW	Register B	RW
0C	Register C	R	Register C	R
0D	Register D	R	Register D	R
0E–3F	RAM Bytes 00–3F		RAM Bytes 00–3F	
40	RAM Byte 40		RTC Model Number	
41	RAM Byte 41		1st Byte Serial Number	
42	RAM Byte 42		2nd Byte Serial Number	
43	RAM Byte 43		3rd Byte Serial Number	
44	RAM Byte 44		4th Byte Serial Number	
45	RAM Byte 45		5th Byte Serial Number	
46	RAM Byte 46		6th Byte Serial Number	
47	RAM Byte 47		CRC Byte	
48	RAM Byte 48		Century Byte	
49	RAM Byte 49		Date Alarm	
4A	RAM Byte 4A		Extended Control Reg 4A	
4B	RAM Byte 4B		Extended Control Reg 4B	
4C	RAM Byte 4C		Reserved	
4D	RAM Byte 4D		Reserved	
4E	RAM Byte 4E		RTC Address – 2	
4F	RAM Byte 4F		RTC Address – 3	
50	RAM Byte 50		Extended RAM Address	

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RTC Offset	Bank 0		Bank 1	
	Description	Access	Description	Access
51	RAM Byte 51		Reserved	
52	RAM Byte 52		Reserved	
53	RAM Byte 53		Extended RAM Data Port	
54–7F	RAM Bytes 54–7F		Reserved	

Table 14 RTC Extended RAM Memory Map

Via 50 & 53	Bank 0		Bank 1 Extended RAM	
00–7F	-		RAM Bytes 00–7F	RW

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6.19 SCSI I/O

PC/II+dx contains an optional SCSI-2 controller. The SCSI-2 bus signals are pulled to the Mass I/O Connector. Active terminators, with a jumper to enable or disable the terminators, is available using a Megatel standard QTB (transition board which provides connectors to interface to all standard devices).

The SCSI interface uses Interrupt Request IRQ11.
The SCSI interface uses DMA channel DRQ6.

For pinout and signal information, see section 8.2.15.

Adaptec AIC6360 Controller

When ordered, the Adaptec AIC-6360 SCSI-2 controller is used as the Host device on a SCSI-2 bus. This controller supports byte, word or 32-bit double word PIO data transfers, and can also utilize 16-bit DMA. With its 128-byte data FIFO, it can burst data at up to 10 MBytes/s across the Host bus, and can support synchronous data transfers at up to 10 MBytes/s across the SCSI bus.

PC/II+dx BIOS ships with a SCSI option BIOS module. In addition, an installable Adaptec driver (ASPI manager for DOS) is available which supports a range of devices and operating environments. For more details, please refer to the Adaptec SCSI documentation, available from Adaptec.

6.20 Serial Ports

PC/II+dx contains 1, 2, 3 or 4 optional full RS-232E ports.

Each serial port option includes all required RS-232 receivers and line drivers.
Each serial port is fully 16C550 compatible.
Each serial port contains standard modem control and data I/O interface signals (2-data, 6-control).
Each serial port contains both receive and transmit FIFOs which are 16-bytes deep.

PC/II+dx uses the ADM211E receiver/driver on each serial interface to provide RS-232 levels. The transceiver is EIA-RS232E and CCITT V.28 compliant. Input tolerance on all inputs is ±25V, and output swing on all outputs is ±9V with all transmitter outputs loaded with 3K ohms to Ground. The transceivers run at +5V and use on-chip voltage doublers and inverters. Refer to the ADM211E datasheet for determining the power which may be drawn by attached devices.

The I/O ports are configured by the BIOS as COM1, COM2, COM3 and COM4.

COM1 uses Interrupt Request IRQ4, and is based in I/O address space at 3F8h.
COM2 uses Interrupt Request IRQ3, and is based in I/O address space at 2F8h.
COM3 uses an assignable IRQ, and is based in I/O address space at 3E8h.
COM4 uses an assignable IRQ, and is based in I/O address space at 2E8h.

For information on interrupts and DMA channels that are assignable, see sections 7.3 and 7.4.

For more detailed information about serial I/O, please refer to the PC97338 and ACC2089 datasheets, found in section 2.1.

For pinout and signal information, see sections 8.2.4 through 8.2.7.

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6.21 Speaker Output

Output sound waveform signals carried by the Speaker Output signal are generated by Timer 2. The Timer 2 output is gated with port 60h, bit 1 (Speaker Data) to drive the Speaker Output. The state of Timer 2 output can be read from port 61h, bit 5.

Speaker Output signal is pulled to the Mass I/O Connector (MS-SPEAKER, J004, pin a7). It is intended to drive a piezo-electric audio transducer connected between the Speaker Output signal pin and Ground.

6.22 Super AT I/O Controllers

AT Super-I/O functionality is provided by two controllers. The ACC MICRO 2089 is part of the basic board functionality while the National PC97338 is an optional controller that is populated when Serial ports COM3 and COM4 are present. Both controllers provide the 4 full 16550-style UARTs with 16-byte FIFOs (full on-board RS232 transceivers are supported), a Parallel ECP/EPP port (also configurable as BPP/SPP), a PS/2-style Keyboard and PS/2 Mouse, an IDE controller with support for two devices, and a standard Floppy controller with support for two 3.5” drives. Additional standard features include generation of PC speaker output, and system reset switch input.

The functionality provided by the two controllers are described in their respective sections in this document.

6.23 Timers/Counters

Three internal counters are provided as basic features of PC/II+dx. The timers/counters are compatible to the AT standard 8254. The clock input for each is tied to a clock of 1.193 MHz, which is derived by dividing the system 14.31818 MHz clock by 12, and which provides a minimum timing resolution of 838ns.

Timer 0 output is tied to IRQ0 (Interrupt controller 1, level 0).
Timer 1 output is used to initiate a refresh cycle for system memory.
Timer 2 is used to generate signals that produce sound waveforms on the Speaker Output signal.

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6.24 Video – Intel/Chips 65550 Super VGA & Panel Controller

PC/II+dx contains a complete analog and flat panel Video interface. When this optional interface is shipped on a PC/II+dx board, the analog CRT display and 24-bit flat panel interface signals are pulled to the Mass I/O connector. The Video Interface option includes 2MB of fast video memory EDO DRAM.

The Video Interface uses the Intel/Chips® 65550 Video Controller and is compatible with the IBM-PS/2 Video Graphics Array (VGA) and supports the SVGA standard. The controller operates on the local bus, and supports both Analog Monitors and a wide variety of Flat Panels. It contains a powerful 64-bit Graphics Engine, Palette/DAC and Clock Synthesizer. The separate 2MB of fast EDO DRAM video memory is accessed from the controller over a direct 32-Bit bus. An 8MB Linear Buffer can also be used, allocated at the high end of main memory. This video memory is used normally, to buffer all video data and is mapped by the controller into Main memory address space. It is also used for frame buffering in LCD-DD interfaces – unused video memory is automatically used for a framestore area by the controller in this case. The hardware register and gate interface is standard VGA, and the BIOS is also VGA compatible. Drivers for all common operating systems are available. Simultaneous CRT and LCD display mode is available.

The Video panel interface can be ordered to support either 5V panels or 3.3V panels. This option affects both the 24-bit panel interface and the compatible video interface. For more information on using the 3.3V panel interface, contact Megatel Engineering.

For pinout and signal information, see sections 8.2.10 and 8.2.16.

6.24.1 Video Hardware Features

Please refer to the Intel/Chips® 65550 reference documentation for a list of features available. The 65550 supports these features (revision 1.5, December 1997):

- Highly integrated design Flat Panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, and Clock Synthesizer
- Hardware Windows Acceleration
  - 64-bit Graphics Engine
    - System-to-Screen and Screen-to-Screen BitBLT
    - 3-Operand Raster-Ops
    - 8/16/24 Color Expansion
  - Transparent BLT
    - Optimized for Windows™ BitBLT format
- High Performance:
  - Deep write buffers
  - EDO DRAM Support
  - 40 MHz
- Display centering and stretching features for optimal fit of VGA graphics and text on 800x600 and 1024x768 panels
- Simultaneous Hardware Cursor and Pop-up Window
  - 64x64 pixels by 4 colors
  - 128x128 pixels by 2 colors
- Game Acceleration
  - Source Transparent BLT
  - Destination Transparent BLT
  - Double buffer support for YUV and 15/16bpp Overlay Engine
  - Instant Full Screen Page Flip
  - Read back of CRT Scan line counters.
- Optimized for High-Performance Flat Panel Display
  - 640x480 x 24bpp
  - 800x600 x 24bpp

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  - 1024x768 x 16bpp

  CRT Support 110 MHz
- Direct interface to Color and Monochrome, Single Drive (SS), and Dual Drive (DD), STN & TFT panels
- Flexible On-chip Activity Timer facilitates ordered shut-down of the display system
- Composite NTSC / PAL Support
- Power Sequencing control outputs regulate application of Bias voltage
- Fully Compatible with IBM® VGA

6.24.2 Video Driver Features

- High Performance Accelerated drivers
- Compatible across HiQVideo family
- Auto Panning Support
- LCD/CRT/Simultaneous Mode Support
- Auto Resolution Change
- HW Stretching/Scaling
- Double Buffering
- Internationalization
- ChipsCPL (Control Panel Applet)
- Direct Draw support
- Games SDK support
- Dynamic Resolution Switching
- VGA Graphics applications in Window
- VESA DDC extensions
- VESA DPMS extensions
- Property Sheet to change Refresh/Display
- Seamless Windows Support
- Boot time resolution adjustment
- DIVE, EnDIVE
- DCAF
- DebugVGA
- Auto testing of all video modes
- ChipsVGA
- ChipsEXT
- BIOS OEM Reference Guide
- Display Driver User's Guide
- Utilities User's Guide
- Release Notes for BIOS, Drivers, and Utilities

6.24.3 Video BIOS Features

- VGA Compatible BIOS
- DDC 1, DDC 2AB
- Text and Graphics Expansion
- Auto Centering
- 44 (40) K BIOS
- CRT, LCD, Simultaneous display modes
- Auto Resolution Switch
- Multiple Refresh Rates
- NTSC/PAL support
- Extended Modes
- Extended BIOS Functions
- 1024x768 TFT, DSTN Color Panels

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- Multiple Panel Support (8 panels built in)
- Get Panel Type Function
- HW Popup Interface
- Monitor Detect
- Pop Up Support
- SMI and Hot Key support
- Set Active Display Type Hook
- Save/Restore Video State Hook
- Setup Memory for Save/Restore Hook
- SMI Entry Point Hook
- Int 15 Calls after POST, Set Mode Hook

6.24.4 Video Display Enhancement Features

A variety of video enhancement features are supported, particularly for flat panels, by the Chips® 65550 Video Controller:

True-Gray

PC/II+dx video supports TRUE-GRAY gray scale algorithm, a polynomial-based frame-rate control (FRC) and dithering algorithm to generate a maximum of 61 gray levels on monochrome panels. This algorithm extends the support of flicker-free gray scales from 16 to 61 on, for example, film-compensated monochrome STN LCDs, without the need to increase refresh rate, a conventional solution which increases power consumption, ghosting and decreases contrast.

RGB Color to Gray Scale Reduction

PC/II+dx video supports RGB Color to Gray Scale Reduction, allowing 24-bit color pallette data to be reduced automatically to 6-bits for 64 gray scales. Reduction techniques include NTSC weighting, Equal Weighting (for blue background operating systems such as Windows), and Green Only for replicating 6-bits of green pallette data such as IBM monochrome monitors.

SmartMap

PC/II+dx video supports SMARTMAP, an algorithm that automatically adjusts the foreground and background of adjacent gray scales to maximize contrast on flat panel displays. This algorithm is particularly useful when displaying information containing multiple colors on monochrome flat panels.

Text Enhancement

PC/II+dx video supports Text Enhancement whereby Dim White is displayed on flat panels as Bright White to optimize contrast level.

Vertical Compensation

PC/II+dx video supports Vertical Compensation techniques for flat panels. Unlike CRT monitors, flat panels have a fixed number of scan lines (eg. 200, 400, 480 or 768 lines). PC/II+dx allows lower resolution software to be displayed on a higher resolution panel by use of manual or automatic Vertical Centering, Stretching, Blank Line Insertion, or Tall Font™.

Horizontal Compensation

PC/II+dx video supports Horizontal Compensation techniques for flat panels, including Horizontal Compression, Horizontal Centering and Horizontal Doubling and text expansion.

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6.24.5 Video Linear Buffer Support

PC/II+dx video frame buffer is supported using 2 MB of fast EDO DRAM. This memory can be mapped by the 65550 controller (under program control by the Video BIOS) (a) at the standard VGA memory window (0xA0000 through 0xBFFFF), or (b) into a linearly-accessible 8MB memory window at an origin located above the system's main memory address space.

When the video DRAM is mapped into the standard video buffer address space below 1MB, option "f" should can be ordered as "0" (see section 10.2.19), and both of the Panel signals, ACTI (activity indicator) and ENABKL (enable backlight) are available on the panel interface.

When the video DRAM is mapped into a linear buffer, the Video BIOS maps it to reside *above* the total main memory configured for the PC/II+dx board. This address window will normally be allocated as shown in the following table.

Table 15 Linear Buffer Options & Option "f" - ACTI, ENABKL

MEMORY INSTALLED	LINEAR BUFFER ORIGIN	OPTION " f " VALUE REQUIRED
4 MB - 128 MB	Linear Buffer Not Used	0 OR 1
4 MB - 32 MB	Linear Buffer at 56 MB	0 OR 1
64 MB	Linear Buffer at 128 MB	1
96 MB	Linear Buffer at 128 MB	1
128 MB	Linear Buffer at 128 MB	1

MEMORY INSTALLED includes all soldered DRAM or SDRAM; if an SODIMM is present, add 64 MB to this total.

LINEAR BUFFER ORIGIN is the base address of the buffer; the buffer size is always 8 MB.

OPTION "f" VALUE REQUIRED refers to the order option "f" (section 10.2.19); when option "f" is 0, the panel signals ACTI and ENABKL are available on the panel I/O interface; when option "f" is 1, these signals are not available because the corresponding pins on the video controller are used for high memory addressing purposes which is required when a Linear buffer is being used. When a linear buffer is not to be used, then select option "f" as 0, which enables ACTI and ENABKL on the panel interface.

6.24.6 Video Analog CRT Display Support

PC/II+dx supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. The video controller supports up to 110 MHz, which provides SVGA resolutions up to 1280 x 1024 – 256 colors, 1024 x 768 – 256K colors or 800 x 600 – 1,677,216 colors. Please refer to the Chips® 65550 documentation for detailed information.

All standard VGA modes are supported on these typical CRT monitors: PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 33.5 KHz horizontal frequency specification); NEC Multi-Sync 3D or equivalent multi-frequency CRT monitor (37.5 KHz minimum horizontal frequency specification); Nanao Flexscan 9070s, Multisync 5D, or equivalent multi-frequency high-performance CRT monitor (48.5 KHz minimum horizontal frequency specification).

6.24.7 Video Flat Panel Display Support

The on-board Chips 65550 controller supports all flat panel display technologies, including plasma, electroluminescent (EL) and liquid crystal (LCD). LCD panel interfaces are provided for single panel, single drive (SS) and dual panel, dual drive (DD) configurations. The controller utilizes the on-board video memory for its integrated frame buffer and 24-bit panel interface; the "C" DRAM is not used on the PC/II+dx. Standard and high-res passive STN and active matrix TFT/MIN LCDs are supported. Up to 16M colors on 24-bit active matrix LCDs, up to 4K colors on passive STN LCDs and up to 64 gray scales on monochrome panels are

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supported. The flat panel interface can interface to a variety of panels, as illustrated in the following table; please refer to the Chips® 65550 Video Controller reference documentation for details.

Table 16 Flat Panel Interface Signal Mapping

Mass I/O Pin#	Mass I/O Pin Name	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 9/12/ 16 bit	Color TFT 18/24 bit	Color TFT HR 18/24 bit	Color STN SS 8-bit (x4bP)	Color STN SS 16-bit (4bP)	Color STN DD 8-bit (4bP)	Color STN DD 16-bit (4bP)	Color STN DD 24-bit	65550 Pin#	65550 Pin Name
B - e6	L1-FPD0	–	UD3	UD7	B0	B0	B00	R1	R1	UR1	UR0	UR0	71	P0
B - a5	L1-FPD1	–	UD2	UD6	B1	B1	B01	B1	G1	UG1	UG0	UG0	72	P1
B - b5	L1-FPD2	–	UD1	UD5	B2	B2	B02	G2	B1	UB1	UB0	UB0	73	P2
B - c5	L1-FPD3	–	UD0	UD4	B3	B3	B03	R3	R2	UR2	UR1	LR0	74	P3
B - d5	L1-FPD4	–	LD3	UD3	B4	B4	B10	B3	G2	LR1	LR0	LG0	75	P4
B - e5	L1-FPD5	–	LD2	UD2	G0	B5	B11	G4	B2	LG1	LG0	LB0	76	P5
B - a4	L1-FPD6	–	LD1	UD1	G1	B6	B12	R5	R3	LB1	LB0	UR1	78	P6
B - b4	L1-FPD7	–	LD0	UD0	G2	B7	B13	B5	G3	LR2	LR1	UG1	79	P7
B - c4	L1-FPD8	P0	–	LD7	G3	G0	G00	SHFCLKU	B3	–	UG1	UB1	81	P8
B - d4	L1-FPD9	P1	–	LD6	G4	G1	G01	–	R4	–	UB1	LR1	82	P9
B - e4	L1-FPD10	P2	–	LD5	G5	G2	G02	–	G4	–	UR2	LG1	83	P10
B - a3	L1-FPD11	P3	–	LD4	R0	G3	G03	–	B4	–	UG2	LB1	84	P11
B - b3	L1-FPD12	P4	–	LD3	R1	G4	G10	–	R5	–	LG1	UR2	85	P12
B - c3	L1-FPD13	P5	–	LD2	R2	G5	G11	–	G5	–	LB1	UG2	86	P13
B - d3	L1-FPD14	P6	–	LD1	R3	G6	G12	–	B5	–	LR2	UB2	87	P14
B - e3	L1-FPD15	P7	–	LD0	R4	G7	G13	–	R6	–	LG2	LR2	88	P15
B - a2	L1-FPD16	–	–	–	–	R0	R00	–	–	–	–	LG2	90	P16
B - b2	L1-FPD17	–	–	–	–	R1	R01	–	–	–	–	LB2	91	P17
B - c2	L1-FPD18	–	–	–	–	R2	R02	–	–	–	–	UR3	92	P18
B - d2	L1-FPD19	–	–	–	–	R3	R03	–	–	–	–	UG3	93	P19
B - e2	L1-FPD20	–	–	–	–	R4	R10	–	–	–	–	UB3	94	P20
B - b1	L1-FPD21	–	–	–	–	R5	R11	–	–	–	–	LR3	95	P21
B - d1	L1-FPD22	–	–	–	–	R6	R12	–	–	–	–	LG3	96	P22
B - e1	L1-FPD23	–	–	–	–	R7	R13	–	–	–	–	LB3	97	P23
B - d6	L1-SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	70	SHFCLK
	Pixels/Clock	8	8	16	1	1	2	2-2/3	5-1/3	2-2/3	5-1/3	8		

NOTES

[1] *The 65550 also supports panel interfaces that transfer one pixel per word, but which use both edges of SHFCLK to transfer one pixel on each edge.*

[2] *The higher order output lines should be used when only 9 or 12 bits are needed from the 9/12/16-bit TFT interface, or when only 18 bits are needed from the 18/24-bit TFT or TFT HR interfaces. The lower order bits should be left unconnected.*

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6.24.8 Video Mode Support – Standard VGA Modes

Which super VGA Graphics modes the Chips® 65550 can support depend upon several factors, including display memory size requirements, dot clock (display pixel rate) requirements, video DRAM memory bandwidth requirement (bytes per pixel, pixel rate and bandwidth available to the CPU). For simultaneous CRT and panel operation, compatibility between panel timing requirements and CRT requirements is also a factor. The PC/II+dx Chips® 65550 uses a 32-bit interface to 2 MB of 50 ns (typical) EDO DRAM memory. It runs at 5V and supports a maximum Dot Clock (DCLK) of 110 MHz. The standard VGA modes supported by the PC/II+dx are summarized in the following table.

Table 17 VGA Standard Modes Supported

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
0, 1	Text	16	40 x 25	8x8	320x200	25.175	31.5	70
0*,1*	Text	16	40 x 25	8x14	320x350	25.175	31.5	70
0+,1+	Text	16	40 x 25	9x16	360x400	28.322	31.5	70
2,3	Text	16	80 x 25	8x8	640x200	25.175	31.5	70
2*,3*	Text	16	80 x 25	8x14	640x350	25.175	31.5	70
2+,3+	Text	16	80 x 25	9x16	720x400	28.322	31.5	70
4	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
5	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
6	Graphics	2	80 x 25	8x8	640x200	25.175	31.5	70
7	Text	Mono	80 x 25	9x14	720x350	25.175	31.5	70
7+	Text	Mono	80 x 25	9x16	720x400	28.322	31.5	70
D	Planar	16	40 x 25	8x8	320x200	25.175	31.5	70
D	Planar	16	80 x 25	8x8	640x200	25.175	31.5	70
F	Planar	Mono	80 x 25	8x14	640x350	25.175	31.5	70
10	Planar	16	80 x 25	8x14	640x350	25.175	31.5	70
11	Planar	2	80 x 30	8x16	640x480	25.175	31.5	60
12	Planar	16	80 x 30	8x16	640x480	25.175	31.5	60
13	Packed Pixel	256	40 x 25	8x8	320x200	25.175	31.5	70

NOTES
[1] *All of the above VGA standard modes are supported directly in the Video BIOS.*
[2] *All VGA modes using 25.175 MHz and 28.322 MHz can also be supported using 32 MHz and 36 MHz respectively.*

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6.24.9 Extended Resolution Modes

For complete details on using any of these modes, refer to the Intel/Chips documentation for the 65550 controller.

Table 18 Extended Resolution Modes Supported - Preliminary

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
20	4-bit Linear	16	80x30	8x16	640x480	25.175	31.5	60
20	4-bit Linear	16	80x30	8x16	640x480	31.500	37.9	72
20	4-bit Linear	16	80x30	8x16	640x480	31.500	37.5	75
22	4-bit Linear	16	100x37	8x16	800x600	36.000	35.1	56
22	4-bit Linear	16	100x37	8x16	800x600	40.000	37.9	60
22	4-bit Linear	16	100x37	8x16	800x600	50.350	48.1	72
22	4-bit Linear	16	100x37	8x16	800x600	49.500	46.9	75
24 I	4-bit Linear	16	128x48	8x16	1024x768	44.900	35.5	43
24	4-bit Linear	16	128x48	8x16	1024x768	65.000	48.4	60
24	4-bit Linear	16	128x48	8x16	1024x768	75.575	57.5	70
24	4-bit Linear	16	128x48	8x16	1024x768	78.750	60	75
28 I	4-bit Linear	16	128x48	8x16	1280x1024	78.750	46.433	43
28	4-bit Linear	16	128x48	8x16	1280x1024	80.000	80.0	43
30	8-bit Linear	256	80x30	8x16	640x480	25.175	31.5	60
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.9	72
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.5	75
32	8-bit Linear	256	100x37	8x16	800x600	36.000	35.1	56
32	8-bit Linear	256	100x37	8x16	800x600	40.000	37.9	60
32	8-bit Linear	256	100x37	8x16	800x600	50.350	48.1	72
32	8-bit Linear	256	100x37	8x16	800x600	49.500	46.9	75
34 I	8-bit Linear	256	128x48	8x16	1024x768	44.900	35.5	43
34	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.4	60
34	8-bit Linear	256	128x48	8x16	1024x768	75.575	57.5	70
34	8-bit Linear	256	128x48	8x16	1024x768	78.750	60.00	75
40	15-bit Linear	32K	80x30	8x16	640x480	50.350	31.5	60
40	15-bit Linear	32K	80x30	8x16	640x480	63.000	37.9	72
40	15-bit Linear	32K	80x30	8x16	640x480	63.000	37.5	75
41	16-bit Linear	64K	80x30	8x16	640x480	50.350	31.5	60
41	16-bit Linear	64K	80x30	8x16	640x480	63.000	37.9	72
41	16-bit Linear	64K	80x30	8x16	640x480	63.000	37.5	75
42	15-bit Linear	32K	100x37	8x16	800x600	72.000	35.1	56
42	15-bit Linear	32K	100x37	8x16	800x600	80.000	37.9	60
43	16-bit Linear	64K	100x37	8x16	800x600	72.000	35.1	56
43	16-bit Linear	64K	100x37	8x16	800x600	80.000	37.9	60
50	24-bit Linear	16M	80x30	8x16	640x480	75.525	31.5	60
60	Text	16	132x25	8x16	1056x400	41.500	31.5	70
61	Text	16	132x50	8x8	1056x400	41.500	31.5	70
6A/70	Planar	16	100x37	8x16	800x600	36.000	35.1	56

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Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
6A/70	Planar	16	100x37	8x16	800x600	40.000	37.9	60
6A/70	Planar	16	100x37	8x16	800x600	50.350	48.1	72
6A/70	Planar	16	100x37	8x16	800x600	49.500	46.9	75
72 I/72 I	Planar	16	128x48	8x16	1024x768	44.900	35.5	43
72/75	Planar	16	128x48	8x16	1024x768	65.000	48.4	60
72 I/72 I	Planar	16	128x48	8x16	1024x768	75.525	57.5	70
72/75	Planar	16	128x48	8x16	1024x768	78.750	60.0	75
78	Packed Pixel	256	80x25	8x16	640x400	25.175	31.5	70
79	Packed Pixel	256	80x30	8x16	640x480	25.175	31.5	60
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.9	72
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.5	75
7C	Packed Pixel	256	100x37	8x16	800x600	36.000	35.1	56
7C	Packed Pixel	256	100x37	8x16	800x600	40.000	37.9	60
7C	Packed Pixel	256	100x37	8x16	800x600	50.350	48.1	72
7C	Packed Pixel	256	100x37	8x16	800x600	49.500	46.9	75
7E I	8-bit Linear	256	128x48	8x16	1024x768	44.900	35.5	43
7E	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.4	60
7E	8-bit Linear	256	128x48	8x16	1024x768	75.525	57.5	70
7E	8-bit Linear	256	128x48	8x16	1024x768	78.750	60.00	75

NOTES
[1] *"I" modes are interlaced.*

6.24.10 Video Resolution, Colors, Refresh & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth supported for CRT displays and/or TFT panels are contained in this section. In the following table, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided. The table applies for both CRT and TFT panels, including simultaneous CRT and TFT operation. This list is not a complete list of all modes that the VGA BIOS can support. Refer to the Chips VGA BIOS documentation for more information above VGA BIOS mode support.

Table 19 Video Resolution, Colors, Refresh, & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth [1]	Screen Refresh [2]	Horiz. Freq.	Dot Clock	Notes
640 x 480 x 8 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 16 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 24 bpp	85 Hz	43.3 KHz	36 MHz	
800 x 600 x 8 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 16 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 24 bpp	60 Hz	37.9 KHz	40 MHz	[3]
1024 x 768 x 8 bpp	85 Hz	68.7 KHz	94.5 MHz	
1024 x 768 x 16 bpp	56 Hz	45.2 KHz	60.7 MHz	[3]
1280 x 1024 x 8 bpp	60 Hz	64 KHz	108 MHz	

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NOTES

[1] Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported. Except for the interlaced modes in this table, all modes apply to both CRT displays and to TFT panels, including simultaneous CRT and TFT operation.

[2] This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth

[3] Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

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6.24.11 Video Resolution, Colors, and Refresh Support – STN-DD Panels

In the following tables, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided for each STN-DD panel type. Video overlay does not apply to the PC/II+dx video interface. See notes for support of simultaneous CRT & panel operation. This list is not a complete list of all modes that the VGA BIOS can support – please refer to the Chips VGA BIOS documentation for more information above VGA BIOS mode support.

Table 20 Video Resolution, Colors & Refresh Support – STN-DD Panels

Resolution and Color Depth [1]	Screen Refresh					
	640x480 Color	640x480 Mono	800x600 Color	800x600 Mono	1024x768 Color	1024x768 Mono
640 x 480 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz	70 Hz
640 x 480 x 16 bpp	85 Hz	75 Hz	75 Hz	75 Hz	70 Hz [4]	70 Hz
640 x 480 x 24 bpp	75 Hz [3]	75 Hz	75 Hz [3,4]	75 Hz [3,4]	70 Hz [5]	70 Hz [5]
800 x 600 x 8 bpp	75 Hz	75 Hz	85 Hz	75 Hz	70 Hz [3]	70 Hz
800 x 600 x 16 bpp	75 Hz	75 Hz	85 Hz [4]	75 Hz [3]	70 Hz [3,4]	70 Hz [3,4]
800 x 600 x 24 bpp	75 Hz [3]	75 Hz	85 Hz [5]	75 Hz [5]	70 Hz [3,5]	70 Hz [5]
1024 x 768 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz
1024 x 768 x 16 bpp	75 Hz	75 Hz	75 Hz [4]	75 Hz [3]	70 Hz [5]	70 Hz [5]
1280 x 1024 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz

NOTES

[1] Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported. Unless otherwise noted (see [4,5]), simultaneous CRT and STN-DD panel operation is supported.

[2] This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth

[3] Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

[4] Simultaneous CRT and panel operation is not supported. Panel-only operation can be supported (see note [5] below).

[5] For panels, graphics raster registers and DCLK must be programmed for half the specified refresh rate, and frame acceleration must be enabled to achieve the specified panel FLM frequency. Simultaneous operation with a CRT is not supported.

[6] STN-DD panels require additional buffering compared to TFT panels and CRT displays. STN-DD panels usually are divided into upper and lower half-panels, which must be refreshed simultaneously. A "DD" buffer allows pixels to be read from display memory in a single-scan manner while refreshing the STN-DD panel in a dual-drive ("DD") manner. In the PC/II+dx, the DD buffer is embedded in the main display memory in an off-screen area. In this case, the DD buffer can be either full-frame or half-frame. With a half-frame DD buffer, the refresh rate of the STN-DD panel (FLM frequency) is double the refresh rate of the CRT. This doubling effect is also referred to as frame acceleration. In all of the STN-DD mode listed, frame acceleration can be used to achieve a panel refresh rate twice as high as the specified refresh rate, except in cases where frame acceleration is already assumed to be enabled.

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6.25 Watchdog & Power Monitor

The PC/II+dx contains a DS1706S Microprocessor Supervisor that provides a Watchdog timer. The Watchdog WDS# output is tied to RST# causing a minimum 200 microsecond CPU reset to occur when the watchdog timer triggers. A jumper (JP01) is included between WDS# and RST# to permanently disable the watchdog function ((remove jumper's shunt to disable Watchdog, install jumper's shunt to enable watchdog function).

At the hardware level, the Watchdog input must be driven low periodically, at a ***minimum rate of once per second***, to prevent the watchdog WDS# output from being activated. This strobe is normally driven by the PC/II+dx board hardware, and in this mode, the watchdog does not trigger, and the Watchdog timer is in inactive mode.

To allow the Watchdog timer to trigger and cause a CPU reset, the Watchdog jumper must be inserted, the Watchdog must be activated by calling BIOS Int 15h, function 0FE00h, and the Watchdog strobe must not have been issued (BIOS Int 15h, function 0FDh) for a duration of 1 second.

A program-accessible interface to the Watchdog Enable/Disable control signal and the Watchdog Strobe signal are provided by the PC/II+dx BIOS Int 15h (functions 0FEH and 0FDh respectively), as described in the following subsections.

1. FUNCTION 0FEh – ACTIVATE AND DEACTIVATE WATCHDOG TIMER

This function activates the watchdog timer to allow software control of strobing, or deactivates the watchdog timer to disable watchdog functionality.

In ACTIVE mode the watchdog will trigger and cause a CPU reset if the watchdog jumper is inserted and a software strobe has not been issued to the watchdog in the last second using function 0FDh. Therefore, issuing one strobe per second rate or faster is required.

In INACTIVE mode strobing is not required and the watchdog will **not** cause a CPU reset to occur. This is the default at boot time.

```
MOV    AH,0FEh
MOV    AL,<Command>                    00h = ACTIVATE watchdog
                                       01h = DEACTIVATE watchdog
INT    15h
-- returns here after the specified watchdog MODE has been entered
       / ALL Registers are preserved
```

2. FUNCTION 0FDh – STROBE WATCHDOG TIMER

This function strobes the watchdog timer, causing its timer to restart. In ACTIVE mode (see function 0FEh), the watchdog must be strobed at a one strobe per second rate, and preferably at a faster rate, to prevent the watchdog timer from expiring and a CPU reset from occurring. In INACTIVE mode this function has no affect.

```
MOV    AH,0FDh
INT    15h
-- returns here after one strobe has been issued to the watchdog
       / ALL Registers are preserved
```

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7 System Resource Maps

7.1 I/O Address Map

Table 21 I/O Map

I/O ADDRESS REGION [1]	USED BY	DESCRIPTION	USED FOR
0000–000F	ACC2089	DMA controller 1	8237A-5
0020–0021	ACC2089	Interrupt controller 1	8259A-MASTER
0040–0043	ACC2089	Timer	8254
0060, 0064	ACC2089	Keyboard controller	
0070–0071	ACC2089	Real-time clock, NMI mask	DS1685
0080–008F	ACC2089	DMA page register	74LS612
0092	ACC2089	Alternate gate a20, fast reset register	
00A0–00A1	ACC2089	Interrupt controller 2	8259A-SLAVE
00C0–00DF	ACC2089	DMA controller 2	8237A-5
00F0	ACC2089	Clear math coprocessor busy	
00F1	ACC2089	Reset math coprocessor	
00F2	ACC2089	ACC2089 configuration register index	BIOS
00F3	ACC2089	ACC2089 configuration register data	BIOS
00F8–00FF	ACC2089	Math coprocessor	
0102	65550	VGA global enable	
0140–015F	AIC6360	SCSI-2 controller – primary	Scsi I/O
0170–0177	ACC2089	Secondary HDC	
0180–019F	CPLD	Reserved	
01F0–01F7	ACC2089	Primary HDC	IDE
0200–0207		Reserved	Game Port 1
0238–023B		Reserved	Bus Mouse
0238–023F		Reserved	Alternate Bus Mouse
0278–027F		Reserved	Printer #2
02B0–02DF		Reserved	Video – EGA
02E0–02E7		Reserved	GPIB
02E8–02EF	PC97338	COM4–IRQ3	Serial I/O – #4
02F8–02FF	ACC2089	COM2–IRQ3	Serial I/O – #2
0300–030F	CS8900	Ethernet controller	Ethernet
0300–031F		Reserved	Prototype Cards
0340–035F	AIC6360	SCSI-2 controller – secondary	Scsi I/O
0370–0377	ACC2089	Secondary FDC	
0378–037A	ACC2089	LPT1 (Standard mode)	Printer #1
037B–037F	ACC2089	LPT1 (EPP mode)	Printer #1 – EPP
0398–0399	PC97338	PC97338 configuration register index-data	BIOS
03B4–03B5	65550	VGA crtc index / data	VGA BIOS
03BA	65550	VGA status register / Feature Control Register	VGA BIOS

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I/O ADDRESS REGION [1]	USED BY	DESCRIPTION	USED FOR
03BD	PC97338	PNP (Plug & Play)	PNP Initialization
03C0–03C1	65550	VGA attrib controller index / data	VGA BIOS
03C2	65550	VGA input status register 0 / MSR	VGA BIOS
03C3	65550	VGA motherboard video system enable	VGA BIOS
03C4–03C5	65550	VGA sequence index / data	VGA BIOS
03C6–03C9	65550	VGA color palette registers	VGA BIOS
03CA	65550	VGA feature control register	VGA BIOS
03CC	65550	VGA misc output register	VGA BIOS
03CE–03CF	65550	VGA graphics controller index/data	VGA BIOS
03D0–03D1	65550	Video flat panel extension regs index/data	VGA BIOS
03D2–03D3	65550	Video multimedia extension regs index/data	VGA BIOS
03D4–03D5	65550	VGA CRTC index/data (CGA emulation)	VGA BIOS
03D6–03D7	65550	Video configuration extensions data/index	VGA BIOS
03DA	65550	VGA status register	VGA BIOS
03E8–03EF	PC97338	COM3–IRQ4	Serial I/O – #3
03F0–03F7	ACC2089	Primary FDC	Floppy
03F8–03FF	ACC2089	COM1–IRQ4	Serial I/O – #1
0778–077A	ACC2089	LPT (ECP mode)	Printer #1 – ECP

NOTES
[1] Addresses are expressed in hexadecimal notation; all addresses are in the 65K physical I/O address space supported by the processor.

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7.2 Memory Map

7.2.1 Memory Map (for SDRAM Controller)

Table 22 Memory Map (for SDRAM systems)

MEMORY ADDRESS REGION (NOTE 1)	LENGTH	DESCRIPTION
0000000 – 009FFFF	640 KB	Base Memory Address Region.
00A0000 – 00AFFFF	64 KB	Video 65550 – VGA Frame Buffer
00B0000 – 00B7FFF	32 KB	Video 65550 – MDA Emulation Character Buffer
00B8000 – 00BFFFF	32 KB	Video 65550 – CGA Emulation Frame Buffer
00C0000 –00CFFFF	64 KB	Option BIOS Memory Address Region. This memory address region is ALWAYS shadowed. All memory accesses to this region are always forwarded to system memory, never to the system bus. This region typically contains the VGA BIOS.
00D0000 – 00DFFFF	64 KB	Flash Memory Address Region (for accessing any 1 of 128– 64K flash sectors). This memory address region is used to access both User Flash pages and Bios Flash pages. It can be shadowed with system memory when access to Flash is not required. Memory accesses are forwarded to the system bus, causing FCS (Flash Chip Select) to be asserted, only if the Flash Window is enabled The page numbers are assigned as follows: page 0 – 127 User flash array page 128 – 131 BIOS flash
00E0000 – 00E7FFF	32 KB	Reserved.
00E8000 – 00EFFFF	32 KB	Disk-on-Chip Memory Address Region. This memory address region is used to access the Disk-On-Chip, and it can be shadowed with system memory when access to Disk-On-Chip is not required. Memory accesses are forwarded to the system bus, causing X32CS# (Disk-on-Chip Chip Select) to be asserted only if X32CS is enabled.
00F0000 – 00FFFFF	64 KB	BIOS ROM Memory Address Region. This memory address region is used for standard BIOS ROM. Memory write accesses to this address region are always forwarded to system memory, never to the system bus. Memory read accesses to this address region are forwarded to the system bus, only if enabled, otherwise they are forwarded to system memory.
0100000 – 7FFFFFF	127 MB	Additional Extended Main Memory (by option)
8000000 – 87FFFFF	8 MB	Video 65550 - Linear Accessible Buffer. This memory region always resides higher than the last main memory address, usually at the 128MB boundary. ***Video BIOS will set the actual address used, which may be higher or lower than at the 128 MB boundary.***

NOTES
(1) Addresses are expressed in hexadecimal notation; all addresses are in the first 1MB of physical address space (also known as 'real memory' address region).
(2) Please refer to the ACC2089 Datasheet for information on the DRAM memory controller.

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7.2.2 Memory Map (for DRAM Controller)

Please refer to the ACC2089 Datasheet for information on the DRAM memory controller.

7.2.3 Memory Shadowing

The Shadowing options for EDO DRAM are controlled by register 02h in the 2089. This register is duplicated within the CPLD, so that if SDRAM is installed, it will provide the same shadowing functions for SDRAM as the 2089 provides for EDO DRAM. These functions are described below. Please refer to the ACC2089 data sheet for further details.

7.2.4 Shadow Disable

After a power-up or a system reset, all shadowing is disabled. Therefore any memory accesses to the area from 000C0000 – 000FFFFF is directed to the system bus.

7.2.5 Shadow Enable

Shadowing may be enabled on a 64 KB-page basis for each of the 64 KB pages beginning at C0000, D0000, E0000 and F0000. When shadowing is enabled, both read and write operations are directed to DRAM rather than to the system bus.

7.2.6 Shadow Protection

In addition, there is a single write-enable bit, which can inhibit write operations to shadow RAM. If a memory region is not shadowed, then both read and write operations are forwarded to the bus. Both the X32 (flash disk - Disk-on-Chip®) device and the User Flash Array device have enable bits, which allow the corresponding chip select to be disabled.

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7.3 Interrupt IRQ Map

Table 23 Interrupt Map

INT. REQ. NUMBER (NOTE 4)	DEFAULT SOURCE in PC/II+dx		PC/104 BUS		COM3 & COM4 (NOTE 6)	ETHERNET (NOTE 7)
	SOURCE COMP.	DESCRIPTION	CONNECTOR PIN	PC/104 BUS NOTES		
IRQ0	ACC2089	TIMER 0	-			
IRQ1	ACC2089	Integrated KEYBOARD	-			
IRQ2	ACC2089	Cascade to Int Controller 2	-			
IRQ3	ACC2089	Integrated COM2	-	1		
IRQ4	ACC2089	Integrated COM1	-	1		
IRQ5	-	-	J001.B23		COM3/4	ETHERNET
IRQ6	ACC2089	Integrated FDC	-	1		
IRQ7	ACC2089	Integrated LPT1	J001.B21		COM3/4	
IRQ8	DS1685	Real Time Clock – Timer/Alarm	-		COM3/4	
IRQ9	-	-	J001.B4		COM3/4	ETHERNET
IRQ10	CS8900	ETHERNET (IRQs 5,9,10)	J002.D3	3, 5	COM3/4	ETHERNET
IRQ11	AIC6360	SCSI	J002.D4	3, 5	COM3/4	
IRQ12	ACC2089	Integrated PS/2 MOUSE	-	1		
IRQ13	-	(Numeric Coprocessor)	-			
IRQ14	ACC2089	Integrated IDE	J002.D7	2, 5		
IRQ15	-	-	J002.D6			

NOTES

[1] Not available on PC/104 bus;
IRQ12 is dedicated to the on-board keyboard controller (Mouse device).
IRQ3 and IRQ4 are dedicated to the ACC2089 serial channels COM1 and COM2.
IRQ6 is dedicated to the ACC2089 floppy disk controller.

[2] IRQ14 is available on the PC/104 bus when IDE has been disabled within the ACC2089 controller.

[3] IRQ10 and IRQ11 are available on the PC/104 bus when ETHERNET and SCSI options, respectively, are not installed or have been assigned another IRQ for their use.

[4] Interrupt request numbers are enumerated from 0 through 15 per the conventional AT standard. Interrupt request levels are numbered 0 through 7 in each physical 8259A interrupt controller. The interrupt controllers are tied together through interrupt level 2 of control #1 (that is, interrupt pending requests are presented from interrupt controller #2 to level 2 of interrupt controller #1). The physical implementation of interrupt controllers is internal to the ACC 2089. This implementation mirrors the implementation of two 8259A controllers, so that the interface is identical to the AT standard. When an interrupt is pending for IRQ8–IRQ15, the interrupt is in-service in both controllers, in controller #1 at level 2, and controller #2 at level 0–7; both controllers are normally acknowledged after service completes to clear the pending interrupt, per the standard AT standard.

[5] Requires verification by megatel for your particular configuration.

[6] COM3 & COM4 are supported by the National 97338 Plug&Play functionality; interrupts noted are least likely to cause conflicts in typical PC/II+dx configurations.

[7] ETHERNET is supported by the configuration utility for the CS8900. For more information contact megatel engineering.

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7.4 DMA Channel Map

Table 24 DMA Map

DMA REQ. NUMBER (NOTE 1)	DEFAULT SOURCE in PC/II+dx		PC/104 BUS		COM4 (PnP) (NOTE 3)	ETHERNET (NOTE 4,5)
	SOURCE	DESCRIPTION	CONNECTOR PIN	PC/104 BUS NOTES		
DRQ0			J002.D9		COM4	-
DRQ1			J001.B18		COM4	-
DRQ2	ACC2089	Integrated FDC		2	-	-
DRQ3			J001.B16		COM4	-
DRQ4	ACC2089	Cascade	-		-	-
DRQ5			J002.D11		-	ETHERNET
DRQ6	AIC6360	SCSI	J002.D13	5	-	ETHERNET
DRQ7			J002.D15		-	ETHERNET

NOTES
[1] DMA request numbers are enumerated from 0 through 7 per the conventional AT standard. Two DMA controllers, the first containing four 8-bit channels (0–3 - DRQ0–DRQ3) is cascaded to channel 0 of the second controller (DRQ4). Controller #2 contains four 16-bit channels.
[2] DRQ2 is dedicated to the ACC2089 Floppy Controller.
[3] DRQ0, DRQ1 & DRQ3 are supported by the National 97338 Plug&Play functionality; DMA requests noted are least likely to cause conflicts in typical PC/II+dx configurations. Contact megatel for assistance on using these DMA requests on COM4.
[4] ETHERNET is supported by the configuration utility for the CS8900. For more information contact megatel engineering.
[5] DRQ6 is available on the PC/104 bus when SCSI option is not installed or SCSI has been configured not to use the DMA channel.
[6] Requires verification by megatel for your particular configuration.

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8 Connector Pinouts

This section contains pinout and signal description details for each connector on the PC/II+dx.

These connectors are described,

J001,J002 – PC/104 Connectors AB and CD
J003,J004 – Mass I-O Connectors (165-pin 2-mm 5X33 grid)
  J003,J004 Mass I/O J003 – Power
  J003,J004 Mass I/O J004 – Power & Miscellaneous
  J003,J004 Mass I/O J003 – IDE Interface
  J003,J004 Mass I/O J004 – Serial COM1 Interface
  J003,J004 Mass I/O J004 – Serial COM2 Interface
  J003,J004 Mass I/O J004 – Serial COM3 Interface
  J003,J004 Mass I/O J004 – Serial COM4 Interface
  J003,J004 Mass I/O J004 – Floppy Disk Interface
  J003,J004 Mass I/O J004 – Keyboard Interface
  J003,J004 Mass I/O J004 – Panel Interface
  J003,J004 Mass I/O J004 – Mouse Interface
  J003,J004 Mass I/O J004 – Reset Interface
  J003,J004 Mass I/O J004 – PC Speaker Output Interface
  J003,J004 Mass I/O J004 – Parallel LPT1 Interface
  J003,J004 Mass I/O J003 – SCSI Bus Interface
  J003,J004 Mass I/O J003 – Video CRT Interface
J005 – Ethernet Connector (2X5)
J007 – +5V Power Connector (1X12)
J008 – Fan Connector
J009 – +3.3V Power Connector (1X5)

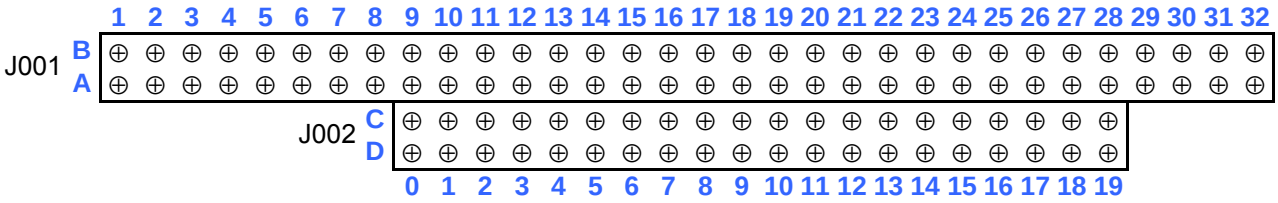
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8.1 J001, J002 – PC/104 Connectors AB and CD

The PC/II+dx board supports a 64-pin (2x32) PC/104 AB Bus connector (J001), and a 40-pin (2x20) PC/104 CD Bus connector (J002).

Please refer to the PC/104 Specification document for a complete description of these connectors; see the reference documents section 2.3.

Figure 4 Diagram – PC/104 J001(A–B), J002 (C–D) – 2X32, 2X20 .100" Header



NOTES
1. *Top (component) view is shown.*
2. *J001 numbering begins with 1, but J002 numbering begins with 0 (per PC/104 spec...)*
3. *J001 top row (as shown) is labelled "A", but J002 top row is labelled "C" (per PC/104 spec...)*
4. *Grid spacing in X-Y direction is .100 inch; Grid spacing between J001-A and J002-C is .100 inch.*

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Table 25 Pinout – PC/104 J001 (Rows A and B) – 2 X 32 .100" Header

PIN GROUP [1,3]	PIN [2]	ROW A	ROW B
PC104 – AB	1	IOCHCHK*	0V
PC104 – AB	2	SD7	RESETDRV
PC104 – AB	3	SD6	+5V
PC104 – AB	4	SD5	IRQ9
PC104 – AB	5	SD4	-5V
PC104 – AB	6	SD3	DRQ2
PC104 – AB	7	SD2	-12V
PC104 – AB	8	SD1	ENDXFR*
PC104 – AB	9	SD0	+12V
PC104 – AB	10	IOCHRDY	(KEY) [3]
PC104 – AB	11	AEN	SMEMW*
PC104 – AB	12	SA19	SMEMR*
PC104 – AB	13	SA18	IOW*
PC104 – AB	14	SA17	IOR*
PC104 – AB	15	SA16	DACK3*
PC104 – AB	16	SA15	DRQ3
PC104 – AB	17	SA14	DACK1*
PC104 – AB	18	SA13	DRQ1
PC104 – AB	19	SA12	REFRESH*
PC104 – AB	20	SA11	SYSCLK
PC104 – AB	21	SA10	IRQ7
PC104 – AB	22	SA9	IRQ6
PC104 – AB	23	SA8	IRQ5
PC104 – AB	24	SA7	IRQ4
PC104 – AB	25	SA6	IRQ3
PC104 – AB	26	SA5	DACK2*
PC104 – AB	27	SA4	TC
PC104 – AB	28	SA3	BALE
PC104 – AB	29	SA2	+5V
PC104 – AB	30	SA1	OSC
PC104 – AB	31	SA0	0V
PC104 – AB	32	0V	0V

NOTES
[1] Refer to the PC/104 Specification.
[2] Pin numbering complies with the PC/104 Specification, which is also used on the PC/II+dx board. Refer to the connector diagram in this section.
[3] Rows C and D are not required on 8-bit modules. B10 and C19 are key locations. Signal timing and function are as specified in the P996 Specification. Signal source/sink currents differ from P996 values.

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Table 26 Pinout – PC/104 J002 (Rows C and D) – 2 X 20 .100" Header

PIN GROUP [1,3]	PIN [2]	ROW C	ROW D
PC104 – CD	0	**0V**	**0V**
PC104 – CD	1	**SBHE***	**MEMCS16***
PC104 – CD	2	**LA23**	**IOCS16***
PC104 – CD	3	**LA22**	**IRQ10**
PC104 – CD	4	**LA21**	**IRQ11**
PC104 – CD	5	**LA20**	**IRQ12**
PC104 – CD	6	**LA19**	**IRQ15**
PC104 – CD	7	**LA18**	**IRQ14**
PC104 – CD	8	**LA17**	**DACK0***
PC104 – CD	9	**MEMR***	**DRQ0**
PC104 – CD	10	**MEMW***	**DACK5***
PC104 – CD	11	**SD8**	**DRQ5**
PC104 – CD	12	**SD9**	**DACK6***
PC104 – CD	13	**SD10**	**DRQ6**
PC104 – CD	14	**SD11**	**DACK7***
PC104 – CD	15	**SD12**	**DRQ7**
PC104 – CD	16	**SD13**	**+5V**
PC104 – CD	17	**SD14**	**MASTER***
PC104 – CD	18	**SD15**	**0V**
PC104 – CD	19	**(KEY)** [3]	**0V**

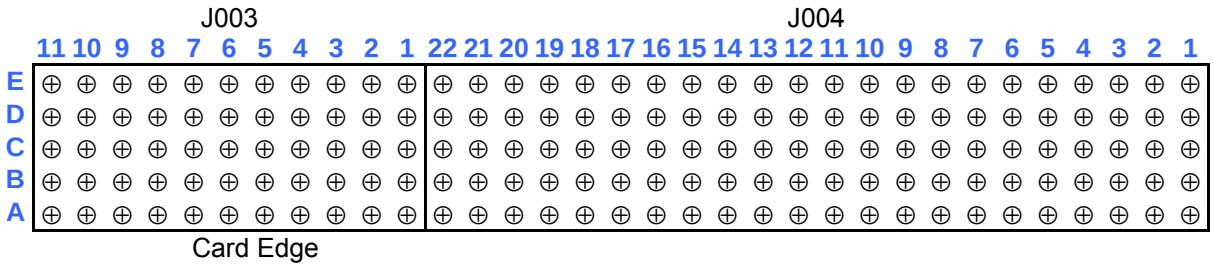
NOTES
[1] Refer to the PC/104 Specification.
[2] Pin numbering complies with the PC/104 Specification, which is also used on the PC/II+dx board. Refer to the connector diagram in this section.
[3] Rows C and D are not required on 8-bit modules. B10 and C19 are key locations. Signal timing and function are as specified in the P996 Specification. Signal source/sink currents differ from P996 values.

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8.2 J003, J004 – Mass I/O Connector

All peripheral I/O, with the exception of Ethernet (J005), is pulled from the PC/II+dx board to a 5 X 33 2mm grid Mass I/O Connector. The Mass I/O Connector is normally provided using two separate connectors, J003, a 5 X 11 2mm connector, and J004, a 5 X 22 2mm connector. The PC/II+dx board can be ordered with either, both or none of these two connectors installed, although both would be installed in a typical case. In addition, the PC/II+dx board can be shipped with any combination of user-specified 2mm headers.

Figure 5 Diagram – MASS I/O J003, J004 (Rows A–E) – 5X11, 5X22 2mm HM Connector



NOTES

[1] Top (component) view is shown. This is the view when facing a either a straight connector from the top, or a right-angle connector facing the outer side (the mating side).

Table 27 Pinout – MASS I/O J003 (Rows A, B, C, D and E) – 5 X 11 2mm HM Connector

PIN GROUP	POS	ROW e	ROW d	ROW c	ROW b	ROW a
V1–VIDEO1 – CRT1	1	V1-R	V1-G	V1-B	V1-HSYNC	V1-VSYNC
A1–IDE1	2	A1-DD7	A1-DD8	A1-DD6	A1-DD9	A1-DD5
A1–IDE1	3	A1-DD10	A1-DD4	A1-DD11	A1-DD3	A1-DD12
A1–IDE1	4	A1-DD2	A1-DD13	A1-DD1	A1-DD14	A1-DD0
A1–IDE1	5	A1-DD15	A1-DMARQ	A1-DIOW#	A1-DIOR#	A1-IORDY
A1–IDE1	6	A1-DMACK#	A1-INTRQ	A1-IOCS16#	A1-DA1	A1-DA0
A1–IDE1 S1–SCSI	7	A1-DA2	A1-CS0#	A1-CS1#	S1-REQ#	S1-MSG#
S1–SCSI	8	S1-C/D#	S1-I/O#	S1-RST#	S1-ATN#	S1-AKN#
S1–SCSI	9	S1-BSY#	S1-SEL#	S1-DP#	S1-D0#	S1-D1#
S1–SCSI	10	S1-D2#	S1-D3#	S1-D4#	S1-D5#	S1-D6#
POWER	11	S1-D7#	GND	GND	+5V	+5V

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Table 28 Pinout – MASS I/O J004 (Rows A, B, C, D and E) – 5 X 22 2mm HM Connector

PIN GROUP	POS	ROW e	ROW d	ROW c	ROW b	ROW a
L1–PANEL	1	L1-PD23	L1-PD22	GND	L1-PD21	+5V
L1–PANEL	2	L1-PD20	L1-PD19	L1-PD18	L1-PD17	L1-PD16
L1–PANEL	3	L1-PD15	L1-PD14	L1-PD13	L1-PD12	L1-PD11
L1–PANEL	4	L1-PD10	L1-PD9	L1-PD8	L1-PD7	L1-PD6
L1–PANEL	5	L1-PD5	L1-PD4	L1-PD3	L1-PD2	L1-PD1
L1–PANEL	6	L1-PD0	L1-SHFCLK	L1-LP	L1-FLM	L1-ENAVEE
L1–PANEL MS–SPEAKER	7	L1-ENAVDD	L1-M	L1-ACT	L1-ENABKL	MS-SPKOUT
MR–RESET MISCELLANEOUS K1–KEYBOARD	8	MR-RSTSW	PWRGOOD	K1-DAT	K1-CLK	+3.3V
M1–MOUSE P1–PARALLEL1 LPT1	9	M1-DAT	M1-CLK	P1-STB#	P1-AFD#	P1-D0
P1–PARALLEL1 LPT1	10	P1-ERR#	P1-D1	P1-INIT#	P1-D2	P1-SLIN#
P1–PARALLEL1 LPT1	11	P1-D3	P1-D4	P1-D5	P1-D6	P1-D7
P1–PARALLEL1 LPT1 C1–SERIAL1 COM1	12	P1-AKN#	P1-BUSY	P1-PE	P1-SLCT	C1-DCD
C1–SERIAL1 COM1	13	C1-DSR	C1-RXD	C1-RTS	C1-TXD	C1-CTS
C1–SERIAL1 COM1 C2–SERIAL2 COM2	14	C1-DTR	C1-RI	C2-DCD	C2-DSR	C2-RXD
C2–SERIAL2 COM2	15	C2-RTS	C2-TXD	C2-CTS	C2-DTR	C2-RI
C3–SERIAL3 COM3	16	C3-DCD	C3-DSR	C3-RXD	C3-RTS	C3-TXD
C3–SERIAL3 COM3 C4–SERIAL4 COM4	17	C3-CTS	C3-DTR	C3-RI	C4-DCD	C4-DSR
C4–SERIAL4 COM4	18	C4-RXD	C4-RTS	C4-TXD	C4-CTS	C4-DTR
C4–SERIAL4 COM4	19	C4-RI	Rsvd	Rsvd	Rsvd	Rsvd
F1–FLOPPY1	20	F1-DENSL0#	F1-INDEX#	F1-MTR0#	F1-DS1#	F1-DS0#
F1–FLOPPY1	21	F1-MTR1#	F1-DIR#	F1-STEP#	F1-WDATA#	F1-WGATE#
F1–FLOPPY1	22	F1-TRK0#	F1-WP#	F1-RDATA#	F1-HDSEL#	F1-DKCHG#

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8.2.1 J003,J004 Mass I/O J003 – Power

Table 29 Signals – Mass I/O J003 – Power

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	b11	+5V	+5v (sourced by CPU board to QTB)
+5V	a11	+5V	+5v (sourced by CPU board to QTB)
GND	d11	Ground	Ground
GND	c11	Ground	Ground

8.2.2 J003,J004 Mass I/O J004 – Power & Miscellaneous

Table 30 Signals – Mass I/O J004 – Power & Miscellaneous

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+3.3V	a8	+3.3v	+3.3v (sourced by CPU board to QTB)
+5V	a1	+5V	+5v (sourced by CPU board to QTB)
GND	c1	Ground	Ground
PWRGOOD	J004 – d8	Power Good	This signal is the Power Good output signal. It pulses low for 200 ms (typical, minimum 130 ms) when triggered by RSTSW# or by a Watchdog Timer Expired event, and it remains low whenever VCC is below the reset threshold or when the RSTSW# signal input is a logic low. This output signal remains low for 200ms (typical, minimum 130 ms) after one of the following occurs: VCC rises above the reset threshold, the watchdog triggers a reset, or the RSTSW# input signal goes low to high.

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8.2.3 J003,J004 Mass I/O J003 – IDE Interface

Table 31 Signals – Mass I/O J003 – IDE Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
A1-DA0	a6	Address Bus 0	This signal is Address Bit 0 of the ATA Address Bus that is connected to IDE Channel.
A1-DA1	b6	Address Bus 1	This signal is Address Bit 1 of the ATA Address Bus that is connected to IDE Channel.
A1-DA2	e7	Address Bus 2	This signal is Address Bit 2 of the ATA Address Bus that is connected to IDE Channel.
A1-CS0#	d7	Chip Select 1 for Ch 0	This is the Chip Select 1 command output pin to enable the IDE device to watch the Read/Write Command.
A1-CS1#	c7	Chip Select 3 for Ch 1	This is the Chip Select 3 command output pin to enable the IDE device to watch the Read/Write Command.
A1-DD0	a4	Data Bus 0	This signal is Data Bit 0 of the Data Bus that is connected to IDE Channel.
A1-DD1	c4	Data Bus 1	This signal is Data Bit 1 of the Data Bus that is connected to IDE Channel.
A1-DD2	e4	Data Bus 2	This signal is Data Bit 2 of the Data Bus that is connected to IDE Channel.
A1-DD3	b3	Data Bus 3	This signal is Data Bit 3 of the Data Bus that is connected to IDE Channel.
A1-DD4	d3	Data Bus 4	This signal is Data Bit 4 of the Data Bus that is connected to IDE Channel.
A1-DD5	a2	Data Bus 5	This signal is Data Bit 5 of the Data Bus that is connected to IDE Channel.
A1-DD6	c2	Data Bus 6	This signal is Data Bit 6 of the Data Bus that is connected to IDE Channel.
A1-DD7	e2	Data Bus 7	This signal is Data Bit 7 of the Data Bus that is connected to IDE Channel.
A1-DD8	d2	Data Bus 8	This signal is Data Bit 8 of the Data Bus that is connected to IDE Channel.
A1-DD9	b2	Data Bus 9	This signal is Data Bit 9 of the Data Bus that is connected to IDE Channel.
A1-DD10	e3	Data Bus 10	This signal is Data Bit 10 of the Data Bus that is connected to IDE Channel.
A1-DD11	c3	Data Bus 11	This signal is Data Bit 11 of the Data Bus that is connected to IDE Channel.
A1-DD12	a3	Data Bus 12	This signal is Data Bit 12 of the Data Bus that is connected to IDE Channel.
A1-DD13	d4	Data Bus 13	This signal is Data Bit 13 of the Data Bus that is connected to IDE Channel.

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
A1-DD14	b4	Data Bus 14	This signal is Data Bit 14 of the Data Bus that is connected to IDE Channel.
A1-DD15	e5	Data Bus 15	This signal is Data Bit 15 of the Data Bus that is connected to IDE Channel.
A1-DIOR#	b5	IO Read Command	This signal is the IOR command output pin to notify the IDE device to assert the Read Data.
A1-DIOW#	c5	IO Write Command	This signal is the IOW command output pin to notify the IDE device that the available Write Data is already asserted by the onboard IDE controller.
A1-DMACK#	e6	DACK for IDE Master	This is the output pin to grant the IDE Channel DMA request to begin the IDE Master Transfer. Use of this signal depends upon the type of board.
A1-DMARQ	d5	DMA Request for IDE Master	This is the input pin from the IDE Channel DMA request to do the IDE Master Transfer. Use of this signal depends upon the type of board.
A1-IOCS16#	c6	Device 16-Bit I-O	This is the input pin from the IDE device which, during PIO transfer modes 0, 1 or 2, indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
A1-IORDY	a5	IDE Ready	This is the input pin from the IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
A1-INTRQ	d6	IDE Interrupt	This is the input pin from the IDE Channel to signal an interrupt. It will be routed to the appropriate Int 14 8259 interrupt controller input. Depending upon the board type, this input may be steerable to other interrupt levels.

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8.2.4 J003,J004 Mass I/O J004 – Serial COM1 Interface

Table 32 Signals – Mass I/O J004 – Serial COM1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C1-CTS	a13	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C1-DCD	a12	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C1-DSR	e13	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit-5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C1-DTR	e14	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C1-RI	d14	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C1-RTS	c13	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C1-RXD	d13	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C1-TXD	b13	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

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8.2.5 J003,J004 Mass I/O J004 – Serial COM2 Interface

Table 33 Signals – Mass I/O J004 – Serial COM2 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C2-CTS	c15	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C2-DCD	c14	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C2-DSR	b14	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit-5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C2-DTR	b15	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C2-RI	a15	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C2-RTS	e15	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C2-RXD	a14	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C2-TXD	d15	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

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8.2.6 J003,J004 Mass I/O J004 – Serial COM3 Interface

Table 34 Signals – Mass I/O J004 – Serial COM3 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C3-CTS	e17	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C3-DCD	e16	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C3-DSR	d16	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit-5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C3-DTR	d17	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C3-RI	c17	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C3-RTS	b16	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C3-RXD	c16	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C3-TXD	a16	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

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8.2.7 J003,J004 Mass I/O J004 – Serial COM4 Interface

Table 35 Signals – Mass I/O J004 – Serial COM4 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C4-CTS	b18	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C4-DCD	b17	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C4-DSR	a17	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit-5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C4-DTR	a18	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C4-RI	e19	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C4-RTS	d18	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C4-RXD	e18	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C4-TXD	c18	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

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8.2.8 J003,J004 Mass I/O J004 – Floppy Disk Interface

Table 36 Signals – Mass I/O J004 – Floppy Disk Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
F1-DENSL0#	e20	Density Select	This signal Indicates whether a low (250/300 Kbit/sec) or high (500/1000 Kbit/sec) data rate has been selected.
F1-DIR#	d21	Direction	This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
F1-DKCHG#	a22	Disk Change	This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
F1-DS0#	a20	Drive Select 0	Active low, output selects drive 0.
F1-DS1#	b20	Drive Select 1	Active low, output selects drive 1.
F1-HDSEL#	b22	Head Select	This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
F1-INDEX#	d20	Index Status	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
F1-MTR0#	c20	Motor On 0	Active-low output selects motor drive 0.
F1-MTR1#	e21	Motor On 1	Active-low output selects motor drive 1.
F1-RDATA#	c22	Read Serial Data	This active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
F1-STEP#	c21	Step Head	This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
F1-TRK0#	e22	Track 00	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.
F1-WDATA#	b21	Write Serial Data	This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
F1-WGATE#	a21	Write Gate	This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
F1-WP#	d22	Write Protected Status	This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.

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8.2.9 J003,J004 Mass I/O J004 – Keyboard Interface

Table 37 Signals – Mass I/O J004 – Keyboard Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
K1-CLK	b8	Keyboard Clock	This output is the keyboard interface clock.
K1-DAT	c8	Keyboard Data	This input is the keyboard serial data line.

8.2.10 J003,J004 Mass I/O J004 – Panel Interface

Table 38 Signals – Mass I/O J004 – Panel Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
L1-ACTI	c7	Activity Indicator	(ACTI or A26 or GP0 or DDAT or CS) This signal is the Activity Indicator output. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). I/O.
L1-ENABKL	b7	Enable Backlight	(ENBKL or A27 or GP1 or DCLK or CS) This signal is the Enable Backlight output signal. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). (Chips Revision 1.5 10/14/97 65550 Subject to Change without Notice). I/O.
L1-ENAVDD	e7	Enable VDD	Power sequencing controls for panel driver electronics voltage VDD. I/O.
L1-ENAVEE	a6	Enable VEE	(ENAVEE or ENABKL) Power sequencing controls for panel LCD bias voltage VEE, I/O. The polarity of this signal can be selected by option "d" - either active low or active high – see section 10.2.17.
L1-FLM	b6	First Line Marker	Flat Panel equivalent of VSYNC. Active high. Output.
L1-FPD0	e6	Data Output P0	Flat panel data output P0. Active high. Output.
L1-FPD1	a5	Data Output P1	Flat panel data output P1. Active high. Output.
L1-FPD2	b5	Data Output P2	Flat panel data output P2. Active high. Output.
L1-FPD3	c5	Data Output P3	Flat panel data output P3. Active high. Output.
L1-FPD4	d5	Data Output P4	Flat panel data output P4. Active high. Output.
L1-FPD5	e5	Data Output P5	Flat panel data output P5. Active high. Output.
L1-FPD6	a4	Data Output P6	Flat panel data output P6. Active high. Output.
L1-FPD7	b4	Data Output P7	Flat panel data output P7. Active high. Output.
L1-FPD8	c4	Data Output P8	Flat panel data output P8. Active high. Output.
L1-FPD9	d4	Data Output P9	Flat panel data output P9. Active high. Output.
L1-FPD10	e4	Data Output P10	Flat panel data output P10. Active high. Output.
L1-FPD11	a3	Data Output P11	Flat panel data output P11. Active high. Output.
L1-FPD12	b3	Data Output P12	Flat panel data output P12. Active high. Output.
L1-FPD13	c3	Data Output P13	Flat panel data output P13. Active high. Output.
L1-FPD14	d3	Data Output P14	Flat panel data output P14. Active high. Output.

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
L1-FPD15	e3	Data Output P15	Flat panel data output P15. Active high. Output.
L1-FPD16	a2	Data Output P16	Flat panel data output P16. Active high. Output.
L1-FPD17	b2	Data Output P17	Flat panel data output P17. Active high. Output.
L1-FPD18	c2	Data Output P18	Flat panel data output P18. Active high. Output.
L1-FPD19	d2	Data Output P19	Flat panel data output P19. Active high. Output.
L1-FPD20	e2	Data Output P20	Flat panel data output P20. Active high. Output.
L1-FPD21	b1	Data Output P21	Flat panel data output P21. Active high. Output.
L1-FPD22	d1	Data Output P22	Flat panel data output P22. Active high. Output.
L1-FPD23	e1	Data Output P23	Flat panel data output P23. Active high. Output.
L1-LP	c6	Latch Pulse	Flat Panel equivalent of HSYNC. Active high. Output.
L1-M	d7	M signal	This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.
L1-SHFCLK	d6	Shift Clock	(SHFCLK or CL2 or SHFCLKL) This signal is the pixel clock for flat panel data. Active high. Output.

8.2.11 J003,J004 Mass I/O J004 – Mouse Interface

Table 39 Signals – Mass I/O J004 – Mouse Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
M1-CLK	d9	Mouse Clock	This output is the PS2 Mouse clock.
M1-DAT	e9	Mouse Data	This input is the mouse serial data line.

8.2.12 J003,J004 Mass I/O J004 – Reset Interface

Table 40 Signals – Mass I/O J004 – Reset Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
MR-RSTSW#	e8	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. A logic low on this signal asserts system reset. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 130ms) after this signal returns high. The active-low input has an internal 52 kΩ pull-up resistor. It can be driven from a CMOS-logic line or shorted to ground with a switch. Leave open or connect to VCC (+5V) if unused.

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8.2.13 J003,J004 Mass I/O J004 – PC Speaker Output Interface

Table 41 Signals – Mass I/O J004 – PC Speaker Output Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
MS-SPKROUT	a7	Speaker Output	This signal is used to control the Speaker Output and should connect to the Speaker.

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8.2.14 J003,J004 Mass I/O J004 – Parallel LPT1 Interface

Table 42 Signals – Mass I/O J004 – Parallel LPT1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
P1-AFD#	b9	Autofeed Output	This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
P1-AKN#	e12	Acknowledge	This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the PACK# input.
P1-BUSY	d12	Busy	This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
P1-D0	a9	Port Data – Bit0	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D1	d10	Port Data – Bit1	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D2	b10	Port Data – Bit2	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D3	e11	Port Data – Bit3	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D4	d11	Port Data – Bit4	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D5	c11	Port Data – Bit5	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D6	b11	Port Data – Bit6	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D7	a11	Port Data – Bit7	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-ERR#	e10	Error	This active low signal indicates an error condition at the printer.
P1-INIT#	c10	Initiate Output	This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
P1-PE	c12	Paper End	This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
P1-SLCT	b12	Printer Selected Status	This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
P1-SLIN#	a10	Printer select input	This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
P1-STB#	c9	Strobe Output	This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.

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8.2.15 J003,J004 Mass I/O J003 – SCSI Bus Interface

Table 43 Signals – Mass I/O J003 – SCSI Bus Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-AKN#	a8	Acknowledge	A signal driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
S1-ATN#	b8	Attention	A signal driven by an initiator to indicate the ATTENTION condition.
S1-BSY#	e9	Busy	An "OR-tied" signal that indicates that the bus is being used. It may be driven by all SCSI devices that are actually arbitrating during Arbitration, driven by the initiator, target or both during Selection & Reselection, or driven by the target during all other phases.
S1-C/D#	e8	Control/Data	A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.
S1-D0#	b9	Data Bus Bit Signal 0	Data bit signal 0. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. S1-D1# thru S1-D8# define eight data-bit signals. Together with the S1-DP# a parity-bit signal, they form a DATA BUS. S1-D7# is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to S1-D0#.
S1-D1#	a9	Data Bus Bit Signal 1	Data bit signal 1. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D2#	e10	Data Bus Bit Signal 2	Data bit signal 2. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D3#	d10	Data Bus Bit Signal 3	Data bit signal 3. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D4#	c10	Data Bus Bit Signal 4	Data bit signal 4. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D5#	b10	Data Bus Bit Signal 5	Data bit signal 5. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D6#	a10	Data Bus Bit Signal 6	Data bit signal 6. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-D7#	e11	Data Bus Bit Signal 7	Data bit signal 7. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-DP#	c9	Data Bus Parity	Data parity bit signal. Parity is Odd. Parity is undefined during the ARBITRATION phase. See S1-D0#.
S1-I/O#	d8	Input/Output	A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.
S1-MSG#	a7	Message	A signal driven by a target during the MESSAGE phase.
S1-REQ#	b7	Request	A signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.
S1-RST#	c8	Reset	An "OR-tied" signal that indicates the RESET condition. The RST signal may be asserted by any SCSI device at any time.
S1-SEL#	d9	Select	An "OR-tied" signal used by an initiator to select a target or by a target to reselect an initiator. NOTE: The SEL signal was not defined as "OR-tied" in SCSI-1. It has been defined as "OR-tied" in SCSI-2. This does not cause an operational problem in mixing SCSI-1 and SCSI-2 devices.

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8.2.16 J003,J004 Mass I/O J003 – Video CRT Interface

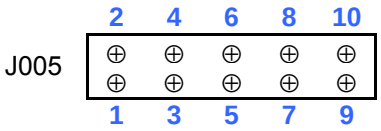
Table 44 Signals – Mass I/O J003 – Video CRT Display Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
V1-B	c1	CRT Blue	This Active High output signal is the BLUE CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-G	d1	CRT Green	This Active High output signal is the GREEN CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-HSYNC	b1	Horizontal Sync	(HSYNC or CSYNC) This Active High/Low output signal is the CRT Horizontal Sync (polarity is programmable) or the "Composite Sync" for support of various external NTSC/PAL encoder chips. Note CSYNC can be set to output on the L1-ACTI pin (Mass I/O pin B - c7) or the L1-ENABKL pin (Mass I/O pin B - b7).
V1-R	e1	CRT Red	This Active High output signal is the RED CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-VSYNC	a1	Vertical Sync	(VSYNC or VISINT) This Active High/Low output signal is the CRT Vertical Sync (polarity is programmable) or "VSync Interval" for support of various external NTSC/PAL encoder chips.

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8.3 J005 – Ethernet Connector

Figure 6 Diagram – Ethernet J005 – 2x5 Pin .100 Inch R/A Male Header



NOTES
1 Top (component) view is shown.

Table 45 Pinout – Ethernet J005 – 2x5 Pin .100 Inch R/A Male Header

PIN GROUP	PIN#	PIN NAME
E2–ETHERNET2 AUI	1	**E2-CLSN-**
E2–ETHERNET2 AUI	2	**E2-CLSN+**
E1–ETHERNET1 10BASE-T	3	**E1-RD-**
E1–ETHERNET1 10BASE-T	4	**E1-RD+**
E2–ETHERNET2 AUI	5	**E2-RCV-**
E2–ETHERNET2 AUI	6	**E2-RCV+**
E1–ETHERNET1 10BASE-T	7	**E1-TD-**
E1–ETHERNET1 10BASE-T	8	**E1-TD+**
E2–ETHERNET2 AUI	9	**E2-TRMT-**
E2–ETHERNET2 AUI	10	**E2-TRMT+**

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Table 46 Signals – Ethernet J005 – 10Base-T Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E1-TD-	7	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 11. Connect to external RJ45 connector Pin 2.
E1-TD+	8	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 9. Connect to external RJ45 connector Pin 1.
E1-RD-	3	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 16. Connect to external RJ45 connector Pin 6.
E1-RD+	4	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 14. Connect to external RJ45 connector Pin 3.

Table 47 Signals – Ethernet J005 – AUI Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E2-CLSN-	1	Negative Collision In	Negative Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 13. Connect to external DB15 connector Pin 9.
E2-CLSN+	2	Positive Collision In	Positive Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 10. Connect to external DB15 connector Pin 2.
E2-TRMT-	9	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 16. Connect to external DB15 connector Pin 10.
E2-TRMT+	10	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 15. Connect to external DB15 connector Pin 3.
E2-RCV-	5	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 10. Connect to external DB15 connector Pin 12.
E2-RCV+	6	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 9. Connect to external DB15 connector Pin 5.

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8.4 J007 – +5V Power Connector

This connector is used to connect the PC/II+dx board to an external +5V supply.

Figure 7 Diagram – +5V POWER Connector J007 – 1x12 PIN .100" R/A Male Header



NOTES
[1] Top (component) view is shown.

Table 48 Pinout – +5V Connector RAIL J007 – 1x12 PIN .100" R/A Male Header

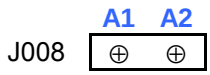
PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	1	**+5V**	+5v 5% sourced by off-board supply
+5V	2	**+5V**	+5v 5% sourced by off-board supply
+5V	3	**+5V**	+5v 5% sourced by off-board supply
GND/KEY	4	**GND/KEY**	Ground (or Key)
GND	5	**GND**	Ground
GND	6	**GND**	Ground
GND	7	**GND**	Ground
GND	8	**GND**	Ground
GND	9	**GND**	Ground
+5V	10	**+5V**	+5v 5% sourced by off-board supply
+5V	11	**+5V**	+5v 5% sourced by off-board supply
+5V	12	**+5V**	+5v 5% sourced by off-board supply

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8.5 J008 – Fan Connector

This connector is optional. It provides power only for an optional Cpu fan. The use of a Cpu fan is dependent upon the environment in which the PC/II+dxe is operating, and the speed at which the processor has been strapped.

Figure 8 Diagram – Optional Fan Connector J008 – 1x2 1.25mm Pitch Molex 53027-0210



NOTES
1 Top (component) view is shown.
2 Pitch is 1.25mm

Table 49 Signals – J008 – Fan Connector 1x2 1.25mm Molex 53057-0210

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	A1	**+5V**	+5V
GND	A2	**GND**	Ground

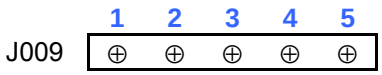
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8.6 J009 – +3.3V Power Connector

PC/II+dx supports dual external power supplies (+5V and +3.3V). This connector connects the PC/II+dx board to an external +3.3V supply.

This connector is optional. It is present when you order the dual supply power arrangement.

Figure 9 Diagram – +3.3v Power Header J009 – 1x5 PIN .100" Vertical Male Header



NOTES
[1] Top (component) view is shown.

Table 50 Pinout – +3.3v Power J009 – 1x15 PIN .100" Vertical Male Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+3.3V	1	**+3.3V**	+3.3v 5% sourced by off-board supply
GND/KEY	2	**GND/KEY**	Ground (or Key)
GND	3	**GND**	Ground
GND	4	**GND**	Ground
+3.3V	5	**+3.3V**	+3.3v 5% sourced by off-board supply

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9 Peripheral Attachment (QTB/dxp)

PC/II+dx and other megatel 104Family Cpu boards can be attached to peripherals by user-supplied cabling that mates directly with the on-board Mass I/O Connector and/.or Ethernet Header.

Megatel also provides an economical transition board set for this family of boards. The transition cards are compatible electrically with prior QTB boards, and pull all Cpu board signals to industry-standard connectors and headers.

The QTB/dxp transition board (shown on the left side in the picture below) mates side-by-side with the PC/II+dx, using both Mass I/O connectors (j003 and J004) and an optional cable from J005, the PC/II+dx Ethernet header. The PC/II+dx in this configuration uses the AMP Z-PACK right-angle receptacle (female) connectors for both J003 and J004; the QTB/dxp uses the plug (male) versions.



The QTB/dxp board is approximately 3.775 by 2.95 inches, and mates to the PC/II+dx on the long side.

Connectors provided on the QTB/dxp board can be user-specified and may include the following:

- Cpu board interface connectors
- Power
- Serial – 4 ports
- Parallel port
- LCD
- VGA
- Keyboard & Mouse
- Ethernet AUI
- Ethernet 10Base-T
- SCSI 26-pin and 50-pin
- IDE 40-pin (.100) and 44-pin (2mm)
- Floppy
- USB (unused)
- Miscellaneous

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The QTB/dxp also contains an active termination circuit for the SCSI bus, using Dallas Semiconductor DS2107 active terminators. Jumper JMP1 on the circuit board can be installed to remove the active terminator from the host end of the SCSI bus. This would be used to insert the host into the middle of the SCSI bus. Without the jumper installed, the host termination is active.

The following table summarizes the connectors and headers available on a QTB/dxp transition board. To obtain detailed information concerning the QTB/dxp board, please refer to the megatel QTB/dxp Technical Reference documentation.

Table 51 QTB/dxp Connector List

Ref	Connector / Header Description
J001	Mass I/O Board Connector – 5x22 AMP Z-PACK 2mm HM Right-angle plug (male)
J002	Mass I/O Board Connector – 5x11 AMP Z-PACK 2mm HM Right-angle plug (male)
J003	4-Pin System Power (+5v, Gnd, Gnd, N/C)
J004	COM1 Header – 10-pin 2x5 (0.100" pitch) Header
J005	COM2 Header – 10-pin 2x5 (0.100" pitch) Header
J006	COM3 Header – 10-pin 2x5 (0.100" pitch) Header
J006	COM4 Header – 10-pin 2x5 (0.100" pitch) Header
J008	LPT1 Parallel Port (Printer) Header – 26-Pin 2x13 (0.100" pitch) Header
J009	LCD Header – 36-pin 2x18 (0.100" pitch) Header
J010	Reset Switch – 3-Pin Standard Straight-Up or 4-pin Right-angle SPST Momentary Switch
J011	Keyboard Connector – MiniDIN6 PS/2-style Keyboard Connector (at edge of card)
J012	Mouse Connector – MiniDIN6 PS/2-style Mouse Connector (mounted at edge of card)
J013	Miscellaneous Header – 6-pin 1x6 (2mm pitch) Header
J014	VGA Monitor Connector – DE15 Female (mounted at edge of card)
J015	Ethernet AUI Power Connector – 4-pin (+12v,Gnd,Gnd,N/C)
J016	Ethernet AUI Header – 16-pin 2x8 (0.100" pitch) Header
J017	Ethernet 10Base-T Connector – RJ-45 Connector (mounted at edge of card)
J018	Ethernet Board Header – 10-pin 2x5 (0.100" pitch) Header
J019	SCSI Header – 26-pin 2x13 (0.100" pitch) Header
J020	SCSI Header – 50-pin 2x25 (0.100" pitch) Header
J021	IDE/ATA Header – 40-pin 2x20 (0.100" pitch) Header
J022	IDE/ATA Header – 44-pin 2x22 (2mm pitch) Header
J023	Floppy Connector – 34-pin 2x17 (0.100" pitch) Header
J024	USB Header (unused) – 8-pin 2x4 (0.100" pitch) Stacked Connector

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10 Ordering Information

The PC/II+dx may be ordered directly from Megatel or through one of our representatives.

Our goal is to provide an off-the-shelf solution that can be tailored to exactly match your requirements in the smallest most cost-effective package possible. And since all manufacturing and design work is performed in-house, it results in the fastest, most reliable lead times in the industry. It also allows Megatel to offer custom Engineering services for high volume applications. Inquire today!

First time buyers might opt to purchase one of our OEM development kits which includes all the necessary items to get started quickly.

Small quantity orders (1–4) are normally available within 2 weeks. For larger orders, please allow 4 to 6 weeks for delivery.

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10.1 PC/II+dx Product Numbering

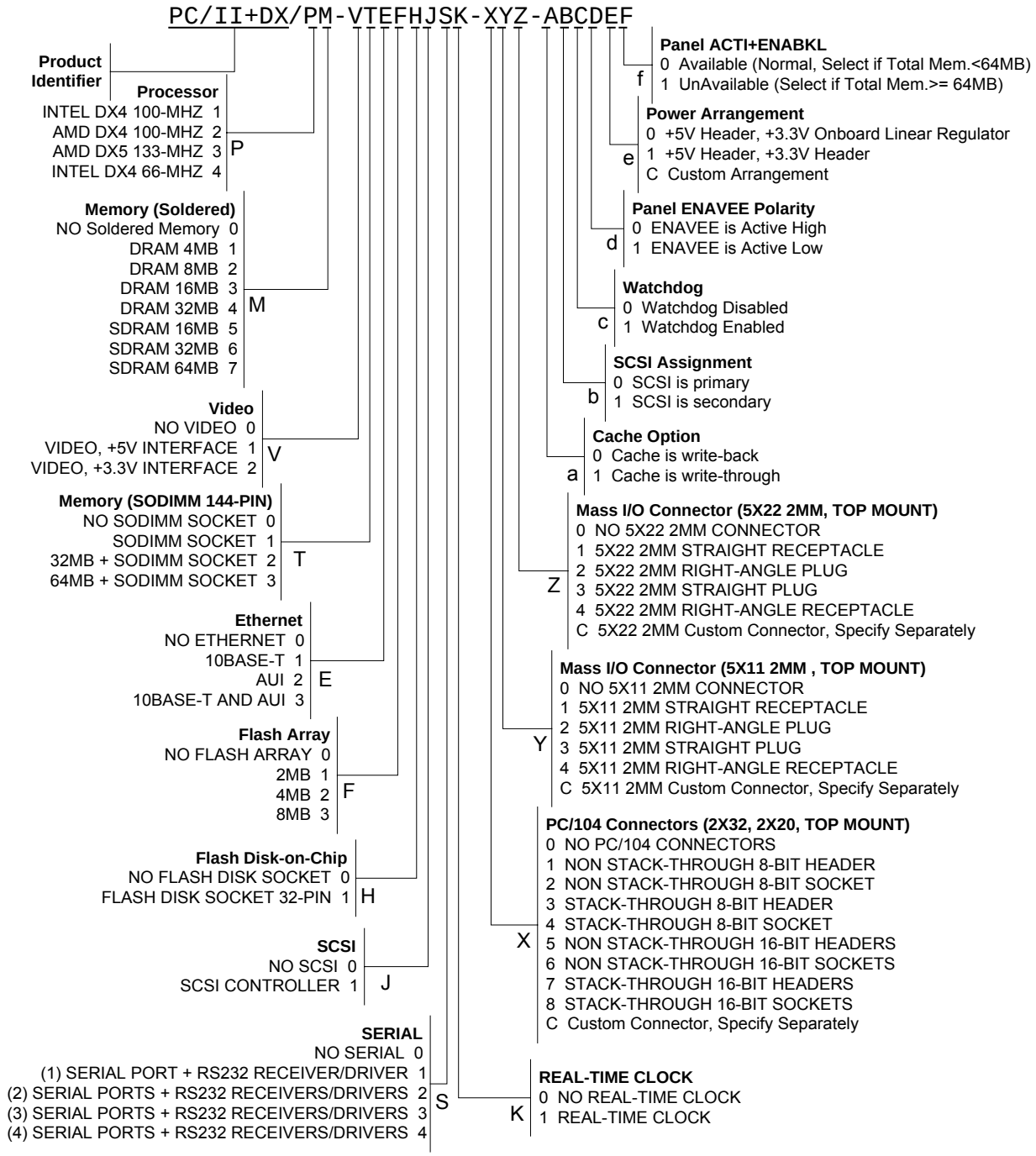


Figure 10 PC/II+dx Product Numbering (v1.33)

Example: PC/II+DX/34-10331141-544-001010

PC/II+dx board with DX5, 32MB soldered DRAM, Video, no SODIMM, Ethernet 10Base-T & AUI, 8MB Flash, Disk-on-Chip socket, 4 Serial ports, Real-Time Clock, Stack-through 16-bit PC/104 bus headers, right-angle female Mass I/O connectors, and with Write-back cache, a primary-configured SCSI controller, Watchdog enabling jumper installed, active high ENAVEE, dual power headers (+5V and +3.3V), and Panel ACTI and ENABKL are available on panel interface.

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10.2 PC/II+dx Order Options

NOTE: Features not included as options in this section are always shipped on every board. Options "Y" and "Z" will be required for any I-O feature to be used.

10.2.1 Processor – Code P

INTEL 100 MHZ DX4, soldered	1
AMD 100 MHZ DX4, soldered	2
AMD 133 MHZ DX5, soldered	3
INTEL 66 MHZ DX4	4

10.2.2 Main Memory – Code M

NO SOLDERED MEMORY	0
DRAM 4 MB, soldered	1
DRAM 8 MB, soldered	2
DRAM 16 MB, soldered	3
DRAM 32 MB, soldered	4
SDRAM 16 MB, soldered	5
SDRAM 32 MB, soldered	6
SDRAM 64 MB, soldered	7

10.2.3 Video – Code V

NO Video	0
Video Option with +5v panel & CRT interface, and with 2MB Video Memory; all video (both CRT and 24-bit panel interfaces) are pulled to the Mass I/O Connector	1
Same as option 1 but with +3.3v panel & CRT interface	2

NOTES: Interface voltage level option applies to CRT HSYNC & VSYNC, and to all panel control & data lines.

10.2.4 Memory (Sodimm 144-Pin) – Code T

No SODIMM Socket or Memory	0
SODIMM Socket for User-supplied SODIMM module, which supports either 32 MB or 32 MB SDRAM SODIMM 144-Pin module.	1
SODIMM Socket, and 32 MB	2
SODIMM Socket, and 64 MB SDRAM memory installed in on-board socket	3

NOTE
[1] Sodimm Socket requires selection of SDRAM Main Memory (M = 5, 6, or 7)

10.2.5 Ethernet – Code E

NO Ethernet	0
Ethernet 10BASE-T with Filters & Transformer	1
Ethernet AUI with Filters & Transformer	2
Ethernet 10BASE-T & AUI with Filters & Transformers	3

10.2.6 Flash Array – Code F

NO User Flash Array	0
2MB User Flash Array, soldered	1
4MB User Flash Array, soldered	2
8MB User Flash Array, soldered	3

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10.2.7 Flash Disk Socket – Code H

NO Flash Disk Socket	0
Flash Disk Socket for User-supplied Disk-on-Chip module	1

10.2.8 SCSI Bus – Code J

NO SCSI Bus	0
SCSI-2 Bus Controller; bus is brought out to MASS I/O connector; if required, QTB/dxp transition (connector) board can also be ordered to provide active termination of the bus	1

10.2.9 Serial Channels – Code S

NO Serial	0
(1) Serial Port with RS232 receiver/drivers	1
(2) Serial Ports with RS232 receivers/drivers	2
(3) Serial Ports with RS232 receivers/drivers	3
(4) Serial Ports with RS232 receivers/drivers	4

10.2.10 Real-Time Clock – Code K

NO Real-Time Clock; board's CMOS configuration is replaced by hard-coded BIOS configuration; contact Megatel for details on how to order hard-coded BIOS configuration	0
Real-Time Clock with Battery Backup is Installed; also provides standard CMOS BIOS configuration capability	1

10.2.11 PC/104 Connectors (J001,J002) – Code X

NO PC/104 Connector(s)	0
J001 PC/104-AB (8-Bit Bus) Header, non stack-through	1
J001 PC/104-AB (8-Bit Bus) Socket, non stack-through, top	2
J001 PC/104AB (8-Bit Bus) Header, stack-through	3
J001 PC/104-AB (8-Bit Bus) Socket, stack-through	4
J001,J002 PC/104AB and PC/104CD (16-Bit Bus) Headers, non stack-through	5
J001,J002 PC/104AB and PC/104CD (16-Bit Bus) Sockets, non stack-through	6
J001,J002 PC/104AB and PC/104CD (16-Bit Bus) Headers, stack-through	7
J001,J002 PC/104AB and PC/104CD (16-Bit Bus) Sockets, stack-through	8
Custom Connector, specify separately	C

10.2.12 MASS I/O Connector (J003) – Code Y

NO Mass I/O J003 Connector.	0
5X11 2MM Straight Receptacle, top mounted	1
5X11 2MM Right-angle Plug, top mounted	2
5X11 2MM Straight Plug, top mounted	3
5X11 2MM Right-Angle Receptacle, top mounted	4
Custom Connector for J003	C

NOTES

[1] Mass I/O J003 and J004 Connectors are normally required if any peripheral function except for Ethernet is required; If in doubt, please refer to section 8.2, "J003, J004 – Mass I/O Connector ", on page 66 of this document, for a complete list of peripheral groups that require this option.

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10.2.13 MASS I/O Connector (J004) – Code Z

NO Mass I/O J004 Connector.	0
5X22 2MM Straight Receptacle, top mounted	1
5X22 2MM Right-angle Plug, top mounted	2
5X22 2MM Straight Plug, top mounted	3
5X22 2MM Right-Angle Receptacle, top mounted	4
Custom Connector for J004	C

NOTES
[1] Mass I/O J003 and J004 Connectors are normally required if any peripheral function except for Ethernet is required; If in doubt, please refer to the section 8.2, "J003, J004 – Mass I/O Connector ", on page 66 of this document for a complete list of peripheral groups that require this option.

10.2.14 CACHE Memory Option – Code a

Cache is WRITE-BACK	0
Cache is WRITE-THROUGH	1

For more information, see section 6.6.

10.2.15 SCSI Assignment – Code b

SCSI is configured as Primary Controller	0
SCSI is configured as Secondary Controller	1

10.2.16 Watchdog Enabling Jumper – Code c

Watchdog is Disabled (Jumper is not inserted)	0
Watchdog is Enabled (Jumper is inserted)	1

10.2.17 Panel ENAVEE Polarity – Code d

ENAVEE is Active High	0
ENAVEE is Active Low	1

NOTES: Use the value of 0 if VIDEO is ordered.

10.2.18 Power Arrangement (J007, J009) – Code e

SINGLE EXTERNAL +5V SUPPLY: J007 (+5V Power) Header Populated J009 (+3.3V Power) not populated +3.3V generated by On-board Linear regulator	0
DUAL EXTERNAL +5V, +3.3V SUPPLIES: J007 (+5V Power) Header Populated J009 (+3.3V Power) Populated	1

10.2.19 Panel ACTI+ENABKL – Code f

AVAILABLE Panel Signals ACTI, ENABKL Available on Panel Interface	0
UNAVAILABLE Panel Signals ACTI, ENABKL Unavailable on Panel Interface	1

NOTES: Select option 0 when total main memory (including SODIMM) is less than 64 MB. Select option 1 when total main memory is 64 MB or greater. See section 6.24.5 for more information concerning how this option affects video performance.

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11 Service Information

If you feel your board requires service, Megatel Service Department will do all it can to get you up and running – quickly.

If you purchased your board from a Distributor:

Our distributors are technically capable and will help you to determine and correct your problem. Since your proof of purchase was obtained from the Distributor, please return your board to them. Please follow their instructions for returning your board for service.

If you purchased your board directly from Megatel:

Please Call or Fax to Megatel's Service Department prior to shipping, to receive your RMA# (Return Materials Authorization number). You may also submit a request for an RMA# from our web-site http://www.metatel.ca. Boards that do not have RMA#s will not receive priority. To receive an RMA#, you will be required to provide the following information:

1. Company Name
2. Board Model Number or Product Order Number
3. Board Serial Number
4. Description of the Problem
5. Purchase Order Number

Special Shipping Instructions

Along with the information on the Megatel SERVICE FORM (see next page), please include the following on one of your commercial invoices:

1. The value of the board(s) – this value must match the invoice(s) we sent with the boards
2. A copy of the invoice(s) we sent with the boards (Proof of Purchase)
3. Be sure to state one of the following
   a) "Canadian Goods Being Returned for Repair"
   b) "Canadian Goods Being Returned for Warranty Repair"
   c) "Canadian Goods Being Returned"

One copy of the above documents is to be placed inside the shipping box and one copy is to be placed on the outside of the shipping box (marked for CUSTOMS). Other products (i.e. disk drives, LCD panels, etc.) that were not purchased from Megatel, but will be used as part of the servicing of the returned board, must be shipped separately and listed in the Megatel SERVICE FORM (next page) under "Equipment Sent Separately" heading. Products not purchased from Megatel should be shipped under a temporary import license of the maximum time limit.

Send PREPAID to the SERVICE DEPT. at:

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125 WENDELL AVENUE
WESTON, ONTARIO
M9N 3K9 CANADA

Our harmonized Number: 8471.92.00

Call us at +1 416 245-2953 between the hours of 9am to 5pm EST or send a Fax to +1 416 245-6505.

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Megatel SERVICE FORM

PRIOR TO SHIPPING:: Please call Megatel to receive your RMA#. Only boards sent with an RMA# will be given priority. This RMA# must appear on all paper work and be clearly marked on the outside of the shipping box.

RMA#: _____

Date Called: _____

Your Company Name: _____

Your Contact Name: _____

Your Company Address:

Ship To: _____ **Bill To:** _____

Your Telephone Number: _____ **Extension:** _____

Your Fax Number: _____ **Extension:** _____

Equipment You are Sending to Us: Pleasefill in the following as completely and accurately as possible

Product #	Serial #	Description of the Problem

Purchase Order Number for this Return _____

Equipment Sent Separately

Courier	Waybill#	Description (include Model#, Serial#)

Courier Company to be Used for Returning this Shipment: Please Circle or Check One

FEDEX	EMERY	UPS AIR	PUROLATOR	ALPHA	TRANS	BAISLEY

OTHER _____

Special Instructions/Comments You have for us: _____

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12 Physical Specifications

The physical size of the PC/II+dx is compliant with the PC/104 Specification. The size is 3.775 x 3.550 inches (95.9 x 90.2 mm). In the diagram, connectors J001 and J002 are specified by the PC/104 specification, and J003, J004, J005, J007, J008 and J009 are the megatel Mass I/O 5X11 connector, Mass I/O 5X22 connector, Ethernet Header, +5V Power Connector, Fan Power Header, and +3.3V Power Connector, respectively.

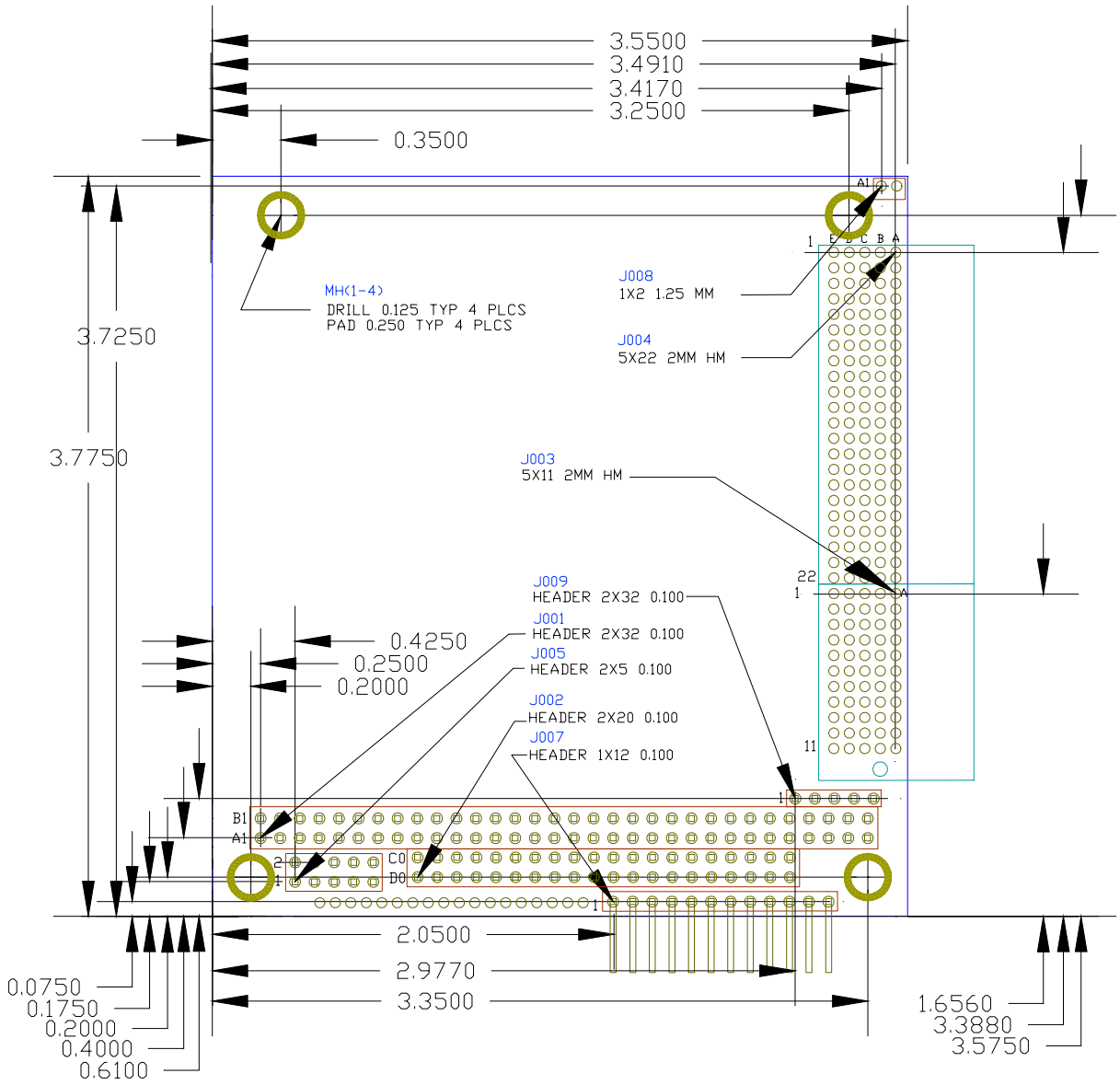


Figure 11 PC/II+dx Physical Dimensions (v1.33)

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