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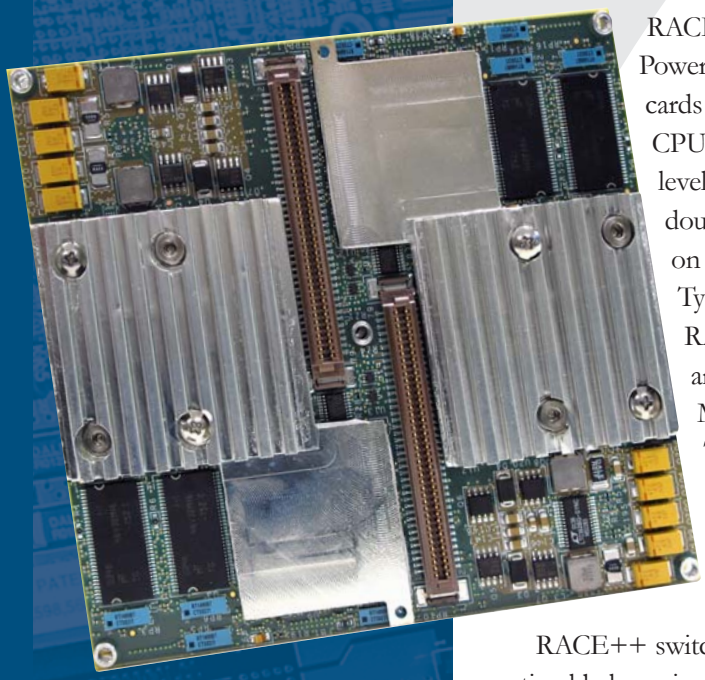
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Find the *Mercury Computer Systems RACE MCJ6* at our website: *Click HERE*

Computer Systems, Inc.
MERCURY

PowerPC 7447A Daughtercards



RACE++® Series PowerPC® 7447A daughtercards combine an 800 MHz CPU (667 MHz for extended level 2 temperature) with double data-rate SDRAM on a standard Mercury Type J daughtercard for RACE++ VME, cPCI, and PowerStream® MP-510 systems. Targeted specifically for today's memory-bound applications, these daughtercards interface directly with the RACE++ switch fabric to form the optimal balance in processing, memory, and data communications attainable for embedded multicomputing applications.

Each PowerPC 7447A daughtercard contains two MPC7447A microprocessors with AltiVec™ technology running 800 MHz, or 667 MHz for extended level 2 temperature. These unique microprocessors combine a superscalar RISC architecture with AltiVec parallel vector execution technology. By maintaining commonality with previous RACE++ Series PowerPC products, Mercury provides an easy upgrade path for existing system designs.

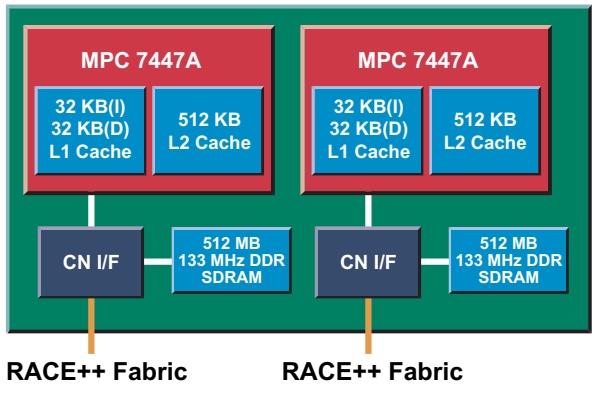
Compute Node Architecture

The computational power of RACE++ Series systems is built from compute nodes (CNs) comprised of processors, memory, and interfaces to the RACE++ interconnect. PowerPC 7447A daughtercards contain two compute nodes, each consisting of an MPC7447A microprocessor with AltiVec technology, fast on-chip Level 2 (L2) cache, double data-rate (DDR) SDRAM, and a Mercury-designed CN interface chip.

The CN interface chip contains architectural advancements that enhance concurrency between arithmetic and I/O operations. Each PowerPC 7447A CN includes a fully pipelined on-chip L2 cache that delivers 32 bytes per clock cycle to the L1 caches. This high-performance cache system provides quick access to data previously loaded from memory but too large to fit into the on-chip cache.

The CN interface chip acts as both a memory controller and as a network interface to the RACE++ switch fabric interconnect. The CN interface includes an enhanced DMA controller, a high-performance memory system with error checking and correcting, metering logic, and a RACE++ interface. By integrating memory control and the network interface, Mercury's compute node provides functionality and performance not achievable from separate components.

PowerPC 7447A Daughtercard Compute Node



800 MHz PowerPC 7447A microprocessors

1K CFFT in 9.57µs

4-way parallel AltiVec technology

133 MHz MPX bus

512 MB SDRAM per processor

267 MB/s RACE++ switch fabric direct interconnect

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High-Performance Memory System

The MPX processor bus used on the PowerPC 7447A daughtercard delivers key memory access and sustained throughput enhancements over the 60x bus used on earlier daughtercards. Mercury's high-performance memory subsystem allows the memory to approach the theoretical limits of its performance capability with:

DDR-266 133-MHz Double Data-Rate DRAM: The double data-rate DRAM provides the additional bandwidth to handle overlapping local processor access and remote accesses over the RACE++ switch fabric.

Virtual Mapping Registers: New virtual mapping registers provide finer granularity of address mapping windows and the ability to simultaneously map connections to SMBs on every node in the system.

FIFO Buffers: These buffers efficiently overlap accesses to SDRAM from the local processor and the RACEway interconnect.

The PowerPC CN contains error-correcting circuitry for improved data integrity. One-bit errors are corrected on the fly, and multi-bit errors generate an interrupt error condition.

AltiVec Vector Processing Unit

The processor has an enhanced AltiVec vector execution unit, a floating-point unit, and four integer units that can operate concurrently with the AltiVec unit. An on-chip, 512-Kbyte, eight-way set-associative L2 cache greatly enhances performance for short- and medium-length vector data.

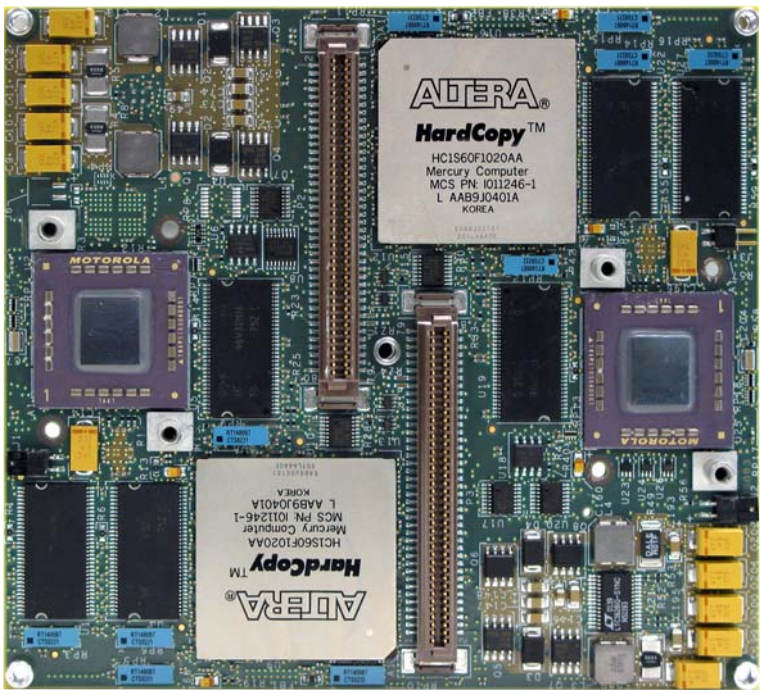
The AltiVec vector processing units operate on 128 bits of data concurrently with the other PowerPC execution units. The 128-bit wide execution units can be used to operate on four floating-point numbers, four 32-bit integers, eight 16-bit integers, or sixteen 8-bit integers simultaneously.

The Permute sub-unit incorporates a crossbar network to perform 16 individual byte moves in a single cycle. This capability can be used for simple tasks such as merging, shifting, packing, and reformatting vector data, or for more complicated tasks such as byte interleaving, dynamic address alignment, or accelerating small look-up tables.

Enhanced DMA Controller

Each CN has an advanced DMA controller to support RACEway transfers at 267 MB/s with chaining and striding. With chained DMA, the DMA controller works from a linked list in memory so that a complex chain of DMA requests requires no overhead from remote processors. DMA requests also support nonsequential access to and from local memory. This strided-DMA capability enables high-performance submatrix transfers as required for distributed 2D applications in image processing and synthetic aperture radar (SAR).

PowerPC 7447A Daughtercard



Performance Metering Logic

The CN FPGA also provides non-intrusive hardware performance metering facilities that enable application performance tuning and real-time data-flow analysis, essential for developing real-time multicomputer applications. A RACE++ node can be directed to collect performance metrics on memory bandwidth utilization, RACEway crossbar port usage and contention, or memory contention. The information can be used to locate sub-optimal code sections during execution of the application.

RACE++ Switch Fabric Interconnect

The PowerPC 7447A daughtercard is fully compatible with the RACE++ interconnect, the second generation of the RACEway switch fabric interconnect. The PowerPC CN FPGA connects the processor and

memory directly to the 66.66-MHz RACEway interconnect. The RACE++ interconnect represents the most cost-effective approach to utilizing the computational power of the newer PowerPC processors, providing unmatched scalability, high communication speed, more richly connected topologies, and augmented adaptive routing.

Crossbar-Connected Communication

All communication paths among compute nodes, memory nodes, and I/O nodes are connected using eight-port crossbars, both onboard and between boards. By providing these point-to-point connections, the RACE++ architecture eliminates the bottlenecks found in systems that use buses to connect processors together on a board or between boards.

Each node on a RACE++ daughtercard is connected to the RACEway switch fabric through an interface FPGA on the daughtercard. The RACE++ VME motherboard contains the first set of crossbars in the RACEway switch fabric. The second set of crossbars is contained on RACEway Interlink modules that connect multiple motherboards. This architecture assures each compute node direct and unblocked access to the RACEway network.

High Bandwidth, Low Latency

Each connection through a RACE++ crossbar can run at a peak bandwidth of 267 MB/s. Each crossbar can connect four simultaneous communication paths for a total peak bandwidth over 1 GB/s.

Low latency is often as important, if not more important, than high bandwidth. When making a connection through a RACE++ system at 66.66 MHz, each crossbar along the data transfer path adds only 75 ns to the latency. Once the connection is established, each crossbar adds only 15 ns of latency.

Priority-Based Communication

Real-time applications demand more than speed alone. The priority-based communication of RACEway is designed to minimize the worst case latency for selected communications.

Adaptive Routing

The RACE++ crossbars adaptively route data using alternate path selections to actively avoid any congestion in the network without user intervention.

RACEway Broadcast Support

The PowerPC compute node supports RACEway crossbar broadcast capabilities for enhanced bandwidth utilization when sending the same data to multiple nodes. This hardware broadcast also reduces latency compared to software-based schemes that emulate a hardware broadcast by repetitively sending the same data in separate transfers.

As the initiator of a broadcast, either the PowerPC processor or the DMA controller may use any of the broadcast or multicast modes provided by the RACEway crossbar. As a receiver of broadcast data, the PowerPC CN has the programmable option of accepting or ignoring the data.

Software

Mercury provides programming tools that simplify development and testing of real-time applications. The RACE++ Series MULTI® Integrated Development Environment (IDE) enables programmers to use familiar, mainstream tools to develop real-time processing routines. The MULTI IDE's integrated debug, program build, profiling, and version control facilities streamline development of complex multiprocessor software.

Mercury's **Scientific Algorithm Library** (SAL) provides the industry's easiest method of accessing the full power of the AltiVec vector unit. The SAL contains hundreds of image and signal processing functions that are optimized for AltiVec execution. For example, a 1K complex FFT runs in just 9.57µs on an 800 MHz PowerPC 7447A in SAL 7.2. These high-performance algorithms can also be accessed through the industry-standard VSIPL interface using Mercury's **VSIPL-Lite** signal-processing library. For applications that require custom algorithms with demanding vector processing requirements, Mercury's C compiler includes the AltiVec C extensions that allow direct access to the AltiVec vector unit.

The **Parallel Acceleration System** (PAS™) supports the DRI industry-standard data reorganization interface for a wide variety of efficient and scalable multiprocessor communication patterns using high-level library calls. Once programmed in PAS, the application can scale to a larger or smaller number of compute nodes merely by changing runtime variables.

The TATL™ **Trace Analysis Tool and Library** from Mercury is also available to assist during software development and debugging. TATL is a minimally intrusive software logic analyzer that allows developers to visualize multiprocessor interactions. Using TATL, developers can spot bottlenecks, such as contention for shared resources or load imbalances.

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Electrical/Mechanical Specifications

	Commercial	Level 1 Rugged	Level 2 Rugged
RACEway ports	2	2	2
Processor frequency	800 MHz	800 MHz	667 MHz
Compute nodes	2	2	2
Memory frequency	133 MHz	133 MHz	133 MHz
DDR DRAM/CN	512 MB	512 MB	512 MB
DDR DRAM/daughtercard	1024 MB	1024 MB	1024 MB
L2 cache frequency	800 MHz (32 Bytes wide)	800 MHz (32 Bytes wide)	667 MHz (32 Bytes wide)
L2 on-chip cache per CN	512 KB	512 KB	512 KB
Weight	0.56 lb	0.57 lb	0.57 lb
Dimensions	5.0" x 4.435"	5.0" x 4.435"	5.0" x 4.435"
Maximum power consumption	30W	30W	27W
Operating temperature	0°C to +40°C	-25°C to +55°C	-45°C to +70°C
Operating altitude	0 to 10,000 ft**	0 to 30,000 ft**	0 to 30,000 ft**
Storage temperature	-40°C to +85°C	-55°C to +85°C	-55°C to +125°C
Humidity	10 to 90% (non-condensing)	5 to 95% (non-condensing)	5 to 95% (non-condensing)
Vibration (random)		0.04g²/Hz, 20-2000 Hz, 1 hr/axis	0.04g²/Hz, 20-2000 Hz, 1 hr/axis
Vibration (shock)			
6U		z-axis: 50g, x+y axes: 80g, 11 ms, ½ sine pulse	z-axis: 50g, x+y axes: 80g, 11 ms, ½ sine pulse
9U		z-axis: 30g, x+y axes: 50g, 11 ms, ½ sine pulse	z-axis: 30g, x+y axes: 50g, 11 ms, ½ sine pulse

Compatible Mercury Motherboards

	Maximum Configuration	Minimum Airflow
Commercial (800 MHz)		
6U VME/RACE++ MCJ6*	2 daughtercards	12 CFM
9U VME/RACE++ MCJ9*	7 daughtercards and 1 I/O card	27 CFM
6U cPCI/RACE++ ImpactRT MB2	2 daughtercards	12 CFM
Level 1 Rugged (800 MHz)		
6U VME/RACE++ MCJ6*	2 daughtercards	14 CFM
Level 2 Rugged (667 MHz)		
6U VME/RACE++ MCJ6*	2 daughtercards	16 CFM

* Requires 5-row connectors and VITA 1.7 Compliant (2 amp/pin) VME backplanes.
** Contact Mercury for operating altitude above 10,000 ft.

As altitude increases, air density decreases, hence the cooling effect of a particular airflow rating decreases. Many manufacturers specify altitude and temperature ranges that are not simultaneous. Note that the above operating temperature is specified simultaneously with an altitude. Different limits can be achieved by trading among altitude, temperature, performance, and airflow. Contact Mercury Computer Systems for more information.

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