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FIC 8230

Fast Intelligent Controller

Addendum, version 1.1

Designation: DOC 8230/UM

PN: 085.209

Addendum Version 1.1 - October 1995

CREATIVE ELECTRONIC SYSTEMS S.A.

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Addendum to FIC 8230 User's Manual version 1.0

The target of this addendum is to bring new information and to give modifications to the FIC 8230 User's Manual version 1.0.

Paragraph 3.3.1.2

CTLVME2

bits <01...00>	BR2,BR1	These 2 bits define the level of BREQ used during the VME request arbitration. <0,0> BREQ level 3 <0,1> BREQ level 2 <1,0> BREQ level 1 <1,1> BREQ level 0
bit <02>	ROR	These two bits define the mode of release during the VME request arbitration. <0> RWD mode <1> ROR mode
bit <03>	FAIR	This bit allows the FIC 8230 VME bus requester to work in FAIR mode. <0> FAIRness mode disabled <1> FAIRness mode enabled
bit <04>	ARB	This bit is only used if the Arbitration module (ARB 8430 / 2) is installed on the FIC 8230. <0> PRI Arbitration mode <1> RRS Arbitration mode
bit <05>	SYSF	This bit allows to generate the VME "SYSFAIL" line. <1> VME SYSFAIL active <0> VME SYSFAIL inactive

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