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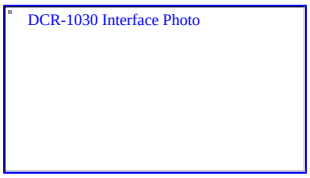
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VME64/RACEway Ampex DCRsi Interface
DCR-1030



The Myriad Logic model DCR-1030 is a VME64 and RACEway interface for the Ampex DCRsi 107 and DCRsi 240 Digital Cartridge Recording Systems. It supports sustained data rates up to 30 MBytes/second to Ampex 733 cartridge tapes (48 GBytes per cartridge). The interface permits the DCRsi to be used with various VME and workstation platforms. Practical applications include data collection/archiving, image processing, simulation, remote sensing, and others.

Features

- 52 MByte/second burst transfer rate
- 26 MByte/second VME32 burst transfer rate
- 160 MByte/second RACEway burst transfer rate
- 30 MByte/second sustained transfer rate to the DCRsi 240
- 13.4 MByte/second sustained transfer rate to the DCRsi 107
- Comprehensive recorder control and buffer management firmware
- DCRsi auxillary data channel support
- 16 kbyte record and playback FIFO buffers
- On-Board 33MHz 68030
- Single 6u x 160mm form factor

Product Description

The Myriad Logic model DCR-1030 is a high-performance VME64 interface for the Ampex DCRsi family of Digital Cartridge Recorder Systems. Designed for use in VME and workstation platforms, this single 6u board provides all connections required to record and playback data, as well as control the DCSRi.

The Ampex DCRsi 240 and 107 Digital Cartridge Recorders use a common tape cartridge, recording format, and host interface. The DCRsi 240 supports sustained record/playback at 30 Mbytes/second, with burst rates up to 37 Mbytes/second (13.4 sustained and 15 burst for the model 107). The common recording format allows cartridges recorded on a DCRsi 107 to be played back on a DCRsi 240. Both DCRsi systems feature fully integrated memory buffers - 72 Mbytes in the DCRsi 240 and 12 Mbytes in the DCRsi 107. These rate buffers allow continuous recording at variable rates up to the maximum rate.

Myriad's DCR-1030 consists of a VME64 interface, buffered record/playback subsystems, and a 6803-based controller, all interconnected via an on-board local bus. A Cypress Semiconductor VIC64 chip-set provides a full- featured VME interface. When operating as a VME64 master in the BLT mode, the DCR-1030 has been benchmarked at 52 MBytes/second between VME64 memory and the FIFO buffers (26 MBytes/second for VME32 operation). The VME interface also allows interleaved VME slave access to the DCR-1030's on-board DRAM. This provides a VME-based host access to on-board control data structures during data transfers.

This high-performance VME interface, critical for sustained 30 MByte/second operation of with the DCRsi 240, proves equally valuable when used with the DCRsi 107. When used with the DCRsi 107, the DCR-1030 supports maximum rate transfers to/from the DCRsi using only 25% of the available VME bandwidth. This efficient operation allows other VME processors to share VME bandwidth and eliminates the need for complex dual bus architectures in most applications.

The DCR-1030's record and playback subsystems include 16 kbyte FIFO buffers. These FIFOs decouple the VME subsystem from the DCRsi interface, allowing the VME subsystem to run at peak efficiency. The record and playback subsystems handle both high-rate data and auxilliary data channels. A bi-directional auxilliary data FIFO buffer allows bursts of auxilliary data to be transferred to/from VME memory. During the record operation, data read from the auxilliary data FIFO provided to the DCRsi data interface in a serial stream. On playback, serial auxilliary data, read from the data interface, is stored in the auxilliary data FIFO any can be DMAed to VME memory.

A comprehensive suite of standard firmware operates on an on-board 33 MHz 68030, providing an efficient host interface for DCRsi commanding, data record/playback operation, and buffer management. The standard firmware eliminates the need for user-generated software for the DCR-1030's 68030 in the vast majority of applications.

The host interface for both control, record, and playback functions is implemented entirely with data structures in VME-accessible memory. Thus, a special device driver is not required to efficiently use the DCR-1030 in most workstation and embedded VME environments.

The control interface provided by the standard firmware provides both pass-through commands and macro commands. The DCR-1030 forwards pass-through commands to the DCRsi and provides responses back to the host. Macro commands are implemented for common functions such as "Search". In this case, the DCR-1030 polls the recorder to determine when the search point has been reached, thus off-loading time-consuming polling operations from the host.

The optional module provides a mechanism to transfer data between the DCRsi and a dual-access memory via the VME Subsystem Bus (VSB). Both the RACEway and VSB modules mount flush to the DCR-1030 and do not require additional VME slots.

Application Notes

Controlling the DCR-1030 with a VME CPU or DSP board
The DCR-1030 Standard Firmware (1030-SF) provides an application program interface for software running in a VME single board computer, DSP, or other processor (host) to direct data transfer between VME memory buffers and the Ampex DCRSi family of digital cassette recording systems.

The 1030-SF is a stand-alone set of firmware for the DCR-1030's 68030 CPU, including functions which control operation of the Ampex DCRSi and DMA data between VME/VSB buffers and the DCRsi. DMA functions are designed to minimize host interaction and are very well suited for real-time operation.

Control Operation
A VME host controls operation of the DCR-1030 via a set of data structures located VME memory both on the DCR-1030 and in system memory (figure 1). Recorder control functions are accomplished via the Command/Acknowledge/Response (CAR) data structure (in DCR-1030 local DRAM). The VME host deposits commands in the command section of the CAR and writes to the command mailbox. This activates the 1030-SF command task, which acknowledges receipt of the command, processes the command, and generates a response. The acknowledgement and responses are stored in the CAR structure and are available to the VME host. The 1030-SF can also generate signals to the host indicating when a new acknowledgement or response is available. The desired signal can be a VME interrupt or mailbox write and is defined in the CAR by the host.

Table 1 - DCR-1030 Standard Firmware Features

Feature	Comment
Data Structure-Based Host Interface	Host-based application software sets up pointers to CMD/ACK/RESP and BAB structures to control the DCR-1030. Host operating system specific device drivers are not required.
DCR-1030 Bus Master	The 1030-SF DMA's data between DCR-1030 FIFO buffers and VME/VSB memory buffers or RACEway Compute Elements.
VME32, VME64, VSB, and RACEway Access Modes	Migration from VME to another supported access mode can be accomplished by changing a single parameter.
Minimal Host Interaction	Circular queue of Buffer Access Blocks (BABs) provides low-overhead method for host to identify next block to record/playback.
Complete Package	User-generated software for DCR-1030 68030 is not required. VxWorks-based 1030-SF provides all required functions.

The 1030-SF recognizes both macro and pass-through commands. Macro commands (initialize, record, and playback) are decomposed into a pre-defined sequence of functions (typically Ampex DCRsi commands) by the 1030-SF. When the sequence is processed a response is generated.

The VME host can communicate directly with the Ampex DCRsi control interface by using pass-through commands. The 1030-SF forwards these commands to the recorder and stores the recorder response in the CAR structure.

The 1030-SF also provides a queue of DCR response messages. All control messages received from the DCRsi are stored in the response buffer queue in the DCR-1030 DRAM. Each message received (both in response to

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specific macro expansions and pass-through command as well as unsolicited DCRsi messages) are available to the VME host. **Record Operation**

Table 2-Macro Commands

Command	Parameters
Initalize	Address of First BAB in VME memory Processed Signal VME Interrupt Processed Mailbox (Address, Mode & Value) Recorder Type (Classic, 107, 240)
Record	Startup Mode Scan address
Playback	Search Type Scan address

Upon receipt of the record macro, the 1030-SF enters the record mode where operation controlled by a circular queue of Buffer Access Blocks (BABs). Each BAB points to a buffer containing data to be recorded on tape. The BAB contains the size (in bytes) of the data set, access mode (VME32, VME64, VSB, or RACEway), a useage flag, and a pointer to the next BAB. BAB head and tail pointers (in VME-accessible memory on the DCR-1030) define the next buffer available to the VME host (for more data to be recorded) and the next buffer to be recorded on tape respectively.

Prior to the record process the VME host initializes a set of buffers in system memory and describes the buffers in a list of BABs. During the record process the VME host is responsible for notifying the 1030-SF when buffers are available for recording by updating the BAB head pointer. Upon detecting a difference between the BAB head and tail pointer (via polling) the 1030-SF outputs the buffer defined by the BAB tail pointer. When the buffer is output 1030-SF clears the useage flag in the BAB, increments the BAB tail pointer, signals the VME host, and continues with the next block.

BAB completion signals generated by the 1030-SF are specified in the initialize macro and can be either a VME interrupt or writing a data value or the BAB tail pointer value to a specified VME location.

Playback Operation

Table 3- Data Structures and Signals

Item	VME Location	Access Mode
Command Mailbox	0x0023	A16/D8
CAR Command Buffer	0x007F,0000	A32/D32
CAR Acknowledge Buffer	0x007F,0080	A32/D32
CAR Response Buffer	0x007F,0100	A32/D32
CAR Error Buffer	0x007F,0180	A32/D32
BAB Head Pointer	0x007F,0400	A32/D32
BAB Tail Pointer	0x007F,0404	A32/D32
Command Buffer *Busy Flag	0x007F,0408	A32/D32
DCRsi Response Head Pointer	0x007F,040C	A32/D32
DCRsi Response Queue	0x007E,0000	A32/D32

Playback operation is controlled by BABs in the same manner as record. Prior to the playback process the VME host initializes a set of buffers and BABs initially indicating all buffers are available. Upon receiving the playback macro the 1030-SF positions the tape to the specified point and commands the DCRsi to reproduce data. When data is present on the DCR-1030 playback interface it is copied to the buffer described by the BAB tail pointer. As each buffer is filled the BAB is updated, the required host signal is produced and the BAB tail pointer incremented.

Since all buffers are initially empty playback always starts immediately and continues as long empty buffers exist in system memory. When there are no more empty buffers the 1030-SF stops accepting playback data from the DCRsi and waits for more empty buffers to become available.



Figure 1 DCR-1030 Standard Firmware Overview

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