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Find the *Mercury Computer Systems / Echotek DCM-V5-XMC* at our website: *Click HERE*

ECHOTEK™ SERIES

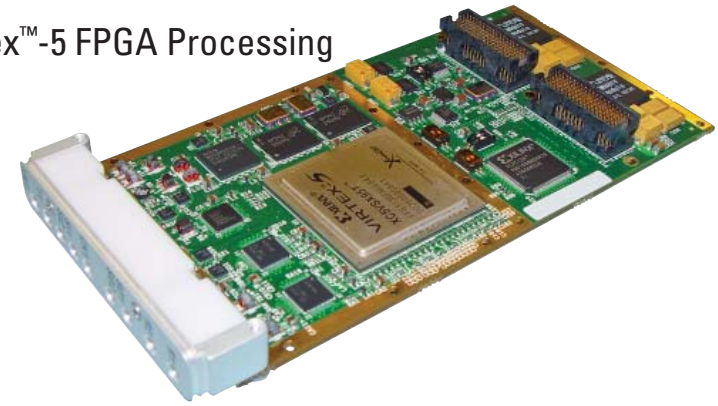
DATASHEET

MERCURY COMPUTER SYSTEMS™

DCM-V5-XMC Digital Receiver

High-Speed A/D and D/A Conversion with Virtex™-5 FPGA Processing

- Flexible, high-performance data conversion
- 14-bit analog-to-digital at up to 250 MSPS
- 12-bit digital-to-analog at up to 2.3 GHz
- Complementary to Echotek™ Series RF 1800GT Wideband Microwave Receiver



The Echotek™ Series DCM-V5-XMC Digital Receiver from Mercury Computer Systems implements a flexible FPGA-based architecture in a space-efficient mezzanine card form factor. The module combines the latest in high-performance A/D conversion with an ultra high-speed D/A converter, both working in conjunction with a powerful Xilinx® FPGA. The user-programmable Virtex-5 FPGA functions as the primary data processor, supported by Mercury's EchoCore™ firmware library.

With this set of flexible resources, the DCM-V5-XMC delivers unique capabilities, such as multi-board coherency, while addressing a range of analog signal requirements found in SIGINT, ELINT, Radar and Weather Tracking applications, as well as advanced scientific equipment such as particle accelerators.

Data Conversion

Analog data conversion is accomplished via two, single IF channel, Texas Instruments ADS6149 analog-to-digital converters. The ADS6149 is capable of digitizing IF signals with 14 bits of precision at sample rates of up to 250 MHz, making this unit ideal for sampling IF frequencies of 70 MHz, 140 MHz, and even 160 MHz. Digital data conversion is performed via a single-channel Maxim MAX19692 digital-to-analog converter. The MAX19692 can reconstruct at up to 2.3 GHz, with 12 bits of precision, making this unit perfect for outputting high bandwidth signals.

FPGA Resources

Ever-changing mission requirements demand flexibility in programmable logic devices, as well as a level of performance to deal with unrelenting high-bandwidth data streams. This is why the DCM-V5-XMC employs a Xilinx Virtex-5 SX95T high-performance FPGA. This 1136-pin package FPGA provides a multitude of high-performance resources, including 58,880 logic cells, 14,720 slices, and 640 DSP48e blocks in a single device. These raw resources make the Virtex-5 FPGA ideal for computationally intensive applications such as digital down-conversion, Fast Fourier transforms (FFTs), and data filtering.

The EchoCore™ Advantage

Mercury's EchoCore firmware streamlines the development of FPGA-based applications. These cores are optimized to deliver maximum performance for a range of common operations. They are designed with straight-forward interfaces for application-specific algorithm IP, greatly reducing the time required to create complete solutions. Included for the DCM-V5-XMC from Mercury's vast array of available cores are the EchoCore Wideband DDC, the EchoCore Narrowband DUC, EchoCore Aurora Interface, EchoCore DDR-II-SDRAM Interface, and the EchoCore PCIe Auto DMA Interface.

FPGA Configuration

The DCM-V5-XMC is a flash-based module capable of storing multiple images. Each FPGA core image is loaded over the PCIe bus to flash memory, which, at 128 MB, can hold up to eight 16-MB flash images. Any FPGA image can be selected to load automatically on power-up or at any time under user control. Both the FPGA itself and the flash memory can be reprogrammed at any time.

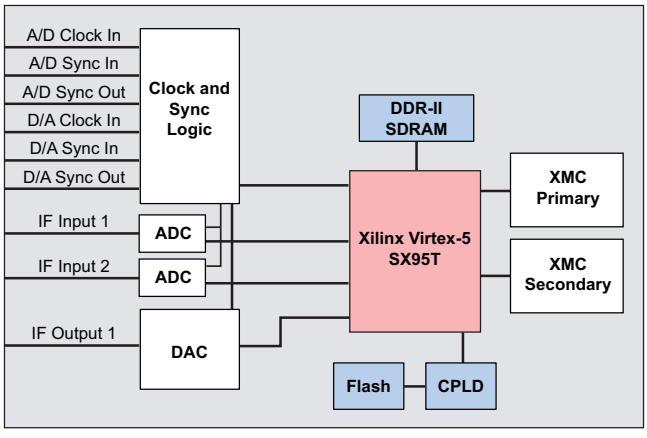


***Figure 1**. DCM-V5-XMC block diagram*

Memory

This XMC card also features 128 MB of DDR-II SDRAM, accessible by user-programmable applications. This memory utilizes a 250 MHz, 32-bit-wide link to the Virtex-5 FPGA for a total bandwidth of 2.0 GB/s, half-duplex.

Software

Mercury provides driver applications for the DCM-V5-XMC supported by the Red Hat® Enterprise Linux® 5 operating system. Alternative OS support may be made available on request.

Clock Inputs

The module design allows users to insert separate clocks for the A/D and D/A. The A/D clock input accepts a single clock input between 33 MHz and 250 MHz via a front-panel MMCX connector. The D/A clock input accepts a single clock input up to 2.3 GHz via a front-panel MMCX connector. Both these clocks drive their respective converters and are made available to the Virtex-5 FPGA for internal timing functions.

Sync Inputs/Outputs

The DCM-V5-XMC provides for separate A/D and D/A syncing, allowing for maximum application flexibility. Both the A/D and D/A offer a sync input and sync output via front-panel MMCX connectors, which can be used to trigger the start of data collection or another user-defined event. Signals sent over sync input are qualified by the A/D clock and are transferred out the sync output connector to allow for multi-board coherent collection in daisy-chained configurations.

XMC Interface

The DCM-V5-XMC is populated with two high-speed serial XMC connectors. The primary XMC connector is designed to implement an industry-standard PCIe interface utilizing the EchoCore™ PCIe Auto DMA Interface. This interface is eight lanes wide with a data transfer capacity of 3.125 Gbaud per lane, for a total theoretical bandwidth of 2.5 GB/s. The secondary XMC connector is capable of implementing a range of user-specified protocols.

Specifications

A/D Conversion

Input channels	2
A/D type	Texas Instruments ADS6149
Resolution	14 bits
Speed	250 MSPS

D/A Conversion

Output channels	1
D/A type	Maxim MAX19692
Resolution	12 bits
Speed	2.3 GHz

FPGA

1 user FPGA	Xilinx Virtex-5 SX95T

Memory

DDR-II-SDRAM	
Size	128 MB
Bus width	32 bits
Bus speed	250 MHz DDR

Datapaths

DDR-II-SDRAM to user FPGA	2.0 GB/s theoretical max
PCIe Interface	8 lanes at up to 2.5 GB/s total

Software

Driver applications

Supported by Red Hat® Enterprise Linux® 5 OS

Consult factory for alternative OS support.

Environmental

Ruggedization level	Commercial
Temperature	
Operating	0°C to 40°C with 300 ft/min appropriate airflow
Storage	-40°C to +85°C
Cooling	Commercial grade, convection-cooled

Consult factory for rugged options.

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