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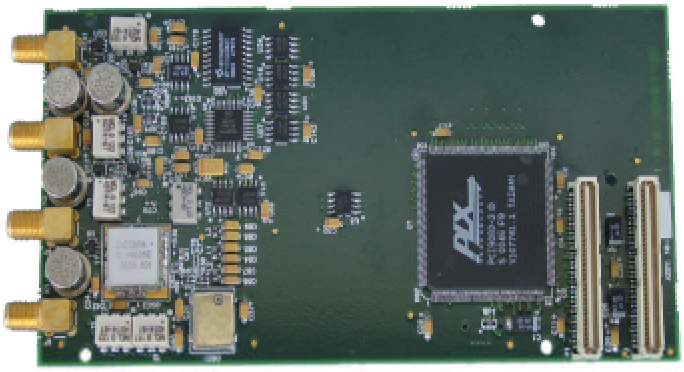
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Find the *Mercury Computer Systems / Echotek ECSG-1R3ADC-PMC* at our website: ***Click HERE***

LOW PHASE NOISE A/D CLOCK GENERATOR

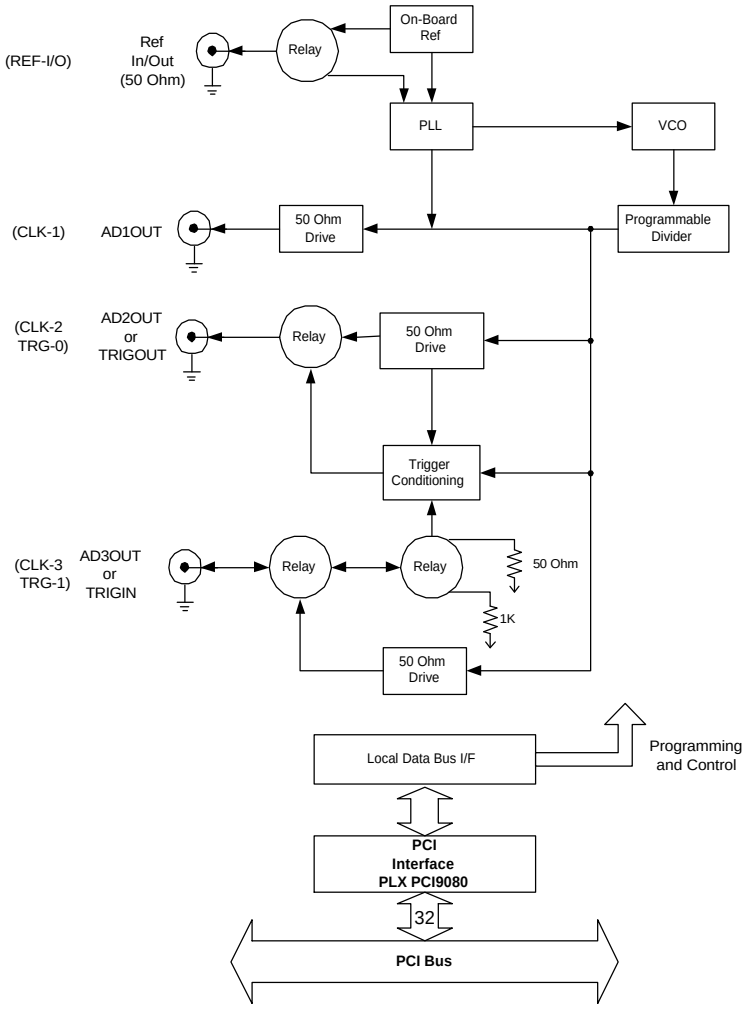
ECSG-1R3ADC-PMC



FEATURES

* PROGRAMMABLY GENERATES A/D CLOCKS FROM < 1 MHz TO >100 MHz
* UP TO THREE LOW PHASE NOISE (> -100 dBc @ >/= 1 KHz OFFSET) A/D CLOCK OUTPUTS
* OPTIONAL TRIGGER ALIGNMENT SUPPORT
* INTERNAL/EXTERNAL FREQUENCY REFERENCE
* PROGRAMMED CONTROL VIA 32-BIT, 33 MHz PCI
* EXTENDED TEMPERATURE OPTIONS AVAILABLE

ECSG-1R3ADC-PMC BLOCK DIAGRAM



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ECSG-1R3ADC-PMC FUNCTIONAL DESCRIPTION

The ECSG-1R3ADC-PMC module provides a means for the generation of low phase noise (> -100 dBc @ >/= 1 KHz offset) Analog-to-Digital Converter (ADC) and/or Digital-to-Analog Converter (DAC) clocks for distribution to board-level, mixed signal products such as ADC's, DAC's, Digital Receivers and Digital Upconverters. A temperature compensated low phase noise Reference Oscillator is available on-board and can be output via the Front Bezzel (REF-I/O) SMA with approximately +7 dBm (50 ohm) drive capability. Alternately, an External Reference Oscillator (between 5 MHz and 100 MHz) may be input via the Front Bezzel (REF-I/O) SMA connector.

The selected Reference is used with an on-board (default: 575 MHz to 675 MHz) low phase noise Voltage Controlled Oscillator (VCO) in a Phase Locked Loop (PLL) circuit. This circuitry generates a low phase noise output clock waveform at programmable rates of from <1 MHz to >100 MHz with the stability determined by the selected Reference Oscillator. The clock waveform is buffered for approximately +7 dBm (50 ohm) drive at each of three available Front Bezzel SMA connectors (CLK-1, CLK-2/TRG-0, CLK-3/TRG-I). Alternately, the Front Bezzel SMA connector CLK-3/TRG-I can be programmably configured to accept a 50 ohm (+7 dBm) or high impedance (1K ohm, TTL levels) External Trigger Input and produce an approximately +7 dBm (50 ohm) External Trigger Output on CLK-2/TRG-0. The output trigger is synchronized with the module's generated clock waveform (i.e., the output trigger's rising edge is aligned with the output clock waveform's rising edge. The width of the output trigger pulse is a multiple of clock waveform cycles as determined by the width of the input trigger pulse. The output trigger pulse driver is DC-coupled and will drive approximately 0 to >/= 1.8 volts into a 50 ohm load or approximately 0 to >/= 3.6 volts into a high impedance load.

Driver Support: Drivers are supplied for WinNT Operating Systems.

Ordering Information

Model	Part Number	Ruggedization	Options
ECSG-1R3ADC-PMC	12-0089/CC414	Commercial	Output level +7 dBm, VCO range 575-675 MHz
ECSG-1R3ADC-PMC	12-0089/CC480	Commercial	Output level +7 dBm, VCO range 320-426.667 MHz
ECSG-1R3ADC-PMC	12-0089/CC571	Commercial	Output level +10 dBm, VCO range 575-675 MHz
ECSG-1R3ADC-PMC	12-0089/CC575	Commercial	Output level +2 - +4 dBm, VCO range 575-675 MHz

Ruggedization Levels	Operating Temp (°C)	Storage Temp (°C)	Vibration	Shock	Humidity	Notes
Commercial	0 to +55°C with 300ft./min. airflow	-50 to +85°C	0.002g2/Hz from 10 to 2000Hz random and 2g sinusidal from 5 to 500 Hz	20g peak sawtooth, 11mS duration	Up to 95% RH	Commercial Grade, cooled by blown air, for use in benign environments and software development applications

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