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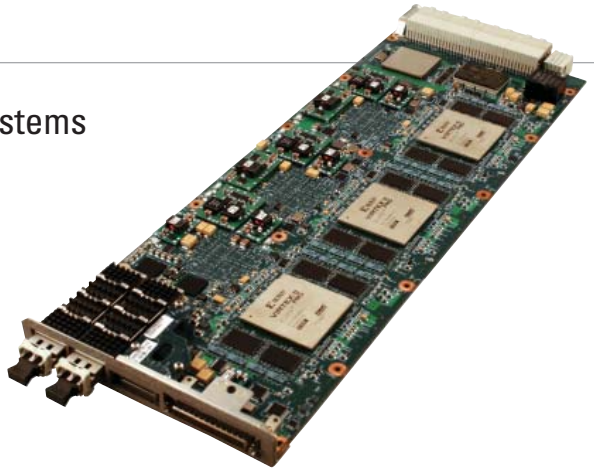
DATASHEET

MERCURY COMPUTER SYSTEMS™

PowerStream 7000 FCN Module

Exploit the Power of FPGAs in PowerStream® 7000 Systems

- 3 fully integrated FPGA compute nodes
- Flexible, high-capacity I/O connections
- Built-in IP for RapidIO and memory control



The PowerStream® 7000 FPGA compute node (FCN) module from Mercury Computer Systems provides a flexible, manageable way to exploit the power of field-programmable gate arrays (FPGAs) in PowerStream 7000 multicomputer systems. The FCN provides massive I/O as part of a scalable system that can expand with minimal application recoding and expense. Because some algorithms can run up to 20 times faster on an FPGA than a RISC processor, developers can partition applications across FPGAs and RISC processors for maximum effectiveness.

The FCN module is an M155-format board with three Xilinx® Virtex-II Pro™ P70-6 FPGAs. Each 7-million gate FPGA is connected to the RapidIO® switch fabric via an onboard RapidIO crossbar. Each FPGA is supported by both local SRAM and local DRAM to maximize its effectiveness as a compute node. Together, an FPGA and its memory chips are referred to as an FPGA compute node (FCN).

FPGA Compute Nodes

Each M155-format board contains three fully connected FPGA compute nodes. The heart of each FCN is a 7-million gate Xilinx Virtex-II Pro FPGA with its own memory, I/O, and RapidIO fabric connections. The 32 MB of QDR II SRAM in each FCN provides low-latency memory with peak access rates of 5.6 GB/s, based on a 175 MHz clock frequency (DDR 350). Larger data sets can be staged in the 128 MB RLDRAM II of each FCN. High-bandwidth data transfers are realized through the Mercury-provided memory controller IP.

The three FPGA compute nodes on each board can work together on the same data set, communicating via multi-gigabit transceiver (MGT) mesh links. Each FCN has five MGT links to the other two FCNs, with each link running at 3.125 Gbaud. One FCNLink connection to the RapidIO bridge device supports 622 MB/s peak bandwidth to the RapidIO fabric. A SelectMAP interface provides connection to the Configuration Manager (CM) module in the FCNLink-to-RapidIO Bridge (FRB).

This communication can be extended to multiple boards by creating an FPGA communication mesh. Each of three FPGAs provides four full-duplex 3.125 Gbps links to front-panel copper connections for board-to-board meshing.

Massive I/O at Your Command

Sensor data can be delivered directly to the FPGAs, where it can undergo data reduction using the massively parallel algorithms particularly suited to deployment on programmable logic devices. This saves processors and interprocessor bandwidth, thereby reducing system size, cost, and complexity.

The PowerStream 7000 FCN modules provide substantial I/O beyond the twelve 3.125 Gbaud mesh links. Two 10-Gbps full-duplex fiber-optic connections, plus 24 LVDS pairs for parallel I/O, provide massive bandwidth for direct I/O. Delivering I/O directly to the FPGAs allows these devices to perform repetitive operations that reduce data volume before passing the data on to the balance of the system. This feature maximizes computational density without increasing the system processor count.

The two independent 10 Gbps serial fiber interfaces provide high-speed streaming I/O at the front panel. Each interface has a 10-Gbps fiber-optic transceiver, LC-style fiber-optic connectors on the module front panel, with a management interface that allows register-based management and control of the data links.

Each 10-Gbps XFP optical module is connected to a PHY transceiver that translates the encoded 10 GHz signals to four

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3.125 GHz XAUI lanes connected to an FPGA compute node. Mercury provides an end-to-end example design as a starting pointer for a customer-supplied 10 GbE implementation. The example design uses Xilinx's XAUI core to provide four bonded channels to the internal FPGA cores. Additionally, the Mercury example provides I2C and MDIO interfaces for control and status monitoring of the XFP and PHY modules. These allow the user to exploit the loopback capabilities present in the 10 GbE onboard sub-system. Because these interfaces connect directly to the design's internal status and control registers, they are accessible from any node within the multicomputer for monitoring and diagnostic purposes. The Xilinx MAC core can be purchased and inserted into the example design, so that the customer does not have to design the interface from scratch.

A set of differential digital signals is provided for general-purpose I/O use. A front-panel connector provides 24 discrete LVDS signal pairs, eight pairs from each of the three FPGAs. Designed for application-defined communications, this interface can be used to support parallel I/O to sensors, or used between boards for direct FPGA-to-FPGA connections.

On a system-wide level, PowerStream 7000 FCN modules can exchange data with any RapidIO devices on other PowerStream 7000 modules via the RapidIO switch fabric. Third-party I/O PMCs and XMCs can also be accommodated in the RapidIO system via the switch card modules in the PowerStream 7000 system.

RapidIO System Connectivity

Full connectivity makes PowerStream 7000 FCN modules part of a scalable system that can expand to provide as many FPGAs and PowerPC microprocessors as changing applications demand, with minimal application recoding and redeployment expense.

When data is required to travel to another board, such as a PowerPC processor board, the PowerStream 7000 FCN system leverages the bandwidth, speed, and scalability of the RapidIO switch fabric communications architecture to move data quickly and efficiently. The FCN module includes an 8-port parallel RapidIO crossbar, with each port capable of operating at a 622 MB/s burst data rate in each direction. Four of the crossbar ports are connected to the module backplane connectors, and one port is connected to each of the three FPGA nodes through its dedicated RapidIO bridge device. These ports connect the board to the system-wide fabric, which can connect dozens of simultaneous communication paths. Using the RapidIO switch fabric, the multiple paths between most points in the fabric greatly reduce the chance of blocking or interruption.

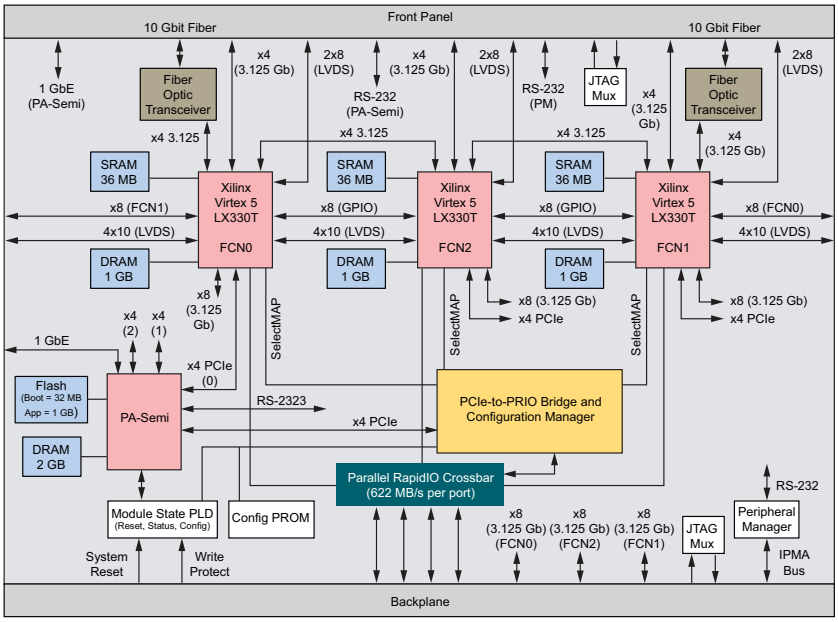
Real-Time Reconfiguration for Mode Changes

Mercury's FPGA technology adds the versatility of nearly instant reconfiguration. High-speed reconfiguration facilitates dynamic, system-level changes in mission and operating mode. The Configuration Manager (CM), located within the FRB, provides an interface to the RapidIO network, allowing remote processor nodes to send commands to the CM and to read status information regarding the FCN. For reconfiguring the FPGA, the CM drives the SelectMAP interface to the FPGA, so that bit-stream data sent across the RapidIO network can be written into the FPGA at a peak speed of 50 MB/s.

The Peripheral Manager (PM) implements the module status and control functions common to all modules in the PowerStream 7000 system. These control functions include various types of reset and monitors for power supplies, configuration status, and application status. The PM communicates module status information over IPMI to a central management processor on one of the PowerStream 7000 switch modules.

Applications use the multicomputer status and control (MSC) service library to retrieve module status information connected by the central management processors and to forward commands through those processors to the modules in the chassis. The MSC service is a status and control interface to the switch card modules in the PowerStream 7000 multicomputer. The MSC allows applications running on the switch card processor nodes to access the status information from FCN modules and to command the FCN modules to change state.

Each FCN module has a set of indicator lights and onboard sensors. These include a temperature sensor for each FCN, as well as current and voltage sensors that provide in-system power dissipation measurements for the FCN module. The measurements for these sensors are available to applications running on the PowerStream 7000 switch card processors through the MSC.



PowerStream 7000 FCN Module functional block diagram

A library of application programming interfaces (APIs) allows applications to interact with the MSC service. The MSC library APIs related to the use of the FCN modules include the following functions:

- Enabling FCN modules in the hardware configuration
- Reading the results of power-on self-test
- Controlling the basic state of the FCN modules
- Joining the FCN modules into the multicomputer cluster
- Reading and controlling sensors on the FCN module

Partition Applications Easily Between FPGAs and PowerPCs

PowerStream 7000 FCN boards can be configured in RapidIO systems with other PowerStream 7000 boards, including boards carrying PowerPC® compute nodes, I/O devices, and other PowerStream 7000 FCN boards. Because FPGAs in Mercury systems operate as a seamless element of the RapidIO environment, developers can partition their application between performance-leveraging segments that run best on the FPGA and portions that can execute on easier-to-program PowerPC microprocessors.

Algorithms such as FFTs, fast convolutions, and pulse compression on incoming data streams can run up to 20 times faster on an FPGA than on a RISC processor. However, algorithms whose functions are data-dependent and conditional in nature are more suited for implementation on a PowerPC. Mercury's FPGA solution implements an architecture where FPGAs and PowerPCs are combined in a RapidIO fabric. An application can be partitioned across FPGAs and PowerPCs for maximum effectiveness. Parts of the application that are simple, fixed-point computations can run on an FPGA, saving space, power, and money. Other parts of the application can run on the PowerPC, which is easier to program, so the overall development time is kept manageable while the performance is maximized.

Scalability

FPGAs in the RapidIO environment become part of a scalable system that can expand to provide as many FPGAs and PowerPC microprocessors as changing applications demand, with minimal application recoding and redeployment expense. Multiple PowerStream 7000 FCN boards can be deployed in a single PowerStream 7000 chassis, along with other boards carrying I/O devices and RISC processors, communicating via a RapidIO switch fabric. FCN modules can be installed in the processor slots of the PowerStream 7000 system, including up to 23 modules in the full-size chassis.

Developers can create and test algorithms on small laboratory systems consisting of only a few processors, with the assurance that the resulting code can move seamlessly to larger deployment platforms. Additionally, as processing requirements change in future program generations, they can readily resize target platforms with minimal impact to their code.

FPGA Developer's Kit (FDK)

The FPGA Developer's Kit (FDK) simplifies and accelerates the development of FPGA-based applications. The FDK suite contains off-the-shelf, ready-to-use IP components for managing input and output data flows, memory transfers, and the RapidIO interface in FPGA applications. Configurable wrapper modules are provided that can be used to compose these IP modules into a complete FPGA design.

The FDK has a set of run-time libraries that can be linked with applications written under the Mercury MCOE™ operating environment, enabling these applications to seamlessly integrate FCN modules into the heterogeneous system, while maintaining a common operating environment. These functions include shared memory buffer (SMB) support for the FCNs, and DX DMA transfer capabilities. Also included is the RoC framework, which is an on-chip communication mechanism among different IP modules on an FPGA. Users can reduce application development time by joining FDK modules with their own algorithm-specific modules to create complete FPGA bitstreams without the costly overhead of reinventing the supporting infrastructure elements.

In effect, the intellectual property of the FDK enables each FPGA compute node to operate as a fully functional RapidIO compute node, capable of reading and writing to local and remote memory locations across the switch fabric. This functionality frees developers to concentrate on coding inner loops for the FPGA platform, and provides them with interfaces for connecting their computational modules with the underlying RapidIO system.

To jump-start the creation of complete application solutions, a Mercury diagnostic bitstream is part of the FDK. When loaded into the FPGA, this bitstream enables system software to monitor system health through a series of tests, including memory test, DMA test, and an I/O loopback test. For the PowerStream 7000 FCN, the diagnostic bitstream also includes a pattern generator and link checker for the 10-Gbps fiber interfaces. The Mercury diagnostic bitstream and other included example designs serve as application examples and are fully documented.

The FDK components are built for easy integration with the leading FPGA development tools available on the market, including Xilinx® ISE, Synplicity Synplify®, and Mentor Graphics ModelSim®. The Xilinx ChipScope™ Pro logic analyzer can also be used while developing applications for the PowerStream 7000 FCN for improved observability of FPGA operations. Note that the FDK does not include these tools; they must be provided by the customer.

Mercury also provides a complete VHDL simulation environment or "harness" that models the FPGA compute node. This environment provides a bus functional model (BFM) for RapidIO communications and other I/O, as well as for SRAM and DRAM attached to the FPGA. The simulation environment enables verification of FPGA applications prior to deployment on final-mission hardware and allows regression test suites to run with a single command.

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Off-the-Shelf IP for RapidIO and Memory Interfaces

Through the FDK, Mercury delivers the PowerStream 7000 FCN module with intellectual property for the RapidIO fabric interface, memory transfers, and I/O management. Users need only incorporate their application-related algorithmic firmware to create complete FPGA bitstreams. If desired, Mercury can help customers create their FPGA-based solutions, or Mercury can be contracted to develop the FPGA-resident portion of an application for a complete turnkey solution.

Specifications

Module Specifications

FPGA compute nodes	3
FPGA processor	Xilinx XC2VP70-6

SRAM

Capacity per FPGA	32 MB
Bandwidth per FPGA	5.6 GB/s full-duplex (peak)

DRAM

Capacity per FPGA	128 MB
Bandwidth per FPGA	2.8 GB/s (peak)
Parallel RapidIO ports per FPGA	1
Fiber links	2 pairs at 10 Gbaud each, full-duplex (1 on each of 2 FPGAs) 850 nm multi-mode fiber with LC connectors
Copper serial links per FPGA	5 at 3.125 Gbaud to each other onboard FPGA, full-duplex 4 at 3.125 Gbaud off board (12 total to front panel)
LVDS lines per FPGA	8 pairs to a front-panel connector (24 pairs total)

Electrical/Mechanical Specifications

Input voltage	48.0 VDC ±5%, main power 5.0 VDC ±5%, management power

Input voltages measured at the backplane pins inclusive of all ripple. Mercury strongly recommends that system-level power designs use a ±2% margin to avoid any potential issues with respect to the system-level operating characteristics and operating environment.

Power	190W (typical max, depends largely on application IP)
Dimensions	M155 format
Slot spacing	1.057 in

Environmental Specifications

Minimum airflow (per slot at sea level)	8 CFM per stacked pair	
Temperature*		
	Operating	0°C to 35°C (stacked pair, sea level)
	Storage	-55°C to +85°C
Rate of change	5°C/min	
Humidity	5-95% (non-condensing)	
Vibration		
	Random	0.02g²/Hz, based on 20 to 2,000 Hz, 1 hr/axis
	Shock	50g in all axes, 11 msec, half-sine
Altitude*		
	Operating	0 to 30,000 ft
	Storage	0 to 50,000 ft
Salt/Fog	Consult factory	

*As altitude increases, air density decreases and, therefore, the cooling effect of a particular number of CFM decreases. Different limits can be achieved by trading among altitude, temperature, performance, and airflow. Contact Mercury for more information.

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