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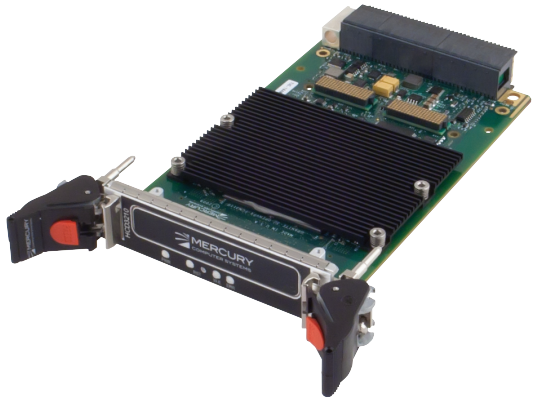
Ensemble™

DATASHEET

MERCURY COMPUTER SYSTEMS™

Ensemble 3000 Series HCD3210 3U OpenVPX Processing Module

High-Density Compute Power with Built-in I/O Capabilities



- High-bandwidth off-board and on-board data paths
- Single slot solution for data acquisition and multi-stage processing
- Rugged versions for harsh environments
- Identical software architecture across Mercury products
- Designed and architected for OpenVPX™ interoperability

The Ensemble™ 3000 Series HCD3210 3U OpenVPX™ Processing Module from Mercury Computer Systems is a single-slot solution for data acquisition and processing. By combining the performance logic of a highly capable Xilinx® Virtex™-6 FPGA with the real-time processing power of a Freescale™ MPC8640D dual-core processor, the HCD3210 supports multi-stage processing for many applications. The addition of the HCD3210's XMC mezzanine site delivers I/O to these powerful processing elements, supporting a single-slot high-performance processing architecture for size, weight, and power (SWaP)-constrained platforms. The multi-plane OpenVPX architecture of the HCD3210 also allows users to scale, knitting together multiple HCD3210s into a powerful processing subsystem.

Designed for High-Performance Processing

The HCD3210 uniquely combines two complementary styles of processing in a single, small form-factor OpenVPX module, creating a unique processing complex that can support a myriad of customer applications.

The Virtex-6 FPGA is a core element of the HCD3210, supplying high-performance processing power to the 3U module. The HCD3210 supports the LX365T as the default FPGA, with the option to support other Virtex-6 FPGAs with the same footprint. FPGA bitstream images can be loaded from the 128-MB on-board flash memory, which can hold up to four distinct images. The FPGA processing complex includes both QDRII SRAM and DDR3 SDRAM memories. Two 9-MB banks of QDRII SRAM are provided for high-speed memory access, as well as 128 MB of DDR3 SDRAM for buffering and other uses. The FPGA processing complex has I/O interfaces to the on-board PCI Express® switch and directly to the backplane, as well as to the local XMC user I/O interface.

The on-board MPC8640D dual-core processor complex utilizes two standard e600 processor cores, one DDR2 memory controller, 1 MB of L2 cache, and a flexible system-on-chip I/O subsystem. The dual e600 cores that make up the heart of the chip are inherited from the MPC7448 processor, and each retains the high-performance AltiVec™ vector-processing unit. Algorithms optimized for the AltiVec engine port seamlessly to the MPC8640D. Additionally, increased bandwidth between both memory and external I/O and the processing cores allows efficient processing beyond that available with prior families of Freescale processors.

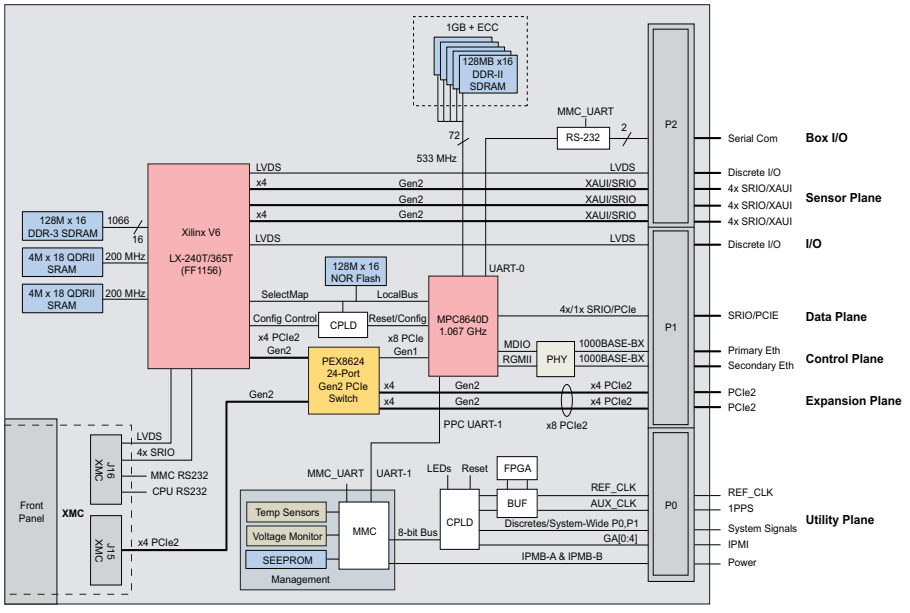


***Figure 1**. HCD3210 functional block diagram*

Mezzanine Card Flexibility

The HCD3210 has a flexible XMC mezzanine site to bring incoming I/O to its on-board processing resources. The standard mezzanine site on the HCD3210 module can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control functions. XMCs are supported with x4, and x1 PCIe (Gen1 or Gen2) supported on the J15 connector per the VITA 42.3 standard and linked to the local PCI Express switch. An x4 high-speed Gen2 SERDES interface and 12 LVDS pairs for XMC user I/O are linked to the Virtex-6 FPGA via the J16 connector.

PCI Express Architecture

The HCD3210 provides a 24-lane PCI Express switch for both on-board switching and off-board expansion. This Gen2 switch provides an x4 PCIe Gen2 interface to the XMC site and the Virtex-6 FPGA. A x8 PCIe Gen1 interface is provided to the MPC8640D processor. This balanced approach allows mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem. Externally, the HCD3210 implements a full x8 PCIe connection to the OpenVPX expansion plane on the P1 VPX connector. This expansion-plane interface allows the HCD3210 to tightly couple with other co-processing modules at the subsystem level. The x8 PCIe connection can be user-configured as dual x4 connections. These configuration options let the module effectively act as an upstream/downstream PCIe switch to allow "chaining" of PCIe devices.

Off-board Communications

In addition to two powerful processing options, the HCD3210 supports application flexibility and throughput with a variety of I/O choices:

- High-speed I/O to the Virtex-6 FPGA is provided by three x4 SERDES interfaces to the P2 VPX connector. These interfaces can bring I/O to the FPGA, or be used for inter-FPGA communications in systems with multiple processing modules.
- An x4 Serial RapidIO interface is provided natively by the MPC8640D processor and routed to the P1 VPX connector as the OpenVPX data plane.
- As described above, a x8 PCIe interface is linked from the PCIe switch to the P1 VPX connector as the OpenVPX expansion plane.
- Dual 1000BASE-BX Gigabit Ethernet interfaces provide control-plane capability to the HCD3210.
- Serial communications are supported by an RS-232 interface to the MPC8640D processor.

System Management Capabilities

The HCD3210 module follows OpenVPX design principles by leveraging the robust, scalable, and well-tested system management infrastructure from the AdvancedTCA®/MicroTCA® architecture. Using the standard I^2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the draft VITA 46.11 standard. This allows the HCD3210 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module FRU (field replaceable unit) information
- Be managed remotely by a Chassis Manager at the system level, such as implemented on the OpenVPX SFM3010 Module

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces, such as RapidIO®. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard – REDI (VITA 48). The HCD3210 module is implemented as a 3U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments. The HCD3210 module can be configured for 1.0" pitch slots in both air-cooled and conduction-cooled configurations.

Targeted primarily for harsh-environmentembedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period, minimizing the potential of damage to the board.

Additional Features

The HCD3210 module provides the features typically found on a single-board computer. In addition to the sophisticated management subsystem and I/O interconnect, the HCD3210 module provides users with a toolkit enabling many different application use cases. Features include:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer that can interrupt the processor upon expiration or reset the processor

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Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the HCD3210 module. Because the processor, memory, and surrounding technologies are leveraged across product lines, software developed on the HCD3210 module can interface seamlessly with other Mercury products. The same Linux® or VxWorks® development and run-time environment is implemented on the HCD3210 module as on other Mercury platforms across the Ensemble 3000, 5000, and 6000 Series.

The MultiCore Plus® (MCP) open software environment gives the HCD3210 module access to a wide ecosystem of stacks, middleware, libraries, and tools. A key software package available for the HCD3210 module is MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the multiple on-chip cores available with the MPC8640D dual-core processor. The MCP software environment also lets applications use industry-standard middleware, such as MPI, DRI, CORBA, or standard TCP/IP sockets ported to run seamlessly over the fabric.

Open Standards Mean Interoperability and Planning for the Future

The OpenVPX Industry Working Group is an industry initiative launched by defense prime contractors and commercial system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application-specific reference solutions. These VITA 65 standard solutions provide clear design guidance to suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX System Specification was ratified as VITA 65 by the VSO in February 2010.

Specifications

Form Factor	3U OpenVPX
OpenVPX Module Profile	MOD3-PAY-1F2F2U

FPGA Compute Node

Xilinx Virtex-6 (LX365T default)	1
QDRII SRAM (200 MHz clock)	Two 9-MB banks
DDR3-900M SDRAM	128 MB

General Purpose Processor

Dual-core MPC8640D	At 1.06 GHz
Cores per device	2
DDR2 SDRAM	1 GB at 533 MHz

XMC Mezzanine Site

XMC sites	1
PCI Express XMC site per VITA 42.3	
XMC user I/O to on-board FPGA	

Data/Control/Management/Expansion Planes

Data plane
- One x4 serial RapidIO link to backplane from MPC8640D processor
  - Configurable as PCI Express, if required

Expansion plane
- One x8 PCI Express interface to backplane from PCIe switch
- User configurable to dual x4 interfaces

Control plane
- Two 1000BASE-BX Gigabit Ethernet interfaces to the backplane

Management plane
- I^2C interface to backplane running IPMI protocol

Off-board Communications

x4 SERDES interfaces to backplane from FPGA	2
LVDS pairs to backplane from FPGA	12
RS-232 serial interface to 8640D processor	1

System Management

On-board IPMI Controller
Voltage and temperature monitor
Geographical address monitor
Power/reset control
FRU and on-board EEPROM interfaces
FPGA, CPU, and CPLD interfaces

Additional Resources

Real-time clock
Watchdog timer
General-purpose 32-bit timers/counters

Environmental

Air-Cooled – Commercial

Temperature	
Operating	0°C to 40°C*
Storage	-40°C to +85°C

*Customer must maintain required cfm level.

Humidity	
Operating	10-95%, non-condensing
Vibration	0.003 g^2/Hz; 20-2000 Hz, 1 hr/axis
Shock	20g, z-axis; 32g, x-, y-axes; 11 ms half-sine pulse
Altitude	
Operating	0-10,000 ft*

*Customer must maintain required cfm level.

Conduction-Cooled – Mercury Rugged Level 3

Temperature	
Operating	-40°C to +71°C at the card edge*
Storage	-55°C to +125°C

*Customer chassis must maintain card edge at 71°C.

Humidity	
Operating	0-100%
Vibration	0.1 g^2/Hz, based on 5-2000 Hz, 1 hr/axis
Shock	50g, z-axis; 80g, x-, y-axes; 11 ms half-sine
Altitude	
Operating	0-70,000 ft

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