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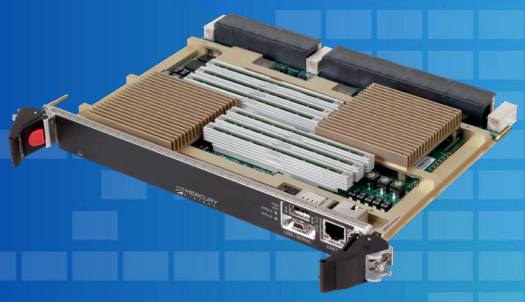
DATASHEET

Ensemble® 6000 Series OpenVPX Intel Xeon Dual Quad-Core HDS6600 Module

Industry-Leading Performance for Rugged Intel® Signal Processing

MERCURY COMPUTER SYSTEMS™

- **6U OpenVPX™-compliant VITA 65/46/48 (VPX-REDI) nodule**
- **Two quad-core Intel Xeon processors at 1.73 GHz for total of 110 GFLOPS peak**
- **Includes POET™, Mercury's protocol-agnostic, multi-standard switch-fabric technology**
- **MultiCore Plus¨ software infrastructure support**
- **Integrated 80-lane PCI Express® switching infrastructure for on-board and off-board co-processing expansion-plane communications**
- **MultiCore Plus® software infrastructure support**



The Ensemble™ 6000 Series OpenVPX Intel Xeon Dual Quad-Core HDS6600 Module from Mercury Computer Systems is a high-density signal and data processing engine, harnessing two of the latest generation of server-class Nehalem-based quad-core Intel Xeon processors for the most demanding applications. The HDS6600 is equipped with a next-generation FPGA for fabric bridging/switching and user application functions, and provides high-bandwidth on-board and off-board communication fabrics in a standard 6U OpenVPX form factor.

By leveraging the power of Intel high-density Xeon processing in combination with the on-board integrated high-performance PCI Express and fabric infrastructure, the HDS6600 delivers a well-balanced and scalable computing architecture, capable of providing groundbreaking levels of processing power for high-end radar, signals intelligence, and image and packet processing applications.

The HDS6600 module is compliant with the VITA 65 module profile MOD6-PAY-4FIQ2U2T012.2.1 with its initial POET instantiation, and is supported in chassis slots compliant with VITA 65 slot profile SLT6-PAY.4F1Q2U2T-10.2.1. Future POET instantiations may allow the HDS6600 to support additional or different VITA 65 module profiles.

Intel Xeon Jasper Forest Nehalem-Class Processor

The HDS6600 features two 64-bit Xeon Nehalem-class quad-core Jasper Forest LC5518 processors. In an industry-first, the HDS6600 utilizes unique packaging technologies to support two instances of a Land Grid Array (LGA) processor in a rugged embedded platform. The dual quad-core processors are linked via the high-speed low-latency QPI interface, which operates with a 19.26 GB/s transfer rate. Each processor can deliver approximately 55 GFLOPS (peak), with three high-speed DDR3-1066 memory channels capable of 17 GB/s raw bandwidth each, for a total peak of 110 GFLOPS and 102 GB/s of raw memory bandwidth.

The HDS6600 supports configurations with 12 to 24 GB of DDR3 SDRAM on-board. The LC5518 Jasper Forest processor supports Gen2 PCIe natively, linking the processing resources directly to the I/O sources on the module. The module also makes use of the Ibex Peak BD3420 Platform Controller Hub (PCH) chipset, which provides additional I/O bridging between the Intel processor and external devices.

The Xeon LC5518 Jasper Forest processor includes a very large 8 MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The Jasper Forest processor supports both the SSE4.1 and SSE4.2 instruction sets, allowing high-performance algorithm development that is portable to future Intel architectures.

POET Fabric Interconnect Technology

The HDS6600 combines the processing power of the Xeon family from Intel with Mercury's protocol-agnostic, multi-standard switch fabric technology, POET (Protocol Offload Engine Technology). POET brings the high-bandwidth, low-latency performance of switch fabrics to the HDS6600, providing the bandwidth necessary to eliminate data starvation and to fully utilize the processing power of Intel Xeon technology.

The HDS6600 POET instantiation supports both the high-bandwidth, low-latency, serial RapidIO switch fabric, and the highly successful 10 Gigabit Ethernet protocol. When configured for 10 Gigabit Ethernet, POET provides the offload and acceleration capability to support standard Ethernet operations with guaranteed deterministic delivery.

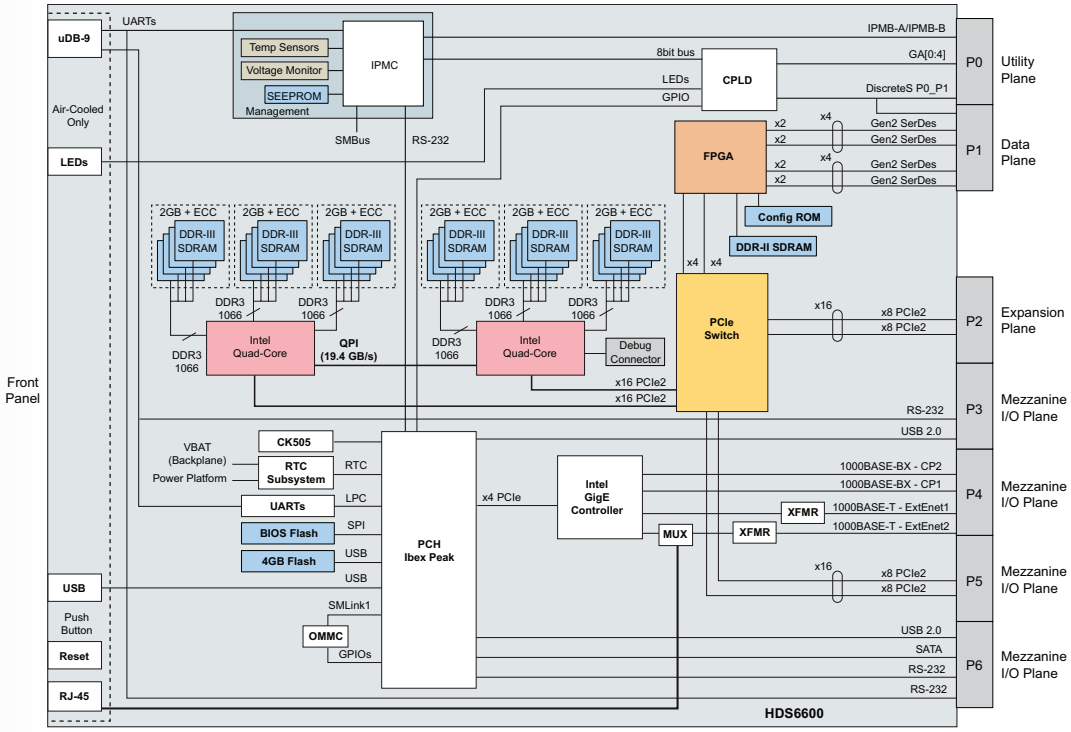


Figure 1. *HDS6600 block diagram*

PCI Express Architecture

The HDS6600 provides a high-end 80-lane PCI Express® switch for both on-board switching and off-board expansion. Each LC5518 Jasper Forest processor is linked to the PCIe® switch via a full x16 interface. The Gen2 switch also provides dual x4 interfaces to the on-board FPGA, allowing bridging to the data plane. These x4 PCIe interfaces can optionally be passed through directly to the backplane in systems where a PCIe data plane is required. Externally, the HDS6600 implements a full x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion-plane interface enables the HDS6600's compatibility with Mercury's GPU or FPGA based co-processing modules.

The x16 PCIe connection can be user-configured as dual x8 connections. These configuration options let the module effectively act as an upstream/downstream PCIe switch to allow chaining of PCIe devices. A similarly featured additional x16 PCIe interface is routed to the VPX P5 connector.

Multiple I/O Options

The HDS6600 offers a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection can be routed to the front panel on air-cooled configurations or to the backplane on conduction-cooled configurations.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection is routed to the backplane
- Two 1000BASE-T SERDES Ethernet connections are routed to the backplane per the OpenVPX control-plane specification.
- One RS-232 serial port can be routed to the front panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either RS-232 or RS-422 signaling.
- One front-panel USB 2.0 interface is available on air-cooled configurations only.
- Two backplane USB 2.0 interfaces are available with both air-cooled and conduction-cooled configurations.
- Two SATA interfaces to the backplane are provided to easily interface with storage devices.
- Two RS-422 interfaces and 16 GPIO interfaces are routed from the on-board FPGA to the backplane.
- Eight GPIO lines act as discrete I/O, usable as input, output, or to generate interrupts on the module.
- Several additional bused signals can be used to enhance the functionality of the module.

System Management Plane

The HDS6600 implements the advanced system-management functionality architected in the OpenVPX™ Specification to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the VITA 46.11 standard. This allows the HDS6600 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module field replaceable unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on the OpenVPX SFM6100 module

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VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard - REDI (VITA 48). The HDS6600 module is implemented as a 6U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period, minimizing potential damage to the module.

Additional Features The HDS6600 provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, it provides users with a toolkit enabling many different application use cases. Features include:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support interrupt or reset
- Power up/down the entire module
- Multiple boot paths, include netboot, USB boot, and boot from SATA or the on-board 2GB flash device

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the HDS6600 module. Because the processor, memory and surrounding technologies are leveraged across product lines, software developed on the HDS6600 module can interface seamlessly with other Mercury products. The same Linux® or VxWorks® development and run-time environment is implemented on the HDS6600 module as on other Mercury platforms across the Ensemble 3000, 5000, and 6000 Series.

The MultiCore Plus® (MCP) open software environment gives the HDS6600 module access to a wide ecosystem of stacks, middleware, libraries and tools. A key software package available for the HDS6600 module is MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the multiple on-chip cores available with the Intel Jasper Forest Xeon quad-core processor.

Software support is available on the HDS6600 module for the following products:

Features include:

- Support for Mercury's standard numeric libraries, VSIPL and SAL (Scientific Algorithm Library), as well as their multi-core variants, is Open development Suite for Linux is an Eclipse-based integrated optimized for the Intel Xeon architecture of the HDS6600 module.
- Open Development Suite for Linux is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker, and a graphical source browser. Mercury provides extensions that allow multiprocessor-aware process launch and debug, as well as a System Supervisor view that allows graphical remote management.
- Support is provided for the Wind River Workbench integrated development environment when the module is running Wind River Linux or VxWorks.
- Interprocessor Communication System (ICS) support is carried forward from the RACE++®/MCOE™ software environment. ICS provides a low-level interprocessor communication API that lets users take advantage of the high-bandwidth, low-latency serial RapidIO fabric with an easy-to-use software interface.
- The Performance Kit provides low-level handles for manipulation of the serial RapidIO fabric and can be used for simple data movement, or as a base on which to build a custom middleware layer.
- Trace Analysis Tool and Library (TATL™) is a "Logic analyzer for software" that provides insight into the dynamic interaction of up to a few hundred processors.

The MCP software environment lets applications use industry standard middleware such as MPI, DRI, CORBA or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE into the MCP domain.

Open Standards Mean Interoperability and Planning for the Future The OpenVPX™ Industry Working Group is an industry initiative launched by defense prime contractors and commercial system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application specific reference solutions. These OpenVPX standard solutions provide clear design guidance to suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX System Specification was ratified by the VSO in February 2010.

Specifications

Intel® 45-nm Nehalem-Class Processor

Quad-core LC5518 Jasper Forest 2 at 1.73 GHz each

Peak performance 55 GFLOPS

Threads per core 2

QPI interface between processors 19.2 GB/s peak performance Intel¨ Virtualization Technology

Integrated x16 Gen2 PCI Express¨ interface

DDR3-1066 12 GB with ECC (up to 24 GB future capability)

Raw memory bandwidth BIOS SPI flash

NAND flash

51 GB/s 8 MB 2 GB

Altera Stratix® IV EP4SGX180 Field-Programmable Gate Array (FPGA)

Logic elements	175,000
Internal memory	11.7 Mb
18x18 multipliers	920
16 SerDes	600 Mbp to 6.25 Gbps per SerDes
High-performance	184 GMACs 200 MHz
DDR3 SDRAM	Up to 128 MB 1066 MT/s

Provides fabric bridging to data plane

Can act as co-processor executing iFFT/FFT, image or signal processing

Configured from CPU or dedicated configuration ROM

Ethernet Connections

1000BASE-BX Ethernet to P4 connector	2

OpenVPX Control Plane

10/100/1000BASE-T Ethernet to P4 connector	1

Accessible via OpenVPX RTM or external chassis interface

10/100/1000BASE-T Ethernet connection 1

to front panel (air-cooled module)

or backplane (conduction-cooled module)

Ethernet functions supported by the chipset include:

UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority), and 802.1Q (VLAN)

IPMI (System Management)

On-board IPMI controller

Voltage and temperature monitor

Geographical address monitor

Power/reset control

FRU and on-board EEPROM interfaces

FPGA, CPU, and CPLD interfaces

OpenVPX Multi-Plane Architecture

System Management via IPMB-A and IPMB-B link on P0 management plane

Dual 4x serial RapidIO or 10 Gigabit Ethernet interfaces on P1 data plane

Full x16 or dual x8 PCIe® expansion plane

Dual 1000BASE-BX Ethernet control plane

Additional I/O Capabilities

RS-232 serial interface to front panel	1

(air-cooled) or backplane (conduction-cooled)

Configurable for RS-422 signalling when routed to backplane

Front-panel USB 2.0 interface	1

(air-cooled configurations only)

USB 2.0 interfaces to backplane	2
SATA interfaces to backplane	2
Single-ended GPIO interfaces to backplane	8

System signals to backplane

NVMRO, ChassisTest, Environmental Bypass, MemoryClear

Mechanical

6U OpenVPX™ (air-cooled and conduction-cooled)

1.0" slot pitch

OpenVPX and VPX REDI

Environmental Air-Cooled - Mercury Rugged Level 1

Temperature

Operating	-25°C to +55°C*
Storage	-55°C to +85°C

*Customer must maintain the required cfm level.

Humidity

Operating	5-95%, non-condensing
Vibration	0.04 g2/Hz; 20-2000 Hz; 1 hr/axis
Shock	50g z-axis; 80g x-, y-axis; 11 ms half-sine

Altitude

Operating	0-30,000 ft*

*Customer must maintain the required cfm level.

Conduction-Cooled - Mercury Rugged Level 3

Temperature

Operating	-20°C to +71°C at the card edge
Storage	-55°C to +125°C

Humidity

Operating	0-100%
Vibration	0.1 g2/Hz, based on 5-2000 Hz, 1 hr/axis
Shock	50g z-axis; 80g x-, y-axis; 11 ms half-sine
Altitude	0-70,000 ft*

*Customer chassis must maintain card edge at 71°C.

Specification Compliance

OpenVPX System Specification encompasses:

VITA 46.0, 46.3, 46.4, 46.6, 46.11, and VITA 48.1, 48.2 (R E D I)

Serial RapidIO®, PCI Express®, 10 Gigabit Ethernet

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