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Computer Systems, Inc.
MERCURY



NEW

RACE++ Series
Memory Daughtercards

Up to 512 MB and 533 MB/s per Daughtercard

High-Performance Memory System

Error Detection and Correction

Advanced DMA Engine for Chained Sub-Matrix Moves

Scalable from Two to Hundreds of Nodes

Full Compatibility with ANSI/VITA RACEway Systems

Applications with large data sets often require more memory than is found on processor daughtercards. The RACE++™ Series Memory Daughtercards from Mercury Computer Systems provide the extra storage close to the processors, with access speed approaching that of local memory. Each daughtercard contains two memory banks, each with a DMA controller that provides direct read/write access to the memory through the high-performance RACEway interfaces to the RACE® and RACE++ Series motherboards.

The RACE++ Series Memory Daughtercards are designed for the most demanding image and signal processing applications. The advanced DMA engine provides both command chaining and strided accesses. These features lower communications overhead and increase performance for applications with unrelenting high-bandwidth data streams.

Memory Nodes

The RACE++ Series Memory Daughtercards contain two memory nodes. Each memory node consists of 128 or 256 MB synchronous DRAM (SDRAM) and the Mercury-designed ASIC that is also used on the PowerPC™ 750 compute nodes (see illustration). This interface ASIC provides a high-performance memory controller and high-speed network interface to the RACEway interconnect.

Systems can be configured to support from two to hundreds of nodes in a standard VME environment spanning multiple VMEbus slots.

DMA Controller

Each memory node has an advanced DMA controller to support RACEway transfers at 267 MB/s with chaining and striding. The DMA controller is managed by a processor node anywhere on the RACEway switching fabric. With chained DMA, the DMA controller works from a linked list in memory so that a complex chain of DMA requests requires no overhead from remote processors. DMA requests also support nonsequential access to and from memory on the daughtercard. This strided DMA capability enables high-performance sub-matrix transfers as required for distributed 2-D applications in image processing and synthetic aperture radar (SAR).

High-Performance Memory System

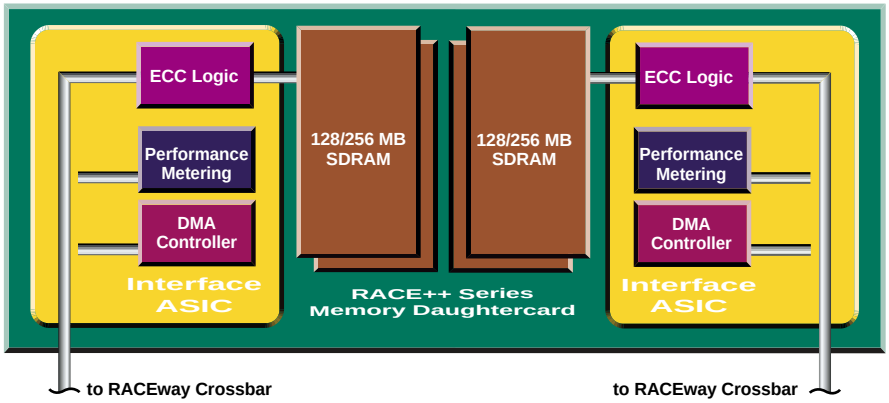
The Mercury interface ASIC offers a high-performance memory system, allowing the memory subsystem to reach the intrinsic limits of its performance capability with:

- Synchronous DRAM – allows fastest available bus frequency and highest data access rate.
- Error-correcting circuitry – provides improved data integrity. One-bit errors are corrected on the fly, and multi-bit errors generate an interrupt error condition.

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Performance Metering Logic

Memory nodes provide non-intrusive hardware performance metering facilities that enable application performance tuning and real-time data-flow analysis, essential for developing real-time multi-computer applications. A memory node can be directed to collect performance metrics on memory bandwidth utilization, RACEway crossbar port usage and contention, or memory contention. The information can be used to locate sub-optimal code sections during execution of the application.



RACEway Broadcast Support

The memory node supports RACEway crossbar broadcast capabilities for enhanced bandwidth utilization. As the initiator of a broadcast, the DMA controller may issue any of the broadcast or multicast modes provided by the RACEway crossbar. As a receiver of broadcast data, the memory node has the programmable option of accepting or ignoring the data.

Daughtercard Configurations

To meet exact application requirements, RACE++ Series motherboards can be populated with any proportion of memory daughtercards – from all memory to none.

Software

The RACE++ Series Memory Daughtercards are supported by Mercury's heterogeneous software package for its RACE and RACE++ Series systems. This software package provides a common development and runtime environment supporting multiple processor types, memory, and I/O in the same system. This environment allows system designers to optimize for performance, low cost, and maximum processor density.

Commercial/Environmental Specifications

Operating temperature	**0ºC to 40ºC at an altitude of 10,000 feet (inlet air temperature at motherboard's recommended minimum airflow)**
Storage temperature	**-40ºC to 85ºC**
Relative humidity	**10 to 90% (non-condensing)**

As altitude increases, air density decreases, hence the cooling effect of a particular number of CFM decreases. Many manufacturers specify altitude and temperature which are not simultaneous. Notice that the above operating temperature is specified simultaneously with an altitude. Different limits can be achieved by trading among altitude, temperature, performance, and airflow.

Daughtercard Mechanical Specifications

Weight (pounds)	**0.26**
Dimensions (inches)	**5.000 x 4.435**

Memory Daughtercard Configurations

	MEM2C128B	MEM2C256B
Configuration:		
RACEway ports 2	**2**	
RACEway throughput (MB/s)	**533**	**533**
Memory nodes 2	**2**	
DRAM per node (MB)	**128**	**256**
DRAM per daughtercard (MB)	**256**	**512**

Computer Systems, Inc.
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