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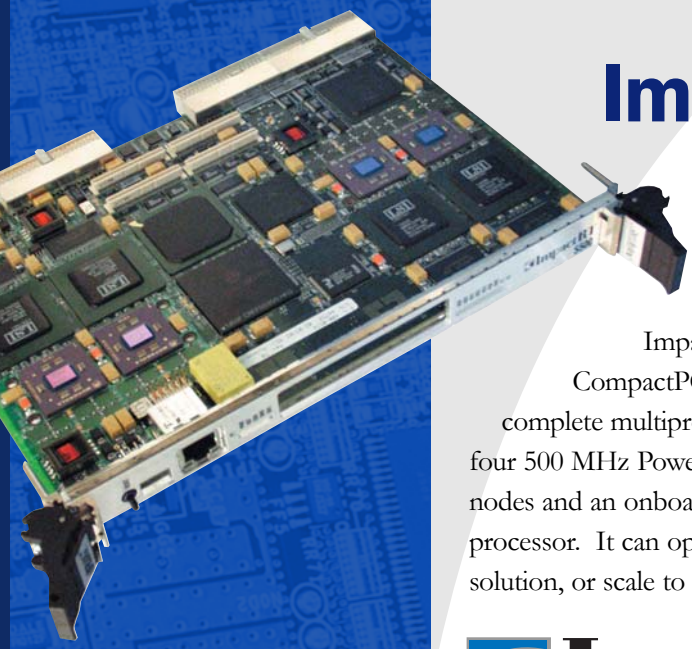
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Find the *Mercury Computer Systems ImpactRT S500* at our website: *Click HERE*

Computer Systems, Inc.
MERCURY

ImpactRT S500 cPCI System Board



Four PowerPC 7410 Processors with AltiVec Technology

Onboard MPC 8240 VxWorks Host

Scales to 32 processors

66.66 MHz RACE++ Switch Fabric Interconnect

PMC Site

Full Support for RACE Software

The Mercury Computer Systems ImpactRT™ S500 CompactPCI system board is a complete multiprocessing system with four 500 MHz PowerPC® 7410 compute nodes and an onboard PowerPC 8240 host processor. It can operate as a single-board solution, or scale to a multi-board configuration connected by a RACE++® Series cable, passive interconnect boards, or a switch fabric interlink module.

ImpactRT™

Designed for the multicomputing of large data streams, ImpactRT systems are fully supported by Mercury's field-proven set of software tools, libraries, and APIs focused on high-performance signal and image processing applications. This combination of hardware and software makes ImpactRT S500 systems the ideal platform for cost-effective signal and image processing.

RACE++ and CompactPCI

The ImpactRT S500 combines the leading-edge performance of PowerPC 7410 processors with a high-bandwidth RACE++ communications fabric in a single-board CompactPCI (cPCI) form factor. RACE++ connections between processors onboard the system board enable high-bandwidth processing and real-time performance in the 6U cPCI form factor. An eight-port crossbar provides high-speed communications paths among the compute nodes and the I/O ports.

The CompactPCI architecture provides inherent advantages such as its natural degree of ruggedness and the ability to interact with the rapidly growing number of cPCI input/output cards. These features help control development costs and simplify the insertion of new technology with off-the-shelf components.

High-Performance Compute Nodes

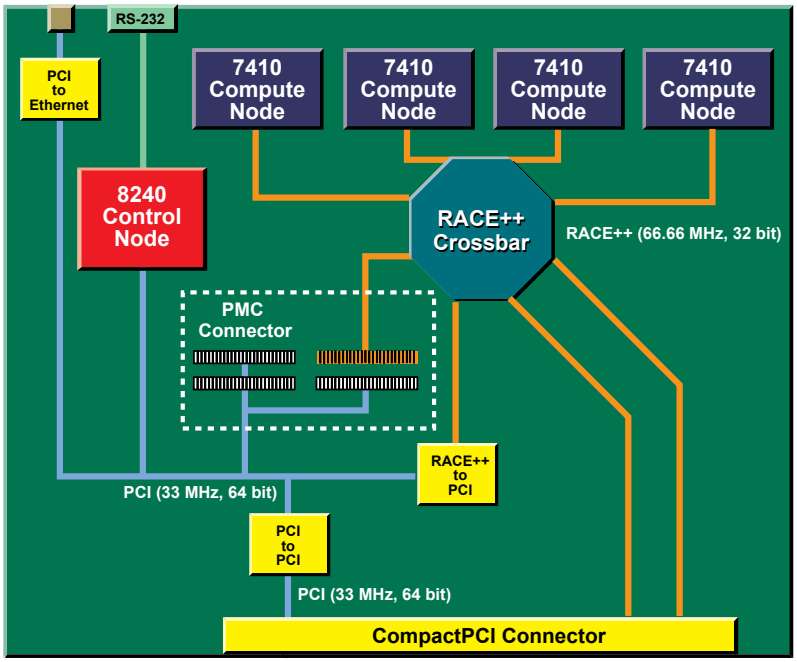
Each ImpactRT S500 board contains four 500 MHz PowerPC 7410 processors with AltiVec™ parallel vector execution units. Each processor is part of a compute node (CN) that also includes 128 MB of SDRAM, 2 MB of L2 cache, and an ASIC that connects the node to the RACE++ fabric. The AltiVec vector processing unit revolutionizes the performance of computationally intensive applications such as image and signal processing by operating on up to four floating-point numbers or up to sixteen 8-bit integers with a single instruction.

High-Performance Switch Fabric

As the latest version of the RACE Series™ architecture, RACE++ is designed

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ImpactRT S500 cPCI Board Architecture



specifically for the real-time multicomputing of large data streams. Implementing a switch fabric interconnect, RACE++ systems use eight-port crossbars to provide multiple simultaneous data transfers between processors, memory, and I/O, with each connection providing a 267 MB/s peak data path. By providing these dynamic point-to-point connections, RACE++ eliminates the bottlenecks found in systems that use buses to connect processors.

In the ImpactRT S500 system board, Mercury's field-proven RACE++ technology is joined with the widely accepted CompactPCI standard. In addition to the RACE++ communications between processors, the board supports PCI communications through its CompactPCI connector to a broad range of CompactPCI devices. RACE++ and PCI communications can occur simultaneously, increasing the overall available system bandwidth.

Onboard Host Processor

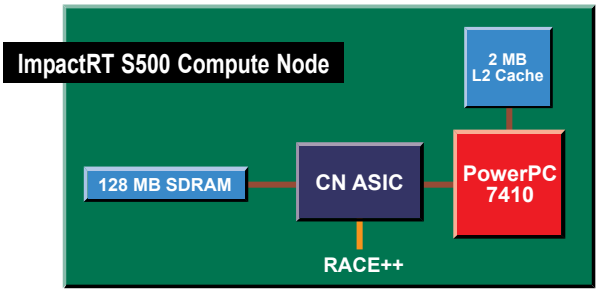
Each ImpactRT S500 includes an onboard Motorola 8240 control processor capable of running the VxWorks® real-time operating system. This processor can act as the runtime host and manages the configuration and loading of the RACE++ compute nodes. The host implements a flash boot capability, and all four PowerPC 7410 compute nodes can be booted from the 8240 host's flash memory, or over the network using standard NFS-mounted file systems. The host also can be used to control any devices connected to the onboard PMC (PCI Mezzanine Card) connector. A VxWorks BSP (Board Support Package) is available.

Compatibility

The ImpactRT S500 board is fully compatible with applications developed for RACE++ systems using other form factors. It is supported by the Mercury RACE++ multiprocessor software environment, a proven and comprehensive set of libraries, APIs, and tools all focused on creating high-performance signal and image processing applications. Each compute node supports the MC/OS™ multicomputer operating environment, the RACE++ Series MULTI® IDE, the Parallel Acceleration System (PAS™), the Scientific Algorithm Library (SAL), Supervisor, and the TATL™ Trace Analysis Tool and Library. Software can be developed for ImpactRT cPCI systems using Windows NT® or Solaris™ hosts.

High-Performance Design

The CN ASIC, included in each compute node, acts as both a memory controller and as a network interface to the RACE++ switch fabric interconnect. The CN ASIC includes an enhanced DMA controller, a high-performance memory system with error checking and correcting, performance metering logic, and a RACE++ interface. By combining memory control and the network interface into a single chip, Mercury's compute node ASIC provides the highest performance with both the lowest power consumption and the highest reliability.



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Mercury's high-performance memory subsystem allows memory to reach the intrinsic limits of its performance capability with:

125-MHz Synchronous DRAM - provides the optimum match to the 500 MHz clock frequency of the PowerPC 7410 processor.

Prefetch Buffers - bring sequential data to the ASIC ahead of explicit requests by the processor. These prefetch buffers greatly improve the performance of the CN in vector operations such as those used in DSP applications.

FIFO Buffers - efficiently overlap accesses to SDRAM from the local processor and the RACE++ interconnect.

The compute node contains error-correcting circuitry for improved data integrity. One-bit errors are corrected on the fly, and multi-bit errors generate an interrupt error condition.

Enhanced DMA Controller

Each compute node has an advanced DMA controller to support data transfers at 267 MB/s through its RACE++ port with chaining and striding. In chained DMA, the controller works from a linked list in memory so that a complex chain of DMA requests requires no overhead from remote processors. DMA requests also support nonsequential access to and from local memory. This strided DMA capability enables high-performance submatrix transfers as required for image processing and other applications with distributed 2-D data sets.

High Bandwidth, Low Latency

Each connection through a RACE++ crossbar can run at 66.66 MHz for a peak bandwidth of 267 MB/s. Each crossbar can connect four simultaneous communication paths for a total peak bandwidth of more than 1 GB/s.

Low latency is often as important, if not more important, than high bandwidth. When making a connection through a RACE++ system at 66.66 MHz, each crossbar along the data transfer path adds only 75 ns to the latency. Once the connection is established, each crossbar adds only 15 ns of latency.

Flexible I/O

The ImpactRT S500 offers a variety of onboard I/O options. An integrated 10/100BaseT Ethernet interface is located on the board's front, as is an RS-232 serial port, which is directly connected to the onboard 8240 host processor. The board also contains a multi-use 64-bit PMC (PCI Mezzanine Card) site. This site can be used for system I/O, supporting industry-standard PMC cards as interfaces to a wide variety of devices, from Fibre Channel disk interfaces to A/D converters. The site can also be used for customized RACE++ I/O daughtercards, providing a direct I/O interface into the board's RACE++ crossbar.

Unique Single-Board Implementation

The ImpactRT S500 is the first RACE++ system with an onboard host. This extends the RACE++ product line to applications that do not require a multiple-board PCI or VME-based solution. In addition to negating the need for a separate runtime host board, the onboard host also reduces the complexity of system configuration management over the system life cycle. Solutions that can run effectively on smaller deployment systems may realize cost advantages by adopting the cPCI environment.

Scalability

ImpactRT S500s can be configured into multiple board systems using cables, interconnect modules, or interlink modules. With Mercury's DLK6c dual-port, six-slot CompactPCI interlink module, systems can scale up to eight ImpactRT S500 boards, supplying up to 32 compute nodes connected by a RACE++ switch fabric. The DLK6c contains 8 connectors: 6 connectors to backplane slots and 2 wing connectors. A cable connects an ImpactRT S500 to a wing connector.

Each DLK6c has three RACE++ crossbars and provides two RACE++ ports to each of its eight slots, using the J4 pins on the cPCI connector. A DLK6c delivers 2.1 GB/s of bandwidth, both aggregate and bisection, preserving the balance between processing and bandwidth that is the hallmark of the RACE++ architecture.

Smaller configurations of two or three boards can be created using cables or passive interconnect modules, referred to as PIMs. PIMs provide board-to-board connections without a crossbar; PIM 2/2 connects 2 adjacent boards and PIM 2/3 connects 2 boards with a vacant slot in between.

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Optimized Operating Environment

The real-time processing of the ImpactRT S500 system is controlled by the MC/OS multicomputer operating environment. The MC/OS multicomputer operating environment was created to support signal and image processing, evolving to support RACE and RACE++ on thousands of mission-critical systems. It is a deterministic real-time system, optimized to support high-bandwidth, low-latency multiprocessor operations.

Preliminary Specifications

Compute node	
Four compute nodes, each with:	
	500 MHz MPC7410 PowerPC with AltiVec
	2 MB L2 cache
	128 MB SDRAM
Control node	**200 MHz MPC8240**
	64 MB SDRAM
	32 MB FLASH
PMC connector	**64-bit PCI @ 33 MHz**
	267 MB/s RACE++ on PMC J4

External Interfaces

Front panel	**10/100BaseT Ethernet** **RS-232**
Backplane	**64-bit 33-MHz PCI**
	32-bit 66-MHz RACE++ (dual)

Environmental Specifications

Operating temperature	**0°C to 40°C**
Non-operating temperature	**-40°C to 85°C**
Airflow requirements	**10 CFM per slot minimum**
Relative humidity	**10 to 90% (non-condensing)**
Operating Altitude	**0 to 10,000 ft.**

Electrical/Mechanical Specifications

Dimensions	**6.3 in. x 9.2 in.**
Power	**50 W typical**
	60 W peak
Input voltage	**5.0 V +/- 5%**
	3.3V +/- 5%
Vibration	**0.003G^2/Hz, 20-2000Hz, 1 hour per axis**
Shock	**Z-axis: 20G, 11 ms, ½ sine**
	X-Y axis: 32G, 11ms, ½ sine

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