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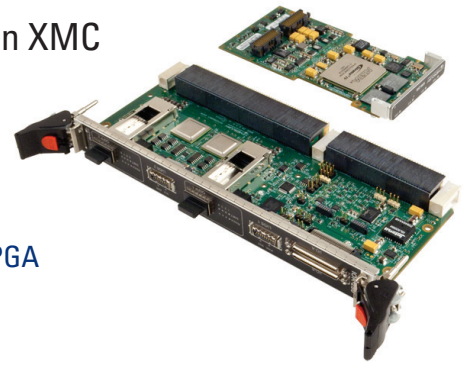
Ensemble™

DATASHEET

MERCURY COMPUTER SYSTEMS™

Ensemble IO Mezzanine Series IOM-200 XMC & IOR-280 RTM Modules

Exploit the Power of High-density 10Gbps Ethernet IO in an XMC



- Industry-leading Quad 10Gbps Ethernet IO density
- Up to eight 10GbE channels per 6U OpenVPX slot
- Rear Transition Module supports two IOM-200 XMCs
- Includes high-performance user programmable Altera® Stratix® IV FPGA
- Leverages open standards

The IOM-200 (IO Mezzanine) XMC Module and IOR-280 RTM from Mercury Computer Systems provide the industry's leading 10Gbps Ethernet IO density. When two IOM-200s are configured with the IOR-280 Rear Transition Module (RTM), up to eight channels of 10Gbps Ethernet can be supported per 6U OpenVPX slot.

The IOM-200 module also includes a high-performance Altera Stratix IV GX field programmable gate array (FPGA) all in a single-wide XMC form factor. Because many algorithms can run up to 100 times faster on an FPGA than a CPU processor, developers can partition applications across FPGAs and CPU processors for maximum performance. The FPGA has 1,288 18x18 multipliers (using GX230HF) and a large supply of memory internally to assist with math intensive algorithms.

The IOM-200 is also designed around an open architecture using open standards such as the Vita 42 XMC form factor. The IOR-280 implements Vita 46 OpenVPX to enable high-speed connectivity with other 6U Open modules, such as Mercury's VPX SBC6521 single board computer and LDS6520 low-density server module.

With this balance of a high-density 10Gbps Ethernet IO and a high-performance FPGA, the IOM-200 is extremely well suited to act as an external connection for a signal processing subsystem. It handles both real-time IO requests and digital signal processing such as a math co-processor for fixed-point operations used in digital image processing. In addition to 10Gbps Ethernet, the Stratix IV's flexible gigabit transceiver blocks allow other high-speed interface protocols to be implemented.

Large data sets can be staged in the 1 GB DDR3 SDRAM..

The multi-port memory controller has a bi-directional data path that is 64 bits wide at the physical connection between the memory and the FPGA. The 64-bit wide data path operates at 800 Mb/s per wire for a total peak bandwidth of 6.4 GB/s. High-bandwidth data transfers are realized through the Mercury-provided multi-port memory controller IP. The multi-port memory controller provides up to eight internal read/write ports to the application. They possess variable width and speed and a large 64-bit port to the external memory, significantly simplifying the application design.

The QDRII SRAM memory banks with independent memory controllers allow concurrent, low-latency read and write operations at a nominal 2.815 GB/s transfer rates on each direction. The SRAM memory bandwidth is paired up with 10 Gb/s channels to provide a balanced IO performance.

The XMC also has 64 MB of on-board flash memory to store several applications.

Applications can have multiple functions or modes of operation to be preloaded in different flash images and then selected at run-time. Different XMC cards can also be configured with different images in flash to execute specific functions in the system.

The IOM-200 has a full-duplex connection to the Intel processor on the base board (host processor) via the PCIe port supporting 5 GB/s peak bandwidth, in each direction, to the host processor.

Additionally, the Mercury example design database provides I2C interface for control and status monitoring of the FPGA device and a JTAG port to allow rapid FPGA reconfiguration through the J16/26 XMC connector or directly through an on-board connector.

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Rear Transition Module (RTM)

Each FPGA has four RXAUI interfaces to an IOR-280 Rear Transition Module (RTM). An IOR can interface to one or two IOM-200s and can provide a single or dual Quad SFP+ 10 GbE interface for a total of four or eight fiber 10 GbE ports with a combined 40/80 Gb/s IO bandwidth. Delivering I/O directly to the FPGAs allows these devices to perform repetitive operations that reduce data volume before passing the data on to the balance of the system.

The FPGA compute nodes on each board can work together on the same data set, communicating via LVDS mesh links. Each FCN has one 4-bit data path in each direction +clock/data wide LVDS links to the other FCN, with each link running at 200 Mb/s per wire giving 100 MB/s per link. With two links there is a total of 200 MB/s.

Real-Time Reconfiguration for Mode Changes

Mercury's FPGA technology adds the versatility of rapid reconfiguration. High-speed reconfiguration facilitates dynamic, system-level changes in mission and operating mode.

Parts of the application that are simple, fixed-point computations can run on an FPGA, saving space, power and money. Other parts of the application can run on the host processor, which is easier to program. Accordingly, the overall development time is kept manageable while the performance is maximized.

The host processor allows better integration, communication and control with the on-board FCNs through the PCIe interface without interfering with the other GTP and LVDS interfaces. For example, DMA operations can be managed from the host processor without requiring additional processor boards in the system. In addition to that, the host processor can be used to manage the loading of the bit streams and diagnostics of the FCNs.

Scalability

FPGAs in the PCIe environment become part of a scalable system that can expand to provide as many FPGAs and microprocessors as changing applications demand, with minimal application recoding and redeployment expense. Multiple FPGA XMC boards can be deployed in a single chassis, along with other boards carrying I/O devices and processors, communicating via a PCIe or a mesh fabric.

Developers can create and test algorithms on small laboratory systems consisting of only a few XMCs, with the assurance that the resulting code can move seamlessly to larger deployment platforms. Additionally, as processing requirements change in future program generations, they can readily resize target platforms with minimal impact to their code.

Software

The IOM-200 is supported by Mercury-provided Intel-based drivers supported under Linux.

Support includes:

- Loading the FPGA flash from the host processor
- Loading the FPGA directly from the system management processor
- Moving data from FPGA DRAM memory to host processor memory using direct PIO or the built in eight-channel DMA engines.

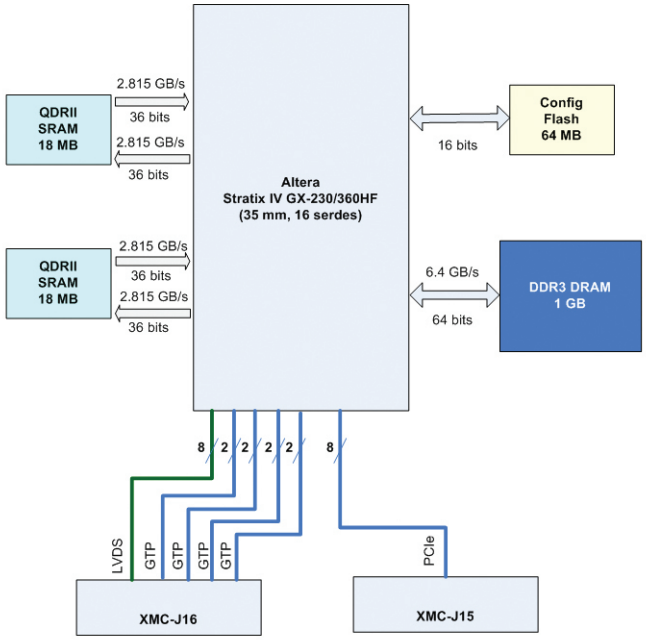


Figure 1. FPGA XMC Block Diagram

- TCP/IP network stack (available in future release – consult factory)

An FDK (FPGA Developer's Kit) is available for the IOM-200 providing a comprehensive suite of Mercury intellectual property (IP). The FDK provides developers with all of the necessary components to provide interconnect, communications, command and control, memory, and I/O interfaces for flexibility and faster time to deployment. A multi-channel DMA engine, also supplied, transfers data very close to the theoretical maximum of the PCIE bus.

Specifications

FPGA Compute nodes

FPGA processor	Altera® Stratix ® IV GX 230HF or 360HF (industrial grade)
Number of FPGAs	1

QDRII SRAM

Capacity per FPGA	32 MB
Bandwidth per FPGA	11.26 GB/s full-duplex (peak)

DDR3 SDRAM

Capacity	1 GB
Bandwidth	6.4 GB/s (peak)

Flash memory

Capacity	64 MB (typically 3–4 bit stream images)

PCIe ports to host processor

Gen 2 x4 or x8 PCIe 2.0

Fiber links (with RTM assembly)

4 pair at 10 Gbps each, full-duplex .850 nm multi-mode fiber with a single QSFP+ module connector.
Total bandwidth: 40 Gbps on each direction.

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LVDS port

8 pairs at 500 Mbps each to J16 XMC connector.
Total bandwidth: 500 MB/s

RTM assembly

IOR-280 provides 8 QSFP+ 10 Gigabit Ethernet ports with two IOM-200s configured.

Open Standards

IOM-200	Vita 42 XMC, Vita 42.3 PCIe
IOR-280	Vita 46.10 RTM

Supported Configurations

Ensemble SBC6521 Single Board Computer
Ensemble LDS6520 Low Density Server

Electrical/Mechanical Specifications

Power

25 W (GX230HF), 28W (GX360HF) (high typical, depends largely on application IP)

Dimensions

VITA 42.0, single-width, shortened-depth XMC format

Environmental Specifications

Air-cooled Version

Minimum airflow**	(per slot at sea level) TBD
Temperature**	
Operating	-0°C to +40°C
Storage	-40°C to +85°C
Rate of Change	N/A
Humidity	10-90% (non-condensing)
Vibration	
Random	0.003G²/Hz, based on 20 to 2,000Hz, 1 hr/axis
Shock	20G Z-axis, 32G X&Y-axis, 11 msec, half-sine pulse, 3-Positive and 3-Negative
Altitude**	
Operating	0 to 10,000 ft
Storage	0 to 30,000 ft
Salt/Fog	Consult factory

Conduction-cooled version Consult factory

* Environmental specifications are as installed on Mercury 6U host/carrier modules.

** As altitude increases, air density decreases and, therefore, the cooling effect of a particular number of CFM decreases. Different limits can be achieved by trading among temperature, altitude, frequency and airflow.

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