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DATASHEET

MERCURY COMPUTER SYSTEMS™

Ensemble 6000 Series
OpenVPX Intel Core i7 Dual-Core LDS6520 Module

Rugged Low-Density Server with High-End Processing and Fabric I/O Capabilities

- 6U OpenVPX™-compliant VITA 65/46/48 (VPX-REDI) module
- High-performance Intel® Core i7 Arrandale (Westmere-class) dual-core processor at up to 2.53 GHz with 40 GFLOPS peak performance
- Serial RapidIO® and/or 10 Gigabit Ethernet fabric enabled
- Integrated 80-lane PCIe switching infrastructure for on-board and off-board co-processing expansion-plane communications
- Mercury MultiCore Plus® software infrastructure support



The Ensemble™ 6000 Series OpenVPX™ Intel® Core i7 Dual-Core LDS6520 Module from Mercury Computer Systems integrates a high-end Westmere-class dual-core Intel Core i7 processor, a next-generation FPGA for both fabric bridging and user-application functions, and high-bandwidth on-board and off-board communication fabrics in a single 6U OpenVPX slot. By leveraging Intel high-density Core i7 processing with on-board integrated high-performance PCI Express infrastructure and I/O mezzanine sites, the LDS6520 delivers a well-balanced and scalable computing architecture that can provide processing and I/O functionality for high-end radar, signals intelligence, and image processing applications.

Intel® Core i7 Arrandale Westmere-Class Processor

The LDS6520 features the Intel 64-bit Core i7 610E Arrandale dual-core processor running at up to 2.53 GHz. This Intel Westmere-class dual-core processor can deliver approximately 40 peak GFLOPS, with two high-speed DDR3-1066 memory channels, providing up to 17 GB/s raw memory bandwidth. Up to 8 GB of DDR3 SDRAM with ECC functionality can be populated on the LDS6520. For more power-constrained applications, the LDS6520 can be configured with the low-voltage 2.0 GHz version of the Core i7 620LE. The LDS6520 makes use of the Ibex Peak HM55 Platform Controller Hub (PCH) chipset, which provides integrated graphics capabilities along with I/O bridging between the Intel processor and external devices.

The Core i7 610E Arrandale processor includes a large 4-MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The Arrandale processor supports the SSE4.2 instruction set, allowing high-performance algorithm development that is portable to future Intel architectures.

POET Fabric Interconnect Technology

The LDS6520 is the first embedded computing product to combine the processing power of the Core i7 family from Intel with Mercury's protocol-agnostic, multi-standard switch-fabric technology, POET™ (Protocol Offload Engine Technology).

POET brings the high-bandwidth, low-latency performance of switch fabrics to the LDS6520, providing the bandwidth necessary to eliminate data starvation and to fully utilize the processing power of Intel Core i7 technology. The LDS6520 POET instantiation supports both the high-bandwidth, low-latency, serial RapidIO switch fabric, as well as the highly successful 10 Gigabit Ethernet protocol. When configured for 10 Gigabit Ethernet, POET provides the offload and acceleration capability to support standard Ethernet operations with guaranteed deterministic delivery.

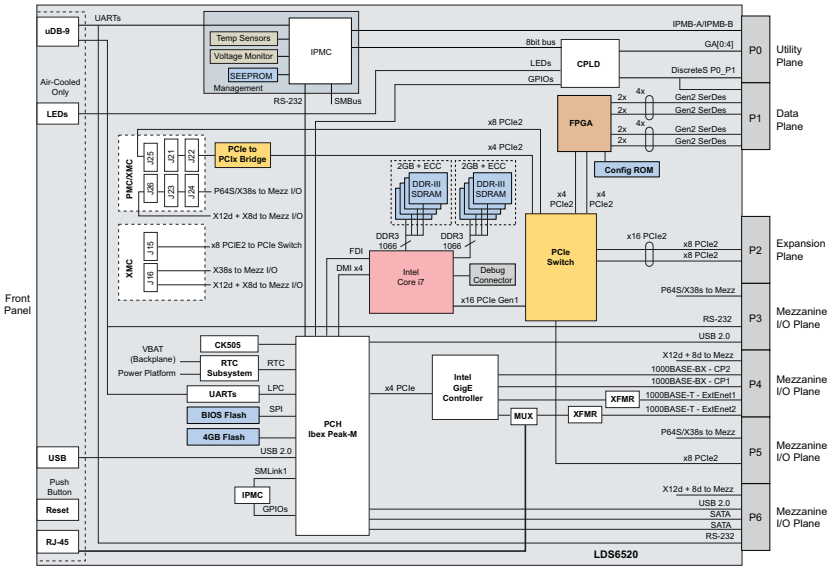


Figure 1. LDS6520 Module functional block diagram

The LDS6520 POET interface can also provide local switching between multiple fabric ports, allowing scalable mesh-based subsystem designs. The open and downloadable nature of POET allows users of the LDS6520 to implement these different protocols on the OpenVPX data plane without hardware changes. Users can also integrate their custom IP with POET to enhance the value of their subsystems.

The LDS6520 module is compliant to the VITA 65 module profile MOD6-PAY-4F1Q2U2T-12.2.1-1 with its initial POET instantiation, and is supported in chassis slots compliant with VITA 65 slot profile SLT6-PAY-4F1Q2U2T-10.2.1. Future POET instantiations may allow the LDS6520 to support additional or different VITA 65 module profiles.

PCI Express Architecture

The LDS6520 provides an 80-lane PCI Express switch for both on-board switching and off-board expansion. This Gen2 switch provides a PCIe interface to each of the two XMC sites as well as an x4 connection to the single PMC site via a PCI-X to PCIe bridge. This allows mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem. Additional x4 interfaces are provided to the on-board FPGA, allowing bridging to the data plane. Externally, the LDS6520 implements a full x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion-plane interface enables the LDS6520's compatibility with Mercury's GPU or FPGA based co-processing modules. The x16 PCIe connection can be user-configured as dual x8 connections. These configuration options let the module effectively act as an upstream/downstream PCIe switch to allow "chaining" of PCIe devices. An additional x8 PCIe interface is routed to the VPX P5 connector.

Mezzanine Card Flexibility

The LDS6520 provides two mezzanine sites, one PMC/XMC and one XMC-only. Each of the standard mezzanine sites on the LDS6520 module can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control. PMC cards are supported with a PCI/PCI-X interface at up to 133 MHz on the PMC/XMC site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8 PCIe (Gen1 or Gen2) supported on the J15/J25 connector per the VITA 42.3 standard. 20 differential pairs of XMC user I/O are mapped to the backplane via the J16/J26 connector.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, the LDS6520 has a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection are routed to the front panel on air-cooled configurations or to the backplane on conduction-cooled configurations.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection is routed to the backplane.
- Two 1000BASE-BX SERDES Ethernet connections are routed to the backplane per the OpenVPX control-plane specification.
- A DVI graphics interface is routed to the backplane, allowing the LDS6520 to provide a full graphical display, if needed by the application.
- One RS-232 serial port is routed to the front panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either RS-232 or RS-422 signaling.
- One front panel USB 2.0 interface is available on air-cooled configurations only.
- Two backplane USB 2.0 interfaces are available with both air-cooled and conduction-cooled configurations.
- Two SATA interfaces to the backplane are provided to easily interface with storage devices.
- Eight GPIO lines act as discrete I/O usable as input, output, or to generate interrupts on the module.
- Several additional bused signals enhance the functionality of the LDS6520 module.

System Management Plane

The LDS6520 module implements the advanced system management functionality architected in the OpenVPX Specification to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I^2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the VITA 46.11 draft standard. This allows the LDS6520 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module field replaceable unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on the OpenVPX SFM6100 module

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard – REDI (VITA 48). The LDS6520 module is implemented as a 6U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the

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system to an operational state in a limited time period, and also minimizes potential damage to the module.

Additional Features

The LDS6520 module provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, the LDS6520 module provides users with a toolkit enabling many different application use cases.

Features include:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support processor interrupt or reset
- Multiple boot paths, include netboot, USB boot, and boot from SATA or the on-board 4-GB flash device

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the LDS6520 module. Because the processor, memory, and surrounding technologies are leveraged across product lines, software developed on the LDS6520 module can interface seamlessly with other Mercury products. The same Linux® or VxWorks® development and run-time environment is implemented on the LDS6520 module as on other Mercury platforms across the Ensemble 3000, 5000, and 6000 Series.

The MultiCore Plus® (MCP) open software environment gives the LDS6520 module access to a wide ecosystem of stacks, middleware, libraries, and tools. A key software package available for the LDS6520 module is MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the multiple on-chip cores available with the Intel Arrandale Core i7 dual-core processor.

Software support is available on the LDS6520 for the following products:

- Support for Mercury's standard numeric libraries, VSIPL and SAL (Scientific Algorithm Library), as well as their multi-core variants, is optimized for the Intel Core i7 architecture of the LDS6520 module.
- Open Development Suite for Linux is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker, and a graphical source browser. Mercury provides extensions that allow multiprocessor-aware process launch and debug, as well as a System Supervisor view that allows graphical remote management.
- Support is provided for the Wind River Workbench integrated development environment when the module is running Wind River Linux or VxWorks.
- Interprocessor Communication System (ICS) support is carried forward from the RACE++®/MCOE™ software environment. ICS provides a low-level interprocessor communication API that lets users take advantage of the high-bandwidth, low-latency serial RapidIO fabric with an easy-to-use software interface.
- The Performance Porting Kit provides low-level handles for manipulation of the serial RapidIO fabric and can be used for simple data movement, or as a base on which to build a custom middleware layer.
- Trace Analysis Tool and Library (TATL™) is a "logic analyzer for software" that provides insight into the dynamic interaction of up to a few hundred processors.

The MultiCore Plus® (MCP) software environment lets applications use industry-standard middleware such as MPI, DRI, CORBA, or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE into the MCP domain.

Open Standards Mean Interoperability and Planning for the Future

The OpenVPX Industry Working Group is an industry initiative launched by defense prime contractors and COTS system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application-specific reference solutions. These OpenVPX standard solutions provide clear design guidance to COTS suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX System Specification was ratified by the VSO in February 2010.

Specifications

Intel Arrandale Westmere-Class 32-nm Processor

Dual-core
- 2.0 GHz 620LE
- 3.53 GHz 610R

Peak performance	40 GFLOPS (estimate)
Threads per core	2
Intel Virtualization Technology	
DDR3-1066	4 GB with ECC (up to 8 GB future capability)
Raw memory bandwidth	17 GB/s (total)
BIOS SPI flash	8 MB
NAND flash	4 GB

Altera Stratix® IV EP4SGX180 FPGA

Logic elements	175,000
Internal memory	11.7 Mb
18x18 multipliers	920
SerDes	16
Each SerDes	600 Mbp to 6.25 Gbps
1066-MT/s DDR3 SDRAM	Up to 128 MB
Provides fabric bridging to data plane	
Can act as co-processor to execute iFFT/FFT, image or signal processing	
Configured from CPU or dedicated configuration ROM	

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IPMI (System Management)

On-board IPMI Controller
Voltage and temperature monitor
Geographical address monitor
Power/reset control
On-board FRU EEPROM interface
FPGA, CPU, and CPLD interfaces

Ethernet Connections

1000BASE-BX Ethernet to P4 connector 2
OpenVPX Control Plane
10/100/1000BASE-T Ethernet to P4 connector 1
Accessible via OpenVPX RTM or external chassis interface
10/100/1000BASE-T Ethernet connection 1
To front panel (air-cooled module)
or backplane (conduction-cooled module)
Ethernet functions supported by the chipset include:
UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588,
flow control, 802.1P (priority), and 802.1Q (VLAN)

OpenVPX Multi-Plane Architecture

System Management via IPMB-A and IPMB-B link on
P0 management plane
Dual 4x Serial RapidIO or 10 Gigabit Ethernet interfaces on
P1 data plane
Full x16 or dual x8 PCIe expansion plane
Dual 1000BASE-BX Ethernet control plane

PMC-X/XMC Sites

Mezzanine sites 1 PMC/XMC, 1 XMC only
PCI-X-to-PCIe bridge
Connects PMC site to on-board PCI Express switch
PMC PCI support 33 and 66 MHz
PMC PCI-X support 66, 100, and 133 MHz
PMC user-defined I/O from P4 to backplane
PCIe XMC sites per VITA 42.3 with XMC user-defined
I/O from J6 to backplane

Additional I/O Capabilities

RS-232 serial interface to front panel 1
(air-cooled) or backplane (conduction-cooled)
Configurable for RS-422 signaling when routed to backplane
Front-panel USB 2.0 interface 1
(air-cooled configurations only)
USB 2.0 interfaces to backplane 2
DVI interface to backplane 1
SATA interfaces to backplane 2
Single-ended GPIO interfaces to backplane 8
System signals to backplane
NVMRO, ChassisTest, Environmental Bypass, MemoryClear

Mechanical

6U VPX (air-cooled and conduction-cooled)
1.0" slot pitch
OpenVPX and VPX REDI

Environmental

Air-Cooled – Mercury Rugged Level 1

Temperature
Operating* -25°C to +55°C
Storage -55°C to +85°C
*Customer must maintain required cfm level.
Humidity
Operating 5-95%, non-condensing
Vibration 0.04 g^2/Hz; 20 to 2000 Hz, 1 hr/axis
Shock 50g, z-axis; 80g, x-, y-axes; 11 ms half-sine
Altitude
Operating* 0-30,000 ft
*Customer must maintain required cfm level.

Conduction-Cooled – Mercury Rugged Level 3

Temperature
Operating -40°C to +71°C at the card edge*
Storage -55°C to +125°C
*Customer chassis must maintain card edge at 71°C.
Humidity
Operating 0-100%
Vibration 0.1 g^2/Hz, based on 5-2000 Hz, 1 hr/axis
Shock 50g, z-axis; 80g, x-, y-axes; 11 ms half-sine
Altitude
Operating 0-70,000 ft

Compliance

OpenVPX System Specification encompasses
VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11
Compatible with VITA 65
VITA 46/48.1/48.2 (REDI)
Serial RapidIO, PCI Express, 10 Gigabit Ethernet

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