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THEMIS COMPUTER

TSVME420-R

16/32 ADC with isolated inputs

USER'S MANUAL

TSVME420-R

16/32 ADC with isolated inputs

A237-01

CUSTOMER COMMENTS

---oOo---

PRODUCT : **TSVME420-R - A237-01**

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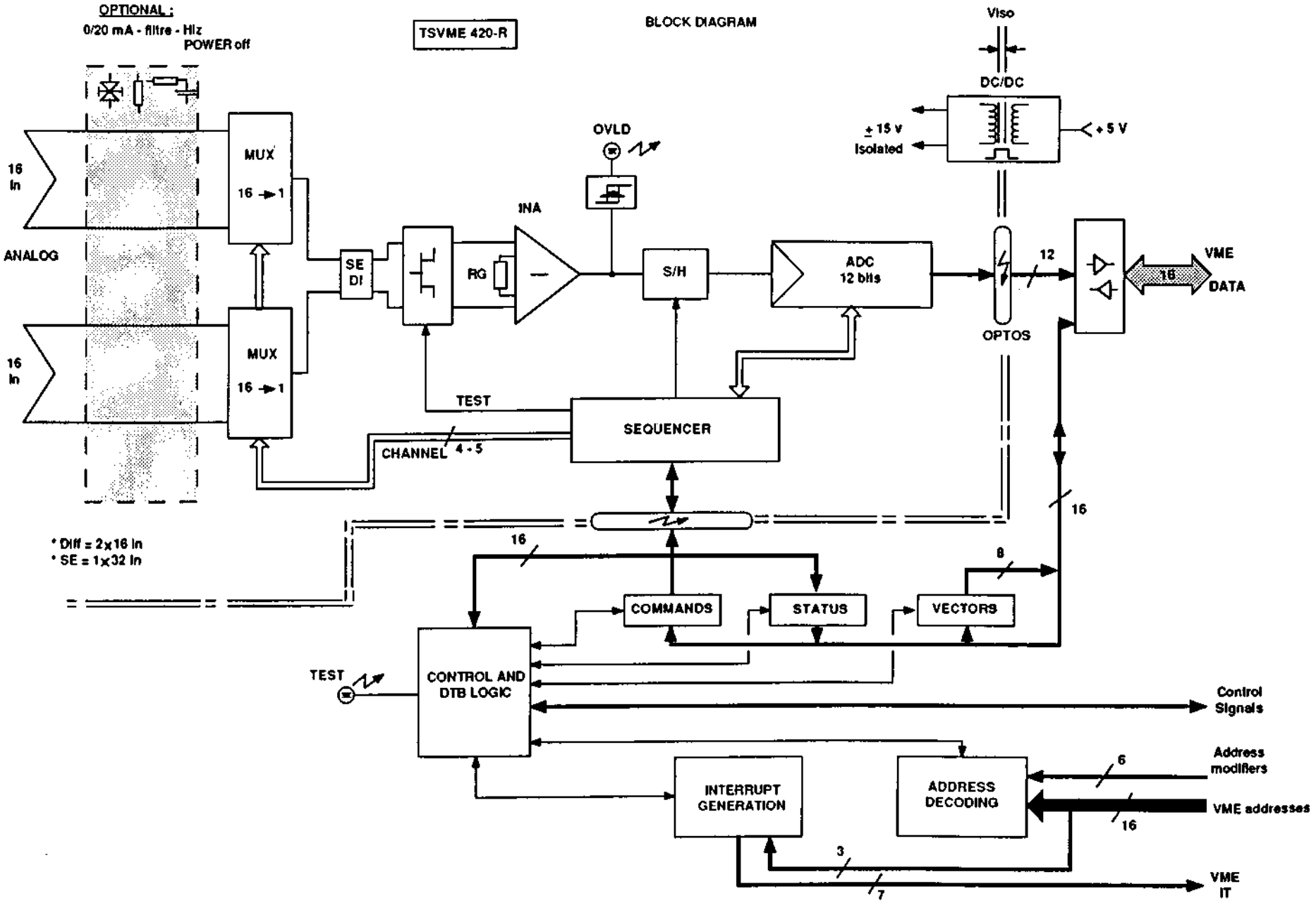
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6.2 - S/H Data sheet
6.3 - ADC Data sheet

NOTE

The name of a signal followed by * means that it is active at low logic level or on the falling edge.

FIGURE 1 - BLOCK DIAGRAM



I - GENERAL

1.1 - INTRODUCTION

This manual gives comprehensive information concerning use of the TSVME420-R board.

- Characteristics and technical specifications are given in chapters I and II.

- Chapter III deals with configuration of the board in the desired operating mode.

- The options available, with their respective technical specifications, are set out in Chapter IV.

- Basic applications are described in Chapter V.

- Data sheets for the MUX, S/H and ADC are appended in Chapter VI.

1.2 - PRINCIPAL CHARACTERISTICS

* The TSVME420-R board is used for 12-bit digitizing on 16 or 32 multiplexed analog inputs with instrumentation amplifier (INA). A high degree of electrical isolation is provided between analog and digital grounds. (Figure 1).

* The analog section performs 32 ---> 1 multiplexing ("Single-ended configuration, SE), or 16 ---> 1 multiplexing ("Differential" configuration, DI). Multiplexing is followed by an INA, with gain variable by means of a resistance (gains between 1 and 1000).

The INA is followed by a sample and hold amplifier and a 12-bit ADC.

* In addition, front panel indication is given of voltage overloads on one or more of the 16/32 analog inputs, for quick diagnosis during troubleshooting. (This operates for all values of INA gain).

* In the "test offset" mode, the various board sensors are isolated, and the INA input automatically grounded. This facilitates offset adjustment by obviating the need to remove the analog input connector and insert a "dummy plug" to ground the 32 inputs. "Test" mode is indicated on the front panel.

* The TSVME420-R board operates as a slave on the VME bus.

The digital section is made up of an address decoding module (4 words), address modifiers (short I/O), and a unit for managing interrupts (selection by 7 jumpers in transmit) or polling mode.

The control logic operates essentially on the various registers, the 16-bit control/status registers (channel number, start, busy, abort, Enable IT, IRQP), and the register of interrupt vector numbers (8 bits).

Only the "Abort" bit can be used to cancel a conversion in progress without having to wait for the end of the entire acquisition process.

A sequencer is used to synchronize acquisition timings and calculate the INA settling time for each board gain setting.

The data register (16 bits) reads the sampled digital value, and also holds 1 "busy" bit.

* ANALOG/DIGITAL isolation is provided by photocouplers and a DC/DC convertor. This gives an excellent breakdown resistance and very good immunity to digital/analog noise (high common mode rejection ratio).

*The front edge strip holds a 37-pin SUB-D male connector for the 32 analog inputs, the overload led ("OVLD"), a led ("TEST") for "test offset" mode, and a access hole for the INA offset potentiometer.

* OPTIONS :

The following optional features are available for the TSVME420-R board :

- OPTION-Z : High input Impedance on "Power Off" ; analog inputs remain at high impedance when the board is no longer powered (cf : redundant systems). TSVME420RZ.

- CONFIGURATION-I : Each of the inputs can take a current loop, thus giving a shunt resistance (standard : 250 ohms, 0.01%, 5 ppm/degrees C.) across the 0/20mA inputs. (Customer configuration).

- CONFIGURATION-F : Each input has a 1st order low-pass filter (or possibly a high-pass filter) for selection of the required passband. (Customer configuration).

TABLE 1 - TABLE OF CONFIGURATION SETTINGS

FEATURE	JUMPER	SOFTWARE
32 inputs (SE) / 16 inputs (DI)	X	
Number of channel converted		X
Gain of channel converted	RESISTOR	
Selection : ADC input voltage	X	
Selection : ADC output code	X	
Adjustment : INA offset	FACTORY SET	
Adjustment : ADC offset	FACTORY SET	
Adjustment : ADC gain	FACTORY SET	
Selection : acquisition rate	X	
Selection : base address	X	
Selection : address modifier	X	
IT/polling mode		X
IT identification number	X	
Number of line sending IT	X	
Number of IT vector		X
"Test" mode command		X
Abort : Halt with conversion in progress		X

1.3 - SPECIFICATIONS

TSVME420-R board, characteristics for Tamb = 25 degrees C., power supply complying with VME bus, Ve = ± 10V, differential mode, except where otherwise indicated.

TABLE 2

INPUT CHARACTERISTICS :	
.Number of analog channels (jumper-selected)	32 single ended/16 differential
.ADC input voltage (jumper-selected)-(1)-	± 5V; ± 10V; 0-10V
.Range of INA gains	1 to 1000 (set by resistor)
.Maximum non-destructive input voltage	± 30V (Power ON) ± 20V (Power OFF)
.Input impedance	500 Mohms//60 pF (on selected channel) 500 Mohms//10 pF (on non-selected channel)
.Bias current : Tamb = 25 degrees C. Tamb = 0 to 55 degrees C	± 3 nA (± 10 nA max.) ± 7 nA (± 90 nA max.)
.Input offset voltage - (2) -	±20µV max., factory set,G=1000
.Range of input offset adjustment	± 200 uV
.Offset voltage drift - INA - (6) - (RTI) -	± 1.5 µV/Degree C. (G=1000) ± 8 µV/Degrees C. (G=1)
.CMRR (differential input, DC to 50 Hz)	90 dB (G=1),105 dB (G=1000)

TRANSFER CHARACTERISTICS :	
.ADC resolution	12 bits
.ADC output code : unipolar bipolar	straight binary : SB offset binary : OB or 2's complement (TC)
.Conversion time, whole chain	160 µs max., G=1 and G=10 250 µs max., G=100 1 msec max., G=1000

ACCURACY :	
.Accuracy over whole chain - (3),(4) -	± 0.05% FSR max. (G=1) ± 0.1 % FSR max. (G=1000)
.Linearity over whole chain	± 0.025% FSR
.Drift in accuracy over whole chain	± 75 ppm/degree C. (G=1000) ± 30 ppm/degree C. (G=1)
.Linearity, ADC	± 1/2 LSB max.
.Differential linearity, ADC	± 1/2 LSB ± 1 LSB max. 5 to 55 degrees C.
.Gain error, ADC (2)	Factory set
.Offset error, ADC (2)	Factory set
.ADC monotonicity (no code missing)	Guaranteed from 0 to 55 degrees C.

DYNAMIC CHARACTERISTICS :	
.Crosstalk channel ON / channel OFF	>100 dB at 1 KHz
.Slew rate, whole chain (before ADC)	0.6 V/µs (G=1)
.Temporal uncertainty on sampling	± 150 nsec.
.Threshold for overload indicator (OVLD)	± 10.4V (+/-3%)
"OVLD" detection time (Attack)	20 µs
"OVLD" hold time (Release)	500 msec.

ANALOG/DIGITAL ISOLATION (5) :	
.Insulation voltage (continuous)	1000 VDC 1500 VDC for 1 minute
.A/D leakage	1G ohms //100 pF
.IMRR (Isolation Mode Rejection Ratio)	
.---> (DC)	>160 dB

VME SECTION (Slave board) :	
.Type of data transfer	A16 - D16
.Command and status registers (R/W*)	16 bits
.Vector number register	8 bits
.Data register	16 bits
.Addressing space (short i/o)	4 word addresses (16 bits) in the 64Kbyte area predecoded by address modifiers AM0-AM5/2D and 2D+29,i.e. "supervisor" mode or "supervisor and user" mode.
Interrupt generator	Dynamic vector programming Level selected by jumper ROAK option "Release On AcKnowledge"
ENVIRONNEMENT :	
.Power supply	+5V; ± 5 %; 2A max.
.Operating temperature	0 to +60 degrees C.
.Storage temperature	-40 to +85 degrees C.
.Relative humidity	0 to 90% non- condensing
.Warm up time	15 mn
.VME compatibility	Electrical and mechanical
Dimensions of board copper area	233.6 x 160 x 1.6 mm

NOTES :

- (1) Board delivered set for ± 10V FSR, G = 1.
- (2) Adjustable
- (3) FSR = Full Scale Range .
- (4) Including offset, linearity, and gain errors.
- (5) Relative humidity = 45%, Tamb = 25 degrees C.
- (6) RTI, Refered To Input.

1.4 - EQUIPMENT REQUIRED FOR USE

- One VME rack with backplane (optional extension not required, as P2 is not used) and power supply.

-One VME-compatible CPU board.

II - TECHNICAL DESCRIPTION

2.1 - INTRODUCTION

- This chapter gives the information required for understanding the operation of the board, i. e.:

* the definition of selectors and connectors, VME interfacing, board mapping, write/read timings.

2.2 - DESCRIPTION OF SELECTORS AND CONNECTORS

Table 3 and Figures 2 and 3 give the identification and board location of selectors and connectors.

TABLE 3

REFERENCE	FUNCTION	CHAPTER
S1, S2	Selection of ADC input range : 0 to 10V (unipolar) ± 5V, ± 10V (bipolar)	3.2.7
S3	Selection of ADC output code : Unipolar; SB Bipolar; OB or TC	3.2.8
S8, S9, S10, S11	Selection of 32 inputs "Single Ended" 16 inputs "Differential"	3.2.6
S12	Selection of board base address (0000 to FFF8)h	3.2.2
S13	Selection of interrupt line number (1 to 7) Transmit/ Receive	3.2.3
S14	Selection of "supervisor" or "supervisor and user" mode	3.2.1
P1	VME interface connector (DIN41612 96-pin male)	2.3
P3	Front panel analog input connector (SUB.D 37-pin male)	3.3
DE1	"OVERLOAD" led indicator (OVLD on front panel)	3.2.5
DE2	"Test Mode" led indicator (TEST on front panel)	3.2.4
R101	INA offset potentiometer (accessible from front panel : "OFFS AMP")	3.4
R103	ADC gain potentiometer (unipolar and bipolar modes)	3.4
R102	ADC offset potentiometer (unipolar mode)	3.4
R104	ADC offset potentiometer (bipolar mode)	3.4
S4, S5, S6, S7	Selection of conversion time -TCONV- (dependant on INA gain set).	3.2.10
P2	Not used	
W5, W6, W7	Solder beads, factory set	
R14	R.GAIN (RG), not wired (GAIN, INA = 1)	
CROSS-HATCHED AREA	Not wired	
W1, W2, W3, W4	Not soldered	
TP1	"Analog ground" test point (OVA) - ISOLATED -	
TP2	"Logic ground" test point (OVL) - VME section -	

FIGURE 2

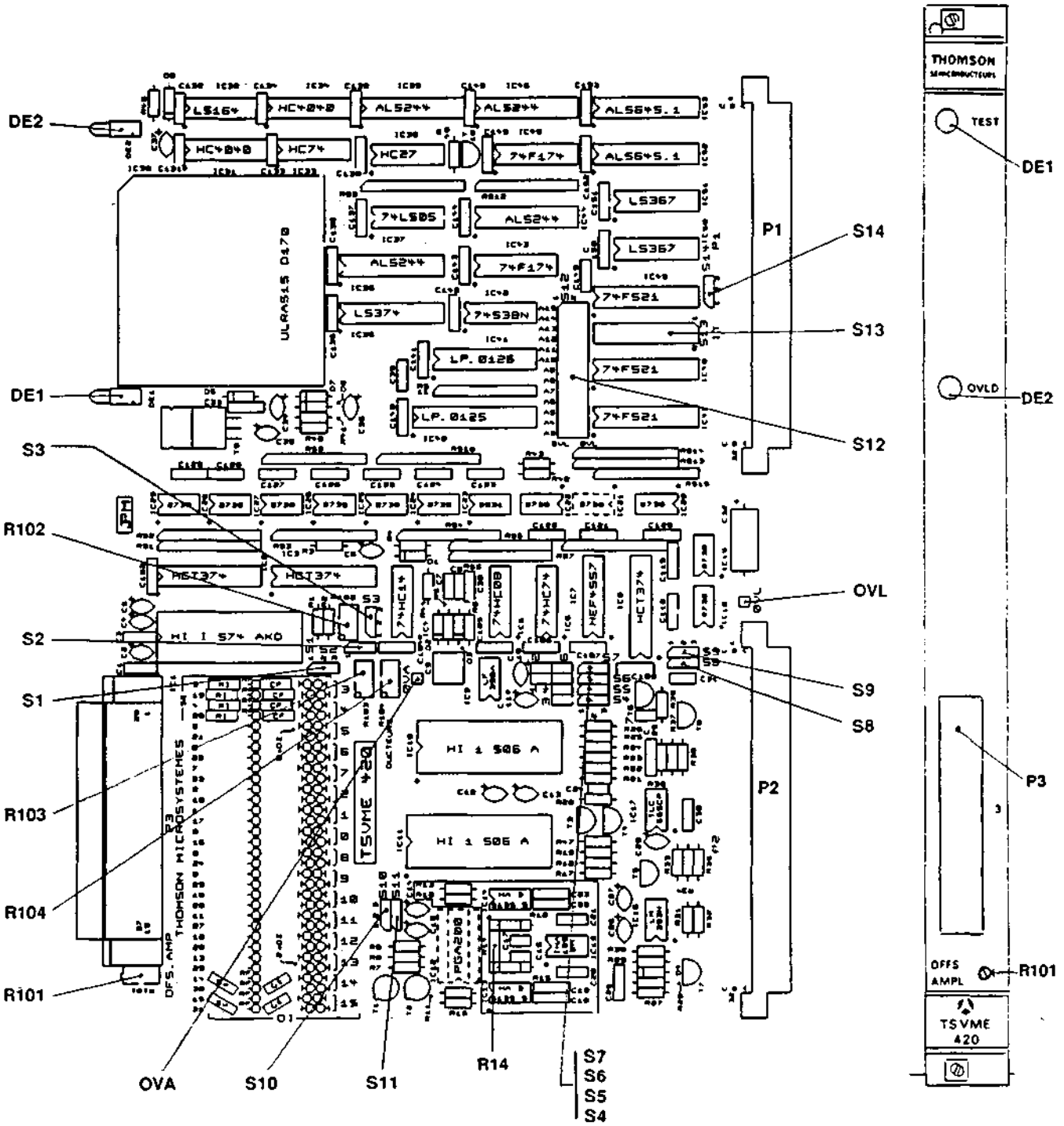
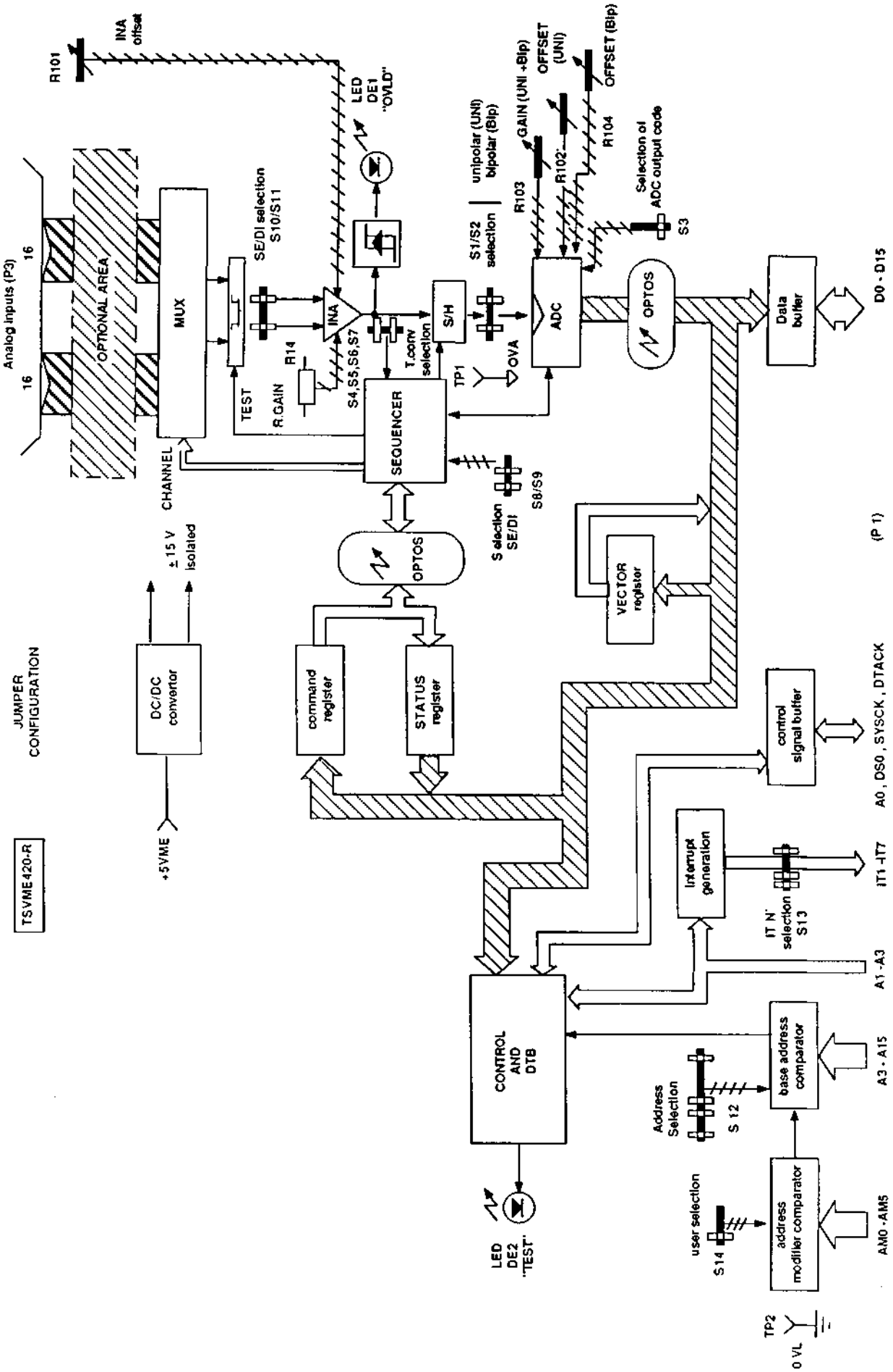

DE2
DE1
S3
R102
S2
S1
R103
R104
R101
OVA
S10
S11
R14
S7
S6
S5
S4
P1
S14
S13
S12
OVL
S9
S8
P2
P3
R101
THOMSON
TEST
DE1
OVLD
DE2
OFFS
AMPL
TSVME
420

FIGURE 3 - JUMPER CONFIGURATION



2.3 - VME INTERFACE

- Only connector P1 of the VME bus is used by the TSVME420-R board. Signals from the VME extension will be ignored.

- For a complete definition of the VME bus, refer to the document "VME BUS SPECIFICATIONS MANUAL" (ref. TSDOC VME) (not supplied).

- Table 4 shows the signals used by the board on connector P1 and their pin assignment.

NOTE : Throughout this manual, signal names followed by the symbol * (e.g. DTACK*) will be used to indicate signals which are active at low level (= 0) or on the falling edge.

TABLE 3 - CONNECTOR P1 - SIGNALS AND PIN CONFIGURATION

PIN No.	ROW A SIGNAL	:USED : (1)	ROW B SIGNAL	:USED : (1)	ROW C SIGNAL	:USED : (1)
1	D0	:	BBSY*	: NU	D8	:
2	D1	:	BCLR*	: NU	D9	:
3	D2	:	ACFAIL*	: NU	D10	:
4	D3	:	BGO IN*	: CH	D11	:
5	D4	:	BGO OUT*	: CH	D12	:
6	D5	:	BG1 IN*	: CH	D13	:
7	D6	:	BG1 OUT*	: CH	D14	:
8	D7	:	BG2 IN*	: CH	D15	:
9	GND	:	BG2 OUT*	: CH	GND	:
10	SYSCLK	:	BG3 IN*	: CH	SYSFAIL*	: NU
11	GND	:	BG3 OUT*	: CH	BERR*	: NU
12	DS1*	:	BR0*	:	SYSRESET*	:
13	DS0*	:	BR1*	:	LWORD*	: NU
14	WRITE*	:	BR2*	:	AM5	:
15	GND	:	BR3*	:	A23	: NU
16	DTACK*	:	AM0	:	A22	: NU
17	GND	:	AM1	:	A21	: NU
18	AS*	:	AM2	:	A20	: NU
19	GND	:	AM3	:	A19	: NU
20	IACK*	:	GND	:	A18	: NU
21	IACKIN*	:	SERCLK	: NU	A17	: NU
22	IACKOUT*	:	SERDAT	: NU	A16	: NU
23	AM4	:	GND	:	A15	:
24	A7	:	IRQ7*	:	A14	:
25	A6	:	IRQ6*	:	A13	:
26	A5	:	IRQ5*	:	A12	:
27	A4	:	IRQ4*	:	A11	:
28	A3	:	IRQ3*	:	A10	:
29	A2	:	IRQ2*	:	A9	:
30	A1	:	IRQ1*	:	A8	:
31	-12V	: NU	+5V STDBY	: NU	+12V	: NU
32	+5V	:	+5V	:	+5V	:

(1) :
signal not used : NU
signal used : (no legend)
signal unused on board but chained : CH

NOTE :

. Connector P1 is a 96-pin DIN 41612 male connector with 3 rows (A - B - C) of 32 pins each.

Table 5 shows the function of MNEMONIC named signals with the type of output used.

- For simplification, the following abbreviations are used to indicate the different types of command circuits :

"Totem-Pole" (high current) ——→ TP HC
"Totem-Pole" (standard) ——→ TP STD
Three-state (high current) ——→ 3 HC
Three state (standard) ——→ 3 STD
Open collector ——→ OC

TABLE 5

SIGNAL MNEMONIC	SIGNAL	TYPE	FROM	TO	Adapt. NETWORK
A01 - A15	Address bus (15 l.)	3STD	CPU	TSVME420-R	YES
AM0 - AM5	Address modifier	3STD	CPU	TSVME420-R	YES
AS*	Address enable	3HC	CPU	TSVME420-R	YES
WRITE*	Write	3STD	CPU	TSVME420-R	YES
DS0* - DS1*	Data enable	3HC	CPU	TSVME420-R	YES
D00 - D15	Data bus	3STD	CPU,VME420R	TSVME420R,CPU	YES
DTACK*	Data acknowledge	OC	VME420R	CPU	YES
BG0IN* to BG3IN* BG0OUT* to BG3OUT*	Bus assignment	TPSTD	Arbiter	TRANSPARENT	NO
IRQ1* to IRQ7*	Interrupt request (7 lines)	OC	TSVME420-R	CPU	YES
IACKIN*	Interrupt acknowledge	TPSTD	CPU/other slave	TSVME420-R	NO
IACKOUT*	(Daisy Chain)		TSVME420-R	Other slave	
IACK*			CPU	TSVME420-R	YES
SYSRESET*	System reinitialization	OC	CPU	TSVME420-R	YES
SYSCLK	System clock	TPHC	CPU	TSVME420-R	YES

2.4 - ADDRESSES, REGISTERS AND INTERRUPTS

2.4.1 - Address

a) Address modifiers

* The board only accepts the following two codes :

- 2D
- 2D or 29

} Selection by jumper S14

Both codes correspond to "short" addressing -16 address bits- reserved for i/o boards (short i/o).

The only difference between them concerns the enabling of board access :

- Supervisor Mode (privileged)
- Supervisor or user mode (non-privileged)

TABLE 6

HEX CODE	ADDRESS MODIFICATION : AMx 5	4	3	2	1	0	FUNCTION	DEFINED BY
3F	H	H	H	H	H	H	Standard supervisory ascending access	VMEbus spec.
3E	H	H	H	H	H	L	Standard supervisory program access	VMEbus spec.
3D	H	H	H	H	L	H	Standard supervisory data access	VMEbus spec.
3C	H	H	H	H	L	L	Not defined	Reserved
3B	H	H	H	L	H	H	Standard non-privileged ascending access	VMEbus spec.
3A	H	H	H	L	H	L	Standard non-privileged program access	VMEbus spec.
39	H	H	H	L	L	H	Standard non-privileged data access	VMEbus spec.
38	H	H	H	L	L	L	Not defined	Reserved
30-37	H	H	L	X	X	X	Not defined	Reserved
2F	H	L	H	H	H	H	Not defined	Reserved
2E	H	L	H	H	H	L	Not defined	Reserved
2D	1	0	1	1	0	1	Short supervisory I/O access	VMEbus spec.
2C	H	L	H	H	L	L	Not defined	Reserved
2B	H	L	H	L	H	H	Not defined	Reserved
2A	H	L	H	L	H	L	Not defined	Reserved
29	1	0	1	0	0	1	Short non-privileged I/O access	VMEbus spec.
28	H	L	H	L	L	L	Not defined	Reserved
20-27	H	L	L	X	X	X	Not defined	Reserved
10-1F	L	H	X	X	X	X	Not defined	User
0F	L	L	H	H	H	H	Extended supervisory ascending access	VMEbus spec.

HEX CODE	ADDRESS MODIFICATION : AMx 5	4	3	2	1	0	FUNCTION	DEFINED BY
0E	L	L	H	H	H	L	Extended supervisory program access	VMEbus spec.
0D	L	L	H	H	L	H	Extended supervisory data access	VMEbus spec.
0C	L	L	H	H	L	L	Not defined	Reserved
0B	L	L	H	L	H	H	Extended non-privileged ascending access	VMEbus spec.
0A	L	L	H	L	H	L	Extended non-privileged program access	VMEbus spec.
09	L	L	H	L	L	H	Extended non-privileged data access	VMEbus spec.
08	L	L	H	L	L	L	Not defined	Reserved
00-07	L	L	L	X	X	X	Not defined	Reserved

b) Base address

- The board is designed to accept short addressing (A to A15), and bits A16 to A23 will be ignored.

- The board occupies 8 bytes (A0 to A2) in short addressing areas. The board address is therefore binary encoded on 13 bits (A3 to A15) by jumper S12, which defines the relative position of the 8 bytes occupied by the board in the VMEbus short addressing area. This represents an address offset and not an absolute address. (Base address).

```
Board address      =    Base address + Addressing space occupied

\------v------/         \-------v-------/  \----------v----------/
absolute address        address offset     access to internal
                       with respect to A0      registers
   (16 bits)              (13 MSBs)             (3 LSBs)

 A15 ···> A0              A15 ···> A3          A2 A1 A0
 \---v---/                \---v---/            \---v---/
 max = FFFF (h)     =     FFF8 (h) max   +     7 (h) max
 min = 0000 (h)     =     0000 (h) min   +     0 (h) min
```

The base address goes from 0000 to FFF8 bytes in modulo 8.
(0, 8, 10, 18(h) ...).

This is included in the "short i/o" space on the VME (FF0000 to FFFFF, for THEMIS CPU board).

c) Address mapping

- Figure 4 shows the mapping of all board access registers.

- The control register is 16-bit accessible.

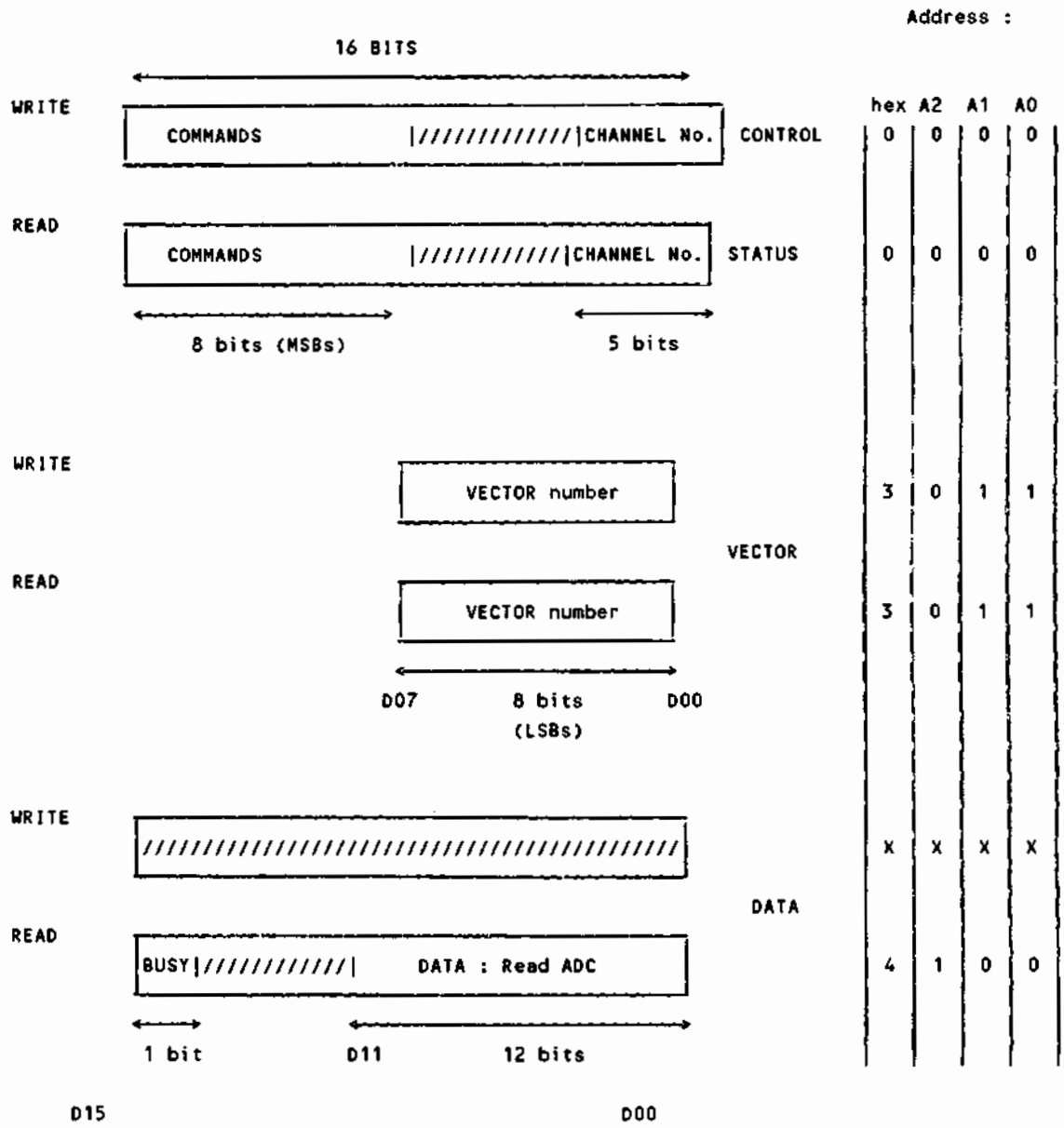
- The status register is 16-bit accessible.

- The vector number register is 8-bit or 16-bit accessible.

- The data register is 16-bit accessible.

* The control register contains the number of the channel to undergo conversion (8LSBs), and commands (8MSBs) (start, etc.). The status register is practically a copy in read mode of the control register : (see chapter 2.4.2 - Registers -).

FIGURE 4 - MAPPING OF ADDRESS REGISTERS



//// : Irrelevant

Notes :

Addresses : A2, A1, A0 are not used

=				
	0	0	1	1(h) → see note 1
	0	1	0	2(h) → see note 2
	1	0	1	5(h)
	1	1	0	6(h)
	1	1	1	7(h)

- We have, then :

* Control register (commands + channel No.) -> "word" address, base @ + $0 (h), 16 bits write only.

* Status register ---> "word" address, base @ + $0 (h), read.

* Vector number register ---> "byte" address, base @ + $3(h) write or read (8 bits).

* Data register ---> "word" address, base @ + $4 (h), read only.

- NOTE 1 : The status register may in fact be accessed by "byte" address in read mode, though the board will still deliver the 16 status bits on the VME bus:

. "Most significant byte" address; base @ + $0 (h) } Read on 16 bits, status
. "Least significant byte" address; base @ + $1 (h) }

- NOTE 2 : The board is protected against "byte" access on $2 (h). This applies for write and read, no DTACK* returned -->" Bus Time Out" -CPU-
If so desired, "word" address access to $2 (write and read) is possible, but only the 8LSBs will be significant.

- NOTE 3 : The board is protected against "byte" access writes to the control register:
$0 (h) } "byte" address, write; --> forbidden
$1 (1) }

Ignored, and no DTACK* returned.

- NOTE 4 : For the data register, the board is protected against "byte" access (read mode):
$4 (h) } "byte" address, read; --> forbidden
$5 (h) }

Ignored, and no DTACK* returned.

- NOTE 5 : The board ignores "write" accesses to the data register.

Ignored, and no DTACK* returned.

- NOTE 6 : The board is protected against "write" accesses on the vector and control registers. If "busy" = 1 (conversion in progress); no DTACK* returned ---> Bus Time Out - CPU. See details on "Abort", 2.4.2 -a.

2.4.2 - Registers

Figure 6 shows the contents of the various registers for board access via the VME data bus (D00 to D15).

a) Control register

* On power up, all control register bits are forced to 0 ---> the corresponding bits are therefore active at level 1.

* Channel number : (V4, V3, V2, V1, V0) = Number of channel for conversion :
- 16 channels (DI) ⟶ coded on 4 bits
- 32 channels (SE) ⟶ coded on 5 bits

TABLE 6

V4	V3	V2	V1	V0	HEX	Channel No.
0	0	0	0	0	00	0
0	0	0	0	1	01	1
|	|	|	|	|	|	|
v	v	v	v	v	v	v
|	|	|	|	|	|	|
0	1	1	1	0	0E	14
0	1	1	1	1	0F	15
1	0	0	0	0	10	16
1	0	0	0	1	11	17
|	|	|	|	|	|	|
v	v	v	v	v	v	v
|	|	|	|	|	|	|
1	1	1	1	0	1E	30
1	1	1	1	1	1F	31

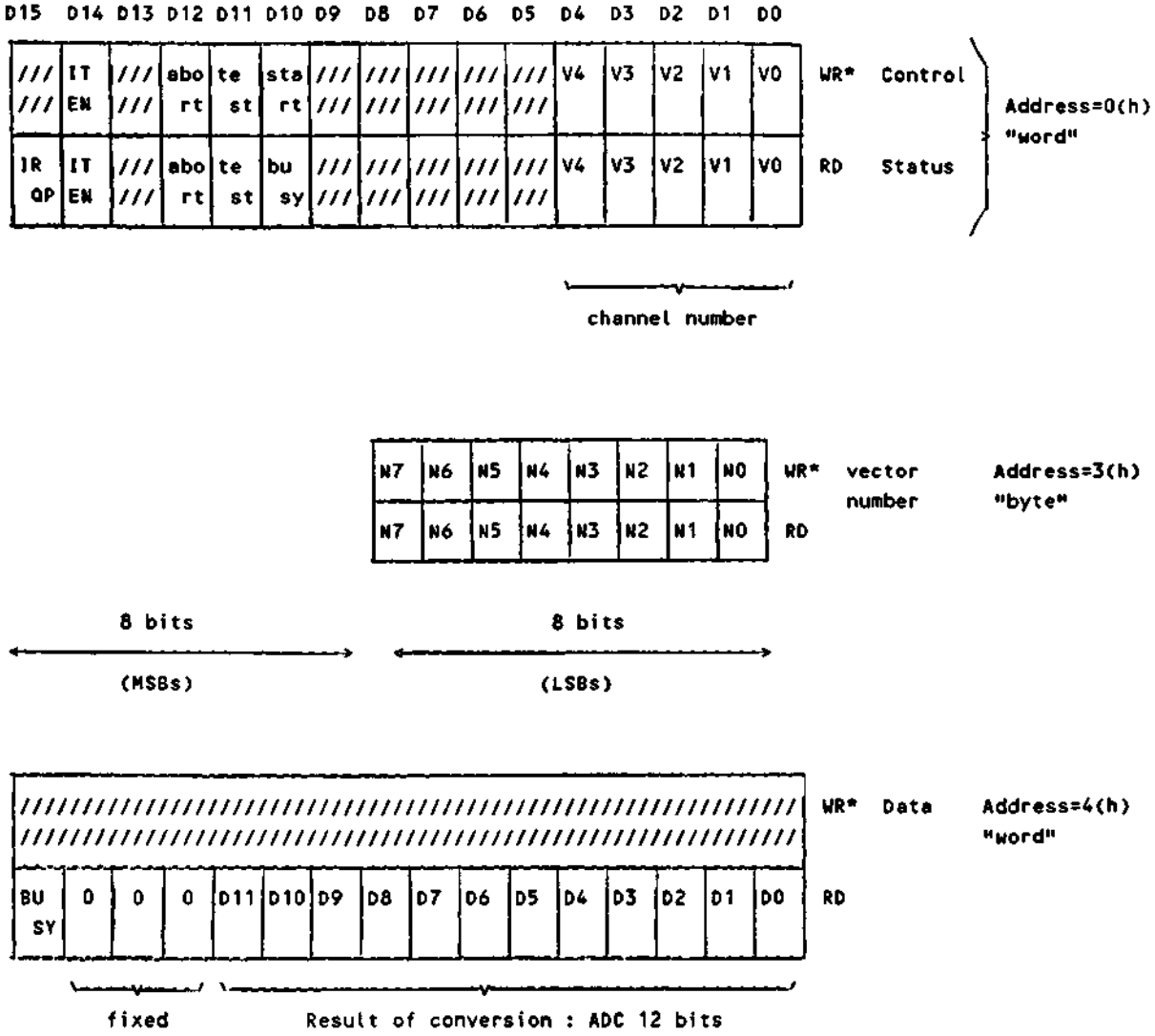
16 channels (differential)

32 channels (Single Ended)

Bit V4 is not used in differential mode, and will be ignored by the board.

REGISTER CONTENTS

FIGURE 5



/// : IRRELEVANT

* Start : performs conversion with all parameters as defined in control register. (start = 1).

* Test : "Test" mode (test = 1) "shunts" the INA inputs to ground and "inhibits" the board's 16/32 analog inputs to allow immediate offset adjustment by R101. This function has priority on channel numbers selected previously.

* Abort : The ABORT bit cancels the conversion in progress. The control register is protected against write access while "busy" = 1, unless "abort" = 1. This avoids conversions being performed unnecessarily (e.g. : g = 1000 ⟶ conversion time = 1 msec.). This bit reinitializes the board's internal sequencer and, 16 µs later, resets "busy" = 0.

The ABORT bit does not destroy the old data in the control register. A new conversion is performed by simply rewriting the new data if necessary (with "abort" = 0 and "start" = 1).
Note : the new conversion (start) must be started 50 µs after writing of the "abort" bit in the control register. (See chapter 2.5.3).

* ITEN : With "ITEN" = 1 (IT ENABLE) the board operates in "INTERRUPT" mode. Once the board has terminated a conversion, it sends an interrupt to the CPU. (Useful for relatively long conversions - high INA gain).

ITEN = 0 selects "Polling" mode, i. e. the CPU surveys the end of conversion ("BUSY") in the status or data register. (See chapters b and d).

b) Status register

The status register is a copy in read mode of the control register as regards channel numbers, "TEST" mode, "Abort function" and "IT ENABLE".

The two registers only differ in the following two functions :
D10 = "BUSY"
D15 = "IRQP" (see figure 5)

- BUSY : The START bit in write mode becomes the "busy" bit in status read mode. Once the board performs a conversion on a channel ("start" = 1), "busy" = 1 immediately appears in the status register. This bit remains at 1 and masks all internal conversion sequencing (not only the ADC), falling to 0 when the converted data is validated. This applies for all INA gains and multiplexing sequences.

- IRQP : IRQP bit = 1 indicates that the board has finished converting a channel and sent out an interrupt. IRQP remains at 1 until this interrupt is registered and serviced by the CPU.

* Note : IRQP is (or becomes) inactive = 0, if :

ITEN = 0 (Polling mode)
ABORT = 1 (Halt conversion)
ADC read (converted value) activated; data register in read.

- NOTE : bits D5, D6, D7, and D13 are fixed to level 0.

c) Vector Number register

When the CPU has registered and acknowledged an interrupt sent from the board, the board sends back a vector number (on 8 bits) to the CPU, which is used to perform the appropriate subroutine.

- Write : The vector number is "dynamically" programmable, which means, for example, that a different vector can be written in the register for each channel in real time, (except when "busy"=1).

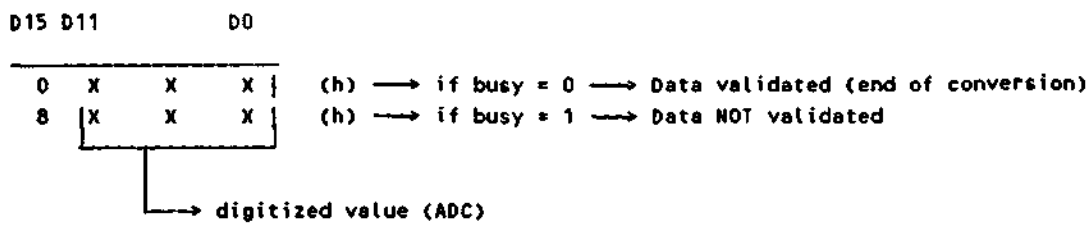
- Read : Copy of previously written register (last write registered).

NOTE : During the acknowledge cycle in interrupt serviced mode, validation of the vector number register in read is no longer 3 (h), but the address @x present on the address bus (A1, A2, A3), if this corresponds to the interrupt line number selected on the board.

d) Data register

This register contains data from the 12-bit ADC (result of conversion) in D0 to D11, and the "busy" bit in D15, which can be tested at the same time as the ADC read (figure 5). This bit is the same as D10 in the status register (chapter b).

The three remaining bits D14, D13, D12 are forced to 0, and the following is read on the data register :



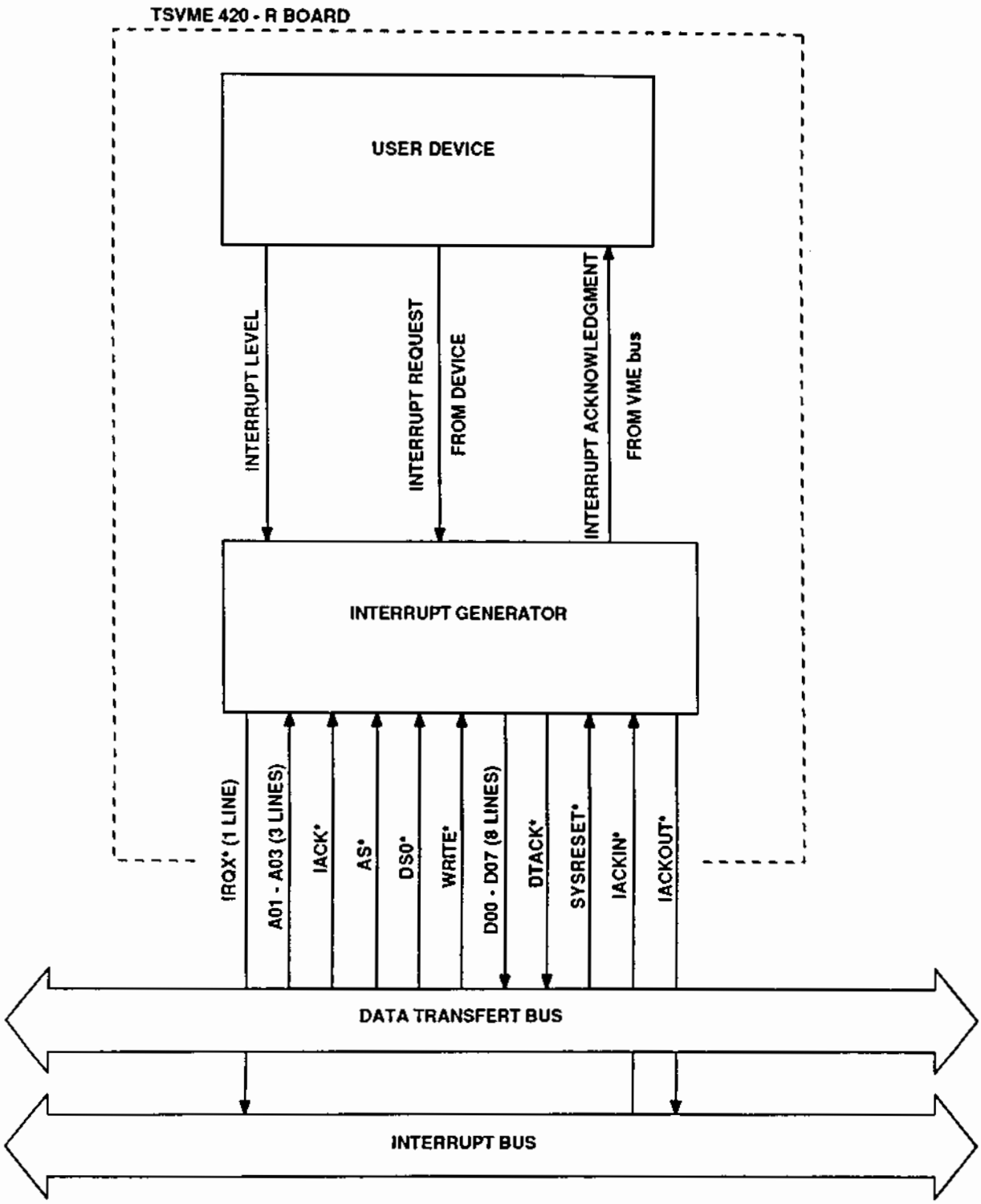
- As the board operates in A/D conversion, the data register is only read-accessible.

2.4.3 - Interrupts

The board may generate an interrupt on the VME bus. This request - 1 line - IRQx - can be sent on one of the 7 different VMEbus lines (IRQ1 to IRQ7) by means of selector S13. Acknowledgement of the interrupt by the CPU is recognized by the board's IT generator (via A1, A2, A3 and the same selector S13), which returns the vector number to the CPU, with DTACK* (figure 6 and chapter 2.6.3).
In this way the board monitors interrupts cycles using IACK*, IACKIN*, and AS*. The board operates in accordance with the VME "daisy chain" principle.

. IACKOUT* = 0 = IACKIN* (continuity)	no IT generated by board IT served by CPU # IT requested
. IACKOUT* = 1 ("daisy chain" interrupted)	IT served by CPU = IT requested

FIGURE 6



Block diagram: INTERRUPT GENERATOR

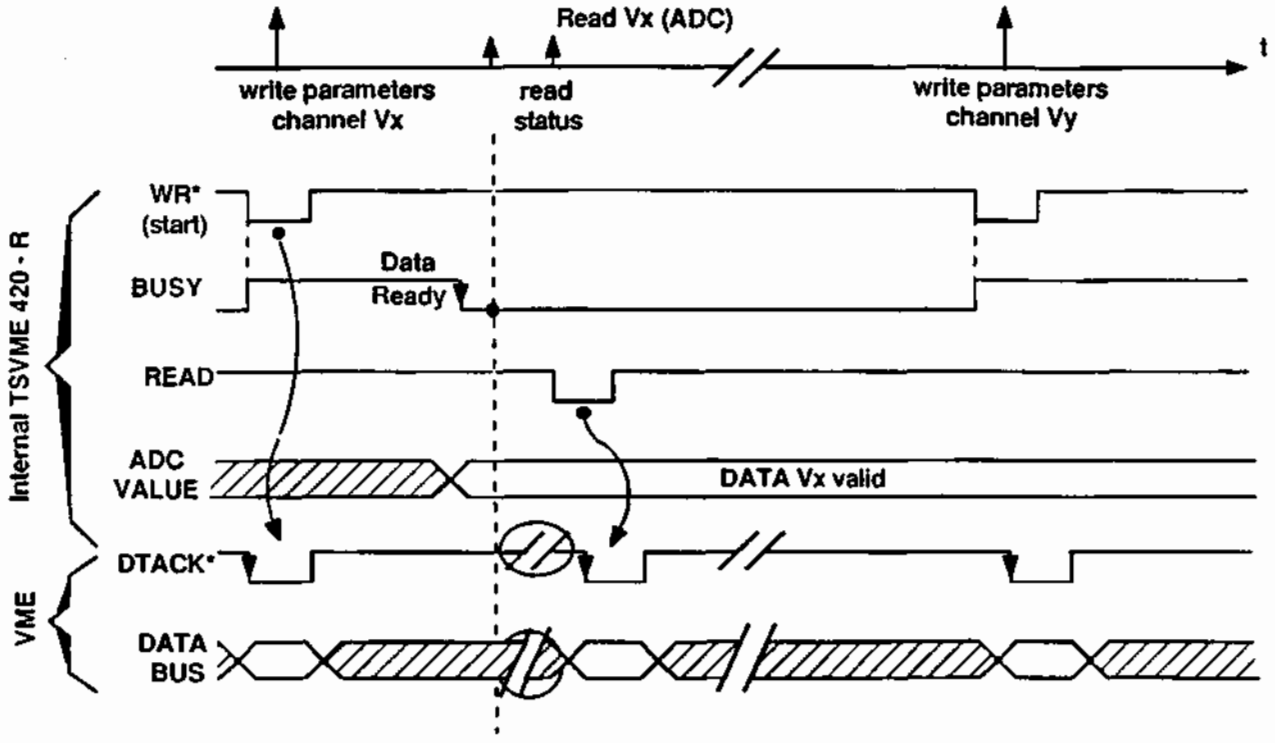
2.5 - OPERATION

The procedure for complete conversion on any one channel is essentially as follows :

"Write" channel Vx/Read channel Vx - "Write" channel Vy/Read etc.

2.5.1 - "Polling" mode

FIGURE 7



NOTE :  See chapter 2.6 for "status" read cycle.

* The "busy" bit (available on status register or ADC data bus in read), is used by the CPU to examine the validity of data from the ADC.

NOTE : The "busy" bit switches back to 1 within 100 nsec.(max) of the falling edge of WR* (write, start).

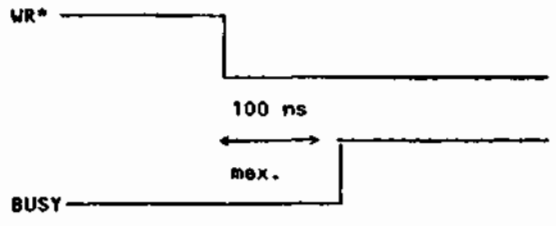
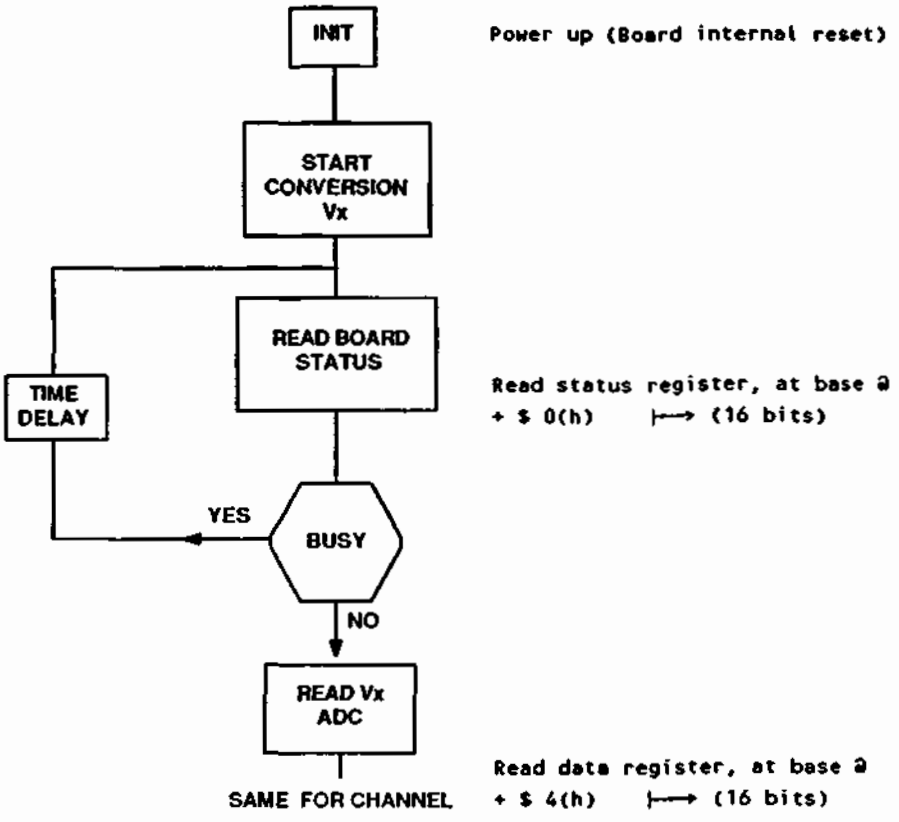


FIGURE 8



2.5.2 - Interrupt serviced mode FIGURE 9

NOTE : See chapter 2.6 for interrupt acknowledge cycle.

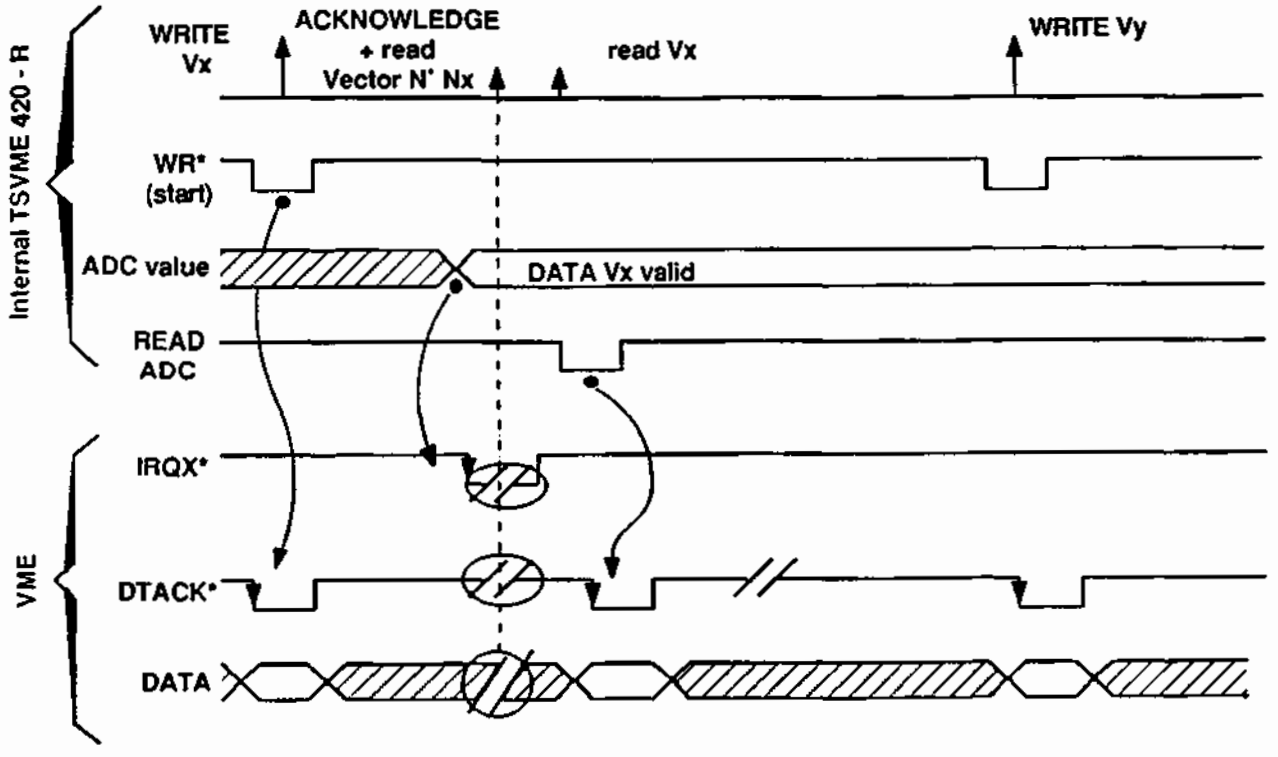
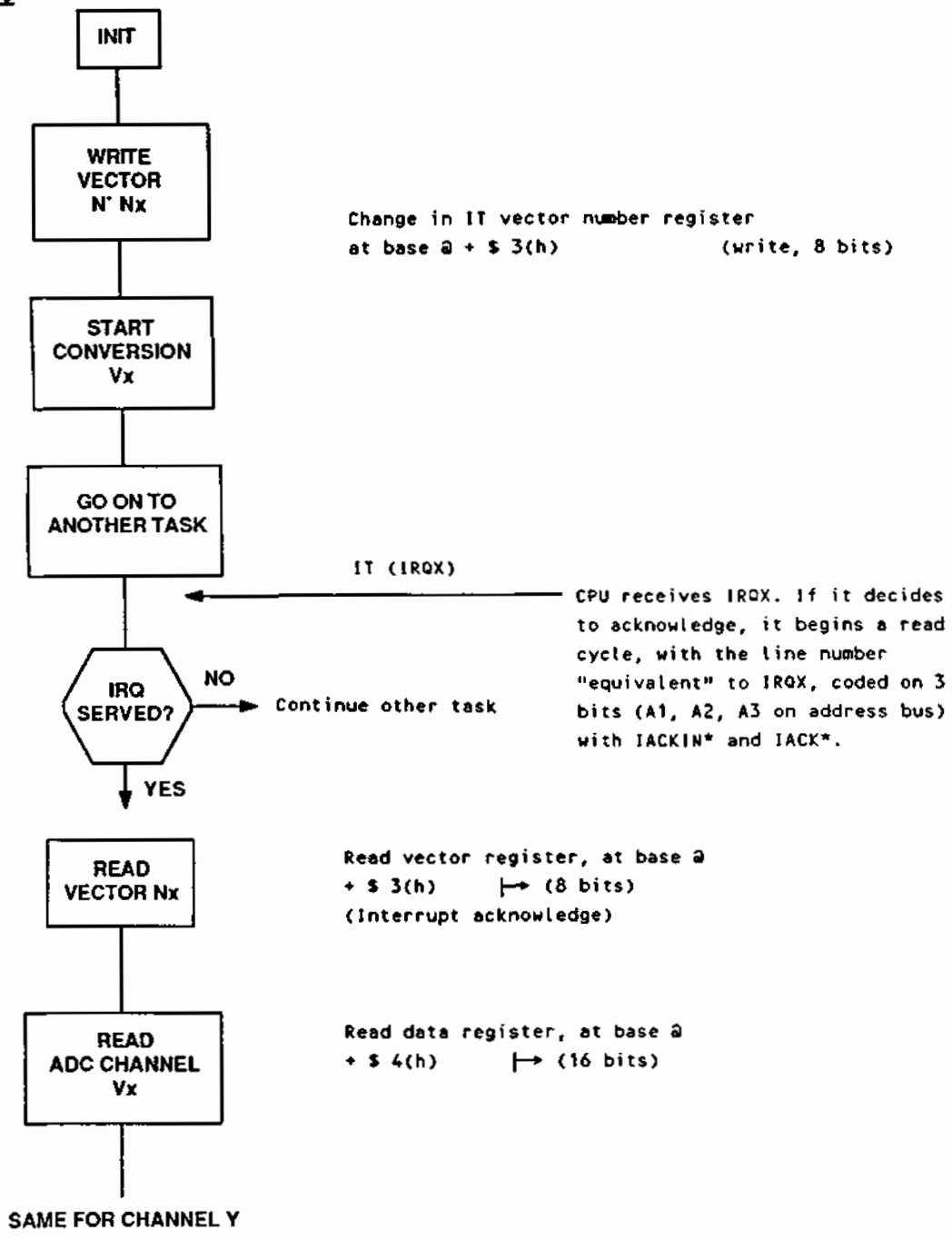
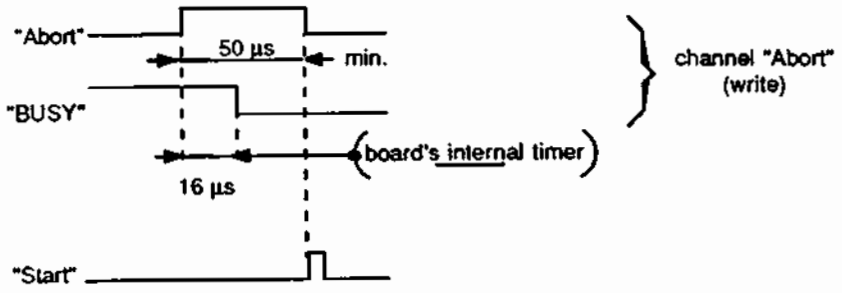


FIGURE 10


INIT
WRITE VECTOR N° Nx
Change in IT vector number register at base @ + $ 3(h) (write, 8 bits)
START CONVERSION Vx
GO ON TO ANOTHER TASK
IT (IRQX)
CPU receives IRQX. If it decides to acknowledge, it begins a read cycle, with the line number "equivalent" to IRQX, coded on 3 bits (A1, A2, A3 on address bus) with IACKIN* and IACK*.
IRQ SERVED?
NO
Continue other task
YES
READ VECTOR Nx
Read vector register, at base @ + $ 3(h) ⊢→ (8 bits) (Interrupt acknowledge)
READ ADC CHANNEL Vx
Read data register, at base @ + $ 4(h) ⊢→ (16 bits)
SAME FOR CHANNEL Y

2.5.3 - Notes

a) All registers are read-accessible when the board is converting (busy = 1). They are write-protected unless, in the case of the control register, "Abort"= 1.



b) It should be noted that the "busy" bit in "interrupt" mode is always accessible at the same places and with the same timing as in "Polling" mode.

2.6 - TIMINGS FOR WRITE/READ AND INTERRUPTS

2.6.1 - Write

Write mode complies with VME standards. (See figure 11).

FIGURE 11 - Write cycle on control or vector register

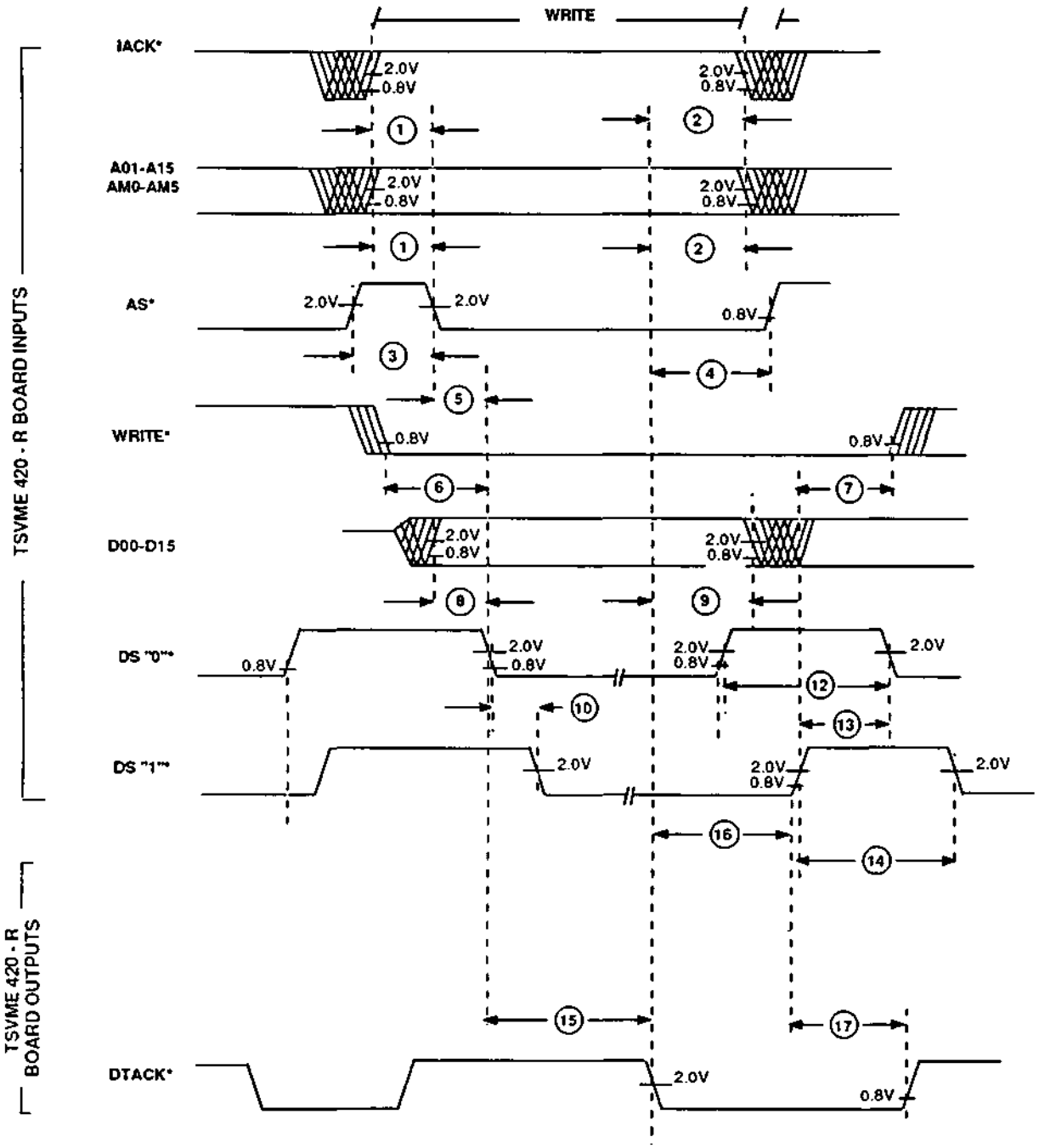


FIGURE 11 - TIMINGS -

No.	PARAMETER	MIN(ns)	MAX(ns)	NOTE
1	Axx and AMx valid and IACK* high to AS* low	10		D
2	DTACK* low to invalid address or IACK* low	0		C
3	AS* high	30		D
4	DTACK* low to AS* high	0		C
5	Offset AS* DS0*	-10		D
6	WRITE* valid to DS0*	10		D
7	DS1 high to invalid WRITE*	0		D
8	Data valid to DS0* low	10		D
9	DTACK* low to invalid data	0		C
10	Offset DS0* to DS1*		20	D
12	DS0* high	30		D
13	DS1* high to DS0* low	30		D
14	DS1* high	30		D
15	DS0* low to DTACK* low	150	300	C
16	DTACK* low to DS1* high	0		C
17	DS1* high to DTACK* high	0	130	B

NOTES :

B - This time is guaranteed between outgoing signal transitions.

C - The board must wait for the incoming signal edge from the MASTER board before changing the level of its output signal

D - This guarantees that the MASTER will not change the incoming signal until the board has changed its outgoing signal.

2.6.2 - Read

Register read mode complies with VME standards (see figure 12).

FIGURE 12 - Read of control, status, and data registers

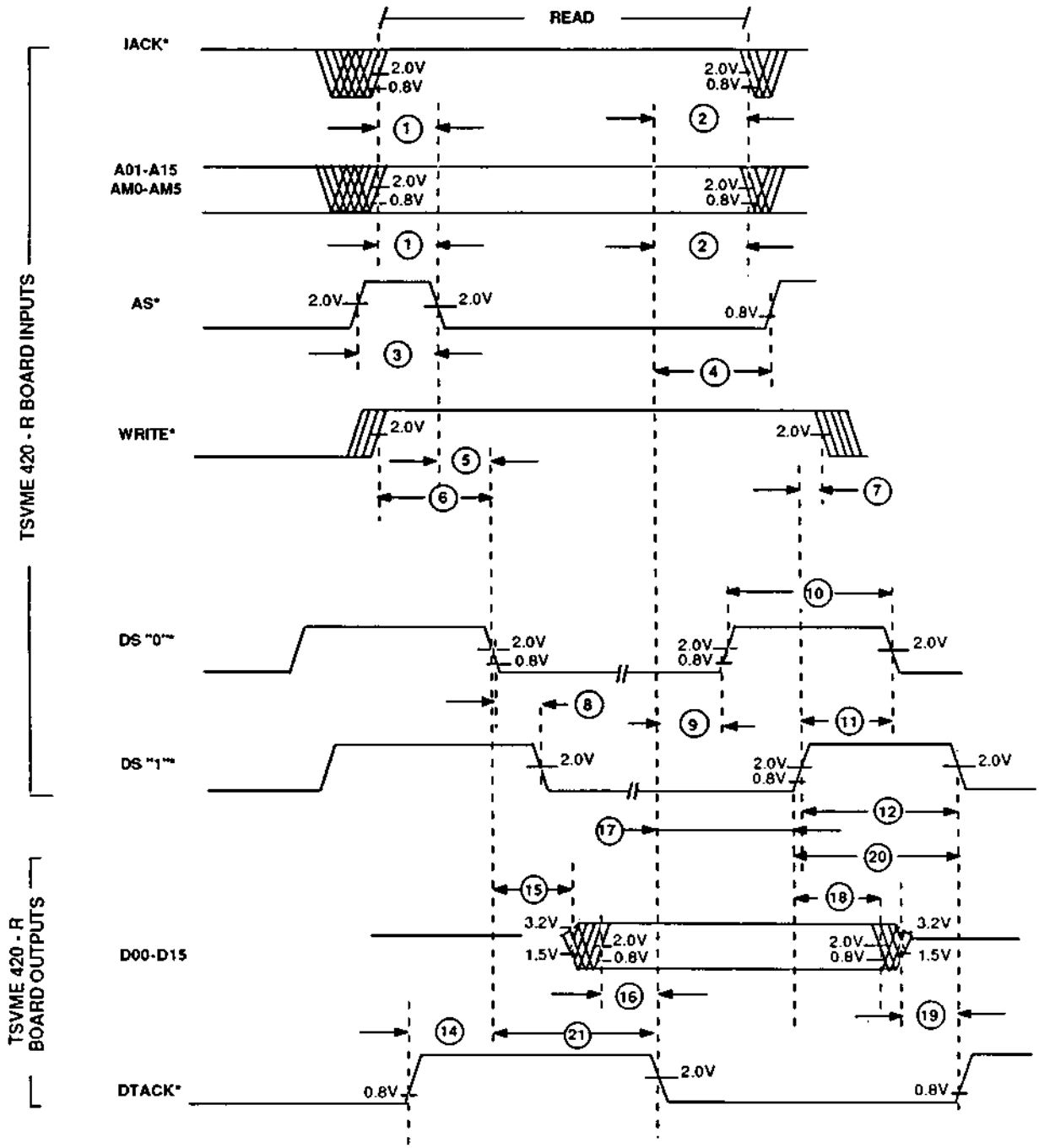


FIGURE 12 - TIMINGS

No.	PARAMETER	MIN(ns)	MAX(ns)	NOTE
1	Axx and AMx valid and IACK* high to AS* low	10		E
2	DTACK* low at invalid address or IACK* low	0		D
3	AS* high	30		E
4	DTACK* low to AS* high	0		D
5	Offset AS* DS0*	-10		E
6	WRITE* valid to DS0* low	10		E
7	DS1 high to invalid WRITE*	0		E
8	Offset DS0* to DS1*		20	E
9	DTACK* low to DS0* high	0		D
10	DS0* high	30		E
11	DS1* high to DS0* low	30		E
12	DS1* high	30		E,C
14	DTACK* high to DS0* low	0		D
15	DS0* low to active data bus	30		C
16	Data valid to DTACK* low	0		B
17	DTACK* low to DS1* high	0		D,C
18	DS0* high to invalid data	0		C
19	Data bus release to DTACK* high	0		B
20	DS1* high to DTACK* high	0		C
21	DS0* low to DTACK* low	150	300	C

NOTES :

B - The board must guarantee this time between two outgoing signal transitions.

C - The board must wait for the incoming signal edge from the MASTER before changing the level of its ougoing signal

D - This guarantees that the MASTER will not change the incoming signal until the board changes its outgoing signal.

E - The board is guaranteed this time between two of its outgoing signal transitions.

2.6.3) Interrupts

See figure 13, interrupt generator complies with VME standards.

FIGURE 13 - INTERRUPT ACKNOWLEDGE CYCLE

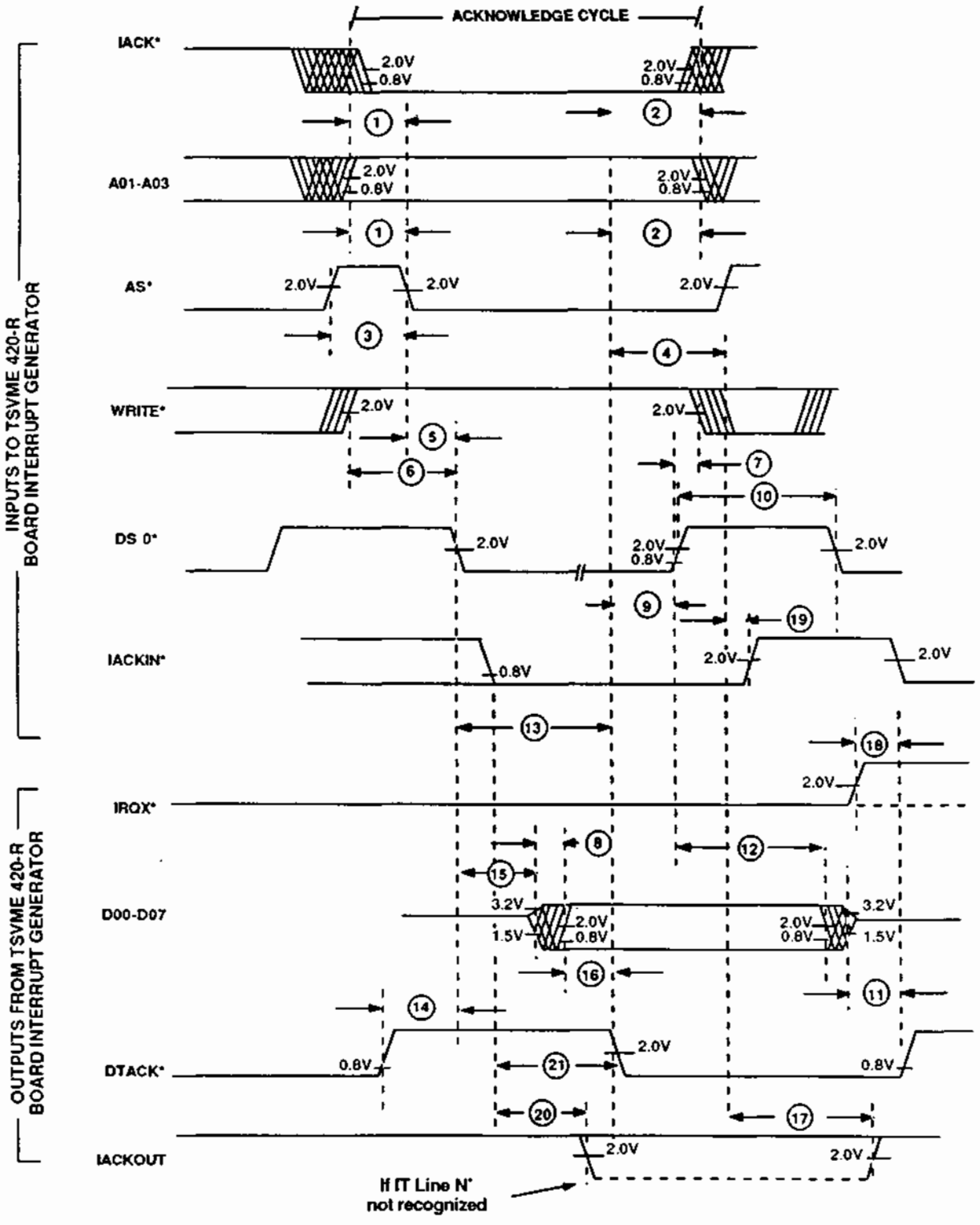


FIGURE 13 - TIMINGS

No.	PARAMETER	MIN(ns)	MAX(ns)	NOTES
1	Axx and AMx valid and IACK* high to AS* low	10		E
2	DTACK* low to invalid address or IACK* high	0		D
3	AS* high	30		E
4	DTACK* low to AS* high	0		D
5	Offset AS* DSO* low	-10		E
6	WRITE* high to DSO* low	10		E
7	DSO* high to invalid WRITE*	0		E
8	IACKIN* low to active data bus	0		C
9	DTACK* low to DSO* high	0		D
10	DSO* high	30		E
11	Data bus release to DTACK* high	0		B
12	DSO* high to invalid data	0		C
13	DSO* low to DTACK* low	0		C
14	DTACK* high to DSO low	0		D
15	DSO* low to active data bus	30		C
16	Valid data to DTACK* low	0		B
17	AS* high to IACKOUT* high		30	F
18	IRQ* release to DTACK* release	0		B
19	AS* high to IACKIN* high		40	E
20	IACKIN* low to IACKOUT* low	40	150	C
21	IACKIN* low to DTACK* low	190	450	C

NOTES :

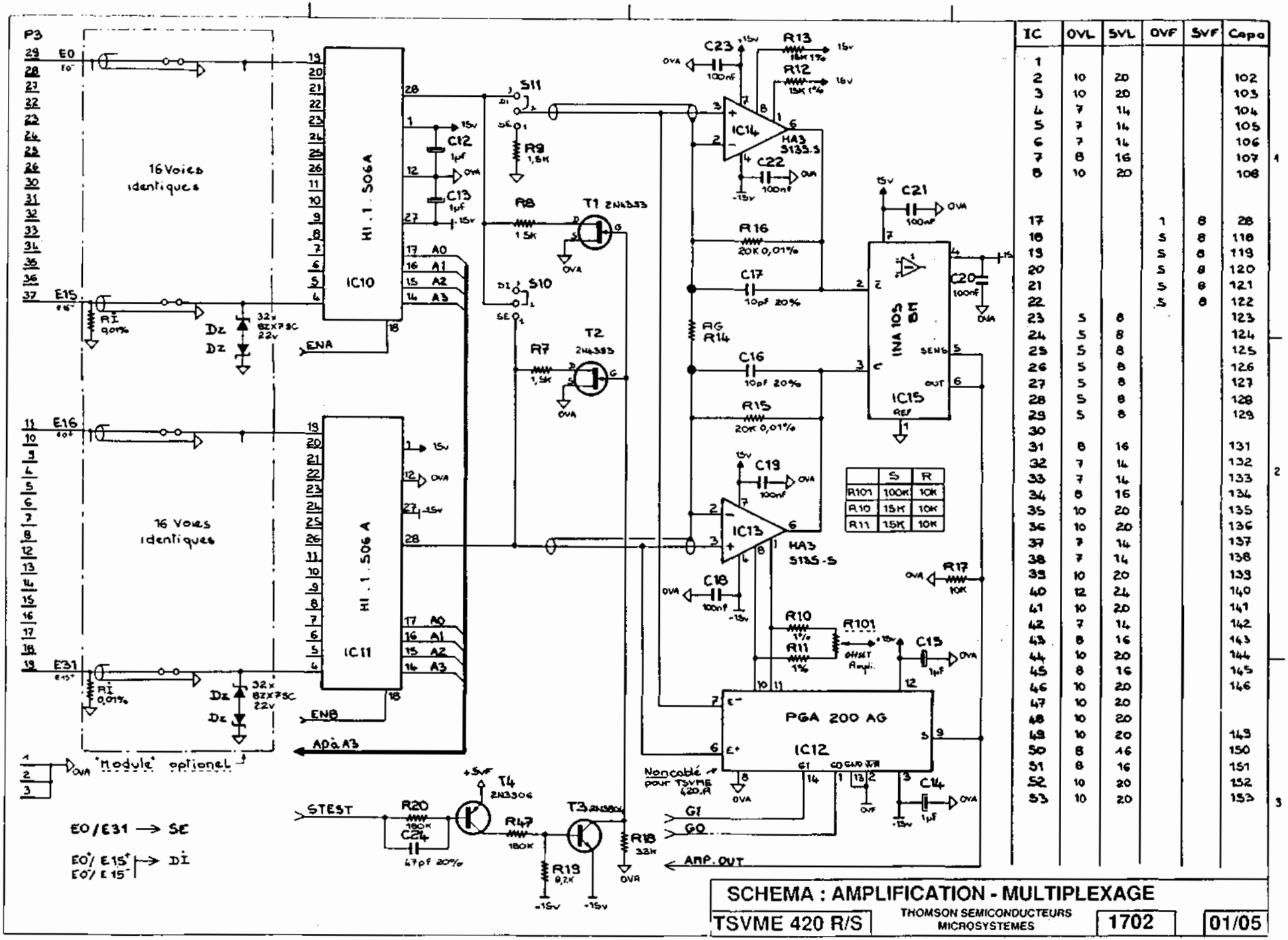
B - The INTERRUPT GENERATOR must guarantee this time between two outgoing signal edges.

C - The INTERRUPT GENERATOR must wait for input signal edge from the INTERRUPT CONTROLLER before changing the level of its outgoing signal.

D - This guarantees that the INTERRUPT CONTROLLER will not change the incoming signal until the INTERRUPT GENERATOR changes its outgoing signal.

E - The INTERRUPT GENERATOR is guaranteed this time between two of its incoming signal edges.

F - The INTERRUPT GENERATOR must guarantee this time between the incoming signal and its ougoing signal.

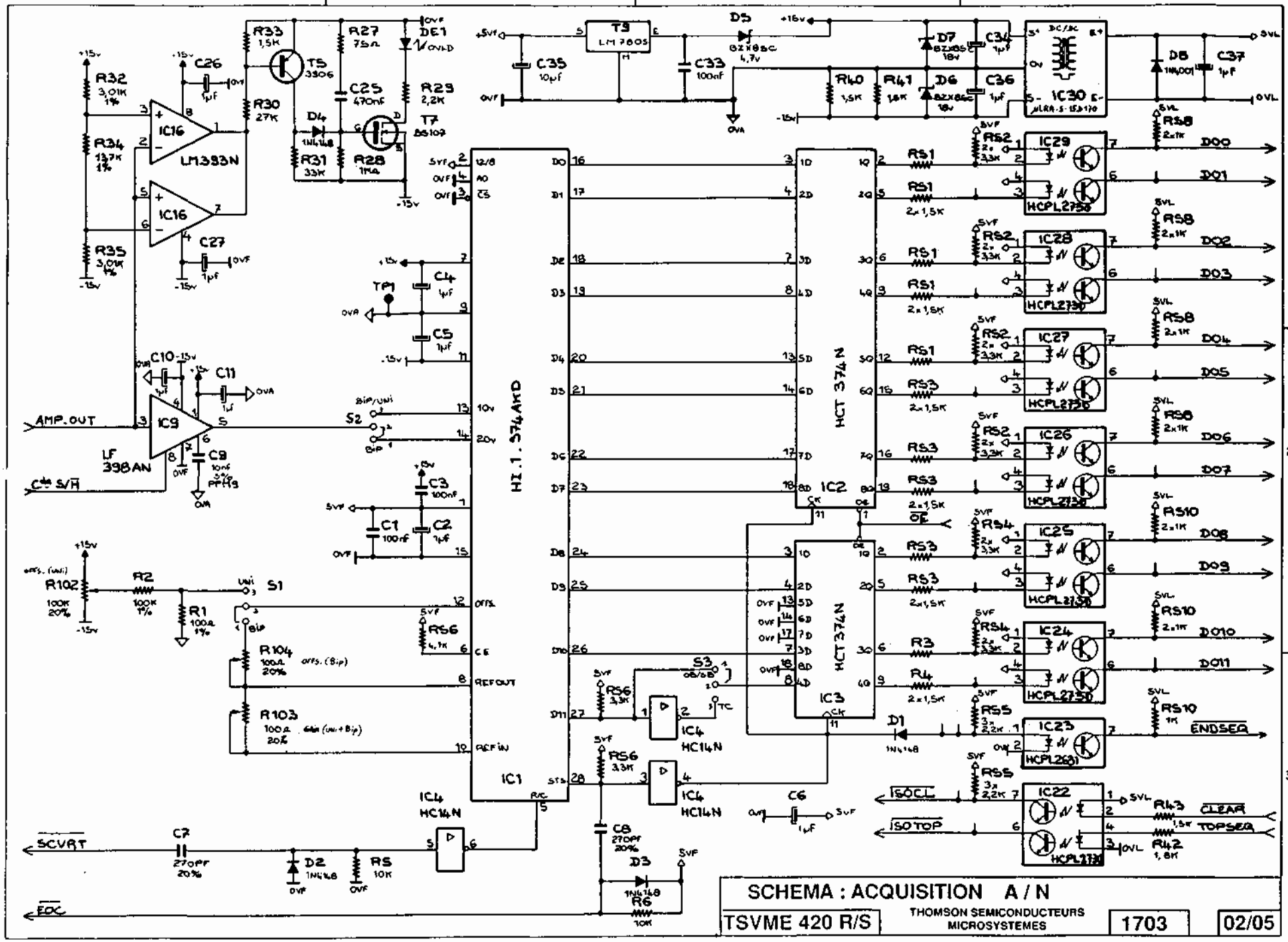


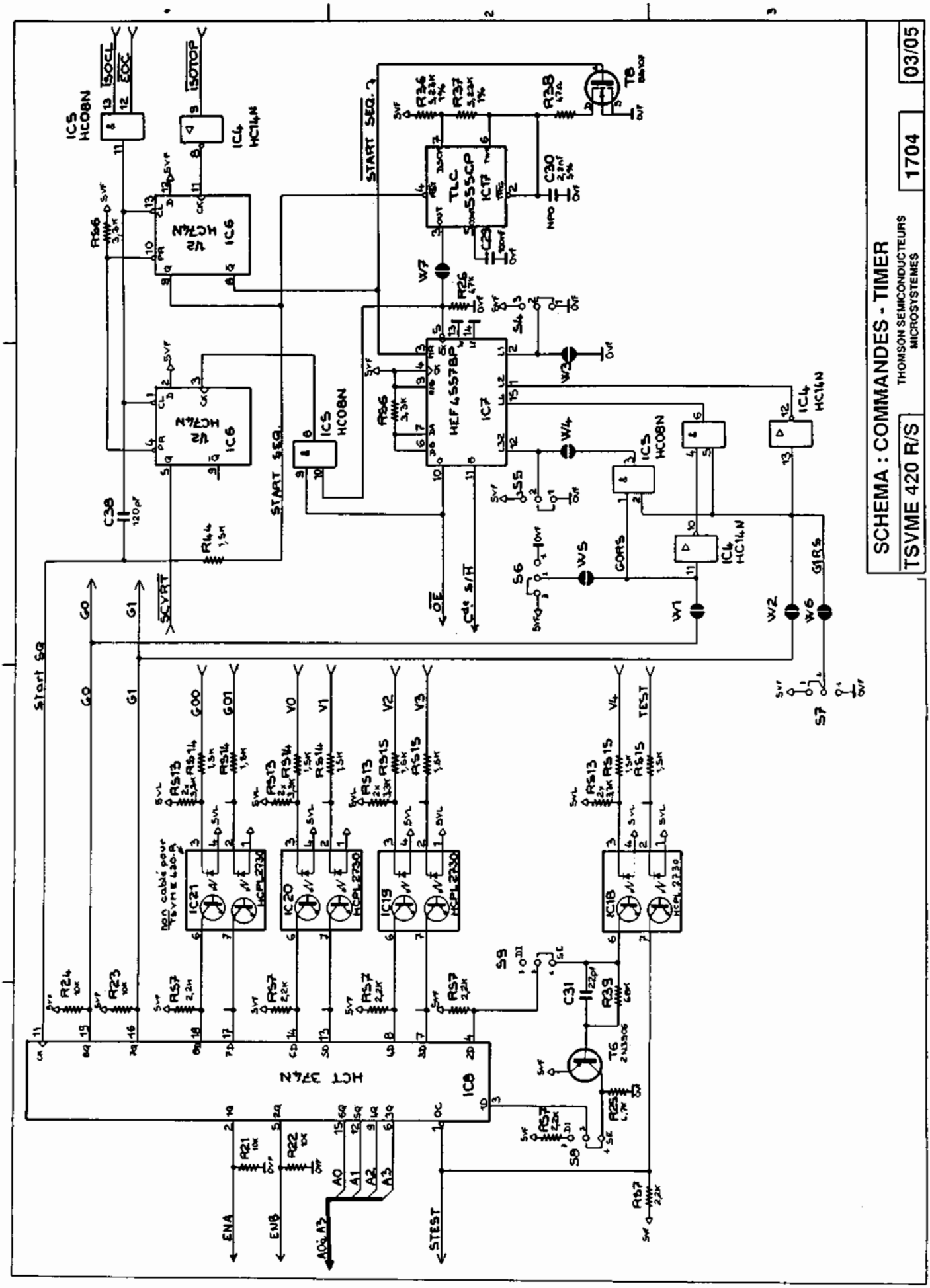
	S	R
R101	100K	10K
R10	15K	10K
R11	15K	10K

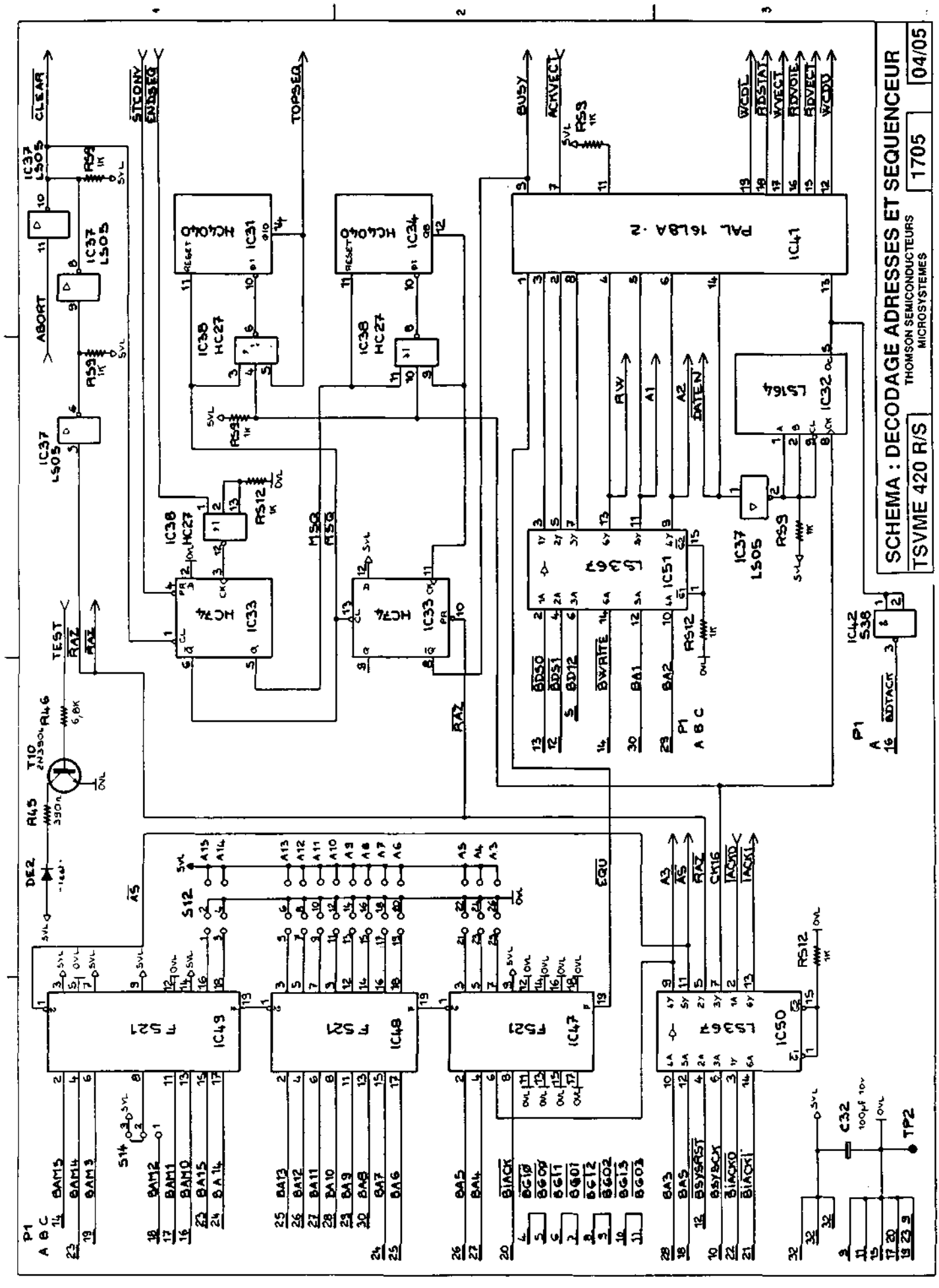
IC	OVL	SVL	OVF	SVF	Capa
1					
2	10	20			102
3	10	20			103
4	7	14			104
5	7	14			105
6	7	14			106
7	8	16			107
8	10	20			108
17			1	8	28
18			1	8	118
19			1	8	119
20			1	8	120
21			1	8	121
22			1	8	122
23	5	8			123
24	5	8			124
25	5	8			125
26	5	8			126
27	5	8			127
28	5	8			128
29	5	8			129
30					
31	8	16			131
32	7	14			132
33	7	14			133
34	8	16			134
35	10	20			135
36	10	20			136
37	7	14			137
38	7	14			138
39	10	20			139
40	12	24			140
41	10	20			141
42	7	14			142
43	8	16			143
44	10	20			144
45	8	16			145
46	10	20			146
47	10	20			
48	10	20			
49	10	20			149
50	8	16			150
51	8	16			151
52	10	20			152
53	10	20			153

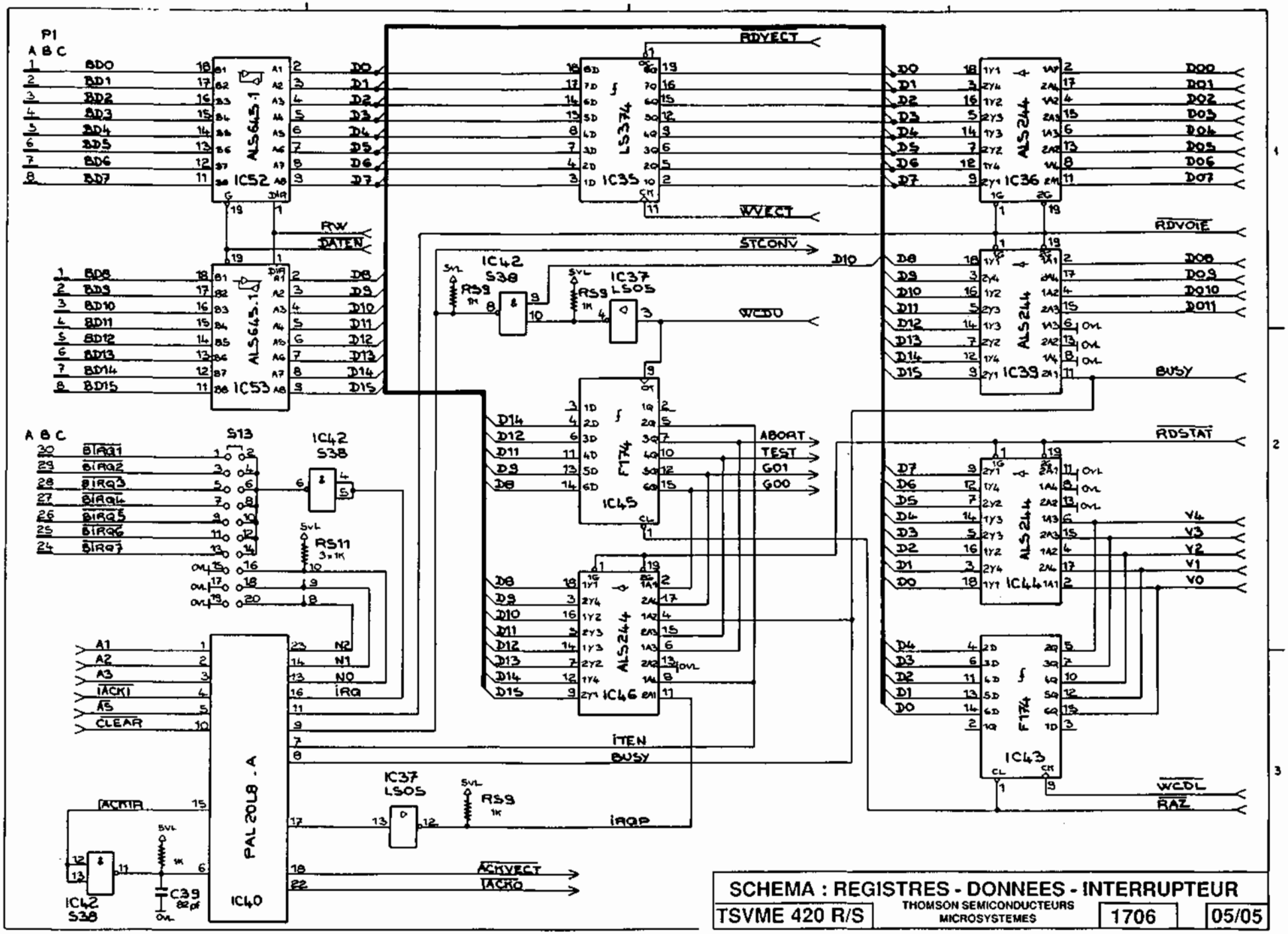
SCHEMA : AMPLIFICATION - MULTIPLEXAGE

TSVME 420 R/S | THOMSON SEMICONDUCTEURS MICROSYSTEMES | 1702 | 01/05


SCHEMA : ACQUISITION A / N
TSVME 420 R/S
THOMSON SEMICONDUCTEURS MICROSYSTEMES
1703
02/05
IC16
LM393N
IC9
LF 398AN
HI.1.574AKD
IC1
HCT 374N
IC2
IC3
IC4
HC14N
IC30
IC29
IC28
IC27
IC26
IC25
IC24
IC23
IC22
HCPL2730
HCPL2631
AMP.OUT
S/H
SCVRT
EOC
ISOCT
ISOTOP
ENDSEQ
CLEAR
TOPSEQ


SCHEMA : COMMANDES - TIMER
TSVME 420 R/S
THOMSON SEMICONDUCTEURS
MICROSYSTEMES
1704
03/05
START SEQ.
HEF4557BP
TLC555CP
HCT 374N
HCPL2230
ENA
ENB
STEST
TEST


SCHEMA : DECODAGE ADRESSES ET SEQUENCEUR
TSVME 420 R/S
1705
04/05
THOMSON SEMICONDUCTEURS
MICROSYSTEMES
PAL 16L8A-2
IC41
LS164
IC32
LS05
IC37
HC00
IC31
IC34
HC27
IC38
HC74
IC33
LS74
IC39
IC51
LS367
IC50
IC42
LS38
F521
IC49
IC48
IC47
CLEAR
ABORT
STCONV
ENDSEQ
TOPSEQ
BUSY
ACKVECT
WDOG
ADSTAT
WVECT
RDVOIE
RDVECT
WCDV
TEST
RAZ
DE2
T10
2N3904
R45
390R
R46
6,8K
S12
S14
TP2
C32
100pF 10V
P1
A B C



SCHEMA : REGISTRES - DONNEES - INTERRUPTEUR

TSVME 420 R/S	THOMSON SEMICONDUCTEURS MICROSYSTEMES	1706	05/05

III - USE

3.1 - RECEPTION OF EQUIPMENT

* Check that the board's packing is in good condition. If this is not the case, make sure that the carrier is present when the package is opened for inspection of the equipment.

* Check that the items mentioned on the product inventory list have all been delivered. It is a good idea to keep the packing for any future transportation. Make sure that no damage has occured to the front edge strip or components.

* The board contains MOS components, and must not, therefore, be exposed to excessive electrostatic charges.

3.2 - BOARD CONFIGURATION

The board is delivered with the following configurations :

- Differential mode (16 inputs)
- ADC code = offset binary
- ADC range = +/- 10 VFSR
- Base address = Customer configuration
- Address Modifiers = Customer configuration
- IT line number = Customer Configuration

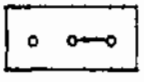
3.2.1 - Address modifiers

* Selector S14, see figure 14 :



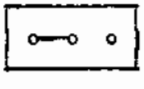
S14 (component layout)

POSITION A :



S14 Supervisor and user mode (code $29, $2D)

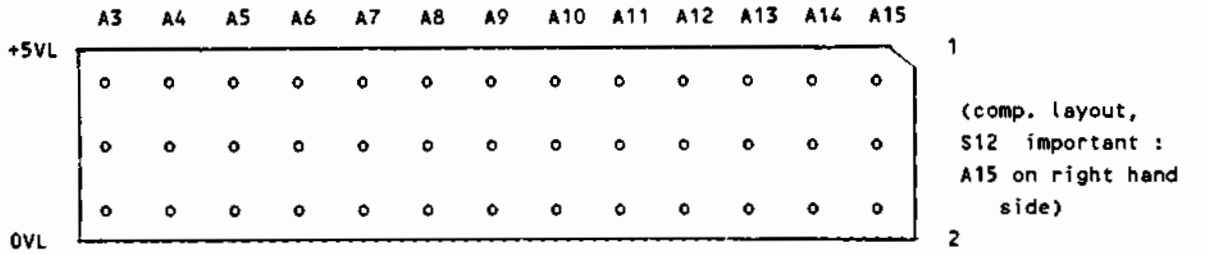
POSITION B:



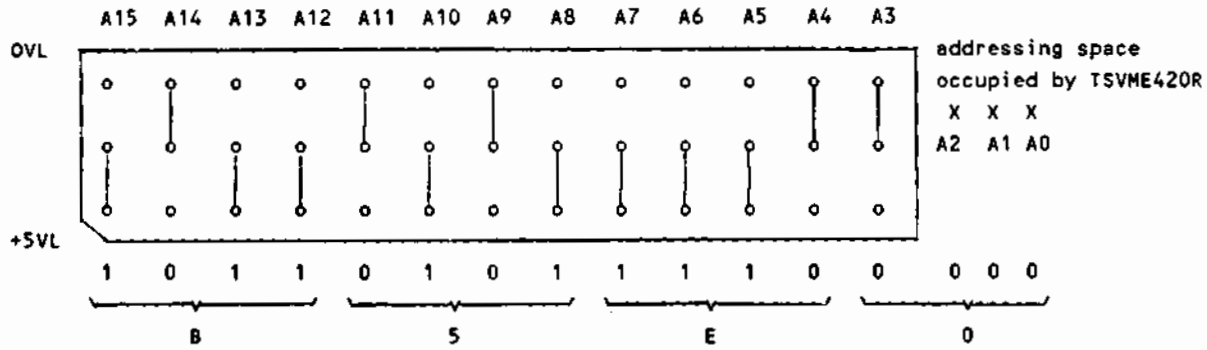
S14 Supervisor mode ($2D code)

3.2.2 - Base address configuration

Selector S12, see figure 14.



Example :



(address = $B5E0)

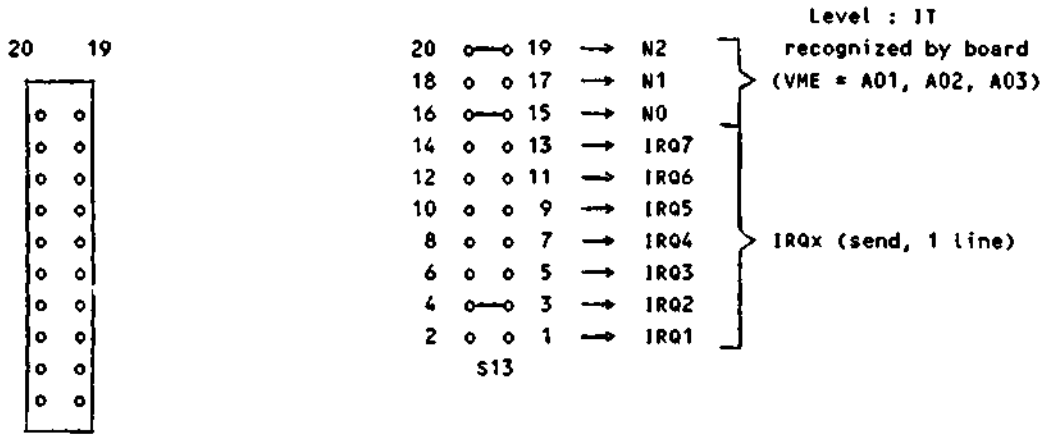
3.2.3 - Selection of interrupt line number

- Selector S13 is used to set the interrupt level on which the board sends out requests after conversion (if bit D14 ITEN in the control register is at 1).

- This selector consists of 7 jumpers for setting the request level, and 3 jumpers for the acknowledge level.

- IMPORTANT : Only one jumper must be set on IRQX, and the corresponding level X must be coded on N0, N1, N2.

Example :



S13 - IT (component layout)

The example shows an interrupt level of 2 (IRQ2) ⟶ (N2, N1, N0) = (0, 1, 0) = 2 (H). This is coded on S13 with the appropriate jumpers.

Table showing correspondence between IRQX and N2, N1, N0. This must be observed for the board to operate correctly in interrupt serviced mode.

IT number recognized	N2	N1	N0	IRQx (send)
1	0	0	1	IRQ1
2	0	1	0	IRQ2
3	0	1	1	IRQ3
4	1	0	0	IRQ4
5	1	0	1	IRQ5
6	1	1	0	IRQ6
7	1	1	1	IRQ7

1 = jumper absent \ N2, N1, N0
0 = jumper present /

above example

ligne cut = jumper absent \ IRQX
ligne enabled = jumper absent/

3-bit coding 1 jumper

S13

If what is wanted is just "hard" protection against interrupts, this is simply a question of removing the jumper on IRQx, and setting the three jumpers on N0, N1, N2.

3.2.4 - "Test" indicator

- Yellow LED (DE2) (see figure 14)

DE2 on → test mode
DE2 off → normal operation

3.2.5 "Overload" indicator

- Red LED (DE1) (see figure 14)

DE1 on → one or more input overloads
DE1 off → no input overloads

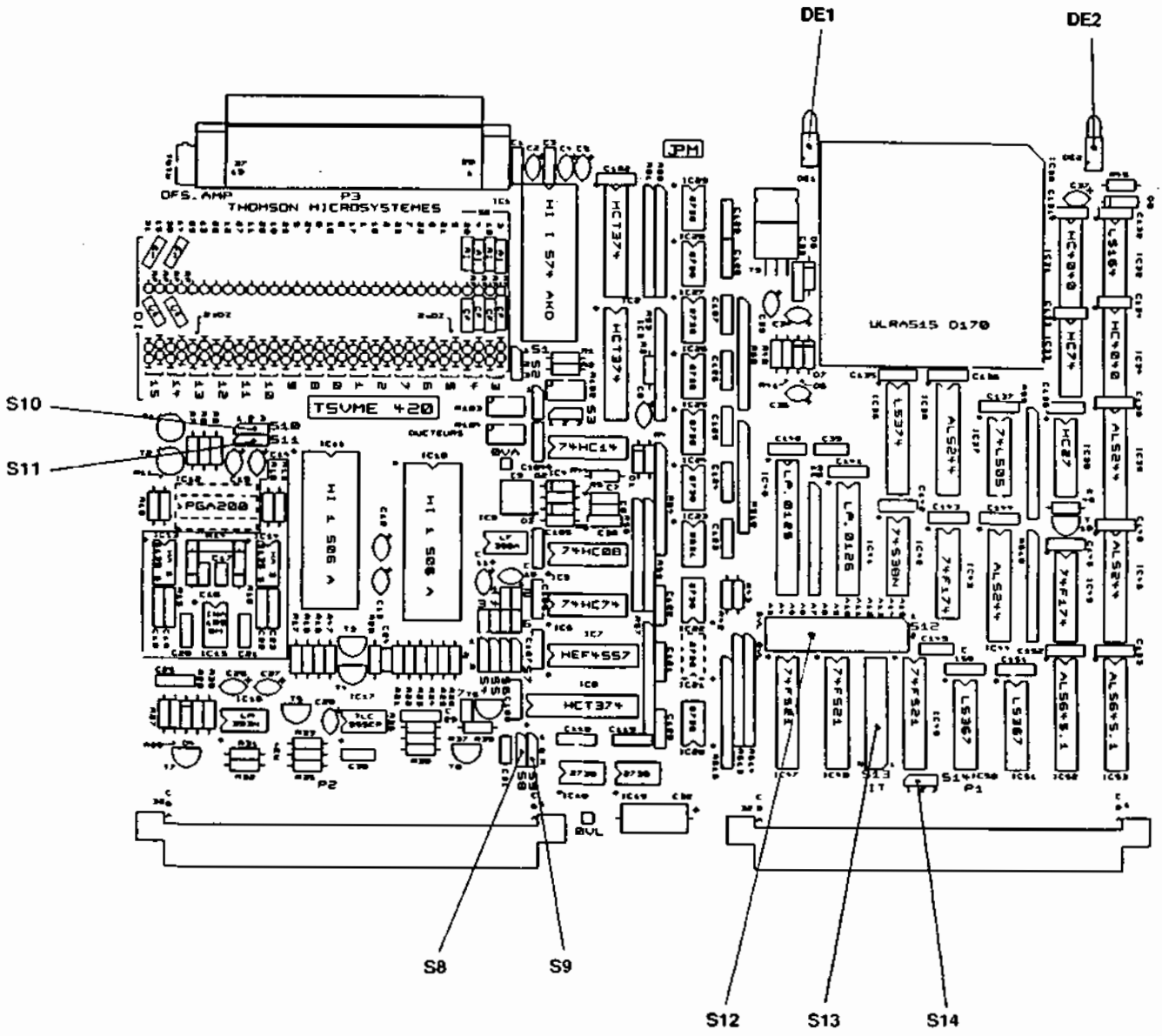
NOTE :

The characteristics of the overload sensor are such that the led will not flicker, even if the programed scanning is slow and with only one channel in "overload".

. Detection comes in at ± 10.4 V, and is therefore valid for ADC ranges = ±10VFSR, or 0/10VFSR.

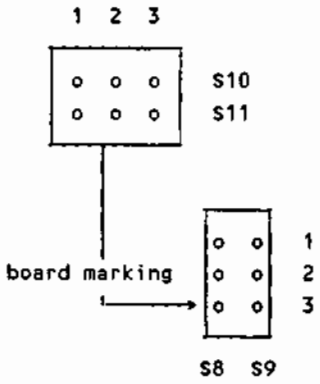
. Overload detection will still be at 10.4V, even for the ADC range = ±5VFSR, though finer detection, at, say, ±5.2V can be obtained by replacing R34 13.7 = Kohm by a resistor of 3.24 Kohm (1% -50 ppm/ °C-1/4W, from RTC -, sovcor etc.)

FIGURE 14


DE1
DE2
S10
S11
S8
S9
S12
S13
S14
TSVME 420
THOMSON MICROSYSTEMES
P3
P2
P1
PGA200
74HC14
74HC08
74HC74
HCT374
HEF4557
ULRA515 0170

3.2.6 - Selection between "differential/single ended" :

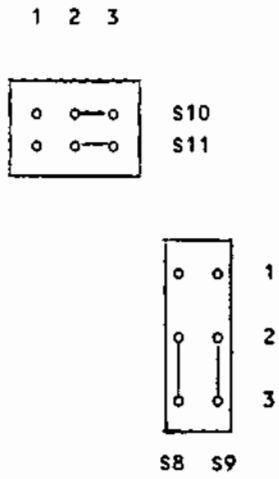
Selectors S8, S9, S10, S11 (see figure 14)



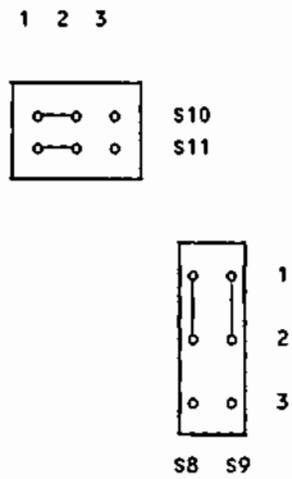
These selectors act on the analog MUX and the MSB side of the channel number.

(DI) = Differential ⟶ 16 analog inputs
(SE) = Single Ended ⟶ 32 analog inputs

DIFFERENTIAL

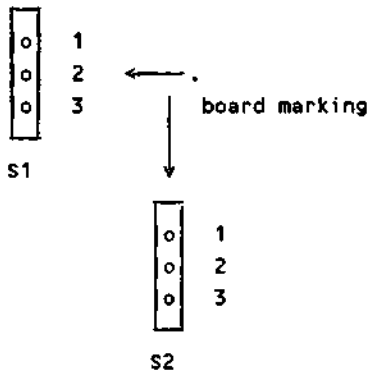


SINGLE ENDED



3.2.7 - Selection of ADC input range

Selector S1, S2 (see figure 15)



* Unipolar input (UNI) : 0/10V -FSR-

* Bipolar input (BIP) : ± 5V, ± 10V
-FSR-
(FSR : Full Scale Range)

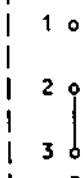
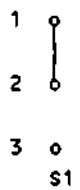
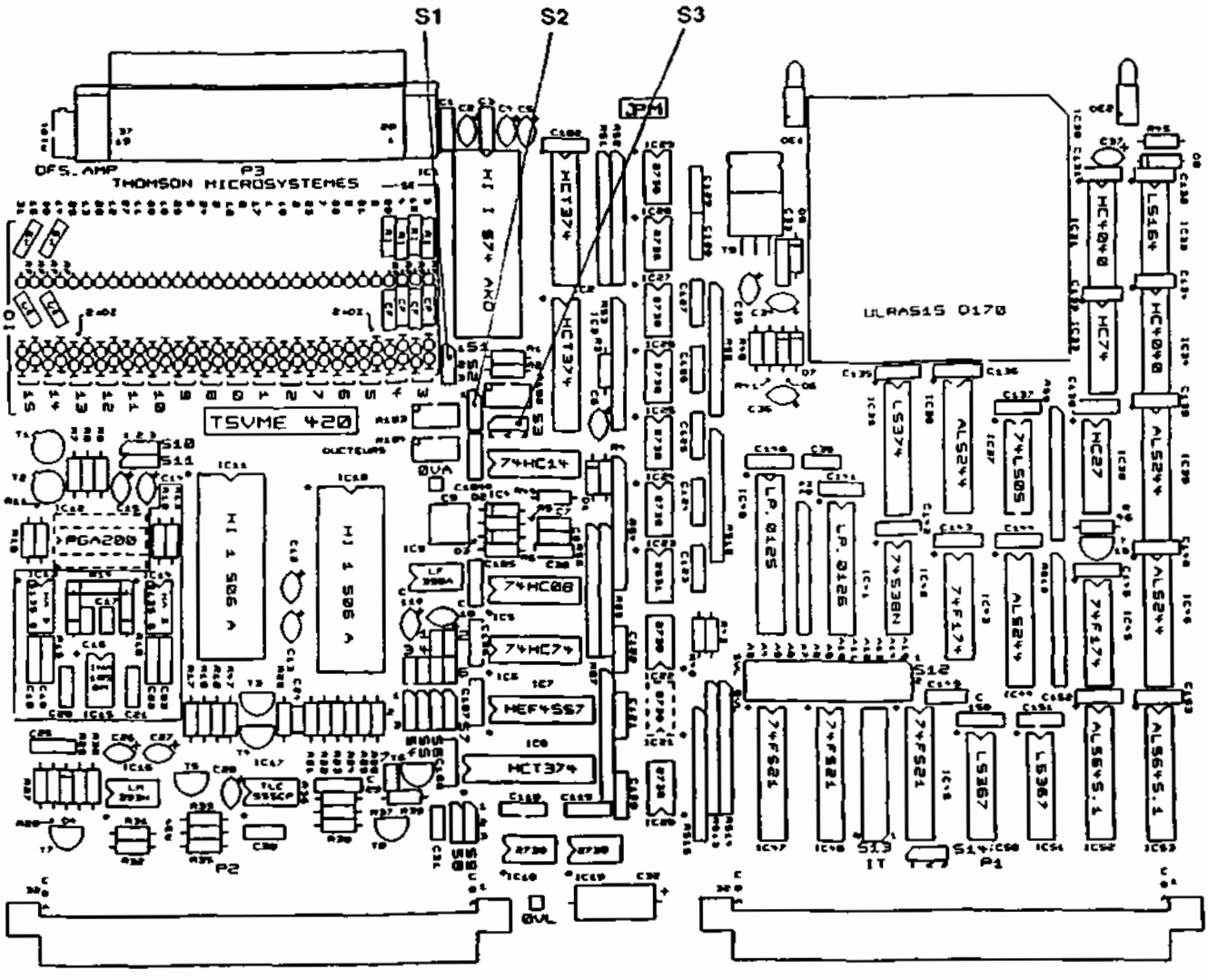
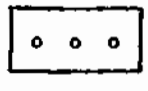
UNIPOLAR	BIPOLAR	
0 to 10 volts	± 5 volts	± 10 volts
		
S1 S2	S1 S2	S1 S2

FIGURE 15



3.2.8 - Selection of ADC output code

Selector S3, see figure 15.



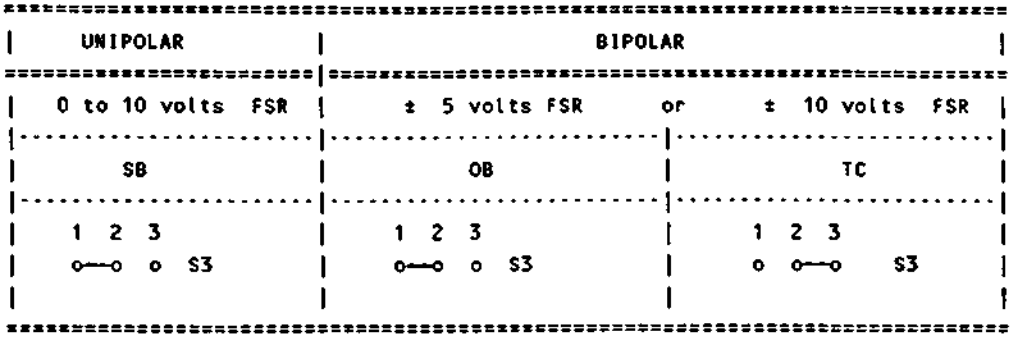
board marking

There are three coding modes. The polarity (+/-) of the voltage on the analog input must be checked before selecting the ADC output code.

Unipolar analog voltage -> "straight binary" coding
Bipolar analog voltage -> "offset binary" coding
"twos complement" coding

It can thus be seen that S1 and S2 must be correctly set (paragraph 3.2.7) before selecting S3.

Straight binary = SB (CSB*)
Offset binary = OB (COB*)
Twos complement = TC (CTC*) MSB of ADC = sign bit



3.2.9 - Selection of INA gain

* INA can take gain values from 1 to 1000. The required gain is obtained by wiring a resistance (Rg) onto the board. (At R14, see Fig. 15 a).

$$\text{. Gain (INA)} = \frac{40 \text{ Kohms}}{Rg} + 1 = G$$

R14 [o o] (board marking)

$$\text{. RG} = \frac{40 \text{ Kohms}}{G-1} \text{ (in ohms)}$$

NOTE : 40 Kohms = 2 x 20 Kohms within the board.

* Example

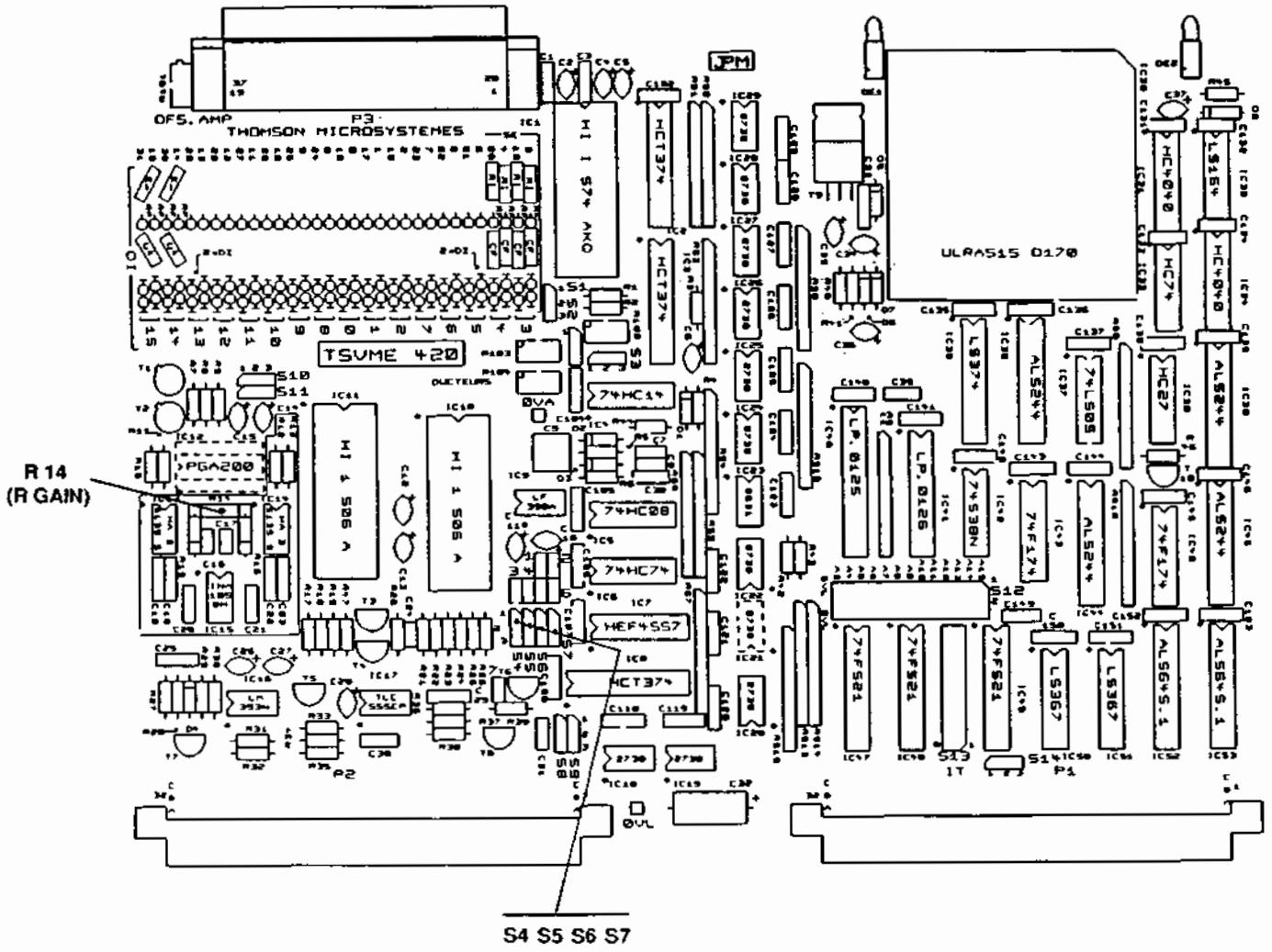
G = 1 (TSVME 420-R board) ⟶ RG ⟶ infinity = no resistance wired
G = 2 ⟶ RG = 40,000 Kohms
G = 1000 ⟶ RG = 40,040 ohms

NOTE : In order not to degrade the nominal specifications of the board, RG should be a high quality metal layer type resistor : - 1/4 W - 0.01% - 5 ppm/degrees C.

Example : VSRJ series (VISHAY), or equivalent from SFERNICE.

3.2.10 - Selection of conversion time (TCONV.)

. Selectors S4, S5, S6, S7 (see figure 15 a)



a

	S4	S5	S6	S7	
1	o	o	o	o	
2	o	o	o	o	board
3	o	o	o	o	marking

These selectors define the overall time required for conversion (TCONV.), with allowance made for INA settling time, dependant on the gain set by Rgain ($1 < G \leq 1000$).

Gain set by R14	$1 < G \leq 10$ Tconv. = 16 µs max.	$10 < G \leq 100$ Tconv. = 250 µs max.	$100 < G \leq 1000$ Tconv. = 1 msec max.
Selection of overall conversion time	S4 S5 S6 S7 1 o o o o 2 o o o o 3 o o o o	S4 S5 S6 S7 1 o o o o 2 o o o o 3 o o o o	S4 S5 S6 S7 1 o o o o 2 o o o o 3 o o o o

3.3 - ANALOG CONNECTIONS

Analog connector P3 is a plastic, 37-pin male, SUB-D "CANNON" type.

a) Mode : Single Ended (SE) : 32 inputs with respect to ground (OVA).
Inputs : Channels 0 to 31, as shown in table.

TABLE 7

Pin number	SIGNAL	Pin number	SIGNAL
19	INPUT 31	37	INPUT 15
18	INPUT 30	36	INPUT 14
17	INPUT 29	35	INPUT 13
16	INPUT 28	34	INPUT 12
15	INPUT 27	33	INPUT 11
14	INPUT 26	32	INPUT 10
13	INPUT 25	31	INPUT 9
12	INPUT 24	30	INPUT 8
11	INPUT 16	29	INPUT 0
10	INPUT 17	28	INPUT 1
9	INPUT 18	27	INPUT 2
8	INPUT 23	26	INPUT 7
7	INPUT 22	25	INPUT 6
6	INPUT 21	24	INPUT 5
5	INPUT 20	23	INPUT 4
4	INPUT 19	22	INPUT 3
3	analog OVA	21	analog OVA
2	analog OVA	20	analog OVA
1	analog OVA		

The analog grounds (OVA) are located together at the end of the connector to facilitate the possible wiring of braiding.

IMPORTANT : The female analog input connector (user) must be a plastic 37-pin SUB-D-37 connector to preserve insulation between inputs and the VME chassis. Equivalent lockable connectors in plastic are available from CANNON and TB & ANSLEY.

b) "Differential" mode (DI) : 16 symmetrical inputs + ground (OVA).
Inputs : Channels 0 to 15, as shown in table.

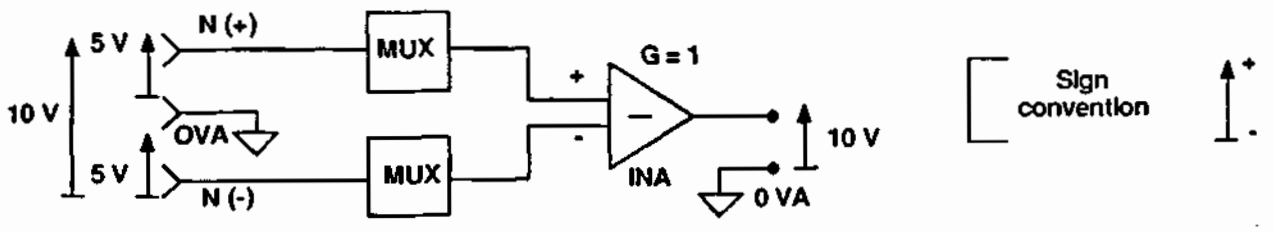
TABLE 8

Pin number	SIGNAL	Pin number	SIGNAL
19	INPUT 15 (+)	37	INPUT 15 (-)
18	INPUT 14 (+)	36	INPUT 14 (-)
17	INPUT 13 (+)	35	INPUT 13 (-)
16	INPUT 12 (+)	34	INPUT 12 (-)
15	INPUT 11 (+)	33	INPUT 11 (-)
14	INPUT 10 (+)	32	INPUT 10 (-)
13	INPUT 9 (+)	31	INPUT 9 (-)
12	INPUT 8 (+)	30	INPUT 8 (-)
11	INPUT 0 (+)	29	INPUT 0 (-)
10	INPUT 1 (+)	28	INPUT 1 (-)
9	INPUT 2 (+)	27	INPUT 2 (-)
8	INPUT 7 (+)	26	INPUT 7 (-)
7	INPUT 6 (+)	25	INPUT 6 (-)
6	INPUT 5 (+)	24	INPUT 5 (-)
5	INPUT 4 (+)	23	INPUT 4 (-)
4	INPUT 3 (+)	22	INPUT 3 (-)
3	analog OVA	21	analog OVA
2	analog OVA	20	analog OVA
1	analog OVA		

The comments concerning the position of the OVA and the use of a female connector in plastic also apply to DI mode. Also, in DI mode, the (+) and (-) inputs for each channel are set out on adjacent pins on connector P3 to facilitate the wiring of screened pairs of cables.

NOTE :

INPUT N (+) represents the INA non-inverting input
INPUT N (-) represents the INA inverting input



NOTE :

In both cases (SE and DI), unused multiplexed inputs should be grounded (OVA).

3.4 - POSSIBLE ADJUSTMENT

* Although all potentiometers are factory set, various reasons may exist for having to recalibrate the board (ageing, thermocouple effects on input wiring, adjustments for sensor drift etc.). Only the ADC potentiometers (gain : R103, and offset : R102, R104) need be altered if the ADC range used is ±5VFSR or 0/10V FSR. The board is factory calibrated for ±10V FSR (ADC range).

* Test procedures have been designed so as to limit the use of instruments on the board itself ; all measurements are read, digitally after A/D conversion from the VME. (on terminal).

* The "warm-up" time (> 15mn) must be observed in all cases. Environmental conditions must be calm (draughts reduced to a minimum), and the temperature maintained constant.

* The measuring equipment should include a standard voltage source, accurate to within ± 0.01 % total (full scale error ± n digits)
(a less accurate power supply may be used if this is monitored using a voltmeter with ±0.01% total error. The low frequency noise of this power supply must also be of this order of magnitude).

* Wiring for this kind of operation should be made with the utmost care, and sources of noise kept as far away as possible.

Note : Certain STANDARD voltage supplies give their lowest noise performance with the common (-) terminal grounded.

3.4.1 - Procedures for the various types of calibration

A - Possible procedure for INA offset (R101-FRONT PANEL-)

For details of this adjustment, see chapter 3.4.2.

a) Adjustment at "board" level

- "Test" mode :

* Switch to "test" mode

* Adjust R101 (offset) to give the correct digital value = 800 (H).

(Mean value centered around 800 (H), if G = 1,000).

NOTE : Valid even if analog inputs are present, valid for any channel and for INA gains greater than about 20.
For gains of less than 20, the INA offset is low compared with the ADC resolution of the TSVME420-R. This gives G = 1, and adjustment is unnecessary.

- "Normal" mode

This more conventional method could be said to have the advantage of being slightly more accurate than "test" mode for high gains (> 100) if the board is subject to air currents.

* Remove the connector bringing in the analog inputs (female)
* Insert a "dummy" female connector (on P3). This has the effect of grounding all analog inputs on the connector to OVA -> INA inputs grounded.
* Program channel number "0"
* Adjust R101 (offset) to give the correct value in digital = 800 (H)
(Mean value centered around 800 (H), if G = 1,000)

NOTE : Both these modes are valid in both SE and DI mode.

In both configurations, S/H and ADC offsets are negligible, for whatever the ADC range selected.

For gains of less than 20, the INA offset is low compared with the ADC resolution.

b) Adjustment at "sensor-link" level

This may be of use in "Single-ended" mode and for high gains (>100). Possible thermocouple and "fragmented" or long link effects can be cancelled out, and compensation made for residual sensor offsets. If the differences are too great, correction will be made for each channel by SOFTWARE, as only one INA offset potentiometer is available after multiplexing. Otherwise, the procedure below should be followed.

- Leave the sensor/board links in place.

- Program the channel which is most representative of the type of correction to be carried out.

- Adjust R101 (offset) to give the correct value in digital = 800 (H) (Mean value centered around 800 (H), if G = 1 000).

NOTE : Both these modes are valid in both SE and DI mode.

In this configuration the S/H and ADC offsets are negligible, for whatever the ADC range selected.

This adjustment is of little effect for INA gains of less than 20.

B-1 Procedure for offset - ADC : (G $\leq$ 20)

- Remove the connector bringing in the analog inputs (P3)

- Select the required ADC range (using S1 and S2)

- Program channel "0".

- Apply VOS1 (unipolar mode), or VOS2-3 (bipolar mode, the different VGs depend on the range). (See values in table 12).

- Adjust R102 or R104 (in accordance with the ADC input range selected) to give the correct value in digital.

NOTE : Valid for both SE and DI modes

In this configuration, the INA offset is negligible compared with that of the S/H and ADC.

NOTE : This procedure -B1- should be performed before adjusting the ADC gain (procedure -C1-).

C-1 Procedure for -ADC gain (G ≤ 20)

- Remove the connector bringing in the analog inputs

- Select the desired ADC range (using S1 and S2)

- Program channel "0".

- Apply VG1-2 on this input. (different VGs depending on range). (See values in table 12).

- Adjust R103 to give the correct value in digital.

NOTE : Valid for both SE and DI modes

One potentiometer for both unipolar and bipolar modes

In this configuration, non-linearities on S/H and PGA gains are negligible. S/H, INA and ADC errors are cancelled out (the first two being of the same order of magnitude). Adjustment, then, concerns the 3 elements which are in common over the whole chain (INA, S/H, ADC), and will remain valid for all other input configurations.

NOTE : This procedure should be carried out after procedure - B-1.

D-1 Complete ADC calibration (G ≤ 20)

This would be the procedure to follow if the ADC range were to be modified. It involves calibration of ADC offset and gain.

Procedure :
B1 - (unipolar) + C1 ; in this order for 0/10 VFSR
B1 - (bipolar) + C1 ; in this order for +/-5V or +/-10V FSR

E-1 Overall board calibration - INA + ADC - ($G \leq 20$)

This would be the procedure to follow in the more unlikely event of maintenance being necessary.

If the highest possible degree of accuracy is to be obtained, the procedures must be followed in the precise order given. (This is in order to avoid the effects of interactions between gain and offsets, and interference of the INA on the ADC). This procedure is the only one able to give accurate calibration over the whole chain without the need for very sophisticated equipment requiring long installation times.

PROCEDURES (in this order) : TABLE 9

UNIPOLAR MODE (0/10V FSR)	BIPOLAR MODE (+/-5V FSR or +/-10V FSR)
. B-1 Unipolar	. B-1 Bipolar
. C-1	. C-1
. A - Mode a or mode b	. A - Mode a or mode b
END OF CALIBRATION	END OF CALIBRATION

B-2 Procedure for ADC offset (G > 20)

The following procedure is to be followed if reciprocal interference between INA and ADC offsets is to be avoided :
- Remove jumper S2 (ADC input)
- Select the desired ADC range (using S1)
- Apply Vos (1-2) on pin 3 of S2 if FSR = 0/10V or ±5V.
  Apply Vos3 on pin 1 of S2 if FSR = ±10V.
  (See values in table 12)
- Adjust R102 (unipolar) or R104 (bipolar) to give correct value in digital.

NOTE :

* INA "outside measuring circuit"
* Perform procedure B2 before C2
* For application of analog voltages on S2, a thin "daisy-chain" type wire such as that used on "Berg" jumpers, or a small "wire-grip" should be used.

C-2 Procedure for ADC gain (G > 20)

- Select the desired ADC range (using S1)
- Remove jumper S2
- Apply VG (1-2) on pin 3 of S2 if FSR = 0/10V or ±5V.
  Apply VG3 on pin 1 of S2 if FSR = ±10V.
  (See values in table 12)
- Adjust R103 to give the correct value in digital.

NOTE : This procedure should be carried out after B.2.

D-2 Complete calibration of ADC (G > 20)

- This involves adjustment of ADC gain and offset, and is the procedure to be used if, for example, the ADC range is modified.
. Procedure : B2 + C2 (in this order)

E-2 Overall board calibration INA + ADC - (G> 20)

- Follow the procedures in the given order for accurate calibration, valid in both unipolar and bipolar modes.

Perform : B2 + C2 + A (a or b) - End of calibration.

REMINDERS :

For INA adjustments (especially at high gains), the board should be plugged into the rack. As the potentiometer (R101) is accessible front the front panel this does not present any problems. Measuring INA output offsets directly with a high precision voltmeter would necessarily require the use of an extension board, thus producing changes in the environmental conditions (temperature, air etc.). This could lead to false measurements being given, especially on the input amplifier.

As the front panel is grounded to the chassis (GROUND) or the logic 0V (as is the digital section), the use of an insulated screwdriver ("television" type, Ø ≤ 3 mm insulated, FACOM type) is recommended when adjusting potentiometers. This should avoid any shifting in offset values at high gains. This precaution becomes a necessity when the voltage between the two grounds (OVA and OVL) exceeds 100 volts with low "internal resistance". (very unlikely).

3.4.2 - Details of adjustments

* Tables 10 and 11 give the theoretical values of ADC output codes for different input voltages.

- FS = Full scale
- OB = Offset binary
- TC = Twos complement (OB with inverted MSB -> 0 volts = 000 (h)
- SB = Straight binary

(tab. 10) Theoretical values of ADC output codes - Unipolar mode

SCALE	LSB voltage level	FSR = + 10 V	ADC code = SB	HEX value
+ FS - 1 LSB	$\frac{10\ V}{2^n}$	+ 9,9976 V	1111 1111 1111	FFF
+1/2 FS		+ 5,0000 V	1000 0000 0000	800
	n = 12			
+ 1 LSB		+ 2,44 mV	0000 0000 0001	001
	LSB = 2,44 mV			
0		0 V	0000 0000 0000	000

(tab. 11) Theoretical values of ADC output codes - Bipolar mode

SCALE	FSR = ± 5 V	FSR = ± 10 V	ADC code = OB	HEX	ADC code = TC	HEX
+ FS - 1 LSB	+ 4.9976 V	+ 9,9951 V	1111 1111 1111	FFF	0111 1111 1111	7FF
+ 3/4 FS	+ 2,5000 V	+ 5,0000 V	1100 0000 0000	C00	0100 0000 0000	400
+ 1/2 FS + 1 LSB	+ 2,44 mV	+ 4,88 mV	1000 0000 0001	801	0000 0000 0001	001
+ 1/2 FS	0 V	0 V	1000 0000 0000	800	0000 0000 0000	000
+ 1/2 FS - 1 LSB	- 2,44 mV	- 4,88 mV	0111 1111 1111	7FF	1111 1111 1111	FFF
- 1/4 FS	- 2,5000 V	- 5,0000 V	0100 0000 0000	400	1100 0000 0000	C00
- FS	- 5,0000 V	- 10,0000 V	0000 0000 0000	000	1000 0000 0000	800

1 LSB = 2,44 mV (10 ÷ 4096)

1 LSB = 4,88 mV (20 ÷ 4096)

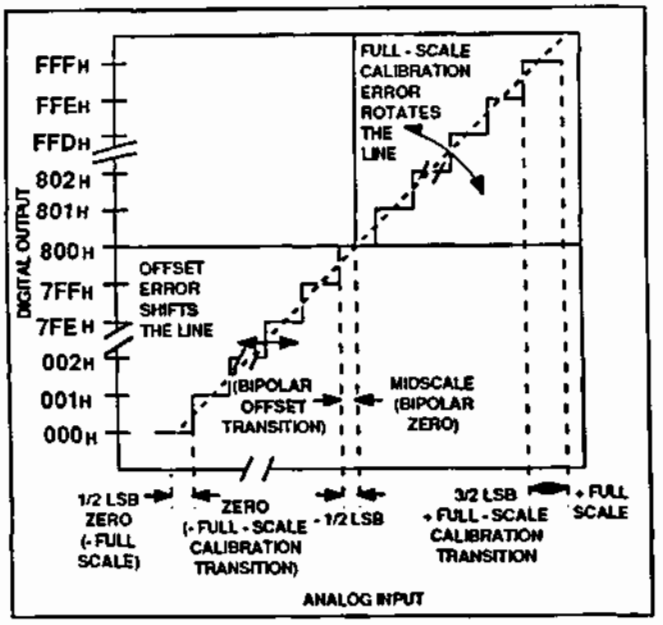
Note : If INA gain = 1 ==> 1 LSB taken to board input = 2,44 mV
If INA = 1000 ==> 1 LSB taken to board input = 2,44 µV theoretical
With FSR = 10 V (ADC)

* Tables 12 and 13 give the exact values to be applied to the ADC input (and, therefore, the INA, with G = 1) for the best possible calibration of the ADC :

If the theoretical voltages (tables 10 and 11) are valid, it should nevertheless be borne in mind that an ideal ADC is only capable of quantifying the exact analog value to within +/- 1/2 LSB. Uncertainty is reduced to a minimum by taking up a position in the "middle" of the transition in order to be as close as possible to this theoretical value (see figure 16). Otherwise, errors of +/- 1/2 LSB may be added.

FIGURE 16 - ADC transitions, SB or OB codes

* Calibration : see tables 12 and 13 and figure 17.



* In tables 12 and 13, only the values VOSn and VGn are required for calibration of the ADC.

. Unipolar mode -> FSR = +10V -> VOS1 = +1.22 mV (offset-R102)
VG1 = +9.9963 V (gain-R103)

. Bipolar mode -> FSR = +/-5V -> VOS2 = -4.9988 V (offset-R104)
VG2 = +4.9963 V (gain-R103)
FSR =+/-10V -> VOS3 = -9.9976 V (offset-R104)
VG3 = +9.9927 V (gain-R103)

TABLE 12 - CALIBRATION VOLTAGE -ADC- :

* For the voltages given, the output code should "oscillate" between the 2 digital values shown.

(tab. 12) Calibration voltages - ADC - Unipolar mode

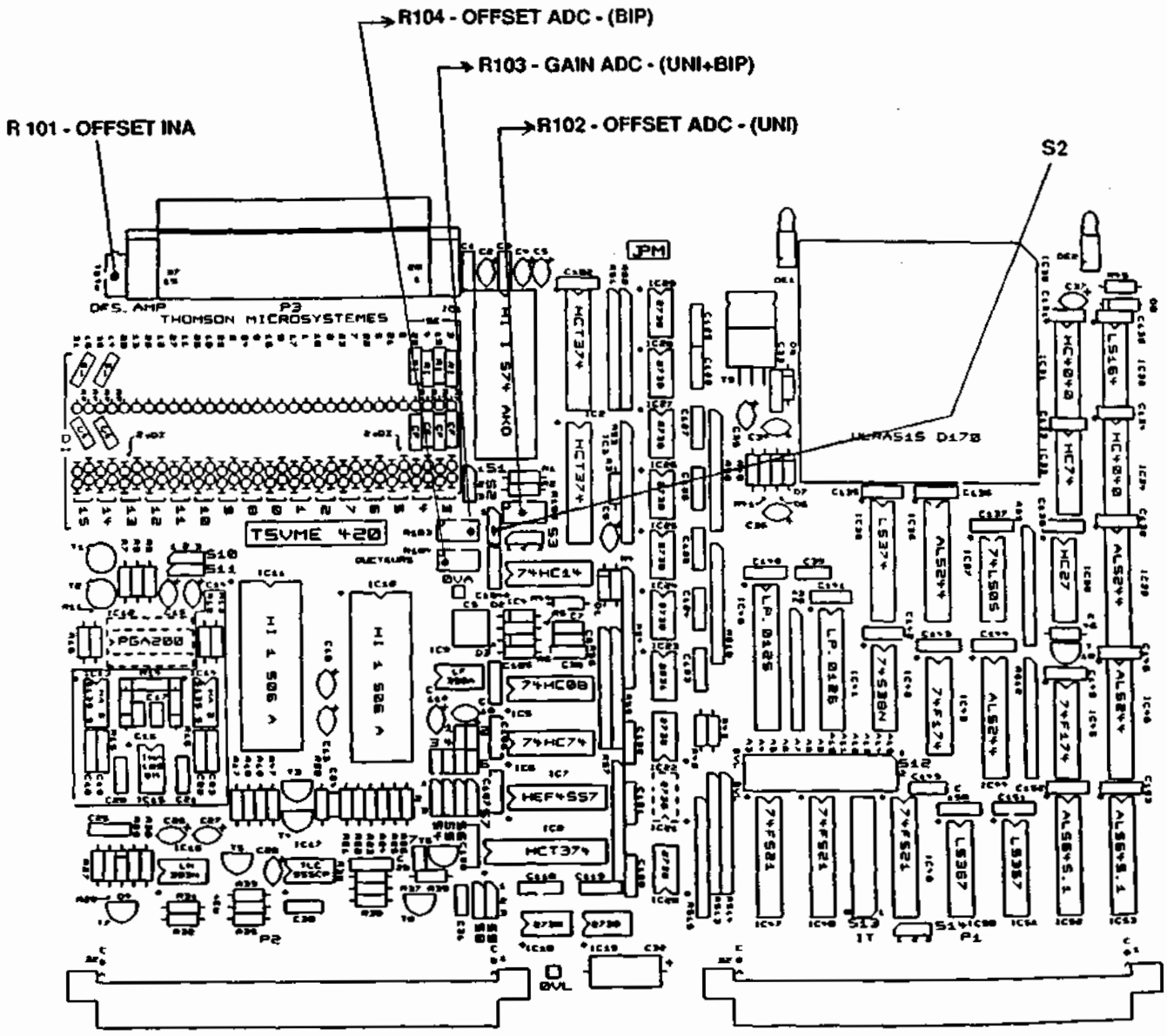
SCALE	FSR = +10 V	STRAIGHT BINARY (transitions)	HEX
FS - 3/2 LSB	+ 9,9963 V = Vg1	1111 1111 1111 1111 1111 1110	FFF FFE
1/2 FS + 1/2 LSB	+ 5,0012 V	1000 0000 0001 1000 0000 0000	801 800
1/2 FS - 1/2 LSB	+ 4,9988 V	1000 0000 0000 0111 1111 1111	800 7FF
+ 1/2 LSB	+ 1,22 mV = Vos1	0000 0000 0001 0000 0000 0000	001 000

* For the voltages given, the output code should 'oscillate' between the two digital values shown

(tab. 13) Calibration voltages - ADC - Bipolar mode

SCALE	FSR = ± 5 V	FSR = ± 10 V	OFFSET BINARY (transitions)	HEXA	TWO'S COMPLEMENT (transitions)	HEX
FS - 3/2 LSB	+ 4,9963 V = Vg2	+ 9,9927 V = Vg3	1111 1111 1111 1111 1111 1110	FFF FFE	0111 1111 1111 0111 1111 1110	7FF 7FE
+ 1/2 FS + 1/2 LSB	+ 1,22 m V	+ 2,44 mV	1000 0000 0001 1000 0000 0000	801 800	0000 0000 0001 0000 0000 0000	001 000
+ 1/2 FS - 1/2 LSB	- 1,22 m V	- 2,44 mV	1000 0000 0000 0111 1111 1111	800 7FF	0000 0000 0000 1111 1111 1111	000 FFF
- FS + 1/2 LSB	- 4,9988 = Vos2	- 9,9976 V = Vos3	0000 0000 0001 0000 0000 0000	001 000	1000 0000 0001 1000 0000 0000	801 800

FIGURE 17 -



NOTE :

The board is set for ± 10V FSR at the ADC, and R104 and R103 are therefore preset. Furthermore, as the ADC uses 2 offset potentiometers, R102 is also already preset.

± 10V -> standard delivered (R103 and R104 set)
± 5V -> adjust R103 and R104 (if so required)
0/10V -> adjust R102 only (if so required)

* INA offset (R101) preset.

3.5 - START-UP

Before plugging the board into a "VME" rack, be sure that no power is applied to it.

1) "HARDWARE" configuration (G = 1; TSVME420-R)

Selector jumpers are set to give the following :

- Differential mode
- ADC code = offset binary
- ADC range = ± 10V, (bipolar)
- Base address = to be set by the customer
- Address modifier = to be set by the customer
- IT line number = to be set by the customer

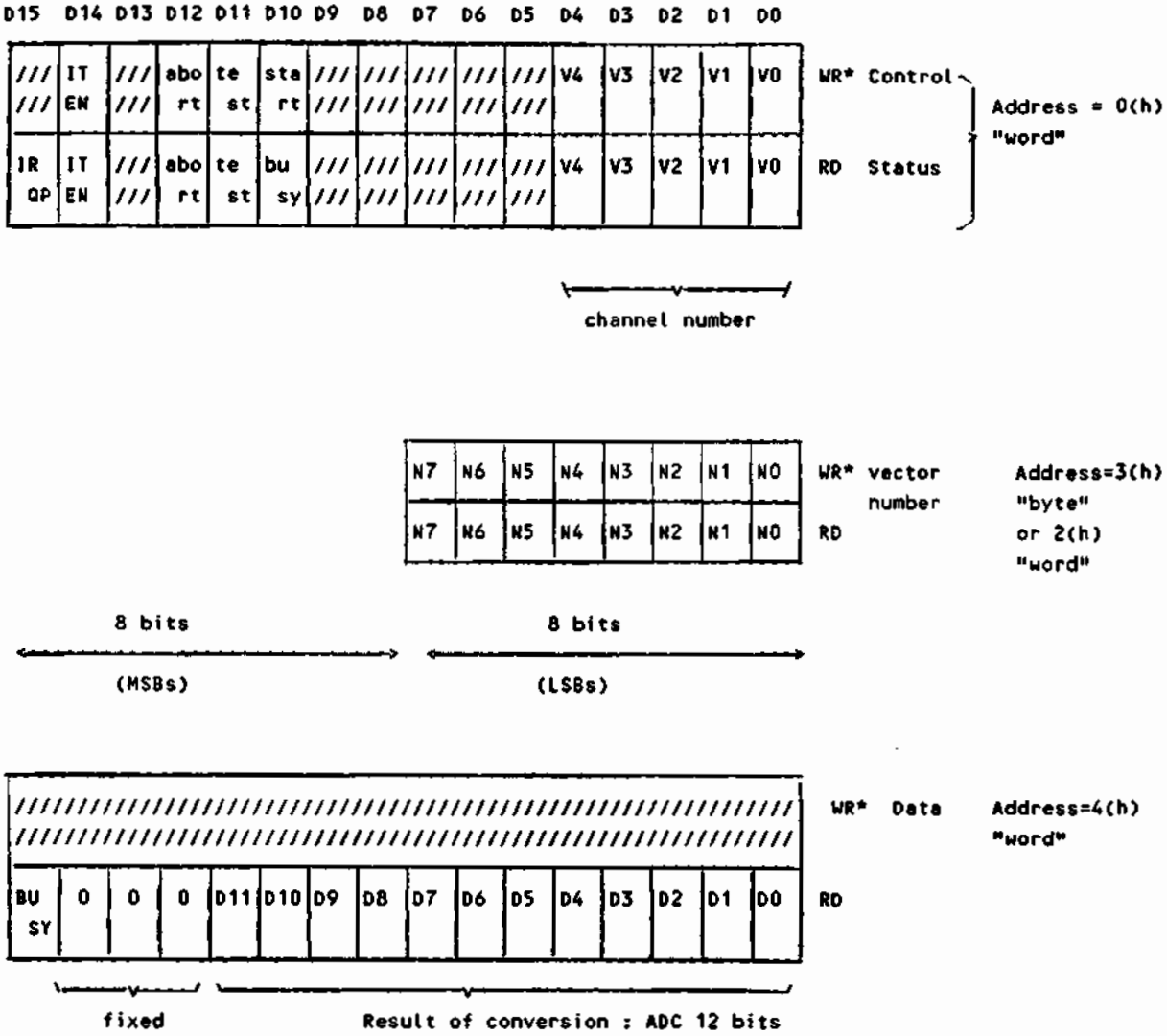
* These configurations may be modified if so required. See chapter 2.3.

2) "SOFTWARE" configuration

(See figure 18). The control register is reset on power up and the board takes on the following configuration :

- Channel number = "channel 0"
- Busy = 0 (board free)
- Test = 0 (normal operation)
- Abort = 0 ("Reset" conversion disabled)
- ITEN = 0 (Polling Mode)
- IRQP = 0 (no IT request pending)

FIGURE 18 - CONTENTS OF REGISTERS



/// : IRRELEVANT

The board should be configured in accordance with one's particular requirements, and the necessary conversions carried out (see chapters 2.5 and 3.6).

```
Motorola M68000 ASM Version  1.90 SYS :   5.TS420   .00CR    .SA 10/16/86 13:14:58
 1


  1                          *                  ****************
  2                          *                  * TSVME 420-R- *
  3                          *                  ****************
  4                          *
  5                          *
  6                          *    MAPPING:
  7                          * If board basis address is 0000(h) ; the address of the internal registers
  8                          * are :
  9                          *
 10                          *    Command/Status : $FF0000  |
 11                          *    Vector         : $FF0003  |---- Short i/o.
 12                          *    Data           : $FF0004  |
 13                          *
 14                          *
 15                          *
 16                          *          Acquisitions on channel 0 , continuous scanning .
 17                          *          ----------------- Polling mode ------------------
 18                          *
 19                          *
 20                          *
 21                          *
 22 0 00000000 33FC0400FF ENTRY    MOVE.W   #$400,$FF0000          PARAMETERS SETTING AND CONVERSION
                 0000
 23 0 00000008 0839000200FF TEST     BTST.B   #2,$FF0000             BIT BUSY TEST (STATUS, MSByte)
                 0000
 24 0 00000010 66F6                  BNE.S    TEST
 25 0 00000012 343900FF0004          MOVE.W   $FF0004,D2             READING DATA ADC BY CPU BOARD
 26 0 00000018 60E6                  BRA.S    ENTRY                  RETURN FOR NEW CONVERSION
```

```
Motorola M68000 ASM Version  1.90 SYS :   5.TS420   .DOCR    .SA 10/16/86 13:14:58
 2


 28
 29
 30
 31
 32                             *        Acquisitions on channel 31, continuous scanning , polling.
 33                             *        ------------------ Reading on terminal -------------------
 34                             *
 35                             *
 36                             *
 37 0 0000001A 33FC051F00FF ENTRY0   MOVE.W   #$051F,$FF0000        PARAMETERS SETTING AND CONVERSION
                0000
 38 0 00000022 0839000200FF TEST0    BTST     #2,$FF0000           BIT BUSY TEST (D10)
                0000
 39 0 0000002A 66F6                  BNE.S    TEST0
 40 0 0000002C 343900FF0004          MOVE.W   $FF0004,D2           READING DATA ADC BY CPU BOARD
 41 0 00000032 2A7C00F41800          MOVE.L   #$F41800,A5          |
 42 0 00000038 2C4D                  MOVE.L   A5,A6                | VBUG SUBROUTINE CALL
 43 0 0000003A 2002                  MOVE.L   D2,D0                |
 44 0 0000003C 4EB900F00040          JSR      $F00040              | FOR PRINTING ON A TERMINAL
 45 0 00000042 4E4F                  TRAP     #15                  |
 46 0 00000044 0002                  DC.W     2                    |
 47 0 00000046 6002                  BRA.S    ENTRY0
 48                             *
 49                             *
 50                             *
 51                             *        "TEST" mode, continuous scanning for offset adjust,polling.
 52                             *        ------------------ Reading on terminal -------------------
 53                             *
 54                             *
 55 0 00000048 33FC0C0000FF ENTRY1   MOVE.W   #$0C00,$FF0000        "TEST" MODE, CONVERSION BEGUN.
                0000
 56 0 00000050 0839000200FF TEST1    BTST     #2,$FF0000
                0000
 57 0 00000058 66F6                  BNE.S    TEST1
 58 0 0000005A 303900FF0004          MOVE.W   $FF0004,D0
 59 0 00000060 2C7C00F41800          MOVE.L   #$F41800,A6
 60 0 00000066 2A4E                  MOVE.L   A6,A5
 61 0 00000068 4EB900F00040          JSR      $F00040
 62 0 0000006E 4E4F                  TRAP     #15
 63 0 00000070 0002                  DC.W     2
 64 0 00000072 6004                  BRA.S    ENTRY1
 65                             *
 66                             *
 67                             *Note: In "TEST" mode, inputs are "off" automatically to procure
 68                             ****** an easy offset adjustment of the INA.
 69                             *
 70                             *
 71                             *
```

```
Motorola M68000 ASM Version  1.90 SYS :   S.TS420   .00CR    .SA 10/16/86 13:14:58
 3


 73
 74
 75
 76                          *                - TEST PROGRAM FOR INTERRUPTIONS -
 77                          *                ---------------------------------
 78                          *
 79                          *       This program makes 170 continuous conversions, with an interruption
 80                          *  at the end of each acquisition cycle ; the CPU board reads each time the
 81                          *  data from the ADC.After the last interruption (170) the program return
 82                          *  to VBUG.
 83                          *       Mode of the board is:  ITENable, channel 0 .
 84                          *
 85                          *
 86                          *                          ==Main program==
 87                          *
 88                          *
 89 0 00000074 49F900F41250 ENTRY3   LEA.L    $F41250,A4          |
 90 0 0000007A 28BC00000000         MOVE.L   #0,(A4)             | INIT OF THE VECTOR TABLE
 91 0 00000080 23FC000000A6         MOVE.L   #ENTRY4,$F40100     |
               00F40100
 92 0 0000008A 46FC2000             MOVE.W   #$2000,SR
 93 0 0000008E 13FC004000FF         MOVE.B   #$40,$FF0003        WRITING VECTOR 40
               0003
 94 0 00000096 33FC440000FF         MOVE.W   #$4400,$FF0000      PARAMETERS SETTING AND CONVERSION
               0000
 95 0 0000009E 0C1400AA     COMPAR1 CMP.B    #$AA,(A4)           CHECKING FOR 170 ITs RECEIVED
 96 0 000000A2 6722                 BEQ.S    ENTRY5              RETURN TO VBUG
 97 0 000000A4 60F8                 BRA.S    COMPAR1
 98                          *
 99                          *
100                          *                     ==Interruption subroutine==
101                          *
102                          *
103 0 000000A6 46FC2700     ENTRY4  MOVE.W   #$2700,SR
104 0 000000AA 343900FF0004         MOVE.W   $FF0004,D2          READING ADC DATA
105 0 000000B0 5214                 ADD.B    #1,(A4)             INCREASING IT NUMBER
106 0 000000B2 0C1400AA             CMP.B    #$AA,(A4)           CHECKING FOR IT 170
107 0 000000B6 6708                 BEQ.S    DEMASK1
108 0 000000B8 33FC440000FF         MOVE.W   #$4400,$FF0000      WRITING PARAMETERS, NEW CONVERSION
               0000
109 0 000000C0 46FC2000     DEMASK1 MOVE.W   #$2000,SR
110 0 000000C4 4E73                 RTE                          RETURN TO MAIN PROGRAM
111                         *
112                         *
113                         *                          ==Return to Vbug==
114                         *
115                         *
116 0 000000C6 4E4F         ENTRY5  TRAP     #15
117 0 000000C8 0000                 DC.W     0000
118                                 END

****** TOTAL ERRORS       0--
****** TOTAL WARNINGS     0--
```

IV - OPTIONS (see figure 24)

4.1 - HIGH IMPEDANCE WITH "POWER-OFF" (PRELIMINARY)

• **OPTION Z :**

In early analog multiplexing systems, it was not possible to avoid "latch up" phenomena without external protection for the multiplexer. This problem is nowadays avoided by means of internal protections, with limitations on maximum voltages for specific inputs. When the power supply is absent from the board, and the analog input voltage present (sensors etc.), such protection remains active, and the board is protected, BUT, the input impedance is low (about 1 Kohm, or even less, cf : standard 420 version).
In systems with "redundancy" (high-reliability surveillance), two boards can be used with separate power supplies, with the "parallel" inputs of the two boards amplifying the same group of sensors. If one of the power supplies fails, measurement is allowed to continue with option-Z (no "loss" of sensor voltage).

NOTE : When the board is powered (Power ON), possible overloads on the analog inputs will increase the input current, as in the standard version.
For excessive overloads (e.g. ±20V as opposed to ±10mV, G=1000), the recovery time may reach 1 mn.

Option-Z : Typical values, t = 25 degrees C., Vi = ±10V, unless otherwise indicated.

* **POWER "ON":**

```
Channel ON | Input current : ±20 nA (±100 nA, max)
           | Input capacitance = 55 pf.                          |
           | Input current (55 degrees C.) = ±300 nA (max)        |
                                                                  | Input specifications with
                                                                  | OPTION-Z
Channel OFF| Input current : ±20 nA (±30 nA, max)                 |
           | Input capacitance = 35 pf.
           | Input current (55 degrees C.) = ±230 n (max)
```

POWER "OFF":

Vi (max) = ± 20 V

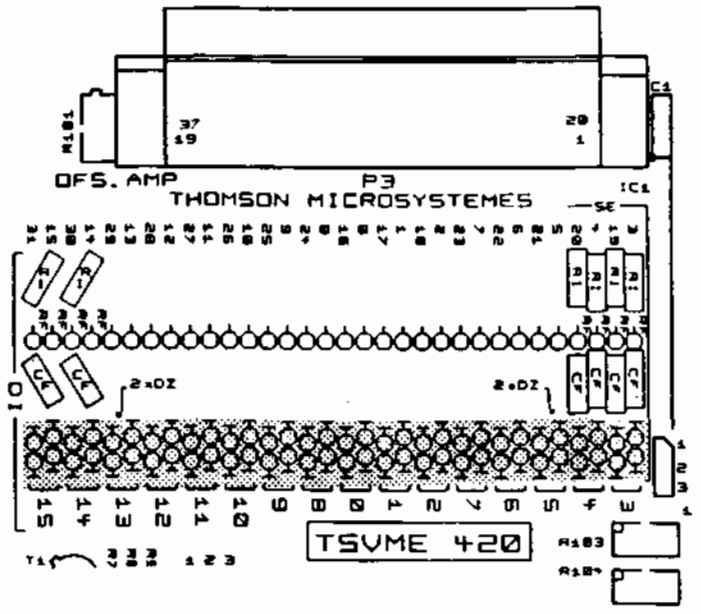
. Input current = ± 50 nA. (non overloaded input in normal operation)
. Input current = ± 40 uA. (overloaded input in normal operation : ±20V instead of ±10mV, G = 1000).

In option-Z, protections are added onto the "optional area" : 32 X [2 x D2] wired ; (see figure 19).

FIGURE 19 - OPTION Z

OPTION-Z : Shaded area

Note : Valid for "SE" and "DI" inputs.



4.2 - 0/20 mA INPUTS

CONFIGURATION - I : (Customer configuration)

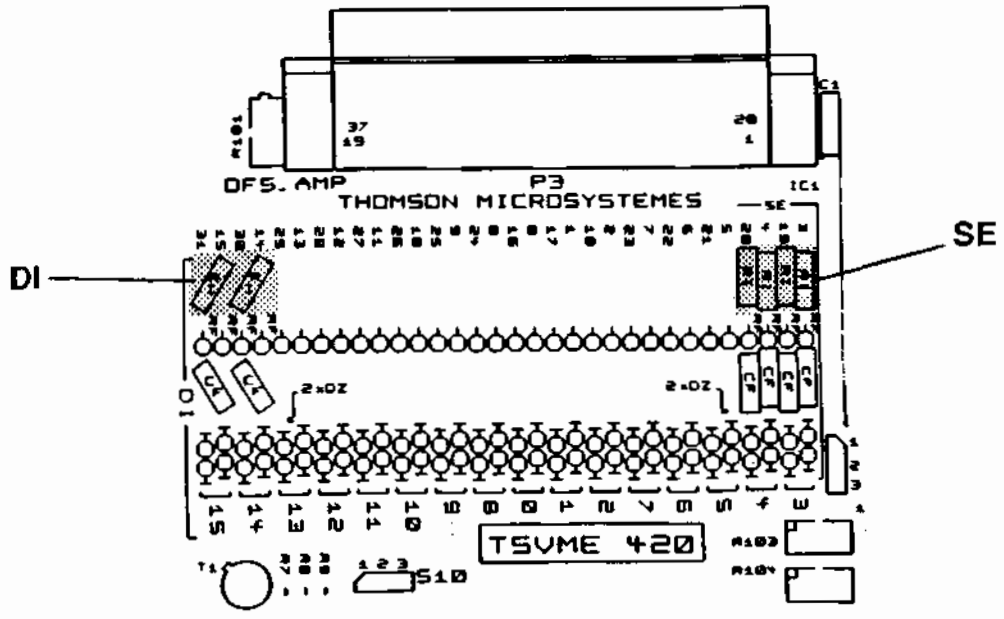
The board may take "current loop" type analog outputs, giving simple and effective protection against drops in "line" voltage and good immunity to noise. 0/20 mA sensors are directly interfaced to give 0/+10V FSR (with INA gain = 2) by wiring onto the board 250 ohm / 0.01% / 5 ppm resistors (see figure 20). 4/20 mA sensors will give 2V/10V FSR, and the offset may therefore have to be SOFTWARE compensated.

IMPORTANT : (see figure 24). In SE mode, the 32 x (Ri = 250 ohms) resistors are wired with respect to ground (OV2). In DI mode, the 16 x (Ri = 250 ohms) resistors are wired "floating".

We also have : INA Gain = 2, therefore RG = R14 = 40 Kohms -0.01%.

- 5 ppm/degrees C resistors (VSRj series from VISHAY for example)

FIGURE 20 - CONFIGURATION I :



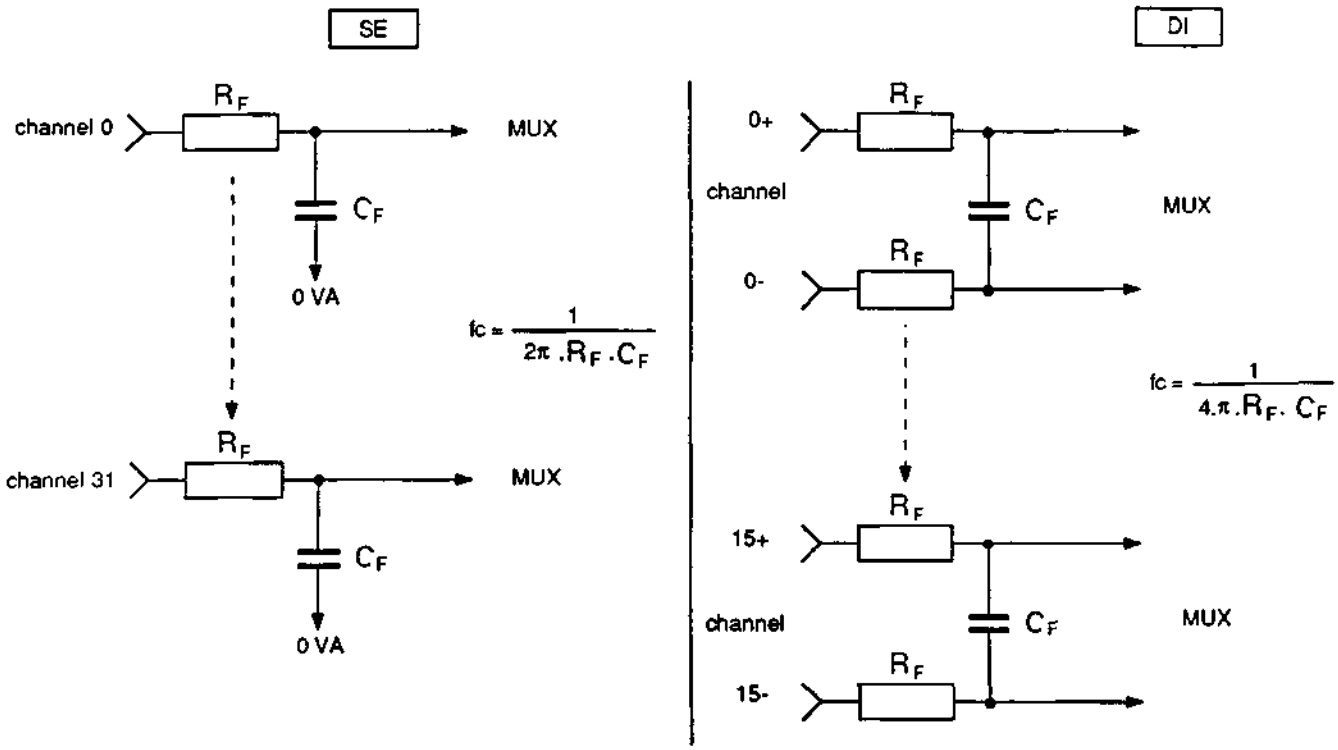
4.3 - INPUT FILTER CONFIGURATION (see figure 24)

CONFIGURATION F:

The modifications for this option are made by the customer in accordance with the desired cut-off frequency.

4.3.1 - Low pass filter

* This involves cutting off the high end of the input signal spectrum, and virtually all applications will fall into this category. Filtering is of the RC type (1st order), and is situated at the head of amplification so as to keep the scanning speed independent of the cut-off frequency fc.



* The filtering configuration is the only option which requires cutting of the copper track. Tracks are cut for each channel filtered, as components are to be added in series with the signal. (The track cut normally shorts RF in the standard form. See figures 21, 22, 23).

NOTE :

RF : RF should preferably be < 20 K ohms, -1/4 W -5% metal layer (GOGECO-RTC, SOVCOR etc.).

If RF > 20 K ohms, bias currents should be taken into account at high gains.

CF should be of the II, Z5U, ceramic "chevril" type (10%, from LCC, SOVCOR etc.) with sufficiently high leakage resistance and small dimensions (rectangular). Preferably, CF < 1 µF, (price).

a) SE mode : N = Number of (SE) channels to be filtered (N = 32 max)

- Cut N tracks across N x RF
- Wire in N x RF and N x CF

b) DI mode : M = Number of (DI) channels to be filtered (M = 16 max)

- Cut 2 x M tracks across 2 x M x RF
- Wire in 2 x M x RF
- Wire in M x CF (CF wired "floating" to avoid deterioration in alternate common mode).

FIGURE 21

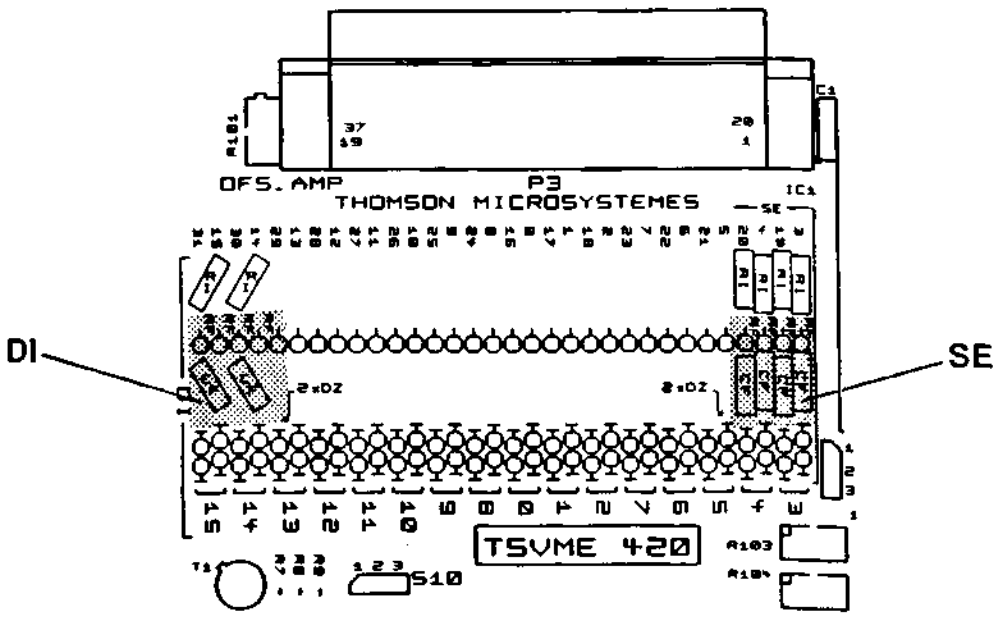


FIGURE 22 - PRINTED CIRCUIT - COMPONENT SIDE

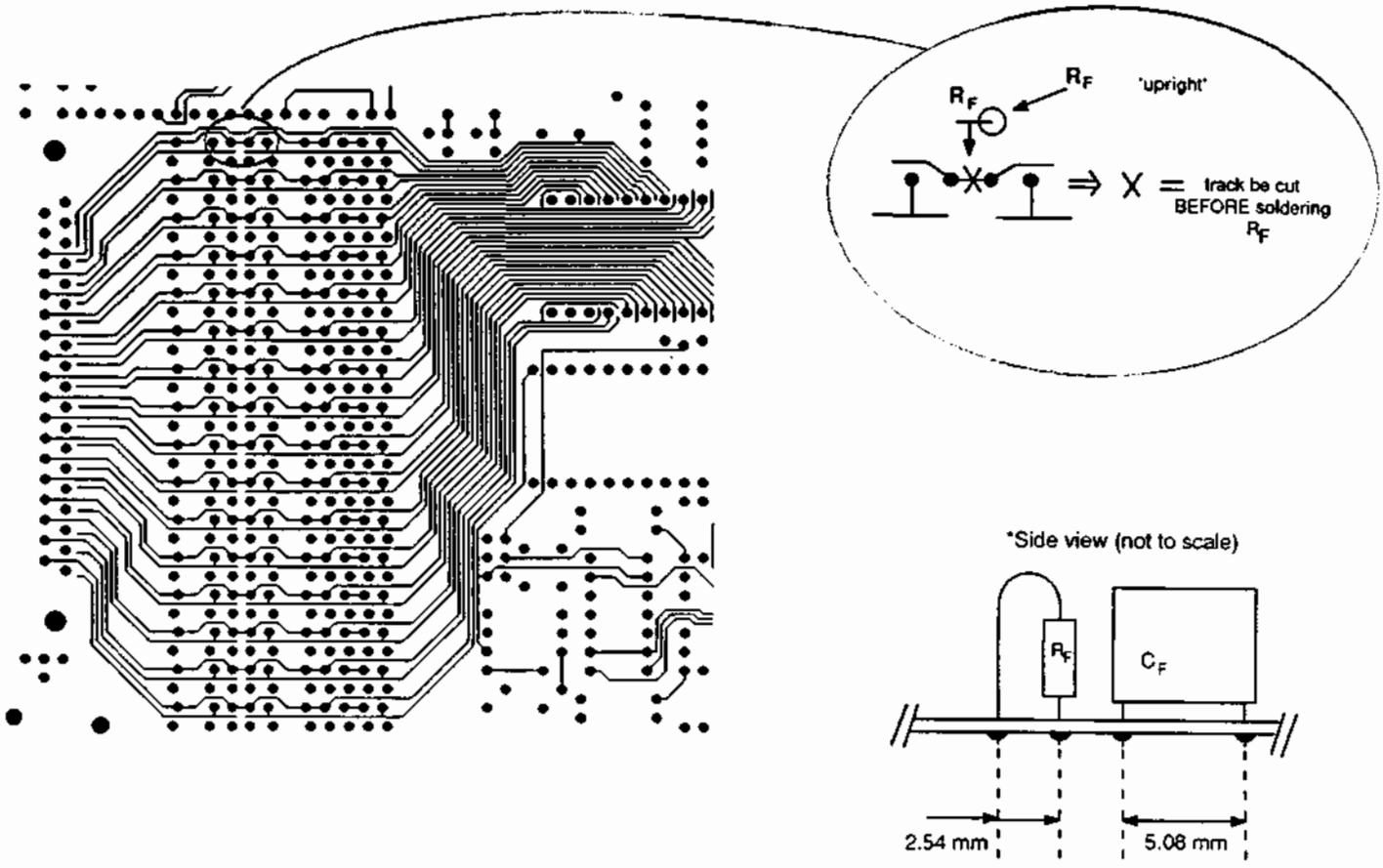


FIGURE 23 - PRINTED CIRCUIT - SOLDERED SIDE

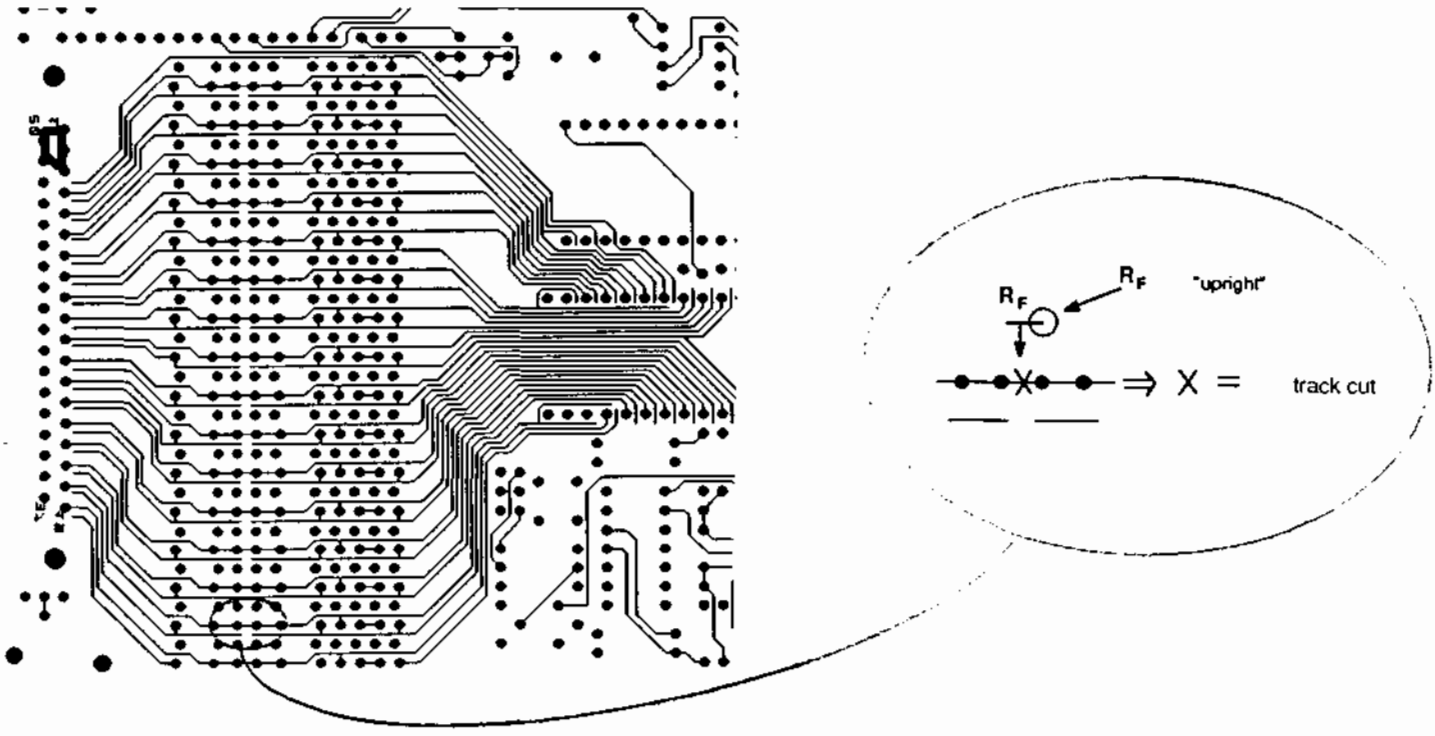
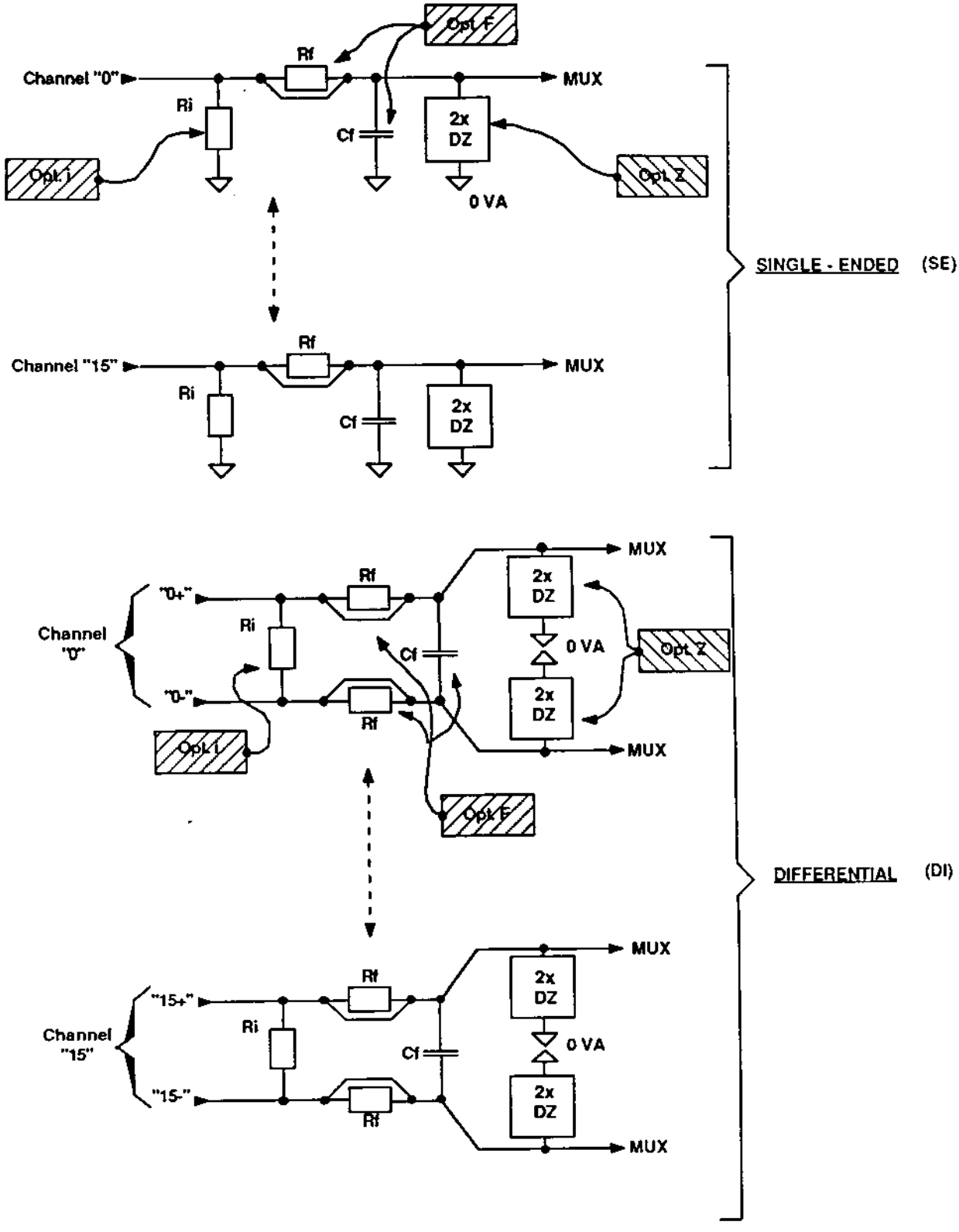


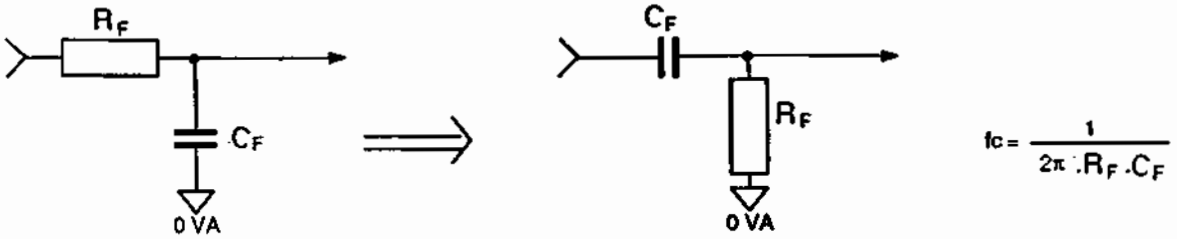
FIGURE 24 - DETAILS OF "OPTIONAL AREA"



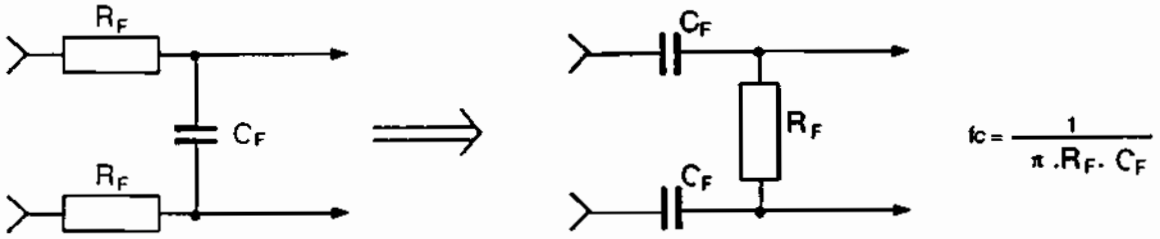
4.3.2 - High pass filter

Situations can be envisaged in which it is wished to cut out the DC component. This can be done by filtering out the low end of the spectrum using a high-pass filter.

The transformation from low-pass to high-pass is carried out as follows : (see figures 21, 24).



Low pass (SE) High pass (SE)

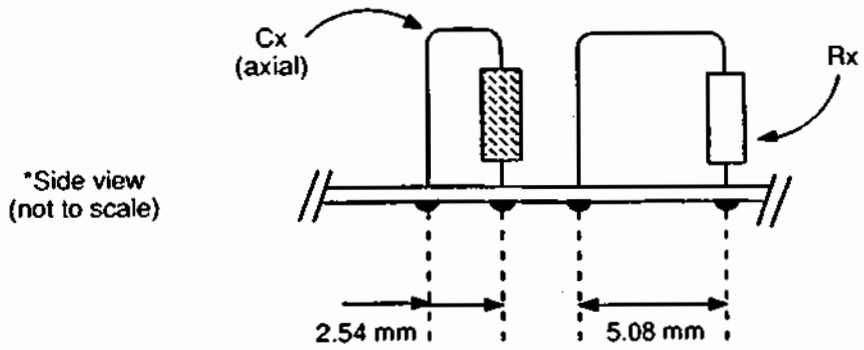


Low pass (DI) High pass (DI)

NOTES :

The same cuts are made for high-pass filtering as for the low-pass configuration, and the same remarks apply (with the physical positions of RF and CF interchanged).

It should be noted, however, that capacitor CX should have the same overall dimensions as a 1/4 Watt resistor. This type of capacitor, with axial wires, is available from RTC, SOVCOR etc.) The spacing for resistor RF is 5.08 mm.



IMPORTANT : RF may be significantly greater than 20 Kohms, as we are not concerned here with the problem of generating offsets.

In DIFFERENTIAL mode, the INA no longer receives well-defined bias currents ; the output voltage is defined by the CMRR only (DC). The following should be carried out for reliable operation :

1) "Short" R18 and R19 (amp. bias).

2) Replace R7 and R8 with resistors of the desired value (between 150 Kohms and 5 Mohms). These values will set the input impedance in common mode.

This configuration gives optimal board operation, in alternate mode. Accuracy will be lower, as R7 and R8 must include an allowance for the differences in "Ron" for ic10/ic11 and T1/T2.

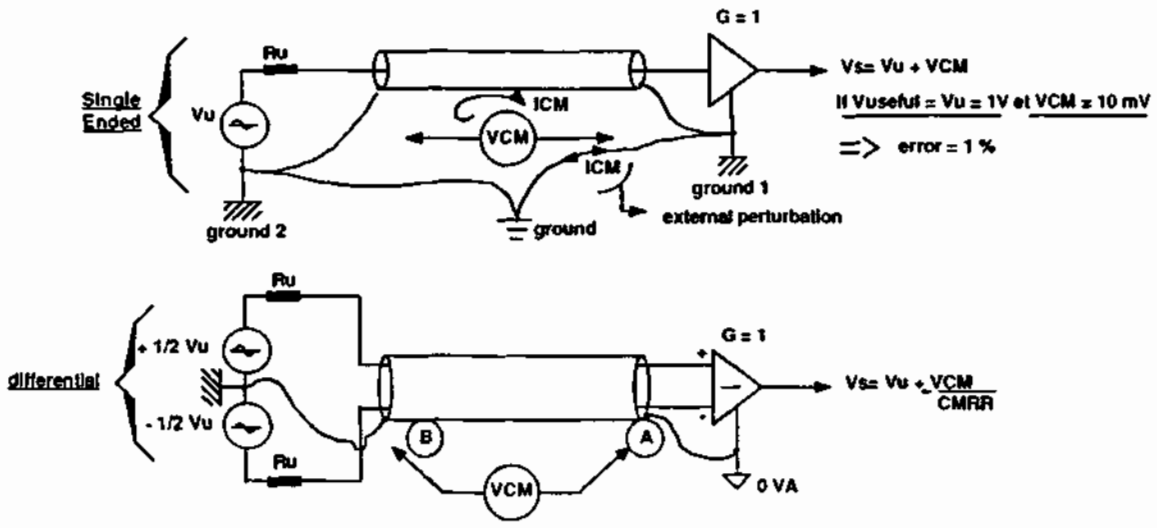
GENERAL NOTE :

Any combination of the above three "options" may be used.

V - APPLICATIONS

5.1 - GENERAL

As the board consists of 16 or 32 multiplexed inputs, the assumption will be made, for simplification of diagrams, that the multiplexer is stable on one input.
With conventional systems (without isolation), it is often difficult to resolve delicate situations involving low signal levels or disturbed external environments. Spurious voltages in common mode, or even voltages drops on grouding straps, may be non-negligible, particularly in "single-ended" mode (if the ground return between two machines has a resistance of 0.1 ohms and carries 100 mA, this gives 10 mV = VCM between two corrsponding grounds). These problems can be resolved in differential mode, though any possible ground loops will remain.



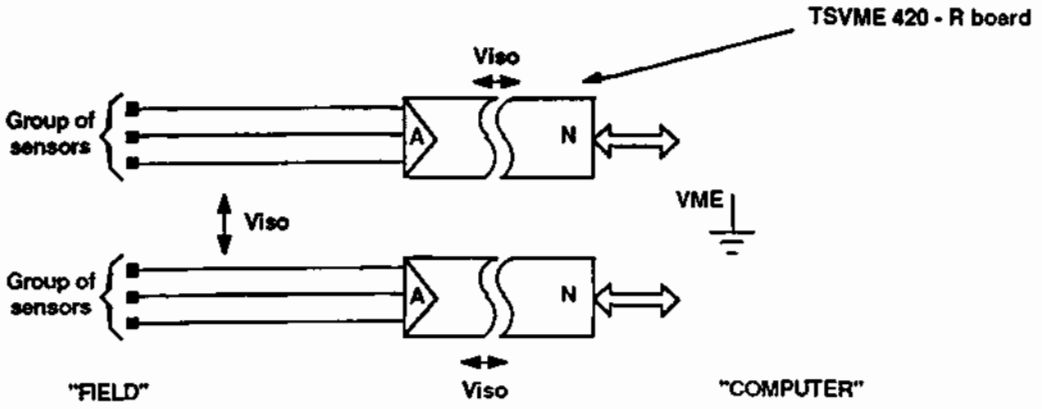
In differential mode, then, A and B must be taken to their respective grounds. Considerations that the A and B ground loop can be eliminated by grounding only A or only B are misleading, as it is virtually impossible to have an amp. with high D.C. input impedance (> 10 Mohms) working correctly in this mode.
(Return bias currents, drift, noise etc.).

5.2 - I/O ISOLATION

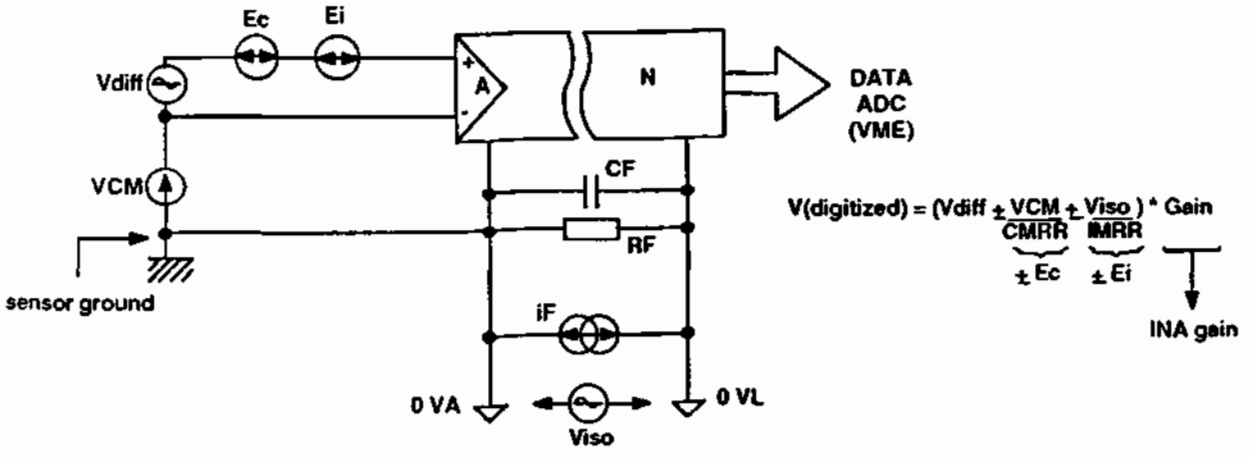
In order to remedy possible problems with certain critical applications, and to give much greater flexibility with regard to ground paths which are independent of the measuring system, the TSVME 420-R board is provided with isolation between analog inputs and digital outputs ("Field to computer" isolation). Without going into details (cable capacitance, "bootstrapp" mountings) the following is a summary of the advantages of I/O isolation :

- Possibility of ohmic isolation between the two grounds ($\geq$ 20 Mohms)
- Handling of signals superimposed on a voltage VCM>10 V.
- Possibility of very high common mode rejection ratio.

The board does not offer analog input/input isolation, but size and price considerations would make this inappropriate for a board such as the TSVME 420-R. Such a feature would perhaps be useful for certain special cases on very sophisticated equipment. If needs be, the problem can be got round by assigning one board to one group of sensors situated in the same physical environment :



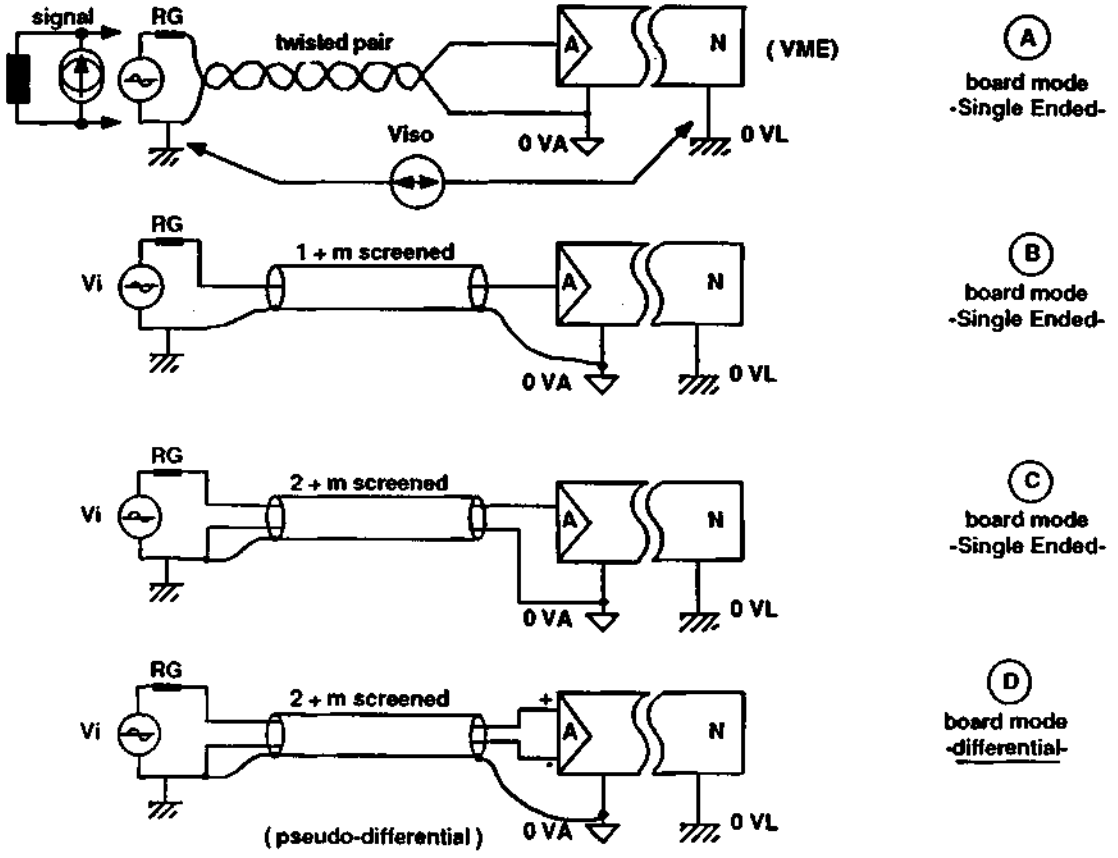
* "Equivalent diagram" of an analog input on the TSVME 420-R board. RF, CF, IF represent I/O leaks (capacitance, resistance, DC/DC common mode current).



5.3 - TYPICAL CONFIGURATIONS

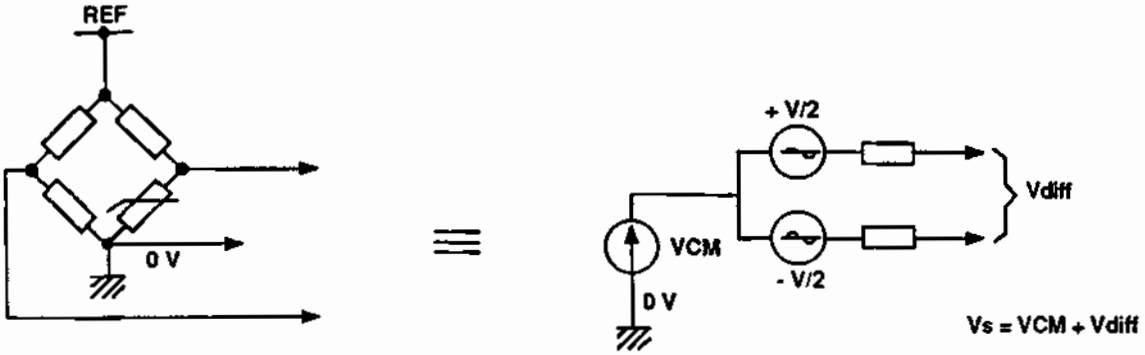
This is a non-exhaustive list of some of the most frequently used connections.

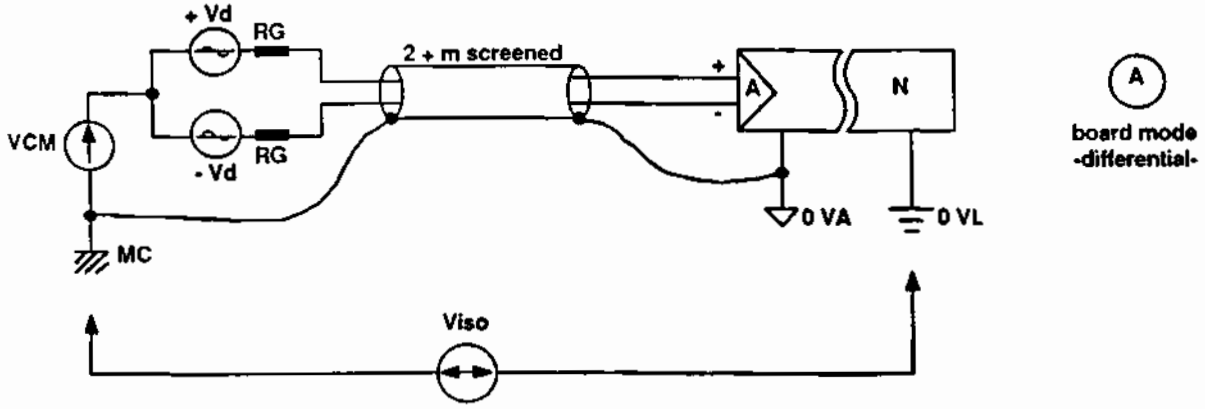
5.3.1 - Asymmetric outgoing sensors



Arrangements A and B are given in increasing order of protection against perturbation. This type of set up will suffice in the vast majority of cases (thanks to i/o insulation). Arrangements C and D are suitable for critical assymetrical applications.

5.3.2 - Symmetric outgoing sensors





In differential mode, the high I/O rejection ratio (IMRR) is also accompanied by CMRR, for surpression of VCM.

Wiring must be carried out with precaution, and unwanted cable capacitance well distributed if the CMRR is to be retained in alternate mode.

VI - APPENDICES

6.1 - DATA SHEET FOR HI-506A (MUX)

6.2 - DATA SHEET FOR LF 398 A (S/H)

6.3 - DATA SHEET FOR HI - 574 - AKD (ADC)

HARRIS

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

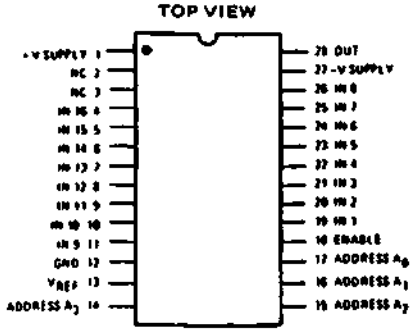
DESCRIPTION

The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

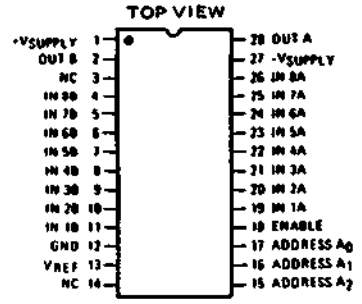
The HI-506A/507A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUT

HI-506A

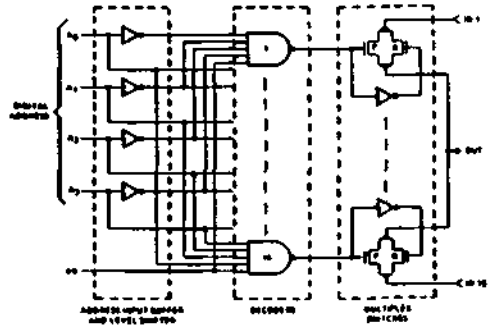


HI-507A

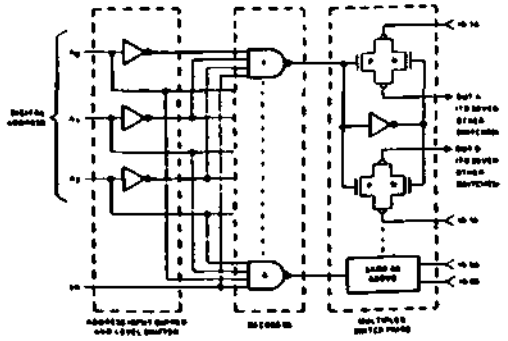


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	44V	Total Power Dissipation*	1200mW
V_{REF} to Ground V+ to Ground	22V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A (V_{Supply} (+))	+4V	HI-506A/507A-5	0°C to +75°C
V_A (V_{Supply} (−))	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S (V_{Supply} (+))	+20V		
V_S (V_{Supply} (−))	-20V	* Derate 19.7mW/°C above T_A = 110°C.	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	2.8		1.8	2.8	kΩ
*I_S (OFF), Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-506A	Full			±300			±300	nA
HI-507A	Full			±200			±200	nA
*I_D (OFF) with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				µA
*I_D (ON), On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-506A	Full			±300			±300	nA
HI-507A	Full			±200			±200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-508 Only)	Full			±50			±50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8			0.8	V
V_{AH} |	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5			0.5		µs
	Full			1.0			1.0	µs
t_{OPEN}, Break-Before Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.3			1.3		µs
(0.025%)	+25°C		4.4			4.4		µs
"Off Isolation" (Note 4)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I_+, Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	2.0	mA
*I_-, Current Pin 27 (Note 5)	Full		0.02	1.0		0.02	1.0	mA
*I_+, Standby (Note 6)	Full		0.5	2.0		0.5	2.0	mA
*I_-, Standby (Note 6)	Full		0.02	1.0		0.02	1.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100 µA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L =15pF, V_S = 7VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

* 100% tested for Dash 8 at +25°C and +125°C only.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

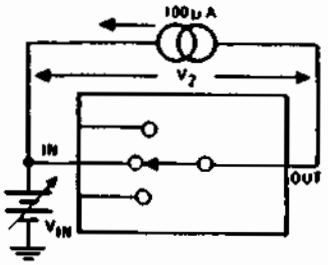
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ AND V_{REF} = OPEN.)

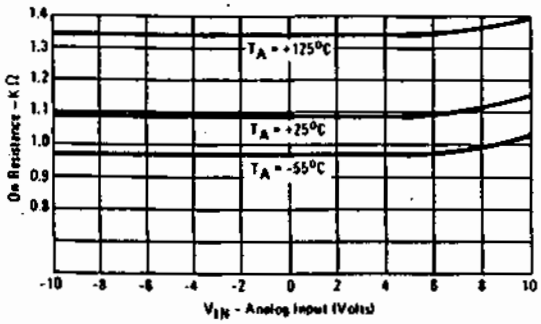
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

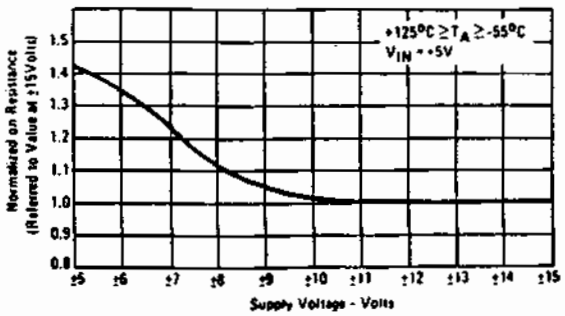
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



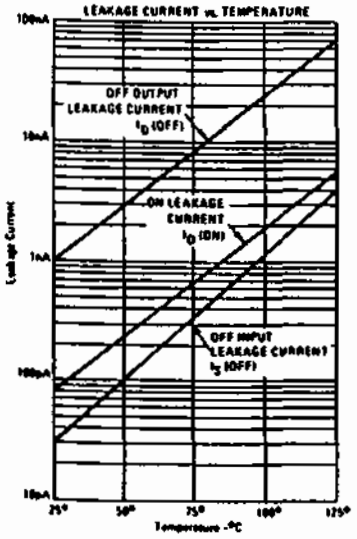
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



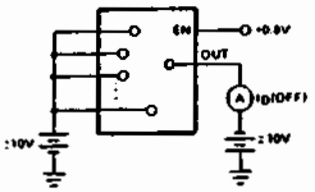
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



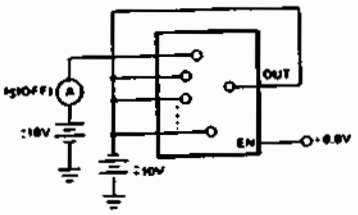
LEAKAGE CURRENT vs. TEMPERATURE



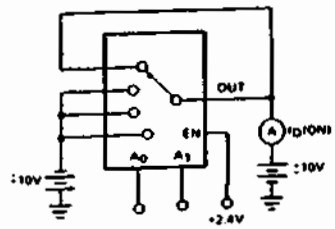
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

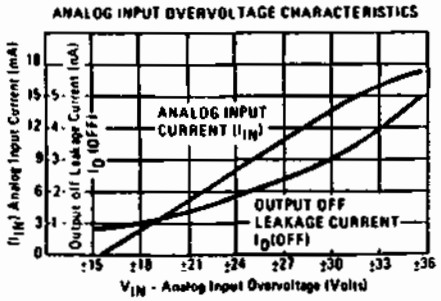


TEST CIRCUIT NO. 4*



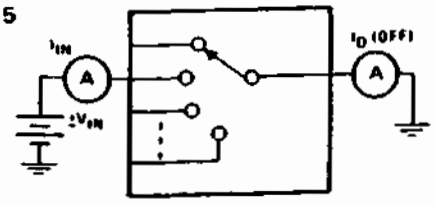
*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



National Semiconductor

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample and Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

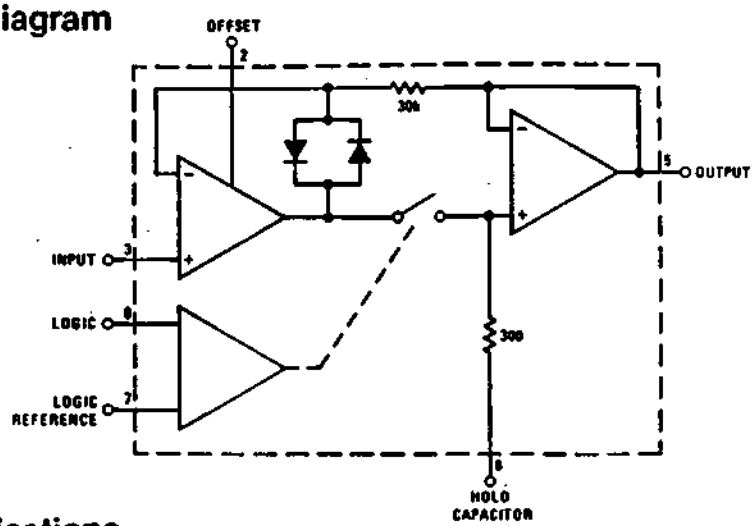
Features

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

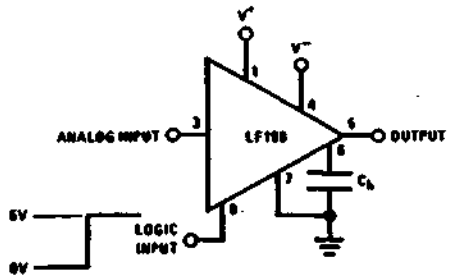
An "A" version is available with tightened electrical specifications.

Functional Diagram

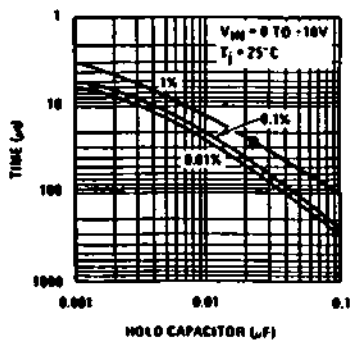


Typical Applications

Typical Connection



Acquisition Time



Electrical Characteristics (Continued) (Note 3)

PARAMETER	CONDITIONS	LF198A			LF398A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	25	nA
	Full Temperature Range			75			50	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.005	%
	Full Temperature Range			0.01			0.01	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	1		0.5	1	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4	6		4	6	μs
	$C_h = 0.01\mu F$		20	25		20	25	μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198/LF198A is 150°C, for the LF298, 115°C, and for the LF398/LF398A, 100°C. When operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10\ k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

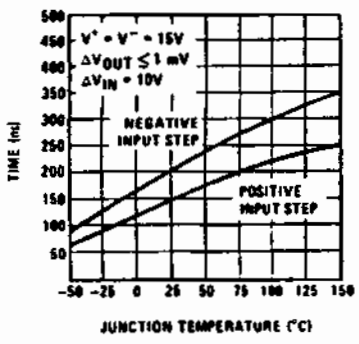
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V.

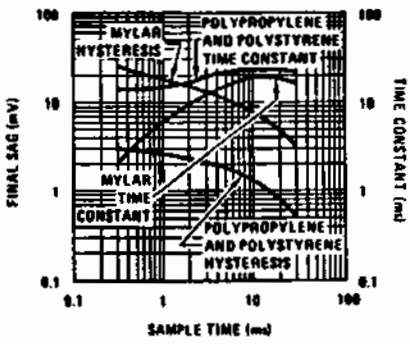
Typical Performance Characteristics

Aperture Time*

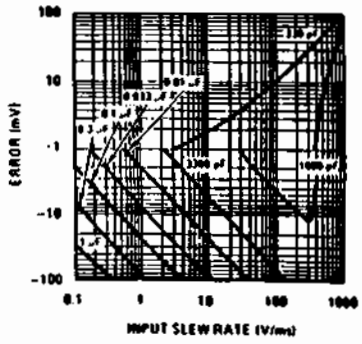


*See Definition of Terms

Capacitor Hysteresis

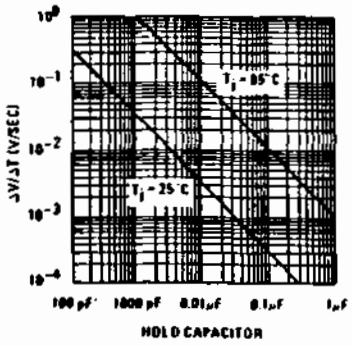


Dynamic Sampling Error

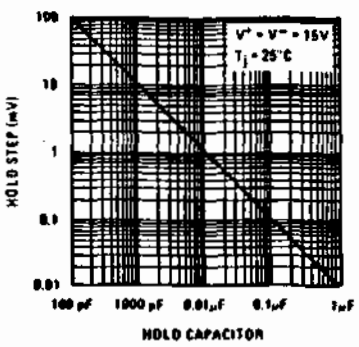


Typical Performance Characteristics (Continued)

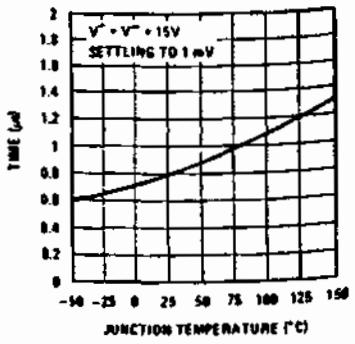
Output Droop Rate



Hold Step

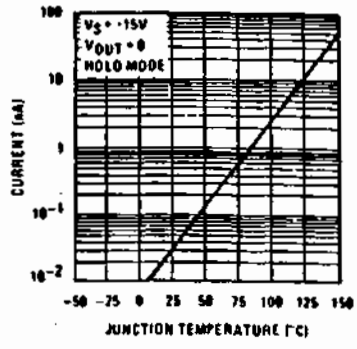


"Hold" Settling Time*

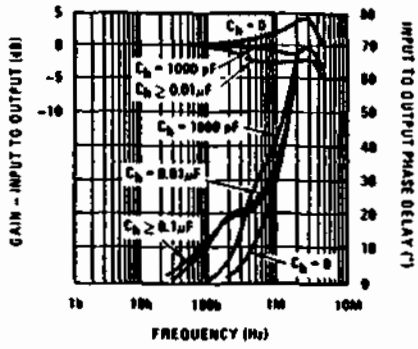


*See definition

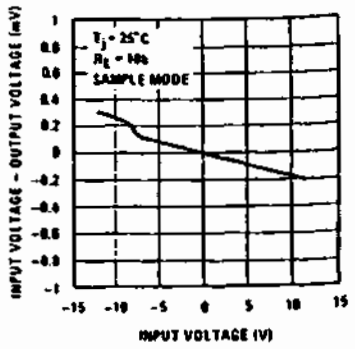
Leakage Current into Hold Capacitor



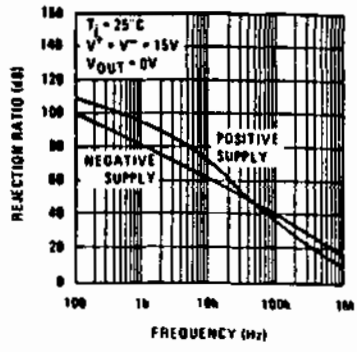
Phase and Gain (Input to Output, Small Signal)



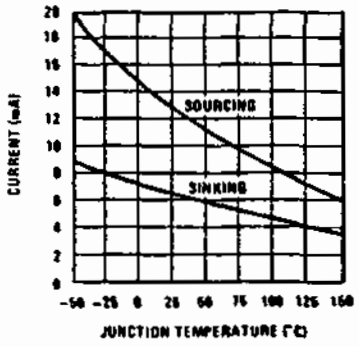
Gain Error



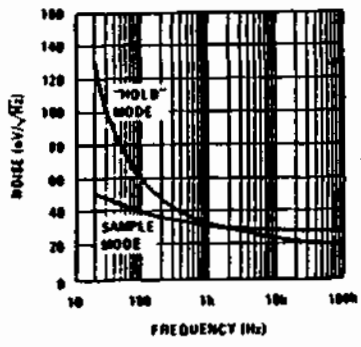
Power Supply Rejection



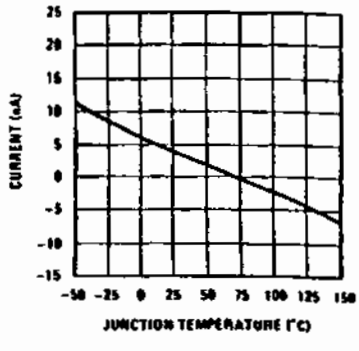
Output Short Circuit Current



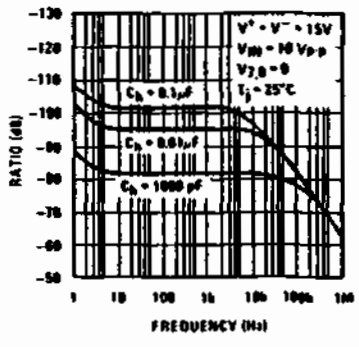
Output Noise



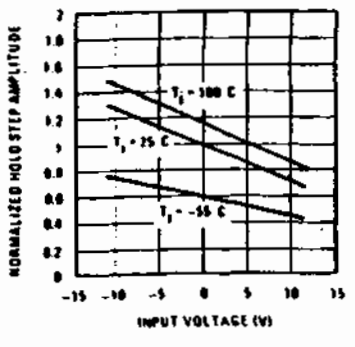
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



Hold Step vs Input Voltage



HARRIS

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

FEATURES

- COMPLETE 12 BIT A/D CONVERTER WITH REFERENCE AND CLOCK.
- FULL 8-, 12- or 16- BIT MICROPROCESSOR BUS INTERFACE.
- 150 nS BUS ACCESS TIME
- NO MISSING CODES OVER TEMPERATURE
- MINIMAL SETUP TIME FOR CONTROL SIGNALS
- 25 μS MAXIMUM CONVERSION TIME
- LOW NOISE, VIA CURRENT-MODE SIGNAL TRANSMISSION BETWEEN CHIPS
- BYTE ENABLE/SHORT CYCLE (A_0 INPUT)
  - GUARANTEES BREAK – BEFORE – MAKE ACTION, ELIMINATING BUS CONTENTION DURING READ OPERATION. LATCHED BY THE START CONVERT INPUT (TO SET THE CONVERSION LENGTH).
- IMPROVED SECOND SOURCE FOR AD574A AND HS574
- ±12V TO ±15V OPERATION

APPLICATIONS

- MILITARY AND INDUSTRIAL DATA ACQUISITION SYSTEMS
- ELECTRONIC TEST AND SCIENTIFIC INSTRUMENTATION.
- PROCESS CONTROL SYSTEMS.

DESCRIPTION

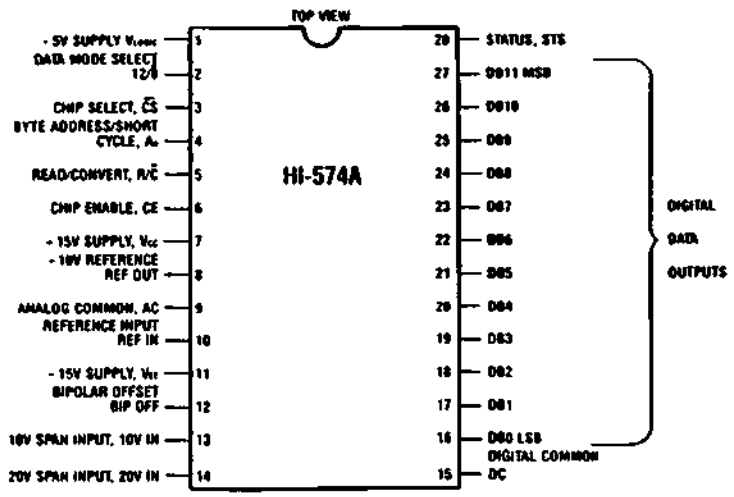
The HI-574A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 ± 1 μs.

The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ± 12V to ± 15V, with typical dissipation of 515 mW. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin side-brazed, ceramic DIP. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix.

PINOUT



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-574AJ	HI-574AK	HI-574AL	UNITS
Temperature Range	0 TO +75			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC}	11 TYP, 15 MAX			mA
I_{EE}	21 TYP, 28 MAX			mA
Power Dissipation	515 TYP, 720 MAX			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			mA

1 When supplying an external load and operating on ± 12V supplies, a buffer amplifier must be provided for the Reference Output.

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)			
Logic "1"	+2.4V[2]		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	0.1μA	+5μA
Capacitance		5pF	

[1] See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.

[2] Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.

ABSOLUTE MAXIMUM RATINGS
(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Chip Temperature (J, K, L grades) ..... 100°C
(S, T, U grades) ..... 150°C
Power Dissipation 1000mW
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C
Thermal Resistance, Θ_{JA} ..... 48°C/W

HI-574A ORDERING GUIDE

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-574AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-574AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-574ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-574ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574AUD-2	−55 to +125°C	±1 LSB	12 Bits	12.5
HI1-574AUD-8*	−55 to +125°C	±1 LSB	12 Bits	12.5

*Hi-Rel product with burn-in. For additional screening information, refer to Hi-Rel Section of current Analog catalog.

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR
Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.
Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)
A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

APPLYING THE HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Ground) and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-574A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6μS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5μS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

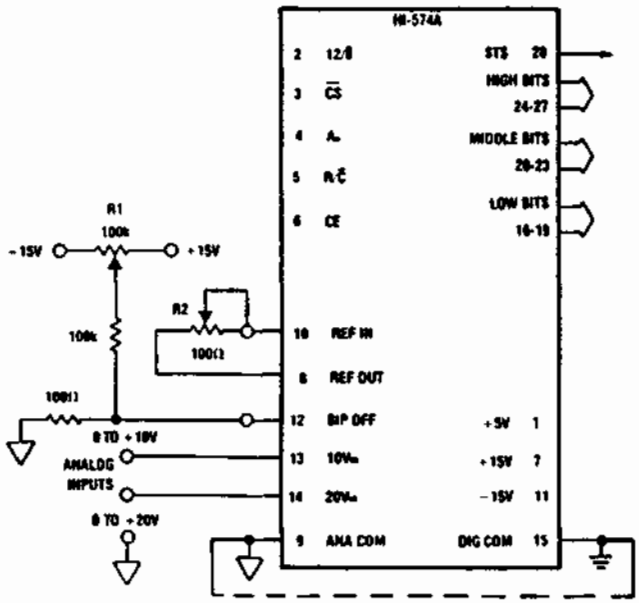


FIGURE 2. UNIPOLAR CONNECTIONS

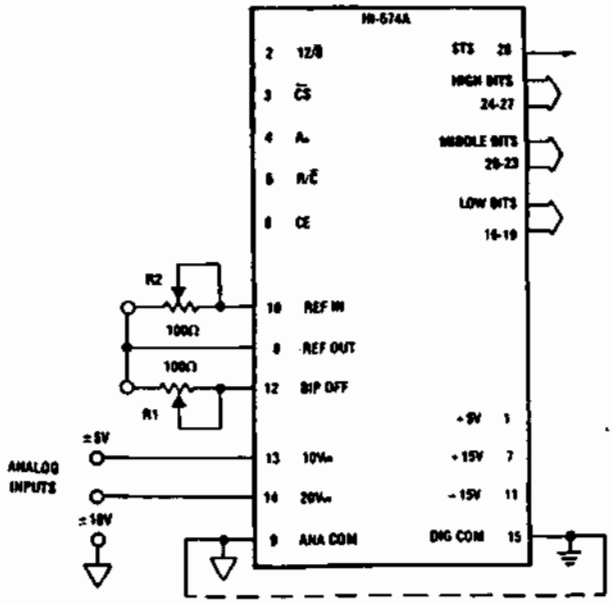


FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provices Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/C̄ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/8̄, CS̄, A_0, R/C̄ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

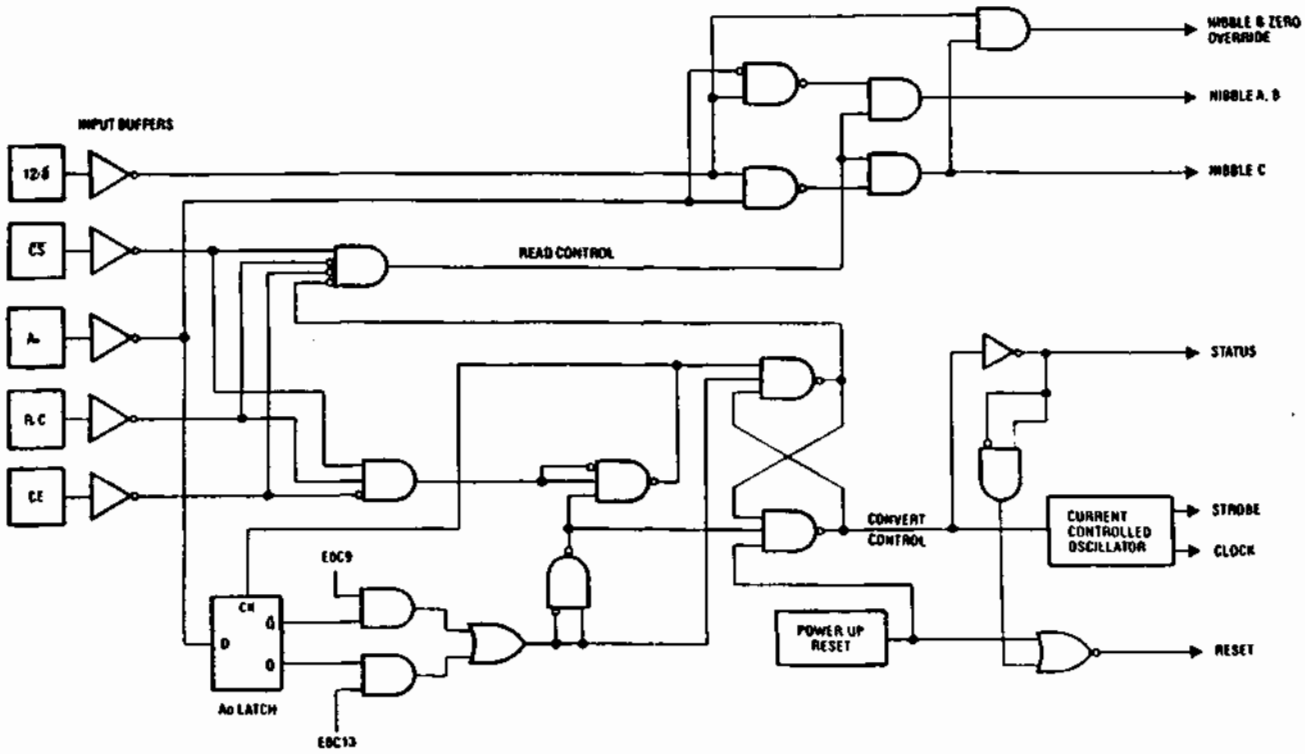


FIGURE 4. HI-574A CONTROL LOGIC

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