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ImpactRT™ 3200S System Guide



TC-3200S-SG-200

02/09/05

Mercury Computer Systems, Inc.
Chelmsford, MA 01824-2820

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- Median filter algorithm: US 6,754,684
- Square root generation: US 6,625,632

The PowerStream 7000 chassis is covered by the following U.S. Patents:

- Chassis: US 6,690,575
- Card Cage: US 6,690,575
- Processor and Switch modules: US 6,683,787, US 6,697,255, US 6,661,657
- Module Covers & Chassis Faceplates: US 6,683,787, US 6,697,255, US 6,661,657

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Preface

About This Guide

This guide provides instructions for the installation, use, and maintenance of the ImpactRT 3200S system hardware and related firmware.

The audience for this document includes the following users:

- **System Managers** — Establish and maintain development systems for application developers. System Manager tasks include installation, configuration, testing, and system startup.
- **System Designers** — Produce high-level designs for embedded hardware subsystems and embedded software applications that are part of a use-domain system.
- **Application Designers** — Produce high-level designs for embedded software applications for multicomputers.
- **Application Developers** — Develop software programs for a multicomputer application. Tasks include program design, coding, debugging, and optimization.
- **System Integrators** — Assemble and verify multicomputer systems consisting of Mercury and non-Mercury hardware and/or software.
- **Hardware Designers** — Design and implement I/O devices and boards.

A general understanding of computing and networking terminology is assumed, including:

- Operation, features, and functions of the host computer, buses, operating system, and third-party devices incorporated into the configuration
- Programming and debugging techniques for the languages used, such as C

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Related Documents

Related documentation from Mercury Computer Systems includes the following titles:

- *MCOE API Reference Manual*
- *MCOE Developer's Guide*
- *MCOE Development Tools and Files Guide*
- *Mercury System Manager's Guide*
- *Mercury Device Drivers Guide*
- *RACEway I/O Products Guide*

Finding Information

Mercury provides a variety of information, examples, and tutorials. The following table describes where to find this information.

For:	Go to:
A list of files by package	`${MC_ROOT_DIR}/install/package_contents`
Coding examples	For development packages only: `${MC_ROOT_DIR}/examples`
Configuration file examples for runtime packages	`${MC_ROOT_DIR}/examples/config`
Simple coding tutorials of Mercury functions	For development packages only: `${MC_ROOT_DIR}/man/tutorials`
Status and error logs by package	`${MC_ROOT_DIR}/spool`
SAL timings	`http://customers.mc.com`
Information about using the `manmc` tool	The *MCOE Development Tools and Files Guide*
Compiler Options for PowerPC®	For development packages only: `${MC_ROOT_DIR}/greenhills/${MC_HOST_DIR}/manuals`

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Conventions

This guide uses the typographic, syntactic, and command line conventions shown in the following tables.

Typographic Conventions

Convention	Description
Note	Notes provide important additional information.
Caution	Cautions provide information to prevent damage to equipment or software.
Warning	Warnings provide information to prevent injury to users.
`/s/node/setup.exe`	File and path names.
`argument-value`	User-specified value.
`MC_ENV`	Environment variables.
`mc_lock_attach()`	Function names.
important term	Indicates a new term or glossary entry.
Mercury Installation Guide	Document titles.
Return, Ctrl–z	Keystrokes.
The Open File dialog.	GUI elements.
Start > Settings	GUI interface menu choices.

Syntactic Conventions

Convention	Description
{ }	Groups syntax elements where needed to avoid ambiguity.
[ ]	Encloses optional syntax elements, implicitly grouping them as well; [{ }] and {[ ]} would never appear.
{*choice* | *choice*} [*choice* | *choice*]	Indicates a choice of alternatives. The first form indicates that one must be chosen, the second that none need be chosen.

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Convention	Description
... [, ...] [; ...]	Indicates that the preceding syntax element can be repeated any number of times, with a separator between elements if so indicated.
0x200	Represents a hexadecimal value.
0b1001	Represents a binary value.
Ellipsis (...)	Indicates omitted text in a list or example.

Command Line Conventions

Convention	Description
`%`	UNIX® user prompt
#	UNIX root prompt
`C:\>`	Microsoft® command prompt
`C:\> remcall -x wr_32`	Interactive input on a command line.

Contacting Mercury

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By fax	(978) 256-3558
By email	support@mc.com
By post	Mercury Computer Systems, Inc. 199 Riverneck Road Chelmsford, MA 01824-2820
Customer web site	`http://customers.mc.com`

Be sure to include your own name as well as your company name when sending a fax or email.

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1

Overview

Introduction

The ImpactRT™ 3200S system is a configurable, turnkey 6U CompactPCI® system, designed for high-bandwidth, high-computation imaging applications. The chassis is built to operate in a controlled commercial environment and is designed for mounting in a standard 19-inch equipment rack. The chassis encases a slotted card cage containing vertical CompactPCI midplanes. It also houses up to nine DC power supply units, up to two fan modules, an embedded hard drive, a CD-RW drive, and a front panel with a liquid crystal display.

The midplane accommodates Mercury processing boards and is designed to allow front and rear access. Mercury-integrated features include a RapidIO® interconnect between processing boards, a CompactPCI module bridging the chassis PCI® bus and the RapidIO fabric, fiber-optic I/O rear transition modules, and a CompactPCI host single-board computer.

System Feature Summary

The system includes the following key hardware and software features:

- CompactPCI midplanes (6-slot system midplane plus up to three expansion midplanes)
  - Processing boards, each with four PowerPC® G4 compute nodes interconnected by RapidIO technology
  - I/O modules
  - Up to four DLK5R dual-port, 5-slot CompactPCI interlink modules and passive cabling to connect them

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- Power supplies
  - Up to nine power supplies per system
  - Capability for supporting N+1 redundancy based on software
  - Self-cooling fan for each power supply unit
- Advanced system monitoring and alarm features, including:
  - Voltage and fan monitoring and alarm system supplied by a monitor board
  - Inlet/outlet air temperature
  - Power supply voltage value
  - Fan health status
  - Power supply health status
- Chassis cooling system
  - Airflow for card cage cooling is from bottom/front to top and bottom/rear sides.
  - Up to two removable blower modules. The primary blower operates in a two-speed configuration (50%, 100%).
  - Fan speed controlled by fan control card and an array of ten temperature sensors located in the exhaust and air vents across the three sides. Fan speed is based on the highest temperature of the ten sensors.
- Software and data storage
  - Embedded hard drive (36 gigabyte, SCSI Ultrawide).
  - One CD-RW drive, rear-mounted as standard. Front mounting is an option for small board-count configurations only because it restricts air flow for slots 1 through 9.
  - Host-appropriate operating system.
  - Basic development software package, basic runtime software package, and associated Mercury software.
  - Mercury drivers for installed peripherals.

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- Chassis enclosure
  - Aluminum chassis
  - Dimensions: 17.2 in. W x 30 in. D x 26.22 in. H (43.7 cm x 76.2 cm x 66.6 cm)
  - 19-inch, front-flush, equipment rack mounting

Table 1-1 shows the combinations of Mercury devices provided in the ImpactRT 3200S.

Table 1-1. ImpactRT 3200S Devices

Devices	ImpactRT 3200S
Processor modules	MC4PK MCP-P4K512R
I/O modules	TIO-2FGR TIO-4FGD TIO-2FGD
PCI-to-RapidIO bridge modules	MCP6-DPRB-3R MCPIO-DPRC

System Configurations

Table 1-2 describes the available configurations for the ImpactRT 3200S.

Table 1-2. ImpactRT 3200S Configurations

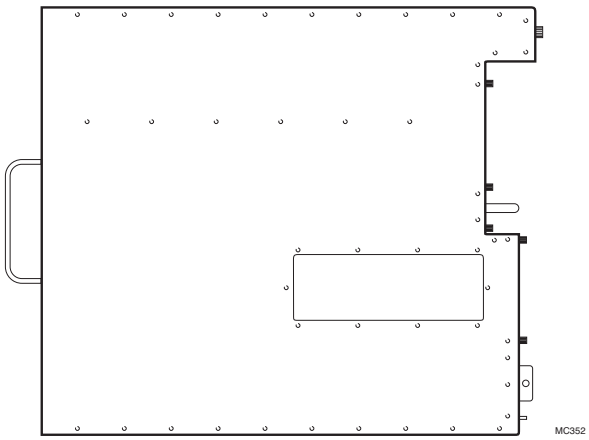
Configuration	Backplanes	Power Supplies	Midplane	Processor Boards	Host
High End	6-slot system 3 5-slot expansion	9	4xCPDLK11 Quadflex 20	up to 19	Solaris™ or Windows 2000™
Mid	6-slot system 3 5-slot expansion	6	4xCPDLK11 Quadflex 20	up to 14	Solaris or Windows 2000
Low End	6-slot system 1 5-slot expansion	3	2xCPDLK5R Dualflex 10	up to 9	Solaris or Windows 2000
Light	6-slot system		1xCPDLK5R	up to 5	Solaris or Windows 2000

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Chassis Profile

The chassis profile, shown in Figure 1-1, allows access to the card cage from the rear and is designed to reduce chassis weight. The side rails support the weight of the chassis when it is mounted in a rack or cabinet. See Table 2-8 on page 20 for configured weights.

Figure 1-1. Chassis Side View



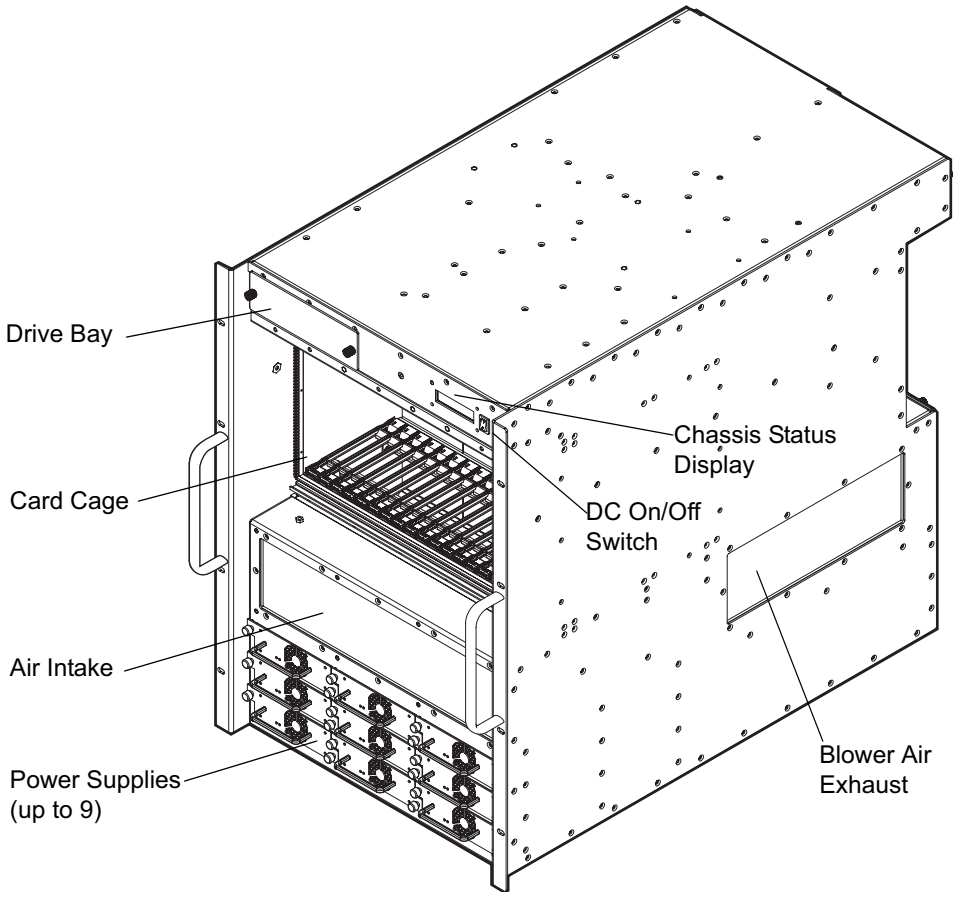
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Front Components

Chassis components accessible from the front are shown in Figure 1-2:

- Card cage (can accommodate up to 21 circuit boards)
- Drive bay (not usable in 16- or 20-slot configurations because of cooling requirements)
- Chassis status display (for messages, refer to "Chassis Status Display" on page 161)
- Card cage air intake
- Up to nine 600W power supplies (configuration-dependent)

Figure 1-2. Chassis Front



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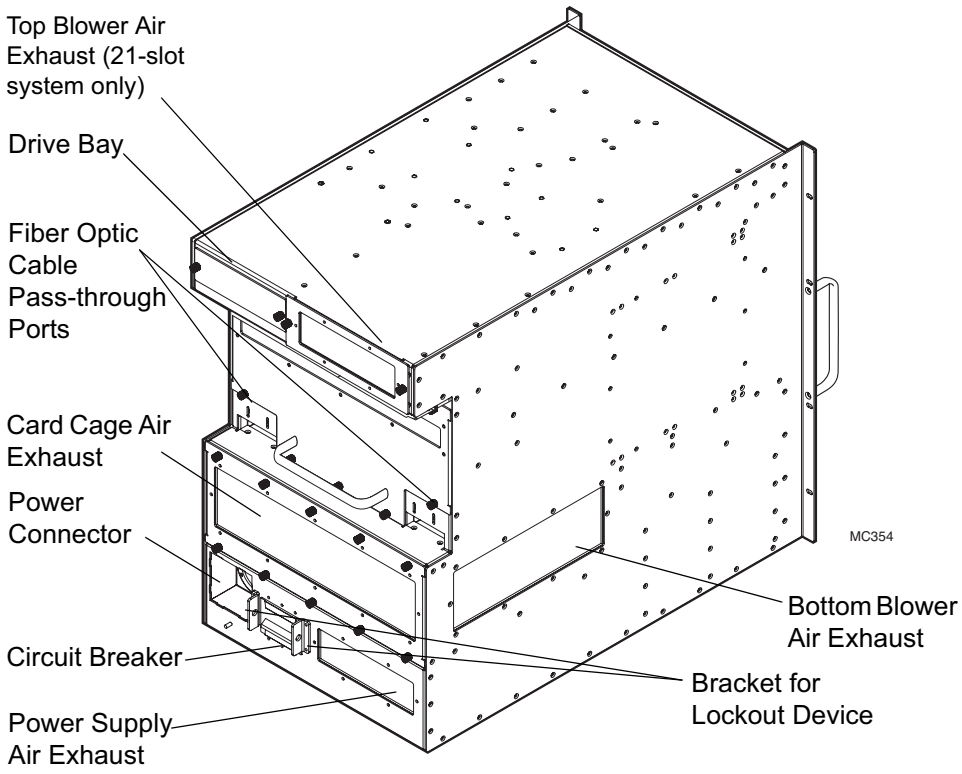
Rear Components

The following features are accessible (see Figure 1-3) from the rear of the chassis:

- Circuit breaker (with bracket for lockout device)
- Power connector
- Reset connector
- Drive bay
- Fiber optic cable pass-through ports

Card cage air exhausts through the honeycomb at the top and bottom of the chassis rear and on the side, near the chassis rear (top exhaust for 21-slot (largest) system with second blower).

Figure 1-3. Chassis Rear



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2

Safety, Regulatory, and Operating Requirements

Introduction

This chapter explains potential hazards and describes important safety precautions that you should observe when operating the system. (Additional warnings and safety information for specific equipment and operating situations are included throughout this guide.) Also described in this chapter are regulatory compliance standards met by the ImpactRT 3200S system chassis and operating requirements related to space, environment, and power.

Note: Follow all warnings and instructions marked on the equipment.

Identifying Hazards

Definitions of the words used in this manual to signal potential hazards are provided in Table 2-1.

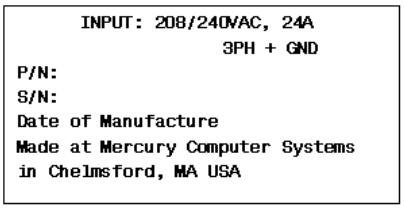
Table 2-1. Hazard Keyword Definitions

Signal Word	Meaning
Warning	Warnings provide information to prevent injury to users.
Caution	Cautions provide information to prevent damage to equipment or software.
Note	Notes provide important additional information for a topic or procedure; they are not safety related.

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Hazard labels affixed to the system are explained in Table 2-2.

Table 2-2. Hazard Labels on System

Symbol	Meaning
	General warning. Refer to accompanying documents.
	The weight of the chassis exceeds the maximum limit for a two-person lift. To move the unit, use a lifting device. Label appears on the top of the chassis and on the rear door.
	Rotating parts and shaft can cause injury. Do not operate with guard removed. Isolate power to the system (lock out/tagout) and allow machine to stop before opening. Label appears on the rear of the chassis and on the rear door.
	Hazardous voltage. Isolate power to the system (lock out/tagout) before servicing. Label appears on the rear of the chassis at upper right of the power supplies and to the right of the AC inlet cover.
	Main system label with voltage specification. Label appears on the chassis rear, center bottom.

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Hazard Summary

The hazards summarized in this section can be encountered during service or maintenance tasks.

Electrical Hazards

Table 2-3 lists the five types of electrical hazards that can exist in any kind of electrical equipment, ranging from the safest (Type 1) to the most dangerous (Type 5). Hazards of Type 1 through 4 can be encountered with the ImpactRT 3200S system.

Table 2-3. Types of Electrical Hazards

Type	Description
1	Equipment is fully de-energized.
2	Equipment is energized but live circuits are covered or insulated to preclude accidental shock.
3	Equipment is energized and live circuits of less than 30 Vrms, 240 VA and 20 joules are exposed to accidental contact.
4	Equipment is energized and live circuits of greater than 30 Vrms, 240 VA or 20 joules are exposed to accidental contact; or radio frequency (rf) is present.
5	Equipment is energized and adjustment requires physical entry into the equipment or equipment configuration does not allow the use of clamp-on probes.

Hazardous Material

A lithium battery is used in the ImpactRT 3200S as a long-term power source to allow memory components to retain necessary information.

Warning: Lithium batteries are potential hazards if misused or tampered with before, during, or after discharge. Do not try to charge the lithium battery. Doing so can result in explosion or fire that can spread toxic material, creating potential for injury or equipment damage. Do not pierce, crush, burn, short-circuit, dismantle, or modify the battery. If the battery ruptures, avoid touching the leaking electrolyte. If skin is exposed to electrolyte, flush with water immediately. In case of eye exposure, consult a physician immediately, and flush eye with water for 15 minutes.

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Power-up Procedure

Before powering up the ImpactRT 3200S system chassis, please note cautions and warning listed in the activation procedure.

Note: Connections to peripheral devices must be made with low-voltage, shielded computer data cables to maintain regulatory compliance.

- **To activate the ImpactRT 3200S system chassis:**

  1. Connect a power cable to the AC power connector at the bottom right rear of the chassis. (See Figure 1-3 on page 6.)
  2. Turn on the circuit breaker in the rear of the chassis. (See Figure 1-3.)
  3. Turn the DC On/Off switch in the front of the chassis to the on position. (See Figure 1-2 on page 5.)

Caution: To avoid potential hazards or damage to the system related to any stored electrical energy, wait five seconds after turning off the chassis before turning it on again.

Warning: Boards installed in the card cage must be securely seated and the ejector handles on the front panel firmly locked and secured with screws. Removing a board without properly shutting down the system can severely damage the board and can expose high-current components, creating a risk of electric shock.

Energy Isolation (Lockout/Tagout) Procedure

Before you remove power supplies or perform any maintenance that requires exposure to internal components, you must isolate the system from external power. Establish and follow an energy isolation (lockout/tagout) procedure to ensure that voltage is not restored without warning to those working on the system.

Note: Each facility installing an ImpactRT 3200S system is responsible for developing its own lockout/tagout procedure. Consult with qualified safety professionals to develop procedures suited to your specific needs.

Use the general lockout procedure outlined in Table 2-4 as a guide for developing your own procedure.

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Note: Only authorized persons should perform the lockout/tagout procedure.

Table 2-4. Lockout/Tagout Procedure

Step	Action
1. Notification	Before beginning work, notify all affected personnel that the system requires a lockout.
2. Preparation for shutdown	Before shutting down the equipment, determine the energies present, their hazards, and the means for controlling them. Collect written maintenance procedures, maintenance tools, and appropriate locks and tags.
3. Equipment shutdown	See "Chassis Shutdown Procedures" on page 140.
4. Isolation of equipment	Isolate the hazardous energy sources by using the methods described in "Chassis Shutdown Procedures" on page 140.
5. Application of lockout/tagout device	Attach a lockout device (padlock) to the circuit breaker in the rear of the chassis. See "Lockout of Main AC Power" on page 12.
6. Release of stored energy	Safely release or dissipate any hazardous electrical energy that remains stored in the equipment after the lockout.
7. Verification of isolation	Prior to beginning work on a locked out piece of equipment, verify that the equipment is in a zero energy state by attempting to turn it on using the controls designed for that purpose.
8. Performance of maintenance tasks	Ensure that work on the equipment is performed only by authorized staff who have applied a lockout device.
9. Equipment inspection	With lockout device still in place, inspect the equipment to ensure that is has been properly reassembled and is ready for operation. Verify that all tools, used parts, cleaners, and rags have been removed from the equipment.

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Table 2-4. Lockout/Tagout Procedure *(continued)*

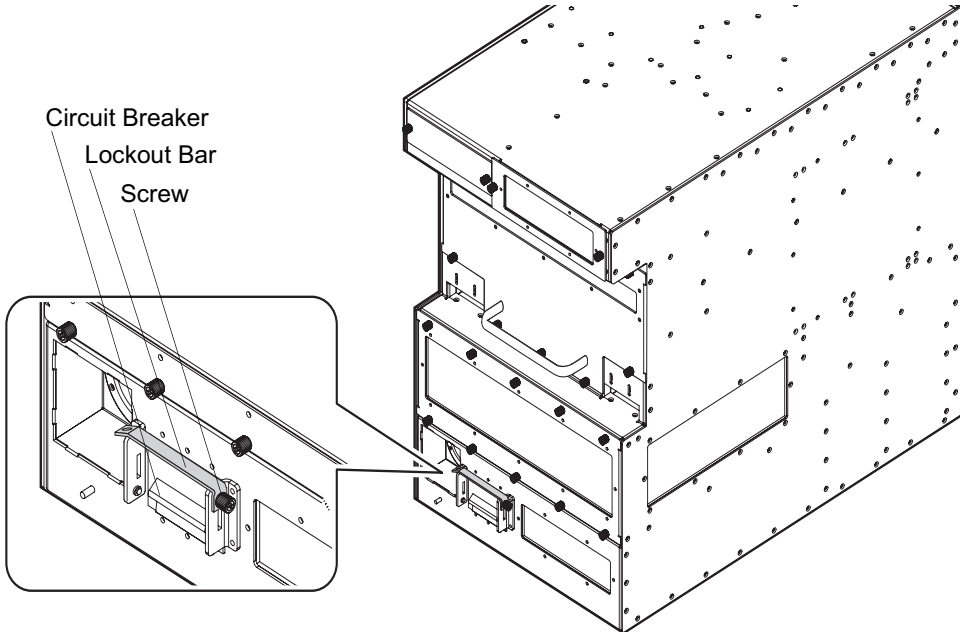
10.	Personal inspection	Verify that all personnel are clear of areas that could be hazardous during operation or malfunction of equipment upon starting. Inform any affected people that locks are about to be removed from the equipment.
11.	Removal of lockout/tagout devices	Ensure that energy isolating (lockout/tagout) devices are removed only by the authorized person who applied them. Return energy isolating devices to operating mode.
12.	Equipment start-up	After power is restored, monitor the startup from a safe position. Should a malfunction occur, shut down the equipment and reapply the lockout/tagout procedures.

Lockout of Main AC Power

A 30 amp, 3-phase, single-toggle circuit breaker is located on the rear of the ImpactRT 3200S chassis. On each side of the circuit breaker are brackets with slots designed to accept a lockout bar. In stowed position, the lockout bar rests on the top of the circuit breaker brackets and is secured with a screw to one of the brackets. (See Figure 2-1.)

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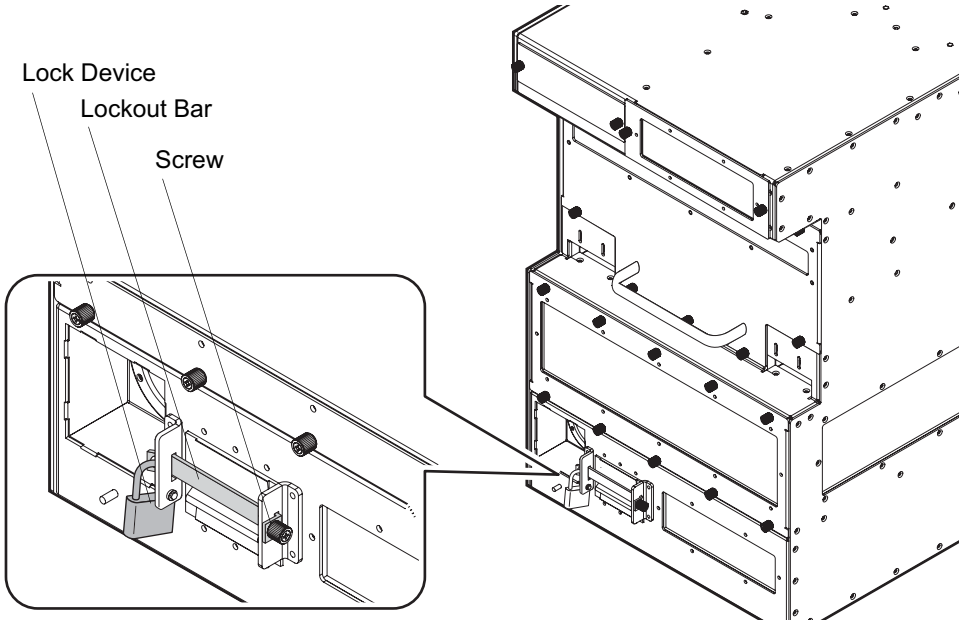
Figure 2-1. Chassis with Lockout Bar in Stowed Position



The lockout bar is designed to accept a lockout/tagout device, shown applied in Figure 2-2. The slots on the brackets are positioned to allow the breaker to be locked only in the off position.

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Figure 2-2. Chassis with Lockout/Tagout Device Applied



■ **To apply a lockout device:**

1. Using a Phillips screwdriver, remove the screw that holds the lockout bar in its stowed position on top of the brackets. (See Figure 2-1 on page 13.)
2. Starting from the right bracket, slide the bar through both bracket slots, orienting the bar as shown in Figure 2-2.
3. Using a Phillips screwdriver, attach the bar to the right end of the bracket using the screw you removed in Step 1.
4. Insert the lockout/tagout device through the hole in the left end of the bracket and lock it securely. (See Figure 2-2.)

   The circuit breaker is now locked in the off position, and the lock must be removed before power can be restored to the system.

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Installation Safety

When you install the ImpactRT 3200S chassis into a larger unit, be sure to connect the chassis to the emergency-off circuit of the integrated system. An emergency off button should be readily accessible and located within 10 feet of all operating and maintenance positions.

Warning: The weight of the ImpactRT 3200S chassis exceeds the maximum limit for a two-person lift. To move the unit, use a lifting device.

To determine safe lifting requirements for all components in the end-user configuration, perform a manual material handling analysis as outlined in the SEMI S8 safety standard.

Power Disconnection

Your system configuration must include a way to disconnect the power to the 3200S system and provide over-current protection with a minimum disconnect rating of 10,000 AIC (ampere interrupt capacity). The means for disconnection must have energy isolation (lockout/tagout) capability.

Rack Mounting Safety

The ImpactRT 3200S system chassis is intended primarily for mounting in a standard 19-inch equipment rack.

Warning: To prevent injury when mounting or servicing this unit in a rack, take special precautions to ensure that the system remains stable. If this unit is the only one in the rack, it should be mounted at the bottom of the rack. (See Table 2-9, “Center of Gravity Measurements” on page 20.)

Follow these rack mounting guidelines to ensure your safety:

- When mounting the unit in a partially filled rack, use the lowest available open space in the rack. Always load the rack from the bottom to the top with the heaviest components at the bottom of the rack.
- If the rack has stabilizing devices, install the stabilizers before mounting or servicing the unit in the rack.
- Mount the unit so that the circuit breaker located in the rear of the chassis (see Figure 1-3) is no more than 64. 5 in. (cm) above the floor.

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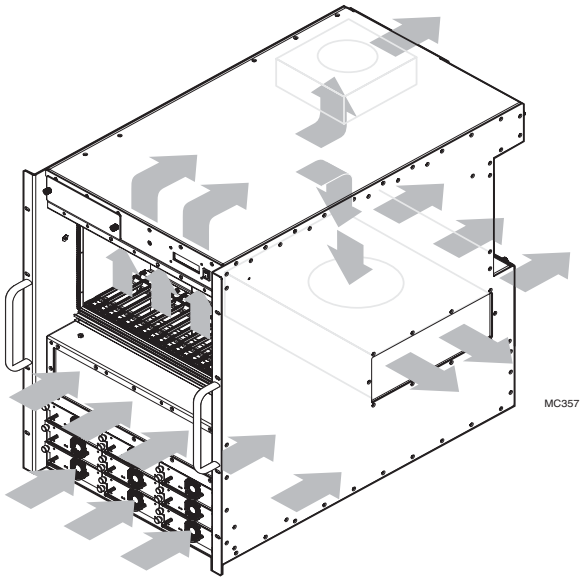
Caution: To prevent personal injury and possible damage to the equipment, do not use the rear handle to lift the chassis. Use the handle only to open the rear door.

Ventilation and Airflow

Cooling in the ImpactRT 3200S system chassis is provided by one or two blowers at the top and bottom of the chassis and by a fan on each power supply (see Figure 2-3).

Caution: Allow at least 3.5 inches (8.9 centimeters) of space for airflow at chassis front and rear and 2.0 inches (5.08 centimeters) at the chassis sides.

Figure 2-3. Airflow Requirements



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Power Ratings

Table 2-5 summarizes power data for the ImpactRT 3200S system.

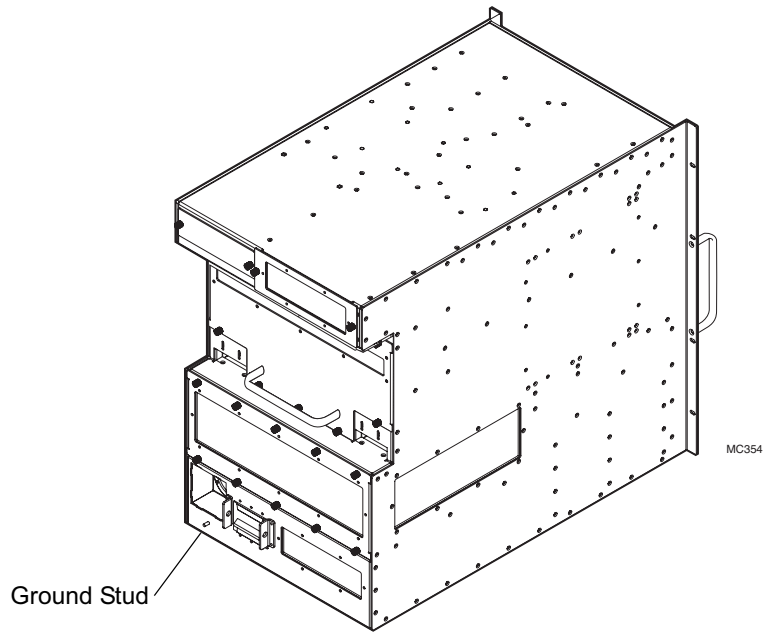
Table 2-5. Power Data

Input range:	208/240 VAC, 50-60 Hz; 3 wire + protective earth; 24A nominal
Equipment classification:	Protection Class 1
Degree of protection:	IPXO (Ordinary)
Pollution degree:	2
Equipment rated for:	Continuous operation

Grounding

To avoid electric shock, ensure that the chassis is connected to an electrical safety (green wire) ground. Connect an auxiliary ground at the ground stud in the rear of the chassis. (See Figure 2-4.)

Figure 2-4. Ground Stud



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Regulatory Compliance

The ImpactRT 3200S system meets the following regulatory criteria:

- 73/23/EEC low-voltage directive per EN 60950: 2000 for product safety of information technology equipment
- FCC Class A emissions
- 89/336/EEC EMC directive:
  - EN 50081-1: 1992, generic emission standard
  - EN 50082-1: 1997, generic immunity standard
  - EN 55024: 1998, ITE– immunity characteristics–limits and methods of measurement
  - EN 55022: 1998, limits and methods of measurement of radio disturbance characteristics of information technology equipment; performance criteria: Class A
  - IEC 61000-4-2: 1995, electrostatic discharge immunity test
    - A1: 1998, performance criteria: B
  - IEC 61000-4-3: 1995, radiated, radio-frequency, electromagnetic
    - A1: 1998, field immunity test, performance criteria: A
- CE Marking: Declaration of Conformity
- SEMI S2-0703 Product Safety Assessment
- SEMI S8-1103 Ergonomic Assessment
- SEMI S14-1103 Fire Risk Assessment
- SEMI F47-0200 Voltage Sag Immunity

Safety and Emissions Certification

This product incorporates laser-based, multi-mode transceivers of Class I (non-hazardous) type and complies with IEC 60825-1 and FDA 21 CFR 1040.10 and 1040.11 when operated within the rated specifications.

Mercury Computer Systems, Inc. is not responsible for regulatory compliance or malfunction of any user-modified product.

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FCC Notice

This equipment generates, uses, and can radiate radio frequency energy. If not installed correctly and used in accordance with the instruction manual, it may cause interference to radio communications.

ESD Precautions

The chassis contains static-sensitive devices. Use static control procedures when installing, removing, and handling all components: use an antistatic wrist strap at all times; never touch the board components with any conductive objects.

Operating Requirements

The installation site for the ImpactRT 3200S system chassis must accommodate the following specifications and operating requirements:

- Space requirements
- Weight requirements
- Environmental requirements
- Power requirements

Space Requirements

Table 2-6 lists the dimensions of the ImpactRT 3200S system chassis.

Table 2-6. System Dimensions

Height	Depth	Width
66.6 cm (26.22 in.)	76.2 cm (30 in.)	43.7 cm (17.2 in.)

For proper ventilation, do not block intake vents in the front of the chassis or outflow vents in the rear and on the sides (see Figure 2-3 on page 16). Clearances required for airflow and for service operations are shown in Table 2-7.

Caution: Adequate space must always exist around the fans and all air inlets and outlets for successful airflow. Insufficient cooling may cause serious hardware damage.

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Table 2-7. Clearances

Purpose	Front	Rear	Sides
Airflow	8.9 cm (3.5 in.)	8.9 cm (3.5 in.)	5.08 cm (2 in.)
Service	25.4 cm (10 in.)	45.7 cm.(18 in.)	N/A

Weight Requirements

Approximate weights for a fully configured and a crated chassis are shown in Table 2-8.

Warning: Chassis weight exceeds the maximum limit for a two-person lift. The chassis requires a mechanical assist for removal.

Table 2-8. Chassis Weights

Configuration	ImpactRT 3200S
Fully integrated system	89.4 kg (197 lbs)
In shipping container	172.4 kg (380 lbs)

Center of Gravity

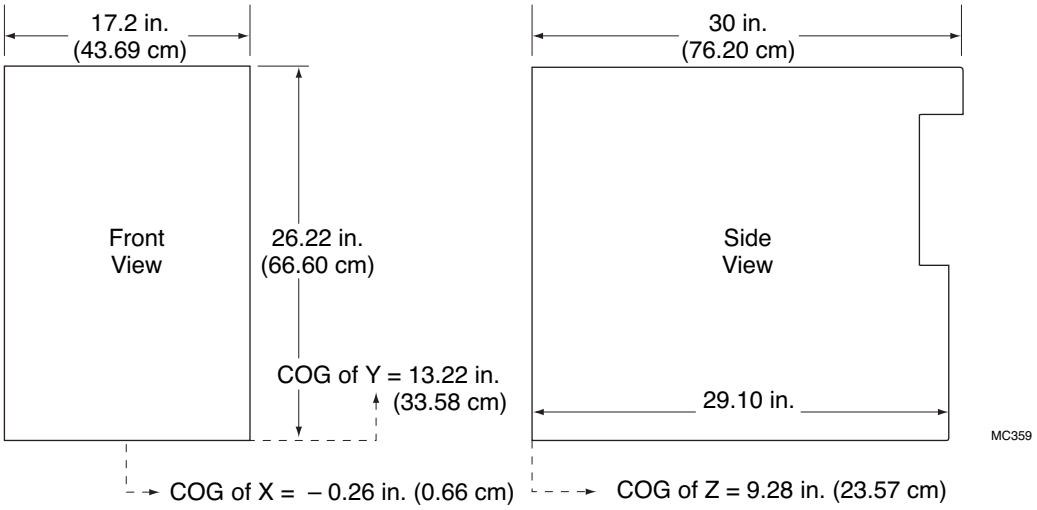
Information to locate the chassis center of gravity is shown in Table 2-9 and Figure 2-5 on page 21.

Table 2-9. Center of Gravity Measurements

Size/COG	X	Y	Z
Size	17.2 in. (43.69 cm)	26.22 in. (66.60 cm)	30 in. (76.20 cm)
COG	-0.26 in. (-0.66 cm)	9.28 in. (23.57 cm)	13.22 in. (33.58 cm)

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Figure 2-5. Chassis Center of Gravity



Environmental Requirements

The chassis is designed to work under the environmental conditions shown in Table 2-10.

Table 2-10. Environmental Specifications

Condition	Specification
Temperature – Operating	0°– 35° C, sea level to 2438 m (8,000 ft)
Temperature – Non-operating	-5° – 50° C, sea level to 10,668 m (35,000 ft)
Humidity – Operating	10% – 90%, non-condensing
Humidity – Non-operating	10% – 90%, non-condensing
Temperature – Operating	0°– 35° C, sea level to 2438 m (8,000 ft)

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Power Requirements

The electrical requirements for the chassis are shown in Table 2-11.

Table 2-11. Power Specifications

Requirement	Specification
Input	Three-phase, 208/240 VAC, 50/60 Hz, 30A input
Source	Three-pole, four-wire connection from an external source
Cord Connector	NEMA L-15-30P flanged inlet connector
Circuit Breaker	Three-phase, series-trip, 30-amp single-toggle breaker (10,000 AIC type)

For additional requirements, see the electrical specifications for the individual system modules (pages 62, 70, and 89).

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3

Chassis Components

Introduction

The main components of the ImpactRT 3200S chassis are described in detail in this chapter:

- Indicator display
- Cooling system
- Fiber-optic cabling
- AC power supply
  - Power input
  - Power distribution
- Monitor card
  - API for Windows NT
  - API for Solaris

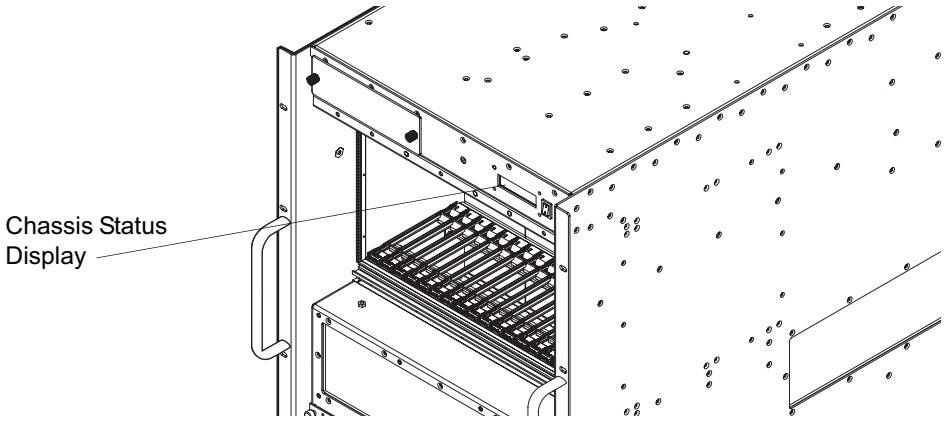
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Chassis Status Display

A liquid crystal display (LCD) on the front panel provides details about current working or alarm conditions. Figure 3-1 shows the location of the display.

For descriptions of the LCD display messages and their meanings, see "Chassis Status Display" on page 161.

Figure 3-1. LCD Display on Card Cage



Midplanes

The card cage houses a 6-slot CompactPCI system midplane plus up to three 5-slot expansion midplane slots designated with physical slot numbers that increase from left to right (as viewed from the front in Figure 3-2). Slot 21 (system slot) is occupied by the CompactPCI host, which initializes the set of boards that makes up the multicomputer.

Mercury-integrated components of the midplane include an interlink assembly of four dual-port RapidIO interconnect modules and a passive rigid-flex cable, which together provide multiport links between modules. Each five-slot interconnect module provides 10 RapidIO ports to connect up to five CompactPCI midplane slots and six RapidIO ports to connect to other interconnect modules. This interlink assembly supports two RapidIO, 8-bit parallel links through CompactPCI P4/J4 connectors to each processing board.

User-replaceable Mercury modules installed in the chassis include the processing modules, bridge modules, and fiber-optic I/O rear-transition modules. For infor-

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mation about installing, configuring, and troubleshooting specific modules, see the following chapters:

Chapter 4, “MC4PK Processing Module”

Chapter 5, “MCP-P4K Processing Module”

Chapter 6, “MCP6-DPRB-3R Bridge Module”

Chapter 7, “MCPIO-DPRC Bridge Module”

Chapter 8, “TIO-2FGR I/O Module”

Chapter 9, “TIO-4FGD I/O Module”

Chapter 10, “TIO-2FGD I/O Module”

For system configuration and troubleshooting information, see Chapter 11 and Chapter 14, respectively.

Warning: Boards installed in the card cage must be securely seated and the ejector handles on the front panel firmly locked and secured with screws. Removing a board without properly shutting down the system can severely damage the board and can expose high-current components, creating a risk of electric shock.

Warning: The system contains static-sensitive devices. Static control procedures should be used when installing, removing, or handling all components. Use an antistatic wrist strap at all times. Never touch the module components with a conductive object.

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Cooling System

The chassis uses two independent cooling systems:

- A blower assembly at the lower rear of the chassis cools the card cage. For 21-slot configurations, a second blower assembly is added at the top rear to provide additional cooling.
- Individual fans cool each power supply unit.

Two airflow pathways cool the front and rear card cage and as the power supply area. Figure 2-3 on page 16 shows the air intake plenum for the card cage (top) and the air intake for the power supplies and drive bays (bottom).

Estimated total air draw for each pathway is as follows:

- From top rear exit (cooling front card cage): 110 CFM (21-slot configuration only)
- From each side exit (cooling front card cage): 150 CFM
- From lower rear exit (cooling front card cage): 150 CFM
- From bottom exit (cooling power supply): 90 CFM

Rear I/O

Table 3-1 lists the I/O connections available from the rear of the chassis.

Table 3-1. I/O Connectors

Jumper	Description
J1	Keyboard/Mouse Combo Connector
J2	DB15 SVGA Connection
J3	Remote Reset Connection
J4	DB25 Expansion Connection
J5	RJ45 Ethernet Connection
J6	RJ45 Ethernet Connection
J7	MTP Fiber Connector
J8	MTP Fiber Connector

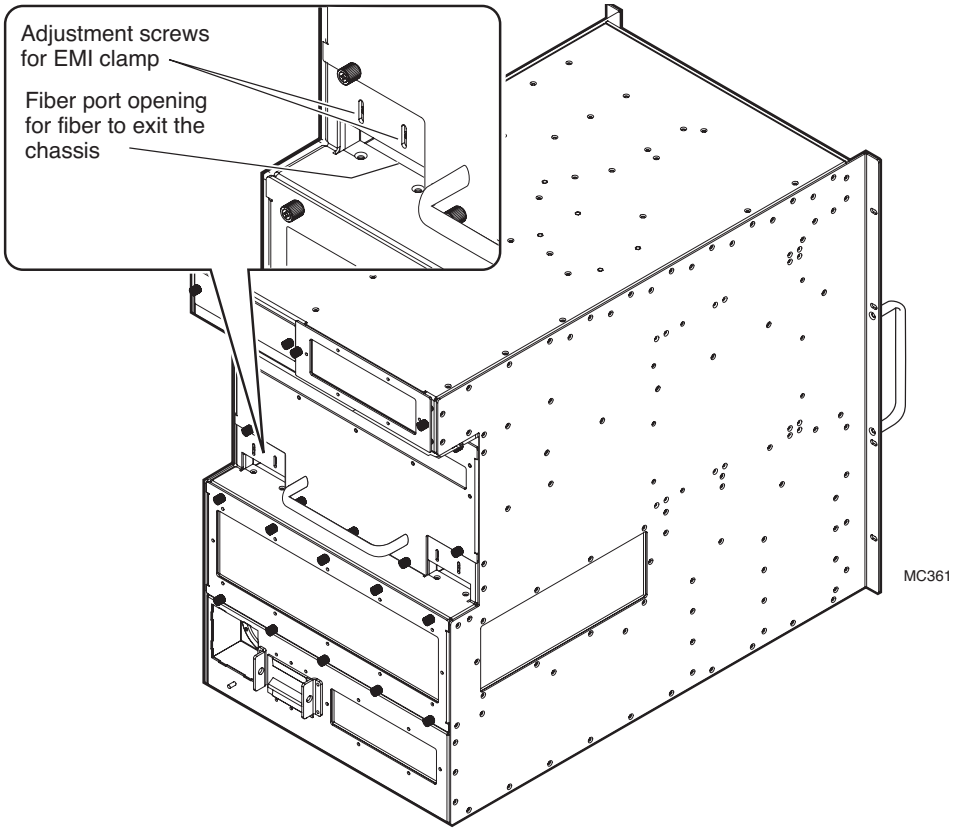
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The rear panel must be removed from the chassis to service the fiber-optic cabling. This panel has an interlock that disables DC power when the panel is removed. Fiber-optic cables are fastened with guide clips and pass through two EMI foam gasket fiber ports.

Fiber I/O ports and fiber cable guide clips, accessible from the rear of the chassis, guide the cables from the faceplates of the I/O modules to the rear of the chassis and out.

Two MTP bulkheads on the connector panel are provided for further expansion. The bulkheads can support up to 24 fiber connectors for each MTP connector, depending on the MTP fiber harness in use.

Figure 3-2. Fiber Optic Cabling

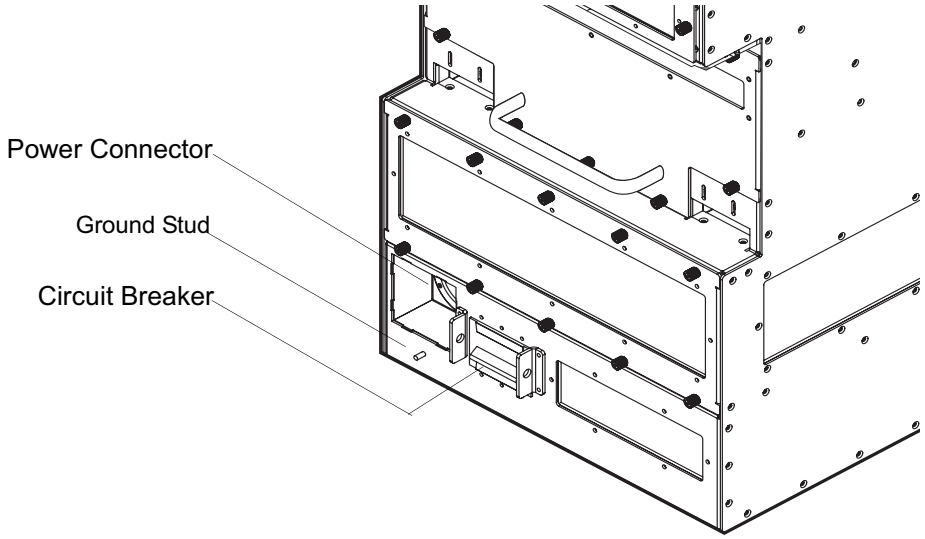


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AC Power Distribution

The system requires a three-phase, 208-240VAC, 50/60 Hz, 24A input in the form of a three-pole four-wire connection from an external source. The power cord connector, a NEMA L15-30p flanged inlet connector, is located on the rear panel of the system chassis, next to the three-pole, series-trip 30A circuit breaker (10,000 AIC type) (Figure 3-3).

Figure 3-3. Rear Panel AC Power Components



The ground lead connects to the chassis enclosure next to the inlet connector, and the three input phase lines are wired to the line terminals of the circuit breaker. From the load terminals of the circuit breaker, each phase of the AC input feeds into the EMI filter, and from there, directly to the power backplane. The input ground connection for each power supply module is connected to the enclosure through the power backplane.

The backplane feeds the AC power to the three banks of power supply connectors. Each bank is for a particular phase-phase combination and has separate AC power feeds through power stubs. Figure 3-4 on page 29 shows a block diagram of the AC power interconnections.

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Figure 3-4. AC Power Interconnections

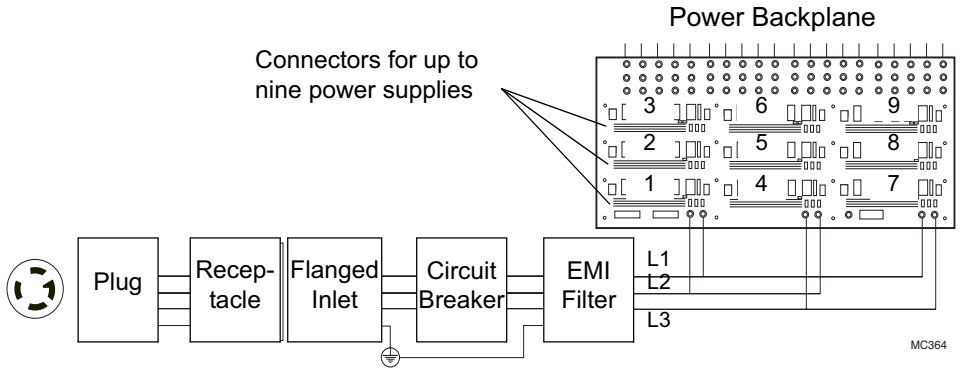
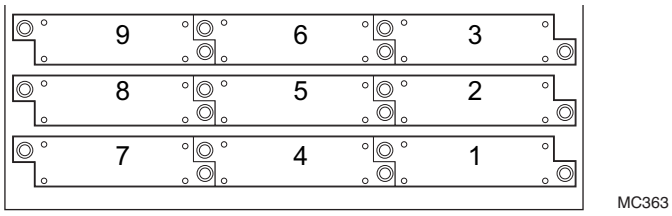


Table 3-2. AC Power Phase-Phase Combinations to Power Supplies

Phase	Power Supply
Phase 1 - Phase 2	1, 2, 3
Phase 2 - Phase 3	8, 5, 2
Phase 1 - Phase 3	7, 8, 9

Figure 3-5. Power Supply Designations (front of chassis)



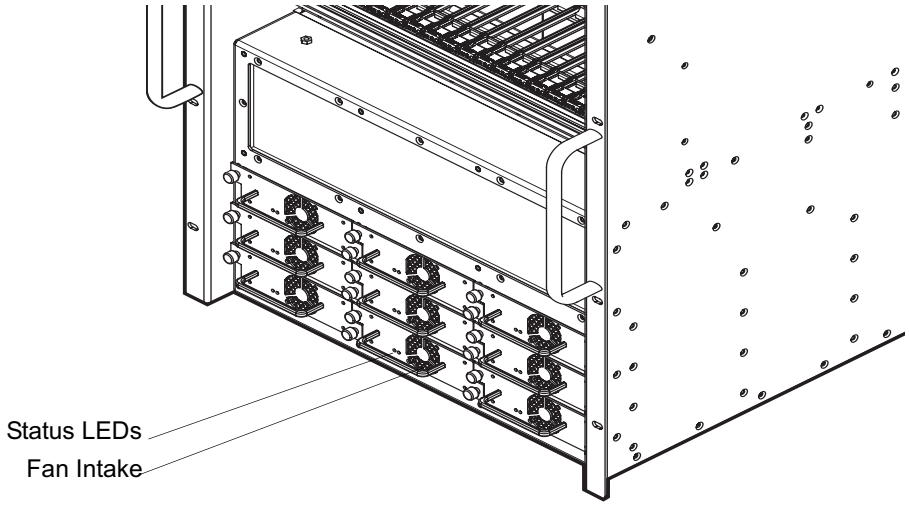
9,6,3 = installed for low end configuration
2,3,5,6,8,9 = installed for mid-level configuration

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Power Supplies

Up to nine power supply modules are located at the bottom of the chassis enclosure, facing the front. Access to the power supplies is at the front of the chassis (see Figure 3-6). Each power supply unit is cooled by an individual built-in fan and includes status LEDs.

Figure 3-6. Power Supply Units



The status indicators are visible on the front panel of each power supply. The "PWR GOOD" LED is green if the power supply is working properly; amber indicates supply is out of specified range. The "AC GOOD" LED is green if AC voltage is present and above minimum level.

Power Supply Output

The power supply modules accept a 208/240 VAC single-phase input, and each delivers 600W of output power under normal operating conditions. The output per power supply is shown in Table 3-3.

Table 3-3. Power Supply Output

Volts	Amperes
5 VDC	80
3.3 VDC	40

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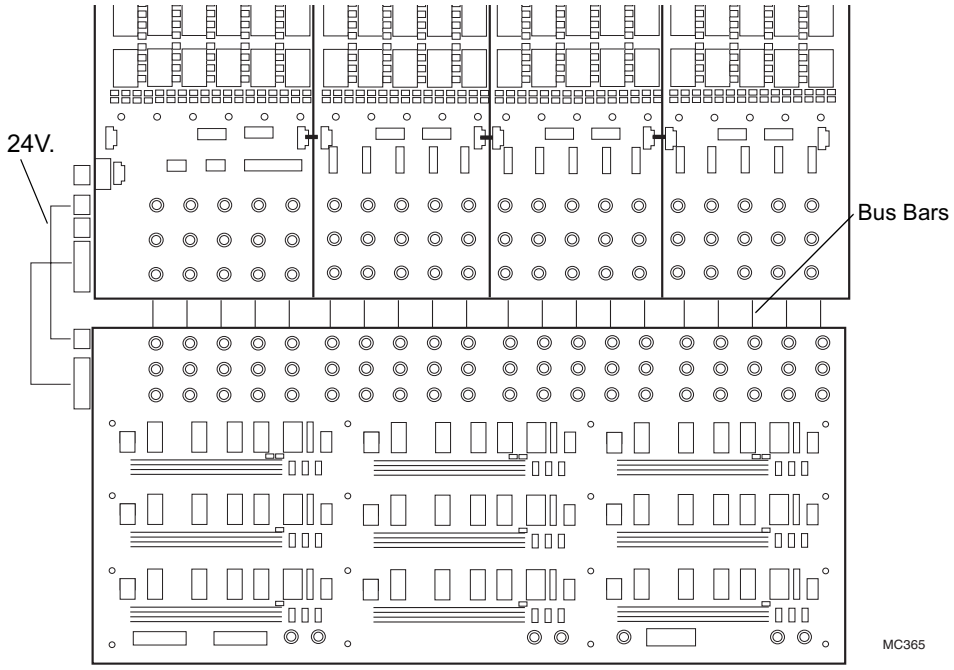
Table 3-3. Power Supply Output *(continued)*

Volts	Amperes
+12 VDC	20
-12 VDC	3
24 VDC	5
+5 VDC	1 (standby)

All output from the power modules to the midplanes is through bus bars, rated for the current they are intended to carry.

Figure 3-7 illustrates the power supply output interconnections.

Figure 3-7. Power Supply Output Interconnections



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Alarms and Controls

Each of the power supply units provides status and alarm information through an Inter-Integrated Circuit Bus (I^2C) interface. These signals are connected to the power backplane through the connector at the rear. Each module also provides separate, isolated +5V emergency power output rated at 100 mA.

Each power supply supports remote voltage sensing for its main output through a pair of leads and provides an Output Good indication through I^2C. In addition, each module can be inhibited by an external signal.

All signals from each power supply reach the power backplane through the rear power supply connector. The sense and return signals for all voltages are connected on the power backplane, and the midplane voltages are connected to the system midplane and expansion midplanes through bus bars.

Specific control connections are as follows:

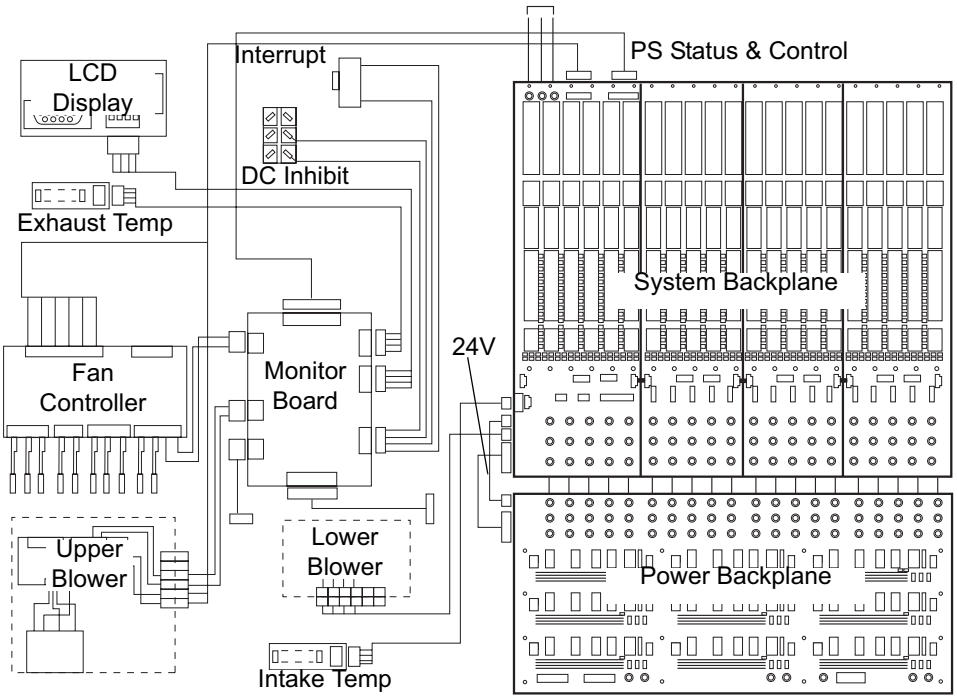
- The 24V output and its associated return are connected from the power backplane to the system midplane through a cable.
- The power supply status and control signals (I^2C buses, DC inhibit, power supply present signals) are connected from the power backplane to the system backplane. These signals are then routed to the monitor board through a cable.
- The intake temperature sensor board signals are connected through a cable that connects to the lower portion of the system midplane. Within the system midplane, the temperature sensor signals are routed on traces to a connector at the upper end of the system midplane, which also carries status signals from the blowers and power supplies.
- The lower blower assembly connects to the midplane through a cable that is then routed to the top of the system midplane for connection to the fan controller along with the 24 VDC power.

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Interconnections

The diagram in Figure 3-8 shows the power supply control and alarm interconnections.

Figure 3-8. Power Supply Control and Alarm Interconnections



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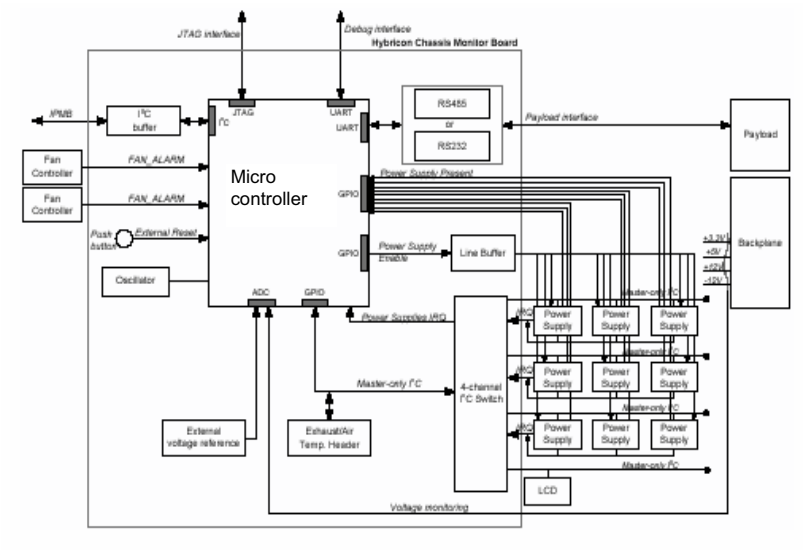
Monitor Board

The monitor board monitors system status and provides information through the LCD and RS-232 line interface connection.

Architecture

The hardware architecture of the monitor board is shown in Figure 3-9.

Figure 3-9. Monitor Board Architecture



The monitor board includes the following features:

- Microcontroller
- External reset on rear of chassis
- Serial debug interface
- Voltage monitoring
- Serial (RS-232) interface to the host
- Fan control: two logical fan failure sensors from the external fan controllers (FAN_ALARM_TOP, FAN_ALARM_BOT)
- External LCD for status message display

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- Nine power supplies for the chassis

Connectors

The monitor board provides on-board connectors, as listed in Table 3-4.

Table 3-4. Monitor Board Connectors

Connector	Function
J1	DC_ENABLE_SW and INTRUSION_SW inputs
J2	LCD display power and I/O connector
J3	Exhaust/air temperature sensor
J4, J5	Upper/lower fan controller connector
J6	Power supplies (1-9) control connector
J7	Rear I/O reset input (PCI reset switch)
J8A, J8B	Host interfaces: two RJ-45 connectors for RS-485 daisy chain (not supported in the current release)
J9	RS-232 host interface (one micro RS-232 connector)
J11	IPMB connector (not used)
J12	JTAG interface to the microcontroller
J13	Serial debug interface (one standard RS-232 connector)

Host Interface

The host interface supports communication between the host and a single monitor board. The monitor board implements the RS-232 interface on the micro DB-9 (J9) connector. The jumper position for the RS-232 host interface is 2-3.

The settings for the line interface to the monitor board are as follows:

- 9600 baud
- 8 data bits
- No parity
- 1 stop bit
- No flow control

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Note: The baud rate for the line interface is set through the firmware and should not be changed.

Power Supplies

Three sets of three power supply modules (for a total of 9) are connected to the first three legs of the off-board, master-only I^2C PC9545 device.

Signalling

A single connector (J6) on the monitor board provides the 12C bus signals and supports these signaling functions:

- Sends enable power supply signals (DC_ENABLE) to power supplies, where the microprocessor drives the power supply enable signal (PS_ENABLE).
- Receives power supply present (PS_PRESENT) signals from each power supply.
- Receives line status interrupts from power supplies (which are sent to the interrupt input of PCA9545).

Power Supply Enable and Disable

A logical device on the monitor board combines the PS_ENABLE signal with inputs from the DC_ENABLE_SW external switch and the INTRUSION_SW external switch (both available on the J1 connector) to implement the following function on the active low DC_ENABLE signal:

```
DC_ENABLE_L = INTRUSION_SW & DC_ENABLE_SW & PS_ENABLE
```

Note: A single DC_ENABLE_L signal enables or disables all nine power supplies simultaneously.

Firmware Functions

You can use the application programming interface (API) to develop system management applications that access the chassis and peripheral cards. The application typically runs on the single board computer (SBC) plugged into the system slot of the cPCI chassis.

To install the API software, follow the instructions on the appropriate installation CD:

- Monitor Windows API— for Windows 2000/NT platforms

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- Solaris API— for Solaris platforms

Using the API

API functions can be used to communicate with the monitor board and retrieve sensor data such as voltages and air temperatures. Access to the monitor board interface is through the RS-232 serial port on the host CPU.

To communicate with the monitor board:

- Use the C functions defined in the next section,"API Header File," and illustrated in Example 3-1, "C Program Sample" to develop a C application. Include the API header file as well as the standard IO header file.
- Link the C program to the monitor board API library description file, `monlib.lib`, and to the serial port library description file, `CUG_serialport.lib`.

API Header File

The API header file reproduced in this section defines the general hardware parameters of the monitor board and provides a synopsis of each C function that can be used to address it.

```
#ifndef __PPSMONITOR_H
#define __PPSMONITOR_H
/*************************************************************************/
/*  ppsmonitor.h */
/*  These C functions allow access to chassis power supply /*  voltages, air
temperatures, fan status etc from the monitor board.
*/
/*  All functions begin with 'pps' to avoid C namespace */
/*  conflicts.                                                           */
*/
/*  This header is a series of function prototypes which serve as the    */
/*  synopsis for each function.                                          */
/*  Typical usage:                                                       */
/*  #include "ppsmonitor.h"
*/
```


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```
/*  char *error = 0;                                                    */
/*  double x = ppsReadSensor("01",&error);    // pass the address of error  */
/*  if ( error ) {                                                      */
/*     printf("error reading the sensor.%s\n",error);                   */
/*  } else {                                                            */
/*     printf("sensor reading=%g\n",x);                                 */
/*  }                                                                   */
/*--------------------------------------------------------------------------*/
static char *ppsversion = "2.6";   // used for comparison with the library
code
/*  some synonyms for the sensors  */
#define PLUS_3PT3_VOLTS "00"
#define PLUS_5_VOLTS "01"
#define PLUS_12_VOLTS "02"
#define MINUS_12_VOLTS "03"
#define INTAKE_TEMPERATURE "06"
#define EXHAUST_TEMPERATURE "07"
#define TEMPERATURE_RISE "011"
#define UPPER_NON_RECOVERABLE 5
#define LOWER_NON_RECOVERABLE 2
#define UPPER_CRITICAL 4
#define LOWER_CRITICAL 2

void ppsOpenComPort(const char *name,int baud,char **errMsg);
/*
ppsOpenComPort description:
Connects to the specified com port, e.g. "COM1" and sets its baud rate.
It does not set the baud rate of the monitor board which defaults to 9600
so this should also be 9600. The errMsg is set to non-null if it can't
```


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```
acquire the com port specified. This should be one of the first commands
issued.
*/
void ppsReleaseComPort(char **errMsg);
/*
ppsReleaseComPort description:
Releases the com port if any attached, for use by other programs.
errMsg is non-null if any error occurs.
*/
int ppsLoadSdrTable(char **errMsg);
/*
ppsLoadSdrTable description:
Reads and parses all the sensor data records and stores them in a table.
This function must be called once to initialize the SDR table otherwise
calling the ppsReadSensor function will produce an error message.
Returns the count of the number of records parsed.
Sets errMsg to non-null if any error occurs.
*/
char *ppsVersion(void);
/*
ppsVersion description:
Gets the version string of the pps C library
*/
const char *ppsGetSensorIdsFromTable(void);
/*
ppsGetSensorIdsFromTable description:
Returns any sensor IDs in the SDR table packed into a space delimited string.
If the table hasn't been populated with the ppsLoadSdrTable funtion,
the returned string will be empty "".
```


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```
*/
void ppsSetPayloadPortBaudRate(int baud,char **errMsg);
/*
ppsSetPayloadPortBaudRate description:
Use this to change the serial port baud rate on the monitor board.
After this command you must release the serial port and
reconnect to the monitor board with the new baud rate.
errMsg is null, i.e. 0 if there is no error.
*/
const char *ppsGetSensorDescText(const char *sensorId);
/*
ppsGetSensorDescText description:
Retrieves the sensor text description where id is 2 digit hex code 02, 0A
for the sensor id. On error it returns this message:
"sensor id invalid or sensor table not initialized."
*/
const char* ppsWriteAndReadRaw(const char *textWithNewLine);
/*
ppsWriteAndReadRaw description:
Writes out the raw hex request string and returns ptr to the response buffer.
Useful for debugging and doing special IPMI commands for which no
high level interface functions have been prepared.
*/
int ppsReadSensorStatus(const char *sensorTokenList,char **errMsg);
/*
ppsReadSensorStatus description:
Reads the status of discrete and thershold sensors.
Returns status bits cooresponding to the order of the token list.
0 if status is ok and 1 if status is fail. It stops
```


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```
getting sensor status as soon as it finds one that is in the
fail state. The firmware shuts down the system if any fail so
if ine fails they will most likely all be in a fail state.
Sets errMsg to non-null if an error occurs.
*/
double ppsReadSensor(const char *sensorId,char **errMsg);
/*
ppsReadSensor description:
Reads the value from a threshold sensor.
Sets errMsg to non-null if an error occurs.
*/
void ppsSetDisplayMessage(const char *message,char **errMsg);
/*
ppsSetDisplayMessage description:
sets the message into the LED display, two lines by 16 chars.
Long messages are truncated.
errMsg is null, i.e. 0 if there is no error.
*/
int ppsReadSensorStatus(const char *sensorTokens,char **errMsg);
/*
description: Gets the status bits for the fans and power supplies
or whatever is in the sensorToken list and packs them
into an int in the order corresponding to the token list. Usage:
    char *errMsg = 0;
    int status = ppsReadSensorStatus("0B 0A 09",&errMsg);
    if ( errMsg ) {
      printf("Error reading status bits, %s\n",errMsg);
    }
return: int value set to the status bits. The value
```


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```
       will be zero if everything is ok. Non-zero if something has failed.
       Negative means an error occurred and errMsg will then be non-null.
       errMsg is null if no error occurred reading he status bits.
       The LSB is bit 0.
*/
double ppsGetThresholdLimit(const char* sensorId,int threshold,char **errMsg);
/*
ppsGetThresholdLimit description:
This function may only be applied to threshold sensors.
Reads out the current value for the specified sensorId threshold.
  5 upper non-recoverable threshold";
  4 upper critical threshold
  3 upper non-critical threshold
  2 lower non-recoverable threshold
  1 lower critical threshold
  0 lower non-critical threshold

Only 2 and 5 are legal for the pps monitor board.
Returns -5E6 and sets errMsg to non-null if error occurs.
*/
void ppsSetThresholdLimit(const char* sensorId,int whichThreshold,double
value, char **errMsg);
/*
ppsSetThresholdLimit description:
This function sets the specified threshold ( 0 to 5 ) of a threshold sensor.
  5 upper non-recoverable threshold";
  4 upper critical threshold
  3 upper non-critical threshold
  2 lower non-recoverable threshold
```


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```
  1 lower critical threshold
  0 lower non-critical threshold

Only 2 and 5 are legal for the pps monitor board.
For sensor 12 only 5, upper non-recoverable, is allowed.
errMsg becomes non zero if an error occurs.
*/

/*---------------  mostly debug related functions below ------------------*/
void ppsSetDebugLogFile(const char* filename,char **errMsg);
/*
ppsSetDebugLogFile description:
This opens a log file for debug messages which otherwise go to stdout.
If it can't open the file for write, it returns a non-null errMsg.
*/
void ppsSetDebugLevel(int newlevel);
/*
ppsSetDebugLevel description:
If debug is enabled i.e. it is a debug build, then more or less debug messages
will be emitted depending on the level. The typical levels are 5,10, and 20.
Setting it to 21 will cause all debug messages to be emitted into the debug
output stream which is stdout by default.
*/
int ppsReadVoltsAndTemps(char **errMsg);  // for debug use, writes to stdout

/* ppsReadVoltsAndTemps description:
if Debug enabled it will write the measured values of all voltage
and temperature threshold sensors to stdout.
It returns a count of how many measurements it made.
```


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```
This is mainly a debug function used for system testing.
*/
#endif /* __PPSMONITOR_H */
```

Retrieving Sensor Data

You use the C functions described in the API header file to retrieve information from the Sensor Data Records (SDR).

Note: You must use the `ppsLoadSdrTable` command to initialize the SDR before issuing SDR commands.

The SDR (see Table 3-5, "Sensor Data Records" on page 44) converts the raw sensor readings for linear sensors into real values in the desired units using this formula:

```
Y = (Mx + (B * 10K1)) * 10K2 Units
```

Where:

- x = raw reading
- y = converted reading
- M = signed integer constant multiplier
- B = signed integer constant offset
- K1 = signed exponent. (Sets decimal point location for B.)
- K2 = signed result exponent. (Sets decimal point location for the results.)

Table 3-5. Sensor Data Records

Sensor ID	Unit	ID String	Multi-plier (M)	Offset (B)	B Exp (K1)	R Exp (K2)
00	Voltage	+3.3V	143	0	9	-4
01	Voltage	+5.0V	216	0	-1	-4
02	Voltage	+12.0V	55	0	4	-3
03	Voltage	-12.0V	143	-45	3	-3
04		Top Fan	0	0	0	0
05		Bottom Fan	0	0	0	0

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Table 3-5. Sensor Data Records *(continued)*

Sensor ID	Unit	ID String	Multi-plier (M)	Offset (B)	B Exp (K1)	R Exp (K2)
06	Degrees C	Intake Temp	100	0	5	-2
07	Degrees C	Exhaust Temp	100	0	5	-2
08		Power Supply 1		0	0	0
09		Power Supply 2		0	0	0
0A		Power Supply 3		0	0	0
0B		Power Supply 4	0	0	0	0
0C		Power Supply 5	0	0	0	0
OD		Power Supply 6	0	0	0	0
OE		Power Supply 7	0	0	0	0
10		Power Supply 8	0	0	0	0
11	degrees C		100	0	5	-2

Program Examples

Example 3-1, “C Program Sample” and Example 3-2, “Sample Output from C Program” on page 50 illustrate the use of the system management API.

Example 3-1. C Program Sample

The following is an example of a simple C program that uses the API to retrieve sensor data.

```
#ifdef __BORLANDC__
  #pragma argsused
#endif
#include <stdio.h>
#include  "../consoleApp/ppsmonitor.h"


int main( int argc, char * argv[] )
{
```


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```
  long retval;
  int count;
  const char *p;
  const char *response;
  char *errMsg = 0;
  double value;
  int i;

  printf("I am a plain vanilla C program.\n");
  printf("Using pps library version %s\n",ppsVersion());
  fflush( stdout);

  ppsSetDebugLogFile("plainc_monitor.log",&errMsg);
  ppsSetDebugLevel(11);  // debug levels are LOW MED and HIGH at 5
10 and 15
  ppsOpenComPort("COM1",9600,&errMsg);

  if ( errMsg ) {
    printf("Error opening serial port,%s\n",errMsg);
    return 1;
  }

  printf("loading all the SDR's, this takes time ...\n");
  fflush( stdout);

  count = ppsLoadSdrTable(&errMsg);

  if ( errMsg ) {
    printf("Error loading the SDR's, %s\n",errMsg);
  }
```


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```
  else if ( count == 0 ) {
    printf("No sensors read into the table!\n");
  }
  else {
    const char *id = PLUS_3PT3_VOLTS;
    double value;
    int status;
    const char *sensors = "00 01 02 03";

    printf("Read %d SDR's\n",count);
    fflush(stdout);

    printf("List of Sensor ID tokens =
%s\n",ppsGetSensorIdsFromTable());

    p = ppsGetSensorDescText(id);

    printf("Now reading status bits for sensor %s\n",sensors);

    status = ppsReadSensorStatus(sensors,&errMsg);

    if ( errMsg ) {
      printf("Error reading status bits, %s\n",errMsg);
    }
    else {
      if ( status ) {
        printf("ppsReadSensorStatus read back failed status bits in
hex= %x\n",
            status);
      }
```


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```
      else {
        printf("ppsReadSensorStatus detected no failed status for
sensors %s\n",
          sensors);
      }
    }

    printf("Sensor Description for sensor id=%s is %s\n",id,p);

    value = ppsReadSensor(id,&errMsg);

    if ( errMsg ) {
      printf("%s\n",errMsg);
      fflush(stdout);
    }
    else {
      printf("Sensor value = %f\n",value);
      fflush(stdout);
    }
  }

  printf("Now testing write and read raw\n");

  response = ppsWriteAndReadRaw("[B8 00 00 00 40 0A]\n");

  printf("response = %s\n" , response);
  fflush(stdout);

  for ( i = 0 ; i < 6 ; i++ ) {
```


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```
    value = ppsGetThresholdLimit(PLUS_3PT3_VOLTS,i,&errMsg);
    if ( errMsg ) {
      printf("%s\n",errMsg);
      fflush(stdout);
    }
    else {
      printf("Threshold %d for sensor %s is
%g\n",i,PLUS_3PT3_VOLTS,value);
      fflush(stdout);
    }
  }

  count = ppsReadVoltsAndTemps(&errMsg);

  printf("after call to ppsReadVoltsAndTemps(), count =
%d\n",count);
  fflush(stdout);

  if ( errMsg ) {
      printf("%s\n",errMsg);
    }
  fflush(stdout);

  ppsReleaseComPort(&errMsg);
  return 0;
} // END PROGRAM
```

The following example shows typical output from running Example 3-1 on page 45.

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Example 3-2. Sample Output from C Program

```
C:<path> \ConsoleAppPlainC.exe
I am a plain vanilla C program.
Using pps library version 2.4
loading all the SDr's, this takes time ...
Read 18 SDR's
Sensor Description for sensor id=01 is +3.3V
Sensor value = 3.331900
Now testing write and read raw
response = [B8 00 00 00 40 0A]
[BC 00 00 00 00 40 0A 03 00 00 00]
Threshold 0 for sensor 01 is 0
Threshold 1 for sensor 01 is 0
Threshold 2 for sensor 01 is 3.1746
Threshold 3 for sensor 01 is 0
Threshold 4 for sensor 01 is 0
Threshold 5 for sensor 01 is 3.4749
------ Now reading all Temperature and Voltage sensors ----
sensor id = 01, measures 33319E-4 Volts for +3.3V ( raw = E9) ,
sensor thresholds: 00 00 DE 00 00 F3
sensor id = 02, measures 50760E-4 Volts for +5.0V ( raw = EB) ,
sensor thresholds: 00 00 DF 00 00 F4
sensor id = 03, measures -107580E-3 Volts for +12.0V ( raw = DC) ,
sensor thresholds: 00 00 CE 00 00 E8
sensor id = 04, measures -12539E-3 Volts for -12.0V ( raw = E3) ,
sensor thresholds: 00 00 E2 00 00 EC
sensor id = 07, measures 1700E-2 degrees C for DS75 Intake ( raw =
11) , sensor thresholds: 00 00 00 23 24 25
```


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```
sensor id = 08, measures 2100E-2 degrees C for DS75 Exhaust ( raw =
15) , sensor thresholds: 00 00 00 23 24 25
sensor id = 12, measures 25100E-2 degrees C for Temp Rise ( raw =
FB) , sensor thresholds: 00 00 00 1E 3C 46
after call to ppsReadVoltsAndTemps(), count = 7
```


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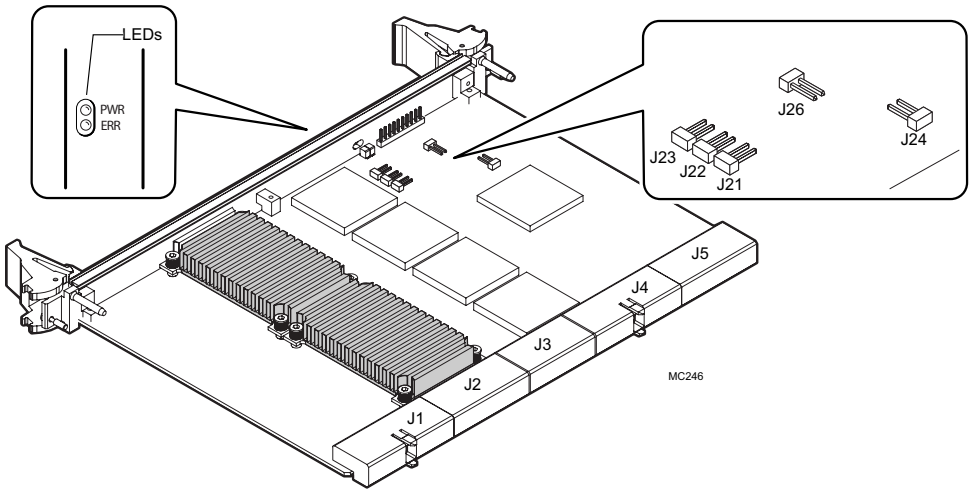
4

MC4PK Processing Module

Overview

The MC4PK512H RapidIO™ processing module features four compute nodes and one eight-port RapidIO crossbar, in a 6U CompactPCI® form factor. The modules provides two RapidIO ports to the backplane interconnect through the J4 connector and two ports to a rear transition module through the J5 connector. Each port is a full duplex, 8-bit, parallel RapidIO port. The module has no connection to the CompactPCI bus, but it uses power supplied by the bus connectors. The MC4PK512H provides 512 MB of SDRAM per node. Figure 4-1 shows the layout of the module and the location of the LED indicators and jumper blocks.

Figure 4-1. Layout of the Module



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LED Indicators

Meanings of the LED indicators on the module are provided in Table 4-1. See Figure 4-1 for the location of the LEDs.

Table 4-1. LED Status Indicators

Label	Indicator Meaning	Color
PWR	The module power subsystem is operating correctly.	Green
ERR	A system error has been detected by the CheckMC diagnostic software. If diagnostics are not run at power up, the LED comes on and stays on.	Yellow

Switches

None.

MC4PK Specifications

The physical, electrical, environmental, and compatibility specifications of the MC4PK modules are provided below.

Physical Dimensions

The physical dimensions and weight of the modules are:

Overall dimensions (mm): 233 x 160 (9.2 x 6.3 in.)

Weight (g): 690 (1.52 lbs)

Electrical Specifications

The input voltage specifications for the modules are 5.0, 3.3 Vdc ±5%

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Compatibility

The MC4PK modules can be installed in front of the following rear transition modules:

- TIO-4FGD I/O module
- TIO-2FGD I/O module

Note: The MC4PK module cannot be used with the TIO-2FGR I/O module. The MC4PK module is supported only by specific chassis from Mercury Computer Systems; it is not supported by a standard CompactPCI chassis.

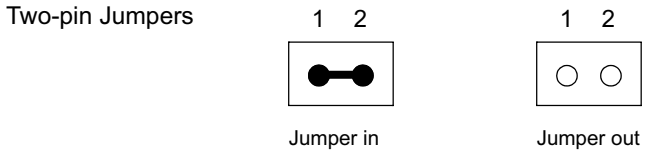
MC4PK Installation

The following sections provide procedures for setting jumpers on the MC4PK module and for installing the module in a backplane.

Jumpers

Figure 4-1 shows the location of the five 2-pin jumper blocks on the module. Table 4-2 explains the functions of the jumpers.

The jumper blocks can be set either in or out, as shown in the following figure:



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Table 4-2. Jumper Settings

Jumper	Purpose	Settings and Results
J21 	Boot compute node 0 from FLASH	Jumper out: Compute node zero boots from FLASH memory. (Default) Jumper in: Compute node zero does not boot from FLASH memory.
J22 	Write-enable FLASH	Jumper out: The FLASH memory is write-enabled. (Default) Jumper in: The FLASH memory is write-protected.
J23 	Write-protect serial EEPROMs	Jumper out: The compute node serial configuration EEPROMs on the module are write-protected. (Default) Jumper in: The compute node serial configuration EEPROMs on the module are write-enabled.
J24 	Xbar config. EEPROM	Jumper out: The crossbar configuration EEPROM is loaded at reset. (Default) Jumper in: The crossbar configuration EEPROM is not loaded at reset.
J26 	For factory use only.	Jumper out.

Assembly

Using even pressure, insert the board into the backplane.

Note: The MC4PK module has keys installed in its connectors. If the backplane in the chassis is keyed, the module might not be installable in certain slots.

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MC4PK Configuration

Use the following configuration file directives for the MC4PK512H module. For general information about creating configuration files and the meaning of the configuration directives, see the *Mercury System Manager's Guide*.

Board Directive

The board directive for the MC4PK512H module is:

```
board MC4PK512H_D1 user-assigned-name
```

where:

user-assigned-name

is a name assigned to the board by the user.

The optional attributes are:

`disable_autoroutes=yes|no`

If set to no (the default), the entire fabric is configured for autorouting, which makes more effective use of the interconnect fabric. Use caution when changing this attribute. If it is set to `disable_autoroutes=yes`, no portion of the fabric is configured for autorouting.

`max_mappings=`*number*

The maximum size in bytes of remote mappings the node can perform. This attribute is used to calculate the size for the node hash table. The default value for max_mappings is 0. The default yields a hash table entry size that is 1/64th of the memory size.

`nalloc=`*number*

Specifies the number of allocations supported from the node's local DRAM. The default is 507. Do not use another value unless you get an error indicating allocation failed.

`num_dma_transfers=`*number*

The maximum number of DMA transfers that can be performed concurrently. The default, 5000, is intentionally high. You can reduce the number to gain more memory (at the expense of the number of DMA transfers).

`pte_size=`*number*

The size in bytes of the hash table on the compute node. This attribute is optional; the default is 1/64 of compute node memory size, or 4 Mbytes. If

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adjusted, the value must be a power of two. Ignored if `max_mappings` is specified.

`num_status_words=`*`number`*

Specifies the number of status words to allocate. The default value is 2500.

`num_chain_lut_entries=`*`number`*

Specifies the number of LUT entries to reserve. The default value is 1024.

`verbose_level=[0|1]`

Sets verbosity. To enable verbosity, set to `1`. The default is `0`, disabled.

`timeout=`*`number`*

Specifies the initial timeout value in msec (`0` = none).

Several of these optional attributes (`max_mappings`, `num_dma_transfers`, and `nalloc`) can be made specific to a CPU by adding the lettered suffix `_A`, `_B`,`_C` or `_D`. For example, the optional attribute `num_dma_transfers` for CPU A can be set to a different value by adding the following to the board directive:

`num_dma_transfers_A=`*`number`*

There are four CPUs on this board from which CEs can be formed. Their names are:

- `CPU_A`
- `CPU_B`
- `CPU_C`
- `CPU_D`

`CPU_A` corresponds to compute node 0, which has the ability to boot from FLASH.

A CE directive has the form:

`CE` *`user-assigned-name`*`.cpu`

where *`user-assigned-name`* is a name assigned to the board and `cpu` is the name of the CPU from the above list.

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Connect Directive

The connect directive for the MC4PK512H module is of this form:

`connect` *`user-assigned-name1.connector1 user-assigned-name2.connector2`*

where:

`user-assigned-name1`

`user-assigned-name2`

are two names assigned by the user in a board directive, one for the MC4PK512H and the other for the hardware device to which it connects.

`connector1`

`connector2`

are two connectors, one a connector on the MC4PK512H and the other a connector on the hardware device to which it connects.

The MC4PK512H connector can be one of the following:

`RAPIDIOJ4_A` – RapidIO link A on the upper portion of the J4 connector

`RAPIDIOJ4_B` - RapidIO link B on the lower portion of the J4 connector

`RAPIDIOJ5_A` - RapidIO link A on the upper portion of the J5 connector

`RAPIDIOJ5_B` - RapidIO link B on the lower portion of the J5 connector

MC4PK Diagnostics

The diagnostic tool CheckMC supports the following test phases on the MC4PK module:

Phase 1 - Local processor(s), including crossbar and ASICs

Phase 3 - RapidIO fabric and hardware, including all crossbars on all boards and all links between crossbars

Additional test phases depend on the hardware configuration. (See the device notes for the other devices in the system.)

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MC4PK Reference

Address Space

The module does not occupy any PCI address space.

Files

The hardware description file for the device can be found at:

```
${MC_ROOT_DIR}/etc/desc/MC4PK512H_D1.desc
```


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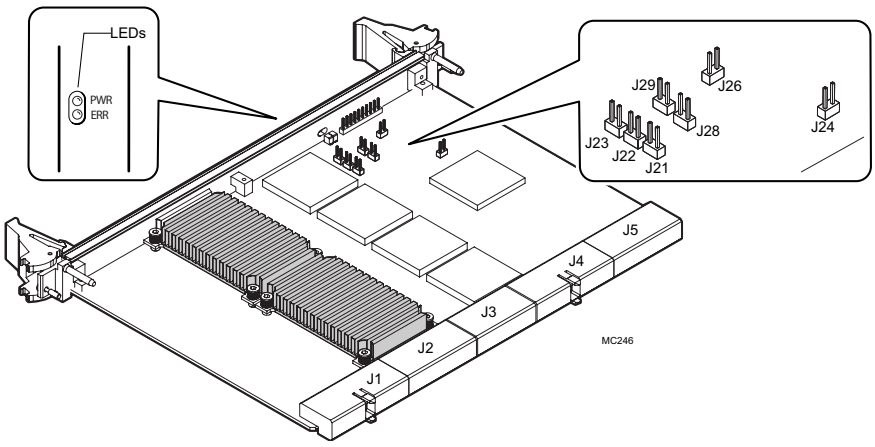
MCP-P4K Processing Module

Overview

The MCP-P4K module features four compute nodes and one eight-port RapidIO crossbar. The module provides two RapidIO ports to the midplane interconnect through the J4 connector and one port to a rear transition module through the J5 connector. Each port is a full duplex 8-bit parallel RapidIO port. There is no connection to the CompactPCI bus, but the module does use power supplied by the bus connectors. The MCP-P4K module is a 6U CompactPCI form factor module. Two versions are available: MCP-P4K256R provides 256 MB of SDRAM per compute node; MCP-P4K512R provides 512 MB.

Figure 5-1 shows the layout of the MCP-P4K module and the location of the LED indicators and jumper blocks.

Figure 5-1. Layout of the MCP-P4K Module



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LED Indicators

Meanings of the LED indicators on the MCP-P4K module are provided in Table 5-1. See Figure 5-1 for the location of the LEDs.

Table 5-1. LED Status Indicators

LED Label	Indicator Meaning	Color
PWR	The module power sub-system is operating correctly.	Green
ERR	A diagnostics software-detected system error has occurred. (If diagnostics are not run at power up, the LED comes on and stays on.)	Yellow

MCP-P4K Specifications

Physical, electrical, and compatibility specifications are provided below.

Physical Dimensions

The physical dimensions and weight of the module are:

Overall Dimensions (mm): 233x160 (9.2 x 6.3 in.)

Weight (g): 690

Electrical Specifications

The input voltage specifications for the module are 5.0, 3.3 Vdc ±5%

Compatibility

The MCP-P4K module can be installed in front of the following rear transition module:

- TIO-2FGR fiber-optic I/O rear transition module

Note: The MCP-P4K module is supported only in specific chassis from Mercury Computer Systems. It is not supported in a standard CompactPCI chassis.

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MCP-P4K Installation

The following sections provide procedures for setting jumpers on the MCP-P4K module and installing it.

Jumpers

Figure 5-1 shows the location of the six jumper blocks on the MCP-P4K module. Table 5-2 provides the functions of the jumpers.

The jumper blocks can be set either in or out, as shown in the following figure:

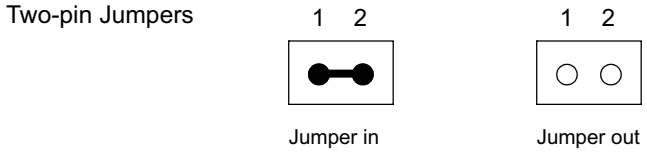


Table 5-2. Jumper Settings

Jumper	Purpose	Settings and Results
J21 	Boot CN 0 from FLASH	Jumper out: Compute node zero boots from FLASH memory. (Default) Jumper in: Compute node zero does not boot from FLASH memory.
J22 	Write-enable FLASH	Jumper out: The FLASH memory is write-protected. Jumper in: The FLASH memory is write-enabled. (Default)
J23 	Write-protect serial EEPROMs	Jumper out: The compute node serial configuration EEPROMs on the module are write-protected. (Default) Jumper in: The compute node serial configuration EEPROMs on the module are write-enabled.
J24 	For factory use only.	Jumper out.

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Table 5-2. Jumper Settings *(continued)*

Jumper	Purpose	Settings and Results
J26 	For factory use only.	Jumper out.
J28 	For factory use only.	Jumper out.
J29 	For factory use only.	Jumper out.

Assembly

Using even pressure, plug the board into the midplane.

Note: The MCP-P4K module has keys installed in its connectors.

MCP-P4K Configuration

The following sections provide configuration file directives for this device. For guidance in creating a configuration file for the ImpactRT 3200S system, see Chapter 11. For general information about creating configuration files and the meaning of the configuration directives, see the *Mercury System Manager's Guide.*

Board Directive

The board directive for the MCP-P4K512R module is:

```
board MCP_P4K512R user-assigned-name
```

where:

user-assigned-name

is a name assigned to the board by the user.

The *optional attributes* are:

```
disable_autoroutes=yes|no
```


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If set to no (the default), the entire fabric is configured for autorouting, which makes more effective use of the interconnect fabric. Use caution when changing this attribute. If it is set to `disable_autoroutes=yes`, no portion of the fabric is configured for autorouting.

`max_mappings=number`

The maximum size in bytes of remote mappings the node can perform. This attribute is used to calculate the size for the node hash table. The default value for `max_mappings` is 0. The default yields a hash table entry size that is 1/64th of the memory size.

`nalloc=number`

Specifies the number of allocations supported from the node's local DRAM. The default is 507. Do not use another value unless you get an error indicating allocation failed.

`num_dma_transfers=number`

The maximum number of DMA transfers that can be performed concurrently. The default, 5000, is intentionally high. You can reduce the number to gain more memory (at the expense of the number of DMA transfers).

`pte_size=number`

The size in bytes of the hash table on the compute node. This attribute is optional; the default is 1/64 of compute node memory size or 4 Mbytes. If adjusted, the value must be a power of two. Ignored if `max_mappings` is specified.

Several of the optional attributes (`max_mappings`, `num_dma_transfers`, and `nalloc`) can be made specific to a CPU by adding the lettered suffix `_A`, `_B`, `_C` or `_D`. For example, the optional attribute `num_dma_transfers` for CPU A can be set to a different value by adding the following to the board directive:

`num_dma_transfers_A=number`

The four CPUs on this board from which CEs can be formed are:

- `CPU_A`
- `CPU_B`
- `CPU_C`
- `CPU_D`

`CPU_A` corresponds to node 0, which has the ability to boot from FLASH.

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A CE directive has the form:

```
CE user-assigned-name.cpu
```

where `user-assigned-name` is a name assigned to the board and `cpu` is the name of the CPU from the above list.

Connect Directive

The connect directive for the MCP-P4K512R module is of the form:

`connect` *`user-assigned-name1.connector1 user-assigned-name2.connector2`*

where:

`user-assigned-name1`

`user-assigned-name2`

are two names assigned by the user in a board directive, one for the MCP-P4K512R module and the other for the hardware device being connected to.

`connector1`

`connector2`

are two connectors, one a connector on the MCP_P4K256R and the other a connector on the hardware device being connected to.

The MCP-P4K512R connector can be one of the following:

`RAPIDIOJ4_A` – RapidIO link A on the upper portion of the J4 connector

`RAPIDIOJ4_B` - RapidIO link B on the lower portion of the J4 connector

`RAPIDIOJ5` - The RapidIO link on the J5 connector

MCP-P4K Diagnostics

The diagnostics tool CheckMC supports the following test phases on the MCP-P4K module:

Phase 1 - Local processor(s), including crossbar and ASICs

Phase 3 - RapidIO fabric and hardware, including all crossbars on all boards and all links between crossbars

Additional test phases depend on the hardware configuration. (See the "Diagnostics" sections in the chapters for the other devices in the system.)

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MCP-P4K Reference

Address Space

The MCP-P4K module does not occupy any PCI address space.

Files

The hardware description file for the MCP-P4K512R module can be found at:

```
${MC_ROOT_DIR}/etc/desc/MCP_P4K512R.desc
```


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MCP6-DPRB-3R Bridge Module

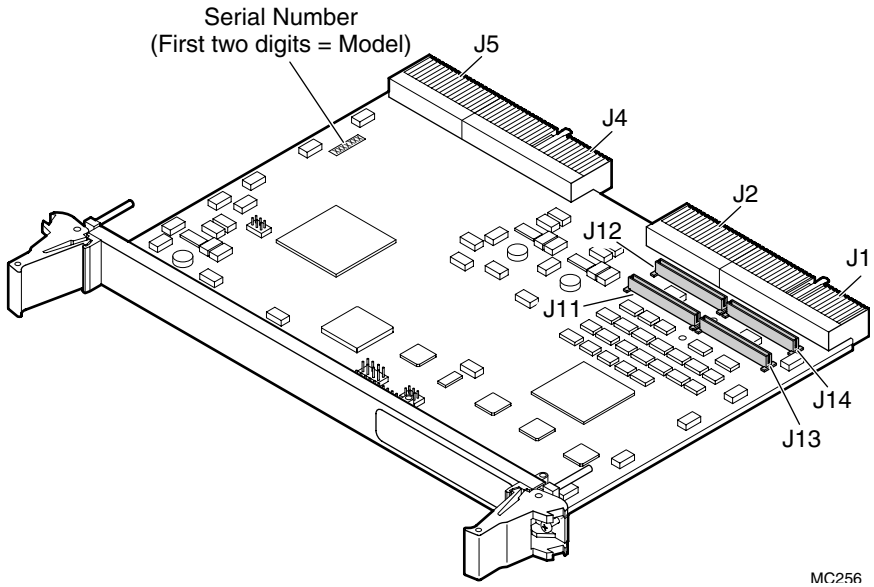
Overview

The MCP6-DPRB-3R module is a PCI-to-RapidIO bridge module in a 6U CompactPCI form factor. The module provides one PCI-to-RapidIO bridge component and one RapidIO crossbar.

Layout

The physical layout of the module is shown in Figure 6-1.

Figure 6-1. Layout of the MCP6-DPRB-3R Module



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Switches

There are no switches on this module.

MCP6-DPRB-3R Specifications

The physical, electrical, and compatibility specifications for the MCP6-DPRB-3R module are provided below.

Physical Dimensions

The physical dimensions and weight are:

- Dimensions (mm): 233 x 160 (9.2 x 6.3 in.)
- Weight (g): 433.5

Electrical Specifications

The power for this module is supplied from the CompactPCI J1 connector. The board local 3.3V supply is generated from the CompactPCI 5V supply.

- Input voltage (Vdc+- 5%): 5.0 and 3.3
- Maximum power consumption (W): 25
- Typical power consumption (W): 7

Compatibility

The MCP6-DPRB-3R module can reside in a system with the following modules:

- MCP-P4K256R and MCP-P4K512R processor modules
- MC4PK512H processor modules
- TIO-2FGR I/O module
- TIO-2FGD and TIO-4FGD I/O modules

Note: The MCP6-DPRB-3R module can physically connect to *only* the TIO-2FGR rear transition module.

MCP6-DPRB-3R Installation

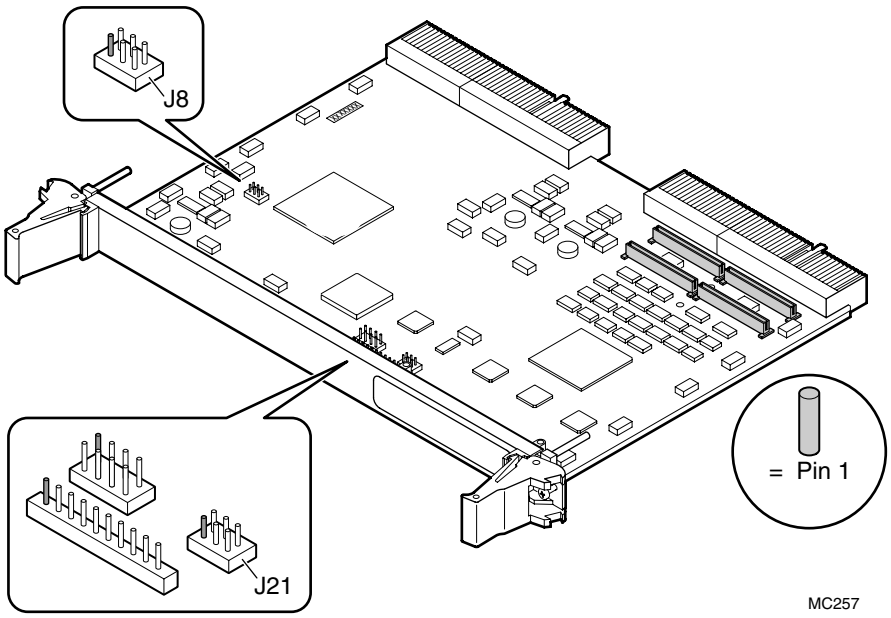
The following sections provide procedures for setting jumpers on the MCP6-DPRB-3R module and installing it.

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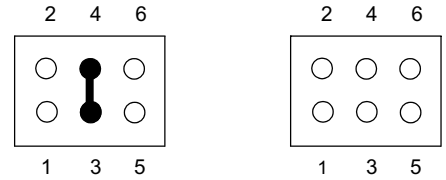
Jumpers

There are two jumper blocks on the module, J21 and J8; only J21 is user-settable. Refer to Figure 6-2 for the location of the jumpers and to Table 6-1 for the function of the jumper settings.

Figure 6-2. Location of Jumper Blocks



A jumper can be set on or off any pair of pins, as shown in the following figure.

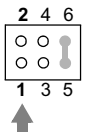


Jumper on pins 3-4 Jumper out

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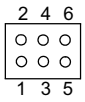
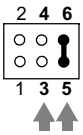
Refer to Table 6-1 to set jumper J21 according to the EEPROM write protection appropriate for your system.

Table 6-1. EEPROM Write Protection Jumper Settings

Jumper	Purpose	Setting and Results
J21 	Configuration EEPROM Write Protect Pins 1-2.	Jumper off pins 1-2: The DPRB serial EEPROM is write-protected. (The default.) Jumper on pins 1-2: The DPBR serial EEPROM is write-enabled.

The jumper settings shown in Table 6-2 are factory settings for J8 and J21. These settings should not be changed; restore them if they have been altered.

Table 6-2. Factory-Set Jumper Settings

Jumper	Factory Settings	Jumper	Factory Settings
J8 	Jumpers off all pins.	J21 	Jumper off pins 1-2 and 3-4. Jumper on pins 5-6.

Assembly

Using even pressure, plug the board into the backplane.

MCP6-DPRB-3R Configuration

The following sections provide configuration file directives used specifically for this device. For guidance in creating a configuration file for the ImpactRT 3200S system, see Chapter 11. For general information about creating configuration files and the meaning of the configuration directives, see the *Mercury System Manager's Guide*.

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Board Directive

The board directive for the MCP6-DPRB-3R is:

```
board MCP6_DPRB_3R user-assigned-name [optional-attributes]
```

where:

user-assigned-name is a name assigned to the board by the user.

The *optional attributes* are:

`bus_number=number`

Specifies the CompactPCI bus segment occupied by the board. Use with `device_number`.

`device_number=number`

Specifies the CompactPCI device number of the board. Use with `bus_number`.

`disable_autoroutes=yes|no`

If set to no (the default), the entire fabric is configured for autorouting, which makes more effective use of the interconnect fabric. Use caution when changing this attribute. If it is set to `disable_autoroutes=yes`, no portion of the fabric is configured for autorouting.

`serial_number=number`

Specifies the serial number of the module. See the serial number label on the board. The `serial_number` and `bus_number`/`device_number` arguments are mutually exclusive.

`packet_prio_p=[0|1]`

Sets the RapidIO packet priority for packets originating from the MCP6-DPRB-3R module. The default is 0, the lowest priority.

`byte_swap=[0|1]`

Specifies host endianness: little-endian (0) or big-endian (1). The default is little-endian (0).

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Connect Directives

The connect directive for the MCP6-DPRB-3R is:

`connect` *`user-assigned-name1.connector1 user-assigned-name2.connector2`*

where:

`user-assigned-name1`
`user-assigned-name2`

Two names assigned by the user in a board directive, one for the MCP6-DPRB-3R and the other for the hardware device to which it is connected, and

`connector1`
`connector2`

Two connectors, one a connector on the MCP6-DPRB-3R module, and the other a connector on the hardware device to which it is connected.

The MCP6-DPRB-3R connector can be:

`RAPIDIOJ4_A` – RapidIO link A on the upper portion of the J4 connector

`RAPIDIOJ4_B` - RapidIO link B on the lower portion of the J4 connector

`RAPIDIOJ5` - The RapidIO link on the J5 connector

`CPCI` - Standard CompactPCI J1/J2 connection

MCP6-DPRB-3R Diagnostics

The diagnostic tool CheckMC supports the following test phase on the MCP6-DPRB-3R module:

Phase 3 - RapidIO fabric and hardware, including all crossbars on all boards and all links between crossbars

Additional test phases depend on the hardware configuration. (See the "Diagnostics" sections of the chapters for the other devices in the system.)

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MCP6-DPRB-3R Reference

Address Space

Address space on the MCP6-DPRB-3R falls into three categories:

- Prefetchable memory space:

  The MCP6-DPRB-3R occupies 64 Mbytes of pre-fetchable memory space on the PCI bus.

- Non-prefetchable memory space:

  The MCP6-DPRB-3R occupies 1 Mbytes of non-prefetchable memory space on the PCI bus.

- I/O space:

  The MCP6-DPRB-3R occupies 0 Mbytes of I/O space on the PCI bus.

Files

The hardware description file for this device can be found at:

```
${MC_ROOT_DIR}/etc/desc/MCP6_DPRB_3R.desc
```


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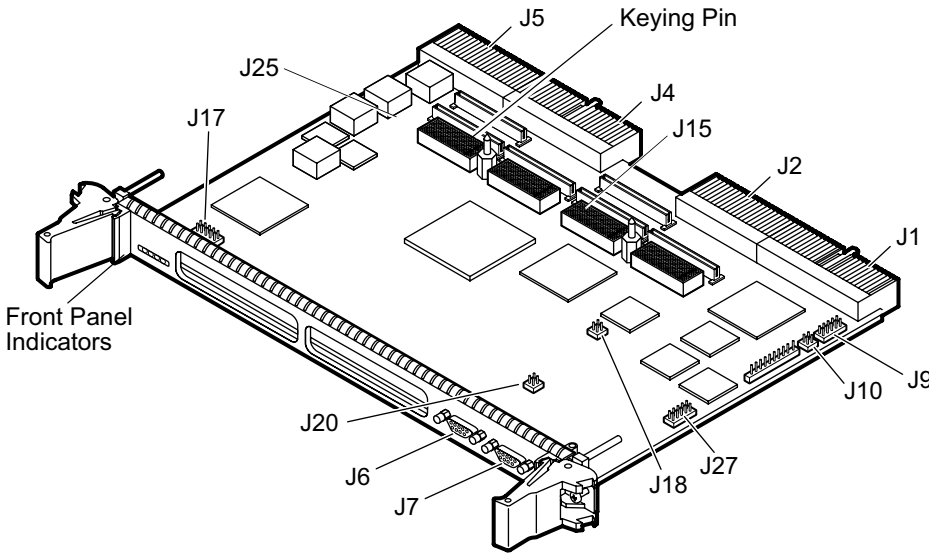
MCPIO-DPRC Bridge Module

Overview

The MCPIO-DPRC module is both a PCI®-to-RapidIO bridge module and a carrier for switched mezzanine cards (XMC) in a 6U CompactPCI® form factor. Two mezzanine sites each support a parallel RapidIO XMC module, with a direct RapidIO connection to the 8-port crossbar ASIC. The MCPIO-DPRC accommodates the multi-protocol adapter module that provides interchassis I/O.

Module features, including backplane connectors (J1, J2, J4, J5), reset connectors J6 (receiver) and J7 (output), XMC connectors (J15, J25), user-settable jumpers, front panel indicators, and keying pins for XMC alignment are shown in Figure 7-1.

Figure 7-1. Layout of the MCPIO-DPRC Module



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Indicators

Meanings of the LED indicators on the module front panel are provided in Table 7-1. See Figure 7-1 for the location of the indicators.

Table 7-1. LED Status Indicators

LED Label	Indicator Meaning	Color
READY	The module is ready for operation. All programmable devices loaded; all reset and initialization operations complete.	Green
CPCI ACT	Main PCI activity. Indicates communication between the system PCI bus and the DPRC carrier module.	Green
CMC1 ACT	Primary XMC activity. Indicates data transfer from the crossbar to the lower XMC site (J15). (XMC data input is not sensed.)	Green
CMC2 ACT	Secondary XMC activity. Indicates data transfer from the crossbar to the upper XMC site (J25). (XMC data input is not sensed.)	Green
RESET	A reset has been applied to the module.	Yellow
PCI CLOCK	PCI clock detected.	Yellow

Switches

None

MCPIO-DPRC Specifications

The physical, electrical, environmental, and compatibility specifications of the MCPIO-DPRC module are provided below.

Physical Dimensions

The physical dimensions and weight of the MCPIO-DPRC module are:

- Dimensions (mm): 266.7 x 266.1 (10.5 x 10.47 in.)
- Weight (g): 440 (0.97 lbs)

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Electrical Specifications

The power for this module is supplied from the CompactPCI J1 connector. The board local 3.3V supply is generated from the CompactPCI 5V supply.

- Input voltage (Vdc+- 5%): 5.0 and 3.3
- Maximum power consumption per XMC connector (W): 20 at 5V; 29.7 at 3.3V
- Typical power consumption (W): 8

Compatibility

The MCPIO-DPRC module can reside in a system with the following modules:

- MCP-P4K256R and MCP-P4K512R processor modules
- MC4PK512H processor modules
- MPA1-I4B adapter module
- TIO-2FGR I/O module
- TIO-2FGD and TIO-4FGD I/O modules

Note: The MCPIO-DPRC module can physically connect to *only* the TIO-2FGD/TIO-4FGD rear transition modules or the MPA1-I4B adapter.

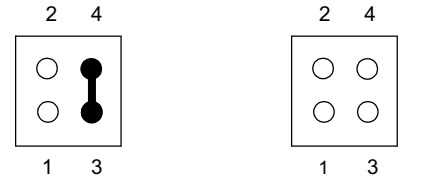
MCPIO-DPRC Installation

The following sections provide procedures for setting jumpers on the MCPIO-DPRC module and inserting it in the backplane.

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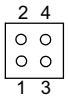
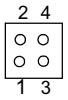
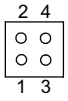
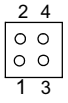
Jumpers

The module has three user-settable jumpers (J10, J18, and J20). Refer to Figure 7-1 for the location of these jumpers and to Table 7-2 for the jumper settings. The jumper can be set either on or off, which is represented in Table 7-2 as follows:



Set MCPIO-DPRC jumpers J10, J18, and J20 according to the requirements of your system, as indicated in Table 7-2.

Table 7-2. User-Settable Jumpers

Jumper	Purpose	Setting and Results
J10 	DPRB EEPROM boot Pins 1-2	Jumper off pins 1-2: The PCI-RapidIO bridge chip (DPRB) uses the contents of its boot EEPROM to initialize registers and route tables. (The default.) Jumper on pins 1-2: The DPRB loads registers from internal defaults.
J10 	RapidIO reset Pins 3-4	Jumper off pins 3-4: A backplane PCI reset propagates to a RapidIO fabric reset. (The default.)
J18 	Crossbar EEPROM boot Pins 1-2	Jumper off pins 1-2: Crossbar uses the contents of its boot EEPROM to initialize its registers. (The default.)
J18 	Module firmware write enable Pins 3-4	Jumper off pins 3-4: All carrier module and XMC module firmware and all on-board EEPROMs are write-protected. (The default.)

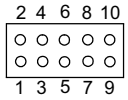
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Table 7-2. User-Settable Jumpers *(continued)*

Jumper	Purpose	Setting and Results
J20  	Interchassis reset input enable Pins 1-2	Jumper off pins 1-2: A received interchassis reset is accepted by the carrier module. (The default.) Jumper on pins 1-2: Received interchassis reset is ignored by the carrier module but is passed to interchassis reset output. Reset in at J6 reset connector; out at J7 connector to next chassis.
J20  	Loading of code to DPRB Pins 3-4	Jumper off pins 3-4: The DPRB (backplane PCI-to-RapidIO bridge) does not load its functional code when module is installed in a non-cPCI slot. (DPRB is non-operational.) (The default.) Jumper on pins 3-4: Primary DPRB loads its functional code when module is installed in a non-cPCI slot.

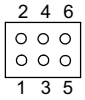
Table 7-3 shows the factory settings for jumpers J9, J17, and J27 (see Figure 7-1). These should not be changed; restore the factory settings if they have been altered.

Table 7-3. Factory Settings

Jumper	Factory Settings	Purpose
J9  	Jumpers off all pins.	Factory-use only.

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Table 7-3. Factory Settings *(continued)*

Jumper	Factory Settings	Purpose
J17 	Jumpers off all pins.	Factory-use only.
J27 	Jumpers off all pins.	Factory-use only.

Replacing a Module

Ejector handles on the front panel of the module apply the insertion force needed to disengage the module from the backplane or to seat and lock the module into position on the backplane.

- **To remove a module:**

  ➔ Disengage the board from the backplane by pulling the ejector handles outward (away from the center of the board).

- **To insert a module:**

  1. Position the module and slide it in to engage the backplane connectors, applying even pressure.
  2. Press the ejector handles inward, toward the center of the panel, to seat the board.

Caution: Be sure that the board is level and slides in straight. Clearance may be limited between board components and the front panel edges of adjacent boards. Use care as you slide the boards in.

Cabling Between Chassis

To connect one chassis to another, attach the serial cable (part number 070404) as follows:

- One end of the cable to the J7 connector on the MCPIO-DPRC module of the primary chassis

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- The other end to the J6 connector on the MCPIO-DPRC module of the secondary chassis

MCPIO-DPRC Configuration

The following sections provide configuration file directives used specifically for this device. For general information about creating configuration files and the meaning of the configuration directives, see the *Mercury System Manager's Guide.*

Board Directive

The board directive for the MCPIO-DPRC is:

```
board MCPIO_DPRC user-assigned-name [optional-attributes]
```

where:

user-assigned-name is a name assigned to the board by the user.

The optional attributes are:

`bus_number=number`

This specifies the CompactPCI bus segment occupied by the board. Use with `device_number`.

`device_number=number`

This specifies the CompactPCI device number of the board. Use with `bus_number`.

`disable_autoroutes=yes|no`

If set to no (the default), the entire fabric is configured for autorouting, which makes more effective use of the interconnect fabric. Use caution when changing this attribute. If it is set to `disable_autoroutes=yes`, no portion of the fabric is configured for autorouting.

`serial_number=number`

Specifies the serial number of the module. See the serial number label on the board. The `serial_number` and `bus_number`/`device_number` arguments are mutually exclusive.

`packet_prio_p=[0|1]`

Sets the RapidIO packet priority for packets originating from the MCPIO-DPRC module. The default is 0, the lowest priority.

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`byte_swap=[0|1]`

Specifies host endianness: little-endian (0) or big-endian (1). The default is little-endian (0).

Connect Directives

The connect directive for the MCPIO-DPRC is:

`connect` *`user-assigned-name1.connector1 user-assigned-name2.connector2`*

where:

`user-assigned-name1`
`user-assigned-name2`

are two names assigned by the user in a board directive, one for the MCPIO-DPRC module and the other for the hardware device to which it is connected, and

`connector1`
`connector2`

are two connectors, one a connector on the MCPIO-DPRC module, and the other a connector on the hardware device to which it is connected.

The MCPIO-DPRC connector can be:

`XMC_A` - Upper RapidIO XMC connector A (location J25)

`XMC_B` - Lower RapidIO XMC connector B (location J15)

`RAPIDIOJ4_A` – RapidIO link A on the upper portion of the J4 connector

`RAPIDIOJ4_B` - RapidIO link B on the lower portion of the J4 connector

`RAPIDIOJ5_A` – RapidIO link A on the upper portion of the J5 connector

`RAPIDIOJ5_B` - RapidIO link B on the lower portion of the J5 connector

`CPCI` - Standard CompactPCI connection on J1 and J2

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Cable Configuration

The serial reset cable used to connect one chassis to another connects two MPA1-I4B modules, each residing on an MCPIO-DPRC module. The reset cable requires the following configuration directives.

Board Directive

`board RAPIDIO_SERIAL_CABLE` *`user_assigned_name`*

where

`user_assigned_name`

is a name assigned by the user.

Connect Directive

`connect` *`user_assigned_name1.connector1 user_assigned_name2.connector2`*

where

`user_assigned_name1`
`user_assigned_name2`

are two names assigned by the user in two board directives: one for the cable and the other for the MPA1-I4B module it connects to.

`connector1`
`connector2`

are two connectors, one a connector on the cable and the other a connector on the MPA1-I4B module. The cable connector can be:

`RAPIDIOS_1` — one end of the cable

`RAPIDIOS_2` — the other end of the cable

MCPIO-DPRC Diagnostics

The diagnostic tool CheckMC supports the following test phase on the MCPIO-DPRC module:

Phase 3 - RapidIO fabric and hardware, including all crossbars on all boards and all links between crossbars.

Additional test phases depend on the hardware configuration. (See the device notes for the other devices in the system.)

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MCPIO-DPRC Reference

Address Space

None.

Files

The hardware description file for this device can be found at:

```
${MC_ROOT_DIR}/etc/desc/MCPIO_DPRC.desc
```


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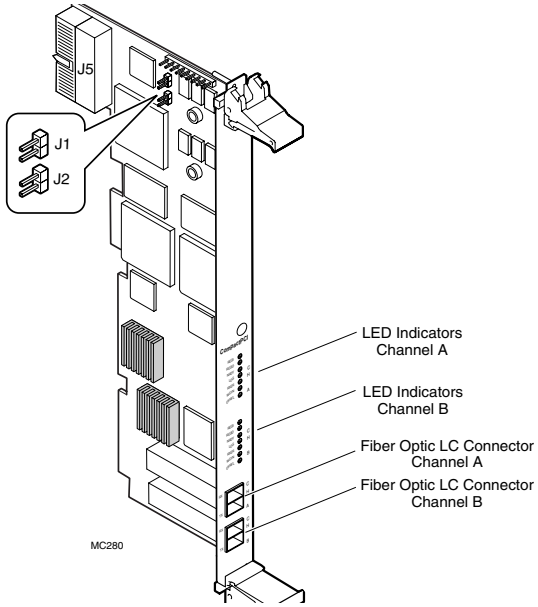
8

TIO-2FGR I/O Module

Overview

The TIO-2FGR module features dual 2.5 Gbaud fiber-optic I/O channels for sending and receiving streaming data. It provides an interface to the RapidIO fabric through a single 8-bit parallel RapidIO port on the CompactPCI J5 connector. The module is a CompactPCI rear transition card. The fiber-optic I/O stream uses the Serial FPDP protocol. Each channel can be independently set to operate at 2.5 Gbaud or 1.0625 Gbaud. Figure 8-1 shows the layout of the TIO-2FGR module and the location of the LED indicators and jumper blocks.

Figure 8-1. Layout and Jumpers of the TIO-2FGR Module



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LED Status Indicators

For each I/O channel on the TIO-2FGR module, a set of status indicators is visible through the front panel. The upper set of indicators is for channel A, the lower set for channel B. Figure 8-1 shows the location of the LED status indicators, and Figure 8-2 shows detail. Table 8-1 explains the meanings of the LED status indicators, which are identical for both channels.

Figure 8-2. LED Status Indicators

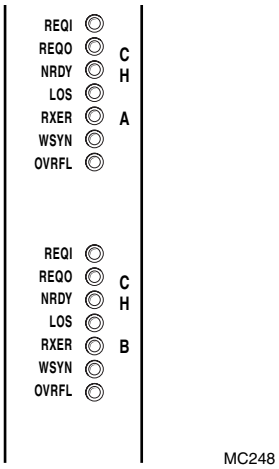


Table 8-1. LED Status Indicators

LED Label	Color	Indicator Meaning
REQI	Green	The RACEway REQ_I signal is asserted.[a]
REQO	Green	The RACEway REQ_O signal is asserted.[a]
NRDY	Yellow	The remote device is not ready.
LOS	Yellow	Loss of received signal from the fiber-optic channel input.
RXER	Yellow	A receive error has occurred.
WSYN	Yellow	Loss of word sync.
OVRFL	Yellow	The receive FIFO has overflowed.

a. An on-board RACEway connects the serial FPDP media interface to a bridge to RapidIO. For more information on RACEway signals, contact Mercury Computer Systems for a copy of the RACEway Interlink Functional Specification.

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Media EEPROM Default Settings

Effects of the factory settings for the TIO-2FGR media EEPROM are listed below. These are in effect when jumper J2 is out (see "Jumpers" on page 90).

- Transmit and receive mode with flow control.

  By default, input is disabled even though receive is enabled. The module receives data from the fiber but does not copy it to the receive FIFO. The application must perform a specific device setup action through the device driver to enable input.

- Baud rate is 2.5 Gbaud.
- Cyclic redundancy check (CRC) is enabled.
- Single beginning of frame (BOF) is enabled, multiple BOFs are disabled.
- Word sync filter is 133 ms.

TIO-2FGR Specifications

The physical, electrical, and compatibility specifications of the TIO-2FGR module are provided below.

Physical Dimensions

The physical dimensions of the module are:

- Overall dimensions (mm): 233 x 81 (9.2 x 3.2 in.)
- Weight (g): 222.3

Electrical Specifications

The electrical specifications of the module are:

- Input voltage (Vdc ±5%): 5.0
- Maximum theoretical power consumption (W at 5V): 19.0
- Typical power consumption (W at 5V): 13.0

Compatibility

The TIO-2FGR module can occupy a rear CompactPCI slot behind the following modules:

- MCP6-DPRB-3R bridge module
- MCP-P4K256R or MCP-P4K512R processor module

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Note: The TIO-2FGR module cannot connect physically to the MC4PK processor modules.

TIO-2FGR Installation

The following sections provide procedures for installing the jumpers on the TIO-2FGR module, for installing the module, and for making the fiber-optic connections. Recommendations for proper handling of the fiber-optic connectors are included.

Jumpers

The TIO-2FGR module has two jumper blocks (J1 and J2), shown in Figure 8-1. Table 8-2 lists the functions of the two jumpers.

The jumper blocks can be set either in or out, as shown in the following figure:

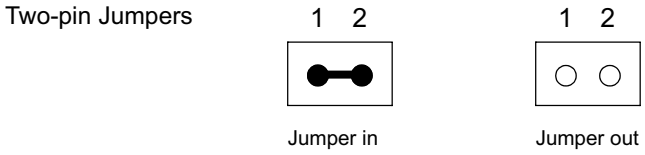


Table 8-2. Jumper Settings

Jumper	Purpose	Settings and Results
J1 	EEPROM Write Enable	Jumper out: Write-disable the media settings EEPROM. (Default) Jumper in: Write-enable the media settings EEPROM.
J2 	EEPROM Media Settings	Jumper out: The media settings stored in the media settings EEPROM are used as the initial device settings at power up or reset. (Default) Jumper in: Do not use the media settings stored in the media settings EEPROM.

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Assembly

Using even pressure, plug the module into the backplane.

The TIO-2FGR module uses fiber-optic cables. Because of the small diameter of the optical fiber, transceiver connections can be compromised by very small quantities of debris on the cable connector or within the socket. The transceivers are fitted with plastic plugs, and the cable connectors with plastic caps, to prevent contamination by debris when cables are not connected to the module.

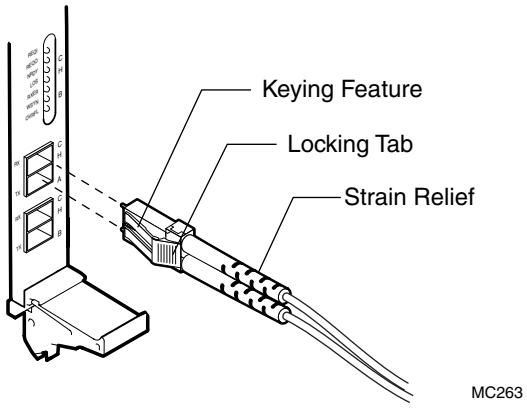
Caution: Do not remove plugs and caps until immediately prior to making the cable connections to the transceivers. Avoid touching the ends of the cable connectors whenever the protective cap is removed.

The following procedures describe how to connect and disconnect a fiber-optic cable.

- **To connect a fiber-optic cable:**

  1. Remove the protective plug from the transceiver and the caps from the cable connectors and store them in a dust-free container for later use.
  2. Align the keying features of the connector with the transceiver socket and insert the connector until the locking tab engages. (See Figure 8-3.)

Figure 8-3. Optical Cable Connector



- **To disconnect a fiber-optic cable:**

  1. Grasp the connector housing, squeeze the locking tab, and pull the cable connector out of the socket. (See Figure 8-3.)

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2. Install the plastic cap over the cable connector and install the plug in the transceiver socket.

TIO-2FGR Configuration

The following sections provide configuration file directives for this device. For guidance in creating a configuration file for the ImpactRT 3200S system, see Chapter 11. For general information about creating configuration files and the meaning of the configuration directives, see the *Mercury System Manager's Guide.*

Board Directive

The board directive for the TIO-2FGR module is:

`board TIO2FGR` *`user-assigned-name1`*

where:

`user-assigned-name1`

is a name assigned to the board by the user.

Connect Directive

The connect directive for the TIO-2FGR module is:

`connect` *`user-assigned-name1`*`.RAPIDIOJ5` *`user-assigned-name2.connector2`*

where:

`user-assigned-name1`

is a name assigned by the user in a board directive for the TIO-2FGR module,

`user-assigned-name2`

is a name assigned by the user in a board directive for the hardware to which the device is connected,

`RAPIDIOJ5`

is the J5 connector on the TIO-2FGR, and

`connector2`

is the connector on the board connected to the TIO-2FGR module.

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Device Directives

The device directives for the channels on the TIO-2FGR module are:

```
DEV user-assigned-name1.RIOJ_EP_A devid=n1 name=logical_name1
```

and

```
DEV user-assigned-name1.RIOJ_EP_B devid=n2 name=logical_name2
```

where:

`RIOJ_EP_A`

is the channel A device.

`RIOJ_EP_B`

is the channel B device.

TIO-2FGR Diagnostics

The diagnostic tool CheckMC supports the following test phase on the TIO-2FGR module:

Phase 2 - All I/O devices, including the MCP6-DPRB-3R bridge module

Additional test phases depend on the hardware configuration. (See the "Diagnostics" sections of the chapters for the other devices in the system.)

TIO-2FGR Reference

Address Space

Not Applicable

Files

The hardware description file for this device can be found at:

```
${MC_ROOT_DIR}/etc/desc/TIO2FGR.desc
```


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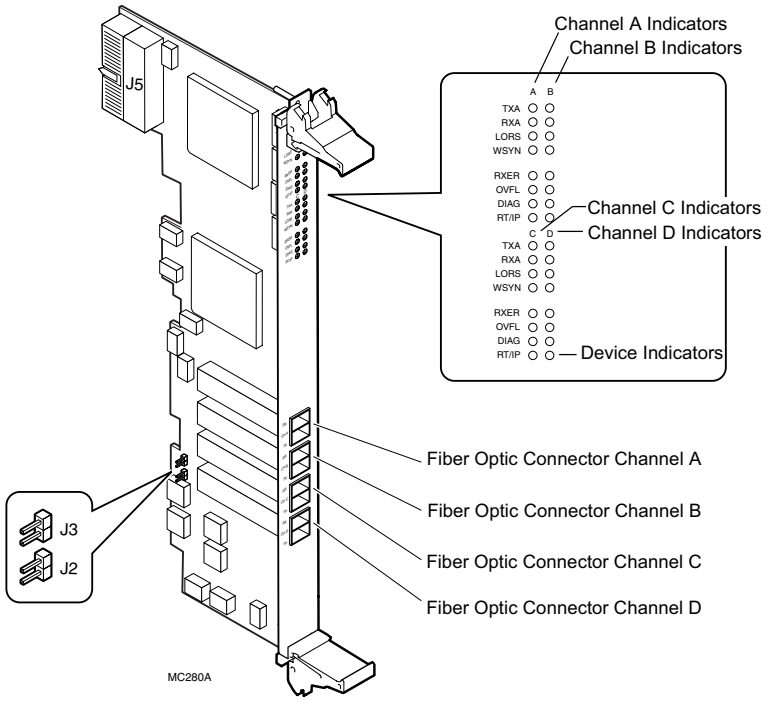
9

TIO-4FGD I/O Module

Overview

The TIO-4FGD I/O module provides a fiber-optic-to-RapidIO interface in a 6U, CompactPCI rear transition card format. The fiber-optic I/O stream uses the serial FPDP (front panel data port) protocol. Connector J5, indicators, and jumper blocks are shown in Figure 9-1.

Figure 9-1. TIO-4FGD Module Layout



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LED Status Indicators

For each pair of I/O channels on the TIO-4FGD module, a set of status indicators is visible through the front panel. The set at the top of the panel applies to channels A and B, the lower set to channels C and D. Figure 9-1 shows the location of the indicators, and Figure 9-2 shows a detailed view. Table 9-1 explains the meanings.

Figure 9-2. Front Panel Indicators

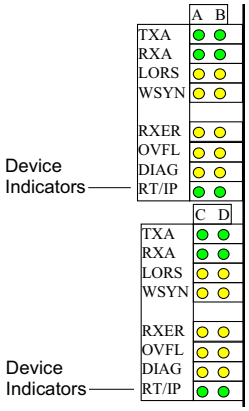


Table 9-1. Meanings of Status Indicators

Label	LED Color	Indicator Meaning
Channel Indicators		
TXA	Green	Signal transmission activity.
RXA	Green	Signal reception activity.
LORS	Yellow	Loss of received signal from the channel input.
WSYN	Yellow	Loss of word synchronization.
RXER	Yellow	Receive error.
OVRFL	Yellow	Receive FIFO has overflowed.

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Table 9-1. Meanings of Status Indicators *(continued)*

Label	LED Color	Indicator Meaning
DIAG	Yellow	Initial light: CheckMC™ diagnostics function is active. At successful completion, light goes off and diagnostics can be user controlled. If the indicator remains lit, diagnostics did not complete successfully.
Device Indicators		
RT	Green	2.5 Gbaud/sec rate selected. (If unlit, 1.065 Gbaud selected.)
IP	Green	RapidIO I/O initialized.

Switches

None.

TIO-4FGD Specifications

The physical, electrical, environmental, and compatibility specifications of the TIO-4FGD module are provided below.

Physical Dimensions

The physical dimensions of the module are:

- Overall dimensions (mm): 233 x 81 (9.2 x 3.2 in.)
- Weight (g): 274

Electrical Specifications

The electrical specifications of the module are:

- Input voltage (Vdc ±5%): 5.0
- Maximum theoretical power consumption (W at 5V): 17.3
- Typical power consumption (W at 5V): 13.1

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Compatibility

The TIO-4FGD I/O module can occupy a rear CompactPCI slot behind the MC4PK processor modules, communicating through the J5 connector.

Note: The TIO-4FGD module cannot be used with the MCP-P4K256R or the MCP-P4K512R module.

TIO-4FGD Installation

The following sections provide procedures for setting the jumpers on the TIO-4FGD module, for installing it, and for making the fiber-optic connections. Recommendations for proper handling of the fiber-optic connectors are included.

Jumpers

The TIO-4FGD module has two jumper blocks (J2 and J3), shown in Figure 9-1. Table 9-2 lists the functions of the jumpers.

The jumper blocks can be set either in or out, as shown in the following figure:

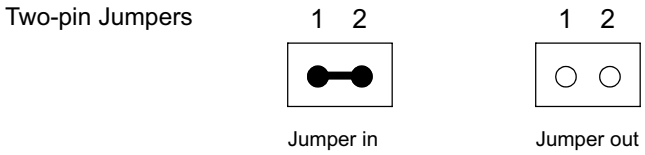


Table 9-2. Jumper Settings

Jumper	Purpose	Settings and Results
J2 	EEPROM Load Settings	Jumper out: The settings stored in the FPGA serial EEPROMs are used as the initial device settings at power up or reset. (Default) Jumper in: The settings stored in the EEPROMs are not in effect.
J3 	EEPROM Write Enable	Jumper out: Write-disables the FPGA serial EEPROM for each pair of channels. (Default) Jumper in: Write-enables the EEPROM for each pair of channels.

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EEPROM Default Settings

Factory settings for the TIO-4FGD FPGA serial EEPROMs (in effect when jumper J2 is out) include:

- Transmit and receive mode with flow control

  By default, input is disabled even though receive is enabled. The module receives data from the fiber but does not copy it to the receive FIFO. The application must perform a specific device setup action through the device driver to enable input.

- Baud rate of 2.5 Gbaud
- Cyclic redundancy check (CRC) enabled
- Single beginning of frame (BOF) enabled; multiple BOFs disabled
- Word sync filter: 133 ms

Assembly

Using even pressure, plug the module into the backplane.

The TIO-4FGD module uses fiber-optic cables. Because of the small diameter of the optical fiber, transceiver connections can be compromised by very small quantities of debris on the cable connector or within the socket. The transceivers are fitted with plastic plugs, and the cable connectors with plastic caps, to prevent contamination by debris when cables are not connected to the module.

Caution: Do not remove plugs and caps until immediately prior to making the cable connections to the transceivers. Avoid touching the ends of the cable connectors whenever the protective cap is removed.

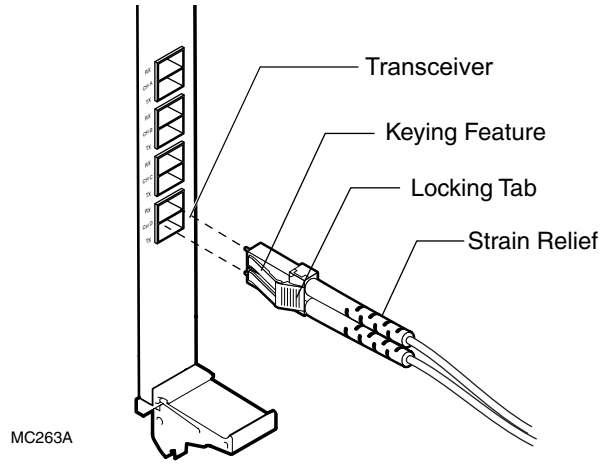
The following procedures describe how to connect and disconnect a fiber-optic cable. (See Figure 9-3.)

■ **To connect a fiber-optic cable to the module:**

1. Remove the protective plug from the transceiver and the cap from the cable connector, and store them in a dust-free container for later use.
2. Align the keying features of the cable connector with the transceiver socket and insert the connector until the locking tab engages, as shown in Figure 9-3.

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Figure 9-3. Optical Cable Connector



- **To disconnect a fiber-optic cable from the module:**

  1. Grasp the cable connector, squeeze the locking tab, and pull the cable connector out of the transceiver socket. (See Figure 9-3.)
  2. Install the plastic cap over the cable connector and install the plug in the transceiver socket.

TIO-4FGD Configuration

The following sections provide configuration file directives for this device. For general information about creating configuration files and the meaning of the configuration directives, see the *Mercury System Manager's Guide.*

Board Directive

The board directive for the TIO-4FGD module is:

`board TIO4FGD` *`user-assigned-name1`*

where:

`user-assigned-name1`

is a name assigned to the board by the user.

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The optional attributes are:

`num_status_words=`*`number`*

Specifies the number of status words to allocate. The default value is 2500.

`num_chain_lut_entries=`*`number`*

Specifies the number of LUT entries to reserve. The default value is 1024.

`verbose_level=[0|1]`

Sets verbosity. To enable verbosity, set to `1`. The default is `0`, disabled.

`timeout=`*`number`*

Specifies the initial timeout value in msec (`0` = none).

Connect Directive

The connect directives for the TIO-4FGD module are:

`connect` *`user-assigned-name1`*`.RAPIDIOJ5_A` *`user-assigned-name2.connector`*

and

`connect` *`user-assigned-name1`*`.RAPIDIOJ5_B` *`user-assigned-name2.connector`*

where:

`user-assigned-name1`

is a name assigned by the user in a board directive for the TIO-4FGD module,

`user-assigned-name2`

is a name assigned by the user in a board directive for the hardware to which the device is connected,

`RAPIDIOJ5_A`

is the upper port on the TIO-4FGD module's J5 connector,

`RAPIDIOJ5_B`

is the lower port on the TIO-4FGD module's J5 connector,

`connector`

is the connector on the device connected to the TIO-4FGD module.

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Device Directives

The device directives for the channels on the TIO-4FGD module are:

`DEV` *`user-assigned-name1`*`.D25RTIO_A devid=n1 name=logical_name1`

and

`DEV` *`user-assigned-name1`*`.D25RTIO_B devid=n2 name=logical_name2`

where:

`D25RTIO_A`

is the channel A device;

`D25RTIO_B`

is the channel B device;

`D25RTIO_C`

is the channel C device;

`D25RTIO_D`

is the channel D device.

Configuration File Example

```
board CPCI_SBC_NO_BUS host memory_defs="MEM_SIZE 0xA00000 SLAVE_ADDR0 0x0
PUBLIC 0"
board CPCIBUS pci_bp

rio_defs="transport_mode=auto disable_autoroutes=no dump_xbars=no"

board MCP6_DPRB_3R dprb bus_number=1 device_number=15 $(rio_defs)

connect host.CPCI pci_bp.CPCI_6
connect dprb.CPCI pci_bp.CPCI_5

board CPDLK5R dlk5 $(rio_defs)

board MC4PK512H_D1 mb1 $(rio_defs)

connect mb1.RAPIDIOJ4_A dlk5.RAPIDIOJ4_3A
connect mb1.RAPIDIOJ4_B dlk5.RAPIDIOJ4_3B
```


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```
connect dprb.RAPIDIOJ4_A dlk5.RAPIDIOJ4_5A
connect dprb.RAPIDIOJ4_B dlk5.RAPIDIOJ4_5B

CE host.SBC host=1 ce_type=CE_HOST ceid=1

CE mb1.CPU_A ce_type=CE_PRAPIDIO
CE mb1.CPU_B ce_type=CE_PRAPIDIO
CE mb1.CPU_C ce_type=CE_PRAPIDIO
CE mb1.CPU_D ce_type=CE_PRAPIDIO

# TIO quad channel board directives & connections
board TIO4FGD tio
connect tio.RAPIDIOJ5_A mb1.RAPIDIOJ5_A
connect tio.RAPIDIOJ5_B mb1.RAPIDIOJ5_B

DEV tio.D25RTIO_A devid=1 name=SIO_1
DEV tio.D25RTIO_B devid=2 name=SIO_2
DEV tio.D25RTIO_C devid=3 name=SIO_3
DEV tio.D25RTIO_D devid=4 name=SIO_4
```

TIO-4FGD Diagnostics

The diagnostic tool CheckMC supports the following test phase on the TIO-4FGD module:

Phase 2 - All I/O devices

Additional test phases depend on the hardware configuration. (See the device notes for the other devices in the system.)

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TIO-4FGD Reference

Address Space

Not Applicable.

Files

The hardware description file for this device can be found at:

```
${MC_ROOT_DIR}/etc/desc/TIO4FGD.desc
```


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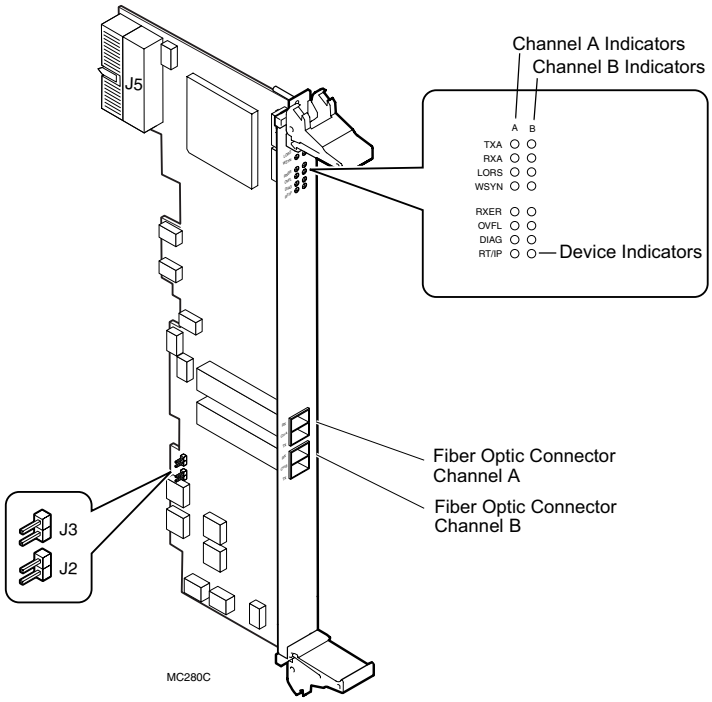
10

TIO-2FGD I/O Module

Overview

The TIO-2FGD two-channel I/O module, a variation of the TIO-4FGD four-channel module, provides a fiber-optic-to-RapidIO interface in a 6U, CompactPCI rear transition card format. Figure 10-1 shows connector J5, indicators, and jumpers.

Figure 10-1. TIO-2FGD Module Layout



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Two fiber-optic channels send and receive streaming data and can be set to operate at 2.5 or 1.0625 Gbaud. Two 8-bit, parallel RapidIO ports on the J5 connector provide an interface to the RapidIO fabric. The fiber-optic I/O stream uses the serial FPDP (front panel data port) protocol.

LED Status Indicators

Status indicators are visible through the front panel. Figure 10-1 shows the location of the indicators, and Figure 10-2 shows a detailed view. Table 10-1 explains the meanings of the status indicators for the device and for channels A and B.

Figure 10-2. Status Indicators

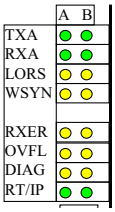


Table 10-1. Meanings of Status Indicators

Label	LED Color	Indicator Meaning
Channel Indicators		
TXA	Green	Signal transmission activity.
RXA	Green	Signal reception activity.
LORS	Yellow	Loss of received signal from the channel input.
WSYN	Yellow	Loss of word synchronization.
RXER	Yellow	Receive error.
OVRFL	Yellow	Receive FIFO has overflowed.
DIAG	Yellow	Initial light: CheckMC™ diagnostics function is active. At successful completion, light goes off and diagnostics can be user controlled. If indicator remains lit, diagnostics did not complete successfully.

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Table 10-1. Meanings of Status Indicators *(continued)*

Label	LED Color	Indicator Meaning
Device Indicators		
RT	Green	2.5 Gbaud/sec rate selected. (If unlit, 1.065 Gbaud selected.)
IP	Green	RapidIO I/O initialized.

Switches

None.

TIO-2FGD Specifications

The physical, electrical, environmental, and compatibility specifications of the TIO-2FGD module are provided below.

Physical Dimensions

The physical dimensions of the module are:

- Overall dimensions (mm): 233 x 81 (9.2 x 3.2 in.)
- Weight (g): 236

Electrical Specifications

The electrical specifications of the module are:

- Input voltage (Vdc ±5%): 5.0
- Maximum theoretical power consumption (W at 5V): 10.5
- Typical power consumption (W at 5V): 6.78

Compatibility

The TIO-2FGD I/O module can occupy a rear CompactPCI slot behind the MC4PK processor modules, communicating through the J5 connector.

Note: The TIO-2FGD module cannot be used with the MCP-P4K256R or the MCP-P4K512R module.

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TIO-2FGD Installation

The following sections provide procedures for setting the jumpers on the TIO-2FGD module, for installing it, and for making the fiber-optic connections. Recommendations for proper handling of the fiber-optic connectors are included.

Jumpers

The TIO-2FGD module has two jumper blocks (J2 and J3), shown in Figure 10-1. Table 10-2 lists the functions of the jumpers.

The jumper blocks can be set either in or out, as shown in the following figure:

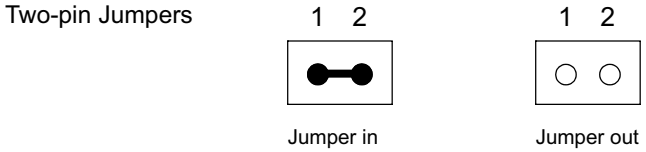


Table 10-2. Jumper Settings

Jumper	Purpose	Settings and Results
J2 	EEPROM Load Settings	Jumper out: The settings stored in the FPGA serial EEPROM are used as the initial device settings at power up or reset. (Default) Jumper in: The settings stored in the EEPROM are not in effect.
J3 	EEPROM Write Enable	Jumper out: Write-disables the FPGA serial EEPROM. (Default) Jumper in: Write-enables the EEPROM.

EEPROM Default Settings

Factory settings for the TIO-2FGD FPGA serial EEPROM (in effect when jumper J2 is out) include:

- Transmit and receive mode with flow control

  By default, input is disabled even though receive is enabled. The module receives data from the fiber but does not copy it to the receive FIFO. The

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application must perform a specific device setup action through the device driver to enable input.

- Baud rate of 2.5 Gbaud
- Cyclic redundancy check (CRC) enabled
- Single beginning of frame (BOF) enabled; multiple BOFs disabled
- Word sync filter: 133 ms

Assembly

Using even pressure, plug the module into the backplane.

The TIO-2FGD module uses fiber-optic cables. Because of the small diameter of the optical fiber, transceiver connections can be compromised by very small quantities of debris on the cable connector or within the socket. The transceivers are fitted with plastic plugs, and the cable connectors with plastic caps, to prevent contamination by debris when cables are not connected to the module.

Caution: Do not remove plugs and caps until immediately prior to making the cable connections to the transceivers. Avoid touching the ends of the cable connectors whenever the protective cap is removed.

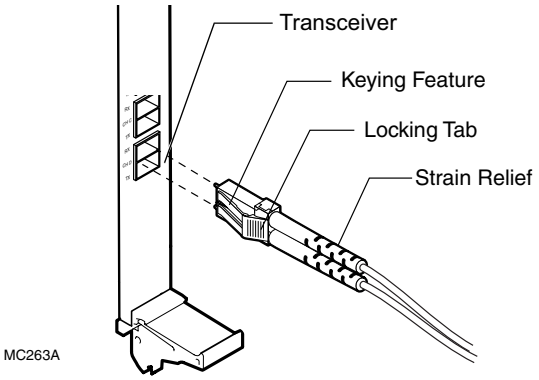
The following procedures describe how to connect and disconnect a fiber-optic cable. (See Figure 10-3.)

■ **To connect a fiber-optic cable to the module:**

1. Remove the protective plug from the transceiver and the cap from the cable connector, and store them in a dust-free container for later use.
2. Align the keying features of the connector with the transceiver socket and insert the connector until the locking tab engages. (See Figure 10-3.)

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Figure 10-3. Optical Cable Connector



- **To disconnect a fiber-optic cable from the module:**

  1. Grasp the cable connector, squeeze the locking tab, and pull the cable connector out of the transceiver socket. (See Figure 10-3.)
  2. Install the plastic cap over the cable connector and install the plug in the transceiver socket.

TIO-2FGD Configuration

The following sections provide configuration file directives for this device. For general information about creating configuration files and the meaning of the configuration directives, see the *Mercury System Manager's Guide*.

Board Directive

The board directive for the TIO-2FGD module is:

board TIO2FGD *user-assigned-name1*

where:

user-assigned-name1

is a name assigned to the board by the user.

The optional attributes are:

num_status_words=*number*

Specifies the number of status words to allocate. The default value is 2500.

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`num_chain_lut_entries=`*`number`*

Specifies the number of LUT entries to reserve. The default value is 1024.

`verbose_level=[0|1]`

Sets verbosity. To enable verbosity, set to `1`. The default is `0`, disabled.

`timeout=`*`number`*

Specifies the initial timeout value in msec (`0` = none).

Connect Directive

The connect directive for the TIO-2FGD module is:

`connect` *`user-assigned-name1`*`.RAPIDIOJ5` *`user-assigned-name2.connector`*

where:

`user-assigned-name1`

is a name assigned by the user in a board directive for the TIO-2FGD module,

`user-assigned-name2`

is a name assigned by the user in a board directive for the hardware to which the device is connected,

`RAPIDIOJ5`

is the J5 connector on the TIO-2FGD, and

`connector`

is the connector on the board connected to the TIO-2FGD module.

Device Directives

The device directives for the channels on the TIO-2FGD module are:

`DEV` *`user-assigned-name1`*`.D25RTIO_A devid=n1 name=logical_name1`

and

`DEV` *`user-assigned-name1`*`.D25RTIO_B devid=n2 name=logical_name2`

where:

`D25RTIO_A`

is the channel A device;

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D25RTIO_B

is the channel B device.

Configuration File Example

```
board CPCI_SBC_NO_BUS host memory_defs="MEM_SIZE 0xA00000 SLAVE_ADDR0 0x0
PUBLIC 0"
board CPCIBUS pci_bp

rio_defs="transport_mode=auto disable_autoroutes=no dump_xbars=no"

board MCP6_DPRB_3R dprb bus_number=1 device_number=15 $(rio_defs)

connect host.CPCI pci_bp.CPCI_6
connect dprb.CPCI pci_bp.CPCI_5

board CPDLK5R dlk5 $(rio_defs)

board MC4PK512H_D1 mb1 $(rio_defs)

connect mb1.RAPIDIOJ4_A dlk5.RAPIDIOJ4_3A
connect mb1.RAPIDIOJ4_B dlk5.RAPIDIOJ4_3B
connect dprb.RAPIDIOJ4_A dlk5.RAPIDIOJ4_5A
connect dprb.RAPIDIOJ4_B dlk5.RAPIDIOJ4_5B

CE host.SBC host=1 ce_type=CE_HOST ceid=1

CE mb1.CPU_A ce_type=CE_PRAPIDIO
CE mb1.CPU_B ce_type=CE_PRAPIDIO
CE mb1.CPU_C ce_type=CE_PRAPIDIO
CE mb1.CPU_D ce_type=CE_PRAPIDIO

# TIO dual channel board directives & connections
board TIO2FGD tio
connect tio.RAPIDIOJ5 mb1.RAPIDIOJ5_A

DEV tio.D25RTIO_A devid=1 name=SIO_1
```


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```
DEV tio.D25RTIO_B devid=2 name=SIO_2
```

TIO-2FGD Diagnostics

The diagnostic tool CheckMC supports the following test phase on the TIO-2FGD module:

Phase 2 - All I/O devices

Additional test phases depend on the hardware configuration. (See the device notes for the other devices in the system.)

TIO-2FGD Reference

Address Space

Not Applicable.

Files

The hardware description file for this device can be found at:

```
${MC_ROOT_DIR}/etc/desc/TIO2FGD.desc
```


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11

Configuration Guidelines

Configuring Hardware

Major reconfiguration of the ImpactRT 3200S system modules is generally unnecessary. In cases where board placement decisions need to be made, however, follow the guidelines in this chapter. Table 11-1 provides guidelines for configuring Mercury modules in the ImpactRT 3200S 21-slot card cage.

In general, the MCP6-DPRB-3R or MCPIO-DPRC bridge module must be installed in slot 19 or 20 for connectivity for the host. Optionally, additional bridge modules can be installed in any of slots 1 through 18 to allow use of an I/O module without a processing board in the front slot.

Note: The TIO-2FGD or TIO-4FGD modules can occupy a rear slot behind MC4PK processing modules only. The TIO-2FGR module can occupy a rear slot behind MCP-P4K processing modules only. The TIO-2FGR module can also occupy a slot behind an MCP6-DPRB bridge module; a TIO-2FGD or TIO-4FGD module can occupy a slot behind an MCPIO-DPRC bridge module.

Table 11-1. ImpactRT 3200S Slot Placement Guidelines

Slot No.	MCP-P4K Processors	MCP6-DPRB Bridge	MCPIO-DPRC Bridge	Host
1	Yes	No	No	No
2	Yes	No	No	No
3	Yes	No	No	No
4	Yes	No	No	No
5	Yes	No	No	No

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Table 11-1. ImpactRT 3200S Slot Placement Guidelines *(continued)*

Slot No.	MCP-P4K Processors	MCP6-DPRB Bridge	MCPIO-DPRC Bridge	Host
6	Yes	No	No	No
7	Yes	No	No	No
8	Yes	No	No	No
9	Yes	No	No	No
10	Yes	No	No	No
11	Yes	No	No	No
12	Yes	No	No	No
13	Yes	No	No	No
14	Yes	No	No	No
15	Yes	No	No	No
16	Yes	No	No	No
17	Yes	No	No	No
18	Yes	No	No	No
19	Yes	Yes	Yes	No
20	No	Yes	Yes	No
21	No	No	No	Yes

Configuring Software

Whenever you move, add, or remove a board or daughter card, you must also update the system configuration file, which describes all hardware elements that function as parts of your multicomputer and all connections among the elements. The Mercury configuration utility (`configmc`) uses the configuration file to establish a configuration database, which is used by the MCOE operating system and by runtime utilities to allocate resources and establish routes between processors and other system devices. The configuration file carries a `.cfg` extension and is located in the following MCOE directory:

```
${MC_ROOT_DIR}/etc
```

The configuration file describes the hardware by defining discrete modules, each commonly referred to as a *board,* which contain at least one of the following system components:

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- Host computer
- Compute nodes
- All other devices, including bulk memories
- Buses and other interconnect fabrics
- Any bridge modules that join buses or interconnects

The configuration file specifies the hardware configuration using two types of directives:

- **`board`** directives identify each hardware module (board) in the system.
- **`connect`** directives specify how the hardware modules are interconnected by naming two mating connectors.

In addition to identifying physical elements, the configuration file defines the logical configuration of programmable elements, which have names and other attributes that allow them to be accessed and used by software applications. The configuration file includes two types of logical directives:

- **`CE`** and **`DEV`** directives identify programmable elements that reside on the hardware modules

Mercury's configuration tool, `configmc`, processes the configuration file, creates configuration databases from it, and supplies these databases to the host kernel. Mercury's boot tool, `sysmc`, supplies the configuration databases to the other elements of the multicomputer.

The MCOE operating environment software includes a specific vocabulary of module names that must be used to identify the hardware elements of a system. These names are derived from the names of board description files. Every type of hardware module in a Mercury multicomputer requires an associated board description file, always located in the following MCOE directory:

```
${MC_ROOT_DIR}/etc/desc
```

The board description file specifies the components of a hardware module, their default physical characteristics, how they connect to one another, and any potential connections to other modules. Together, the board description file and the configuration file completely describe the system hardware architecture. The default characteristics in the board description file can be overridden by specific attributes included in the configuration file.

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Creating an ImpactRT 3200S Configuration File

The goals in generating configuration file directives for the ImpactRT 3200S system are, in overview:

1. Describe the system hardware (board and connect directives).
2. Define logical programmable components of the system (CE and DEV directives).

Describing the System Hardware

To describe system hardware modules, the directives in the configuration file must use the names shown in Table 11-2.

Table 11-2. ImpactRT 3200S System Modules and Names

Name in Configuration File	System Hardware Module
`CPCI_SBC_NO_BUS`	CompactPCI-resident single-board computer. The description file `CPCI_SBC_NO_BUS.desc` represents a generic CompactPCI-resident single-board computer (`CPCI_SBC`); . The `NO_BUS` in the module name indicates that the module itself does not contain any relevant segment of the CompactPCI bus. Instead, the module must be connected to another module named `CPCIBUS`.
`CPCIBUS`	CompactPCI bus segment on which the SBC resides. The description file `CPCIBUS.desc` represents the CompactPCI bus embedded in the chassis midplane. Although the bus segment is not an identifiable, removable module, it must be called out in the configuration file. In the chassis, the CompactPCI bus of interest covers only the right-most three slots of the chassis. Although the chassis numbers these slots 19, 20, and 21, they are considered slots 1, 2, and 3 of the bus segment designated by `CPCIBUS`.

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Table 11-2. ImpactRT 3200S System Modules and Names *(continued)*

Name in Configuration File	System Hardware Module
CPDLK20R	RapidIO crossbar fabric in the chassis midplane. The description file CPDLK20R.desc describes the active RapidIO interconnect fabric embedded in the chassis midplane. Although the CPDLK20R module is not an identifiable, removable module, the crossbar fabric must be called out in the configuration file. The CPDLK20R module covers 20 consecutive slots in the midplane, numbered 1 to 20 from left to right. These correspond to the numbered chassis slots 1 to 20. Each slot has two distinct RapidIO connections. For details, see "Configuration File Directives for the CPDLK20R Module" on page 123.
CPDLK10R	The CPDLK10R module covers 10 consecutive slots in the midplane, numbered 1 to 10 from left to right. These correspond to the numbered chassis slots 1 to 10. Each slot has two distinct RapidIO connections.
CPDLK5R	The CPDLK5R module covers 5 consecutive slots in the midplane, numbered 1 to 5 from left to right. These correspond to the numbered chassis slots 1 to 5. Each slot has two distinct RapidIO connections.
MCP_P4K512R	Four-node RapidIO-resident processing board. (See Chapter 5.)
MC4PK512H_D1	Four-node RapidIO-resident processing board. (See Chapter 4.)
MCP6_DPRB_3R	Bridge module from the host's CompactPCI bus to the RapidIO fabric. (See Chapter 6.)
MCPIO_DPRC	Bridge module from the host's CompactPCI bus to the RapidIO fabric. (See Chapter 7.)
TIO2FGR	Dual-channel fiber-optic I/O module in the rear area of the chassis. (See Chapter 8.)
TIO4FGD	Four-channel fiber-optic I/O module in the rear area of the chassis. (See Chapter 9.)
TIO2FGD	Two-channel fiber-optic I/O module in the rear area of the chassis. (See Chapter 9.)

The following sections provide example configuration file directives to define ImpactRT 3200S system components.

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Defining the Host and CPCI Bus: The first two of the following directives define the host SBC and the segment of CompactPCI bus it resides on; the third connects the SBC to the bus:

```
board CPCI_SBC_NO_BUS host
board CPCIBUS pci_bp
connect host.CPCI pci_bp.CPCI_3
```

Note that the CompactPCI bus segment is only three slots wide and covers chassis slots 19, 20, and 21. The `CPCIBUS` module has three defined connections: `CPCI_1`, `CPCI_2`, and `CPCI_3`. Since the host SBC is in chassis slot 21, which corresponds to the third connection of the `CPCIBUS` module, the `connect` directive specifies `CPCI_3`.

Defining the PCI-to-RapidIO Bridge and Midplane RapidIO Fabric: The first of the following directives defines the bridge module that connects PCI to RapidIO; the second defines the midplane RapidIO fabric:

```
board MCP6_DPRB_3R dprb bus_number=1 device_number=15
board CPDLK20R dlk20
```

The `bus_number=1` and `device_number=15` attributes apply to an MCP6-DPRB `module` mounted in slot 20. If the board, or another such board, is mounted in slot 19, different `bus_number` and `device_number` values apply. After mounting the board in slot 19, run `configmc scan_pci` to obtain the applicable `bus_number` and `device_number` values, as described in the *Mercury System Manager's Guide*.

The following directives connect the bridge module to the two fabrics, PCI and RapidIO, enabling the module to perform its bridging function:

```
connect dprb.CPCI pci_bp.CPCI_2
connect dprb.RAPIDIOJ4_A dlk20.RAPIDIOJ4_20A
connect dprb.RAPIDIOJ4_B dlk20.RAPIDIOJ4_20B
```

Since the MCP6-DPRB module is in chassis slot 20, which is the second slot of the CompactPCI bus segment, the directive indicates `CPCI_2`. Similarly, since chassis slot 20 corresponds to slot 20 on the CPDLK20R module, the bridge module connection is to `RAPIDIOJ4_20A(B)`. Only one connection exists to CompactPCI, but two connections exist to RapidIO. The directives call out both of these connections, using the `A` and `B` suffixes.

Defining Processor Modules and Connections to Midplane: The following directives define one processor module and connect it to the RapidIO midplane

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fabric. The defined module occupies chassis slot 3, the third slot from the left (viewing the midplane from the front).

```
board MCP_P4K512R proc_mod3
connect proc_mod3.RAPIDIOJ4_A dlk20.RAPIDIOJ4_3A
connect proc_mod3.RAPIDIOJ4_B dlk20.RAPIDIOJ4_3B
```

Again, note that you must call out both the A and B connections to RapidIO.The configuration file must contain additional directives, similar to the preceding, that define all other processor modules in the system and their connections to the RapidIO midplane fabric.

Defining Fiber-Optic I/O Modules and Their Connections: The final step in describing the hardware is to define one or more fiber-optic I/O modules, plus their connections. These I/O modules occupy the rear transition area of the CompactPCI chassis. Although they appear to connect to the midplane, in fact, they plug into pass-through pins that go directly to the front of the chassis, where a processing module or a bridge `(DPRB)` module must be installed to service each I/O module.

The following directives define the I/O module that occupies chassis slot 3, which, from a rear view is the third slot from the right—the same slot that contains the processing module defined in the preceding directives.

```
board TIO2FGR tio3
connect tio3.RAPIDIOJ5 proc_mod3.RAPIDIOJ5
```

The configuration file must contain additional directives, similar to the preceding, that represent all other fiber-optic I/O modules and their connections to the corresponding modules installed in the front of the chassis.

Defining Logical Programmable Components

Besides describing hardware components, the configuration file identifies the programmable elements residing on the hardware modules. The programmable elements are either compute environments (CEs) or other devices and are identified in the configuration file by the `CE` and `DEV` directives.

Defining the Host CE: The host SBC contains a single CE, which functions as the runtime host. The board directive in "Defining the Host and CPCI Bus" on page 120 defines a `CPCI_SBC_NO_BUS` module, giving it the name `host`. This module has a single programmable element on it, called `SBC`, which can be referred to by a CE directive. In this directive, `host.SBC` refers to that particular element on that particular board.

The following CE directive defines `host.SBC` as the host CE:

```
CE host.SBC host=1 ceid=1
```


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The host=1 attribute specifies that host.SBC is the host CE. MCOE requires the host CE to have a CEID of 1. The ceid=1 attribute makes this assignment.

Defining Other CEs: Each processor module contains four PowerPC® CPUs, each of which can be referenced by a CE directive. The four CPUs are called CPU_A, CPU_B, CPU_C, and CPU_D. The following directives define the four CEs on the processor module called proc_mod3, which was specified in the board directive in "Defining the Host and CPCI Bus" on page 120.

```
CE proc_mod3.CPU_A
CE proc_mod3.CPU_B
CE proc_mod3.CPU_C
CE proc_mod3.CPU_D
```

These directives allow the system to assign default CEIDs to the four CEs. You can use additional CE directive attributes to specify CEIDs explicitly, and assign names to CEs, as described in the *Mercury System Manager's Guide*.

Defining Fiber-Optic Channels: Each TIO-2FGR fiber-optic I/O module contains two independent fiber-optic I/O channels. Each channel can be defined as a programmable device. The two channels on the board are called RIOJ_EP_A and RIOJ_EP_B. The next two directives define the two devices on the fiber-optic I/O module called tio3, which was specified in "Defining Fiber-Optic I/O Modules and Their Connections" on page 121.

```
DEV tio3.RIOJ_EP_A devid=1 name=RINOJ_1
DEV tio3.RIOJ_EP_B devid=2 name=RINOJ_2
```

Note that, unlike a CE directive, a DEV directive requires that you assign both a device ID and a name to a device. The device ID and the name must be unique.

Defining Shared Memory on the Host SBC: Your application may need to define memory on the host SBC that is accessible to the other compute nodes in the system. The board directive shown in "Defining the Host and CPCI Bus" on page 120 did not define any such memory:

```
board CPCI_SBC_NO_BUS host
```

You can use optional attributes to the host's board directive to define host memory that is accessible to other CEs. The following example sets aside 10 Mbytes (0xA00000 bytes) of host memory that is visible to RapidIO-resident compute nodes:

```
board CPCI_SBC_NO_BUS host memory_defs="MEM_SIZE 0xA00000
SLAVE_ADDR0 0x0 PUBLIC 0"
```

Like all configuration file directives, this directive must be entered as a single line, or must contain a back slash character ('\') immediately before any line break.

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Additional Directives

The board, connect, CE, and DEV directive examples in the preceding section, "Creating an ImpactRT 3200S Configuration File," cover the host SBC, the CPCI bus segment of the midplane, as well as the processing, bridge, and I/O modules for the ImpactRT 3200S system. Additional directives for the RapidIO crossbar fabric in the midplane (CPDLK20R module) are covered in the next section. A complete sample configuration file for the ImpactRT 3200S system exists in the following directory:

```
${MC_ROOT_DIR}/examples/config
```

Configuration File Directives for the CPDLK20R Module

Configuration file directives in this section are specific to the RapidIO crossbar fabric in the midplane (CPDLK20R module).

Board Directive: The board directive for the CPDLK20R module is:

```
board CPDLK20R user-assigned-name [disable_autoroutes=yes|no]
```

user-assigned-name

A name assigned to the board by the user.

disable_autoroutes=yes|no

Disables autorouting if specified with yes. If specified with no (the default) or omitted, autorouting is enabled.

Connect Directive: The connect directive for the CPDLK20R module is:

```
connect user-assigned-name1.connector1 user-assigned-name2.connector2
```

user-assigned-name1
user-assigned-name2

Two names assigned by the user in a board directive, one for the CPDLK20R module and the other for the hardware device connected to the CPDLK20R module.

connector1
connector2

Two connectors, one a connector on the CPDLK20R module and the other a connector on the hardware device connected to the CPDLK20R module.

The CPDLK20R module has 20 double connections to 20 contiguous CompactPCI midplane slots. Table 11-3 shows the CPDLK20R connector names.

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Table 11-3. CPDLK20R Connector Names

Connector Name	Connector Description
RAPIDIOJ4_1A	The upper slot 1 J4 connection
RAPIDIOJ4_1B	The lower slot 1 J4 connection
RAPIDIOJ4_2A	The upper slot 2 J4 connection
RAPIDIOJ4_2B	The lower slot 2 J4 connection
RAPIDIOJ4_3A	The upper slot 3 J4 connection
RAPIDIOJ4_3B	The lower slot 3 J4 connection
RAPIDIOJ4_4A	The upper slot 4 J4 connection
RAPIDIOJ4_4B	The lower slot 4 J4 connection
RAPIDIOJ4_5A	The upper slot 5 J4 connection
RAPIDIOJ4_5B	The lower slot 5 J4 connection
RAPIDIOJ4_6A	The upper slot 6 J4 connection
RAPIDIOJ4_6B	The lower slot 6 J4 connection
RAPIDIOJ4_7A	The upper slot 7 J4 connection
RAPIDIOJ4_7B	The lower slot 7 J4 connection
RAPIDIOJ4_8A	The upper slot 8 J4 connection
RAPIDIOJ4_8B	The lower slot 8 J4 connection
RAPIDIOJ4_9A	The upper slot 9 J4 connection
RAPIDIOJ4_9B	The lower slot 9 J4 connection
RAPIDIOJ4_10A	The upper slot 10 J4 connection
RAPIDIOJ4_10B	The lower slot 10 J4 connection
RAPIDIOJ4_11A	The upper slot 11 J4 connection
RAPIDIOJ4_11B	The lower slot 11 J4 connection
RAPIDIOJ4_12A	The upper slot 12 J4 connection
RAPIDIOJ4_12B	The lower slot 12 J4 connection.
RAPIDIOJ4_13A	The upper slot 13 J4 connection
RAPIDIOJ4_13B	The lower slot 13 J4 connection

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Table 11-3. CPDLK20R Connector Names *(continued)*

Connector Name	Connector Description
RAPIDIOJ4_14A	The upper slot 14 J4 connection
RAPIDIOJ4_14B	The lower slot 14 J4 connection
RAPIDIOJ4_15A	The upper slot 15 J4 connection
RAPIDIOJ4_15B	The lower slot 15 J4 connection
RAPIDIOJ4_16A	The upper slot 16 J4 connection
RAPIDIOJ4_16B	The lower slot 16 J4 connection
RAPIDIOJ4_17A	The upper slot 17 J4 connection
RAPIDIOJ4_17B	The lower slot 17 J4 connection
RAPIDIOJ4_18A	The upper slot 18 J4 connection
RAPIDIOJ4_18B	The lower slot 18 J4 connection
RAPIDIOJ4_19A	The upper slot 19 J4 connection
RAPIDIOJ4_19B	The lower slot 19 J4 connection
RAPIDIOJ4_20A	The upper slot 20 J4 connection
RAPIDIOJ4_20B	The lower slot 20 J4 connection

For More Information

The *Mercury System Manager's Guide* provides further information on configuration file syntax and the use of the `configmc` and `sysmc` tools to provide hardware configuration information to MCOE.

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12

System Architecture

System Architecture Overview

The electrical infrastructure of the ImpactRT 3200S system consists of seven major subsystems:

- Power input and protection circuits
- Power supply (up to nine units and power backplane)
- A 6-slot system midplane (including power distribution and signal routing) and up to three 5-slot expansion midplanes
- Monitor board and fan control card along with the external reset input connector and the LCD display
- Two temperature sensor cards
- One or two blower modules

The midplane assembly provides the primary connectivity between all elements of the system. The logical interconnection of the subsystems is shown in Figure 12-1 on page 128. Not shown is a SCSI cable connecting the SCSI drives with the single-board computer (SBC). Also not shown are the Ethernet and serial connections on the rear transition module or the I/O connections.

System Topology

The topology description in this section is meant as a resource for understanding and configuring the ImpactRT 3200S system midplane. Although any application mapping depends upon the application itself, the design features shown here can provide guidelines to obtain the best overall interconnect and adaptive routing performance.

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Figure 12-1. System Architecture Overview

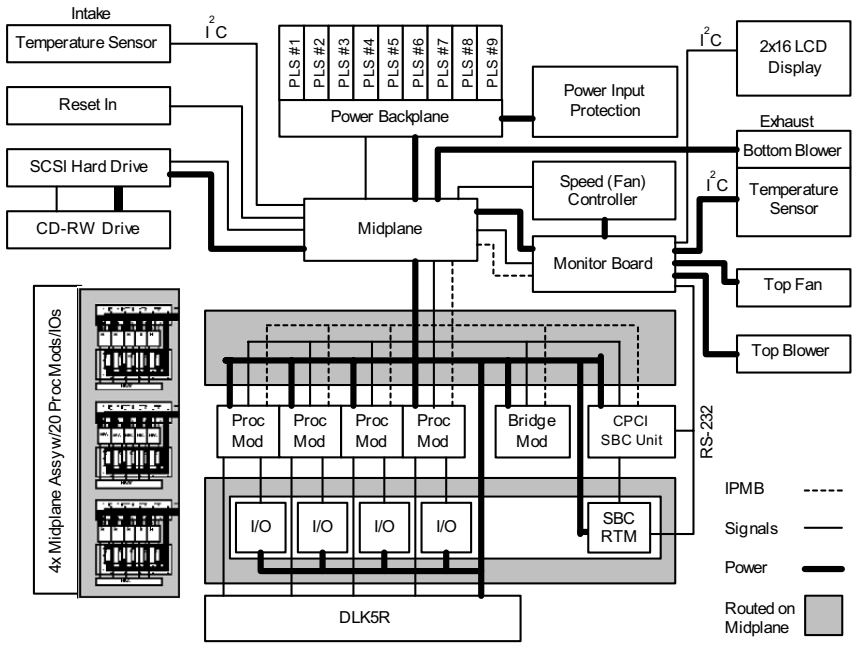


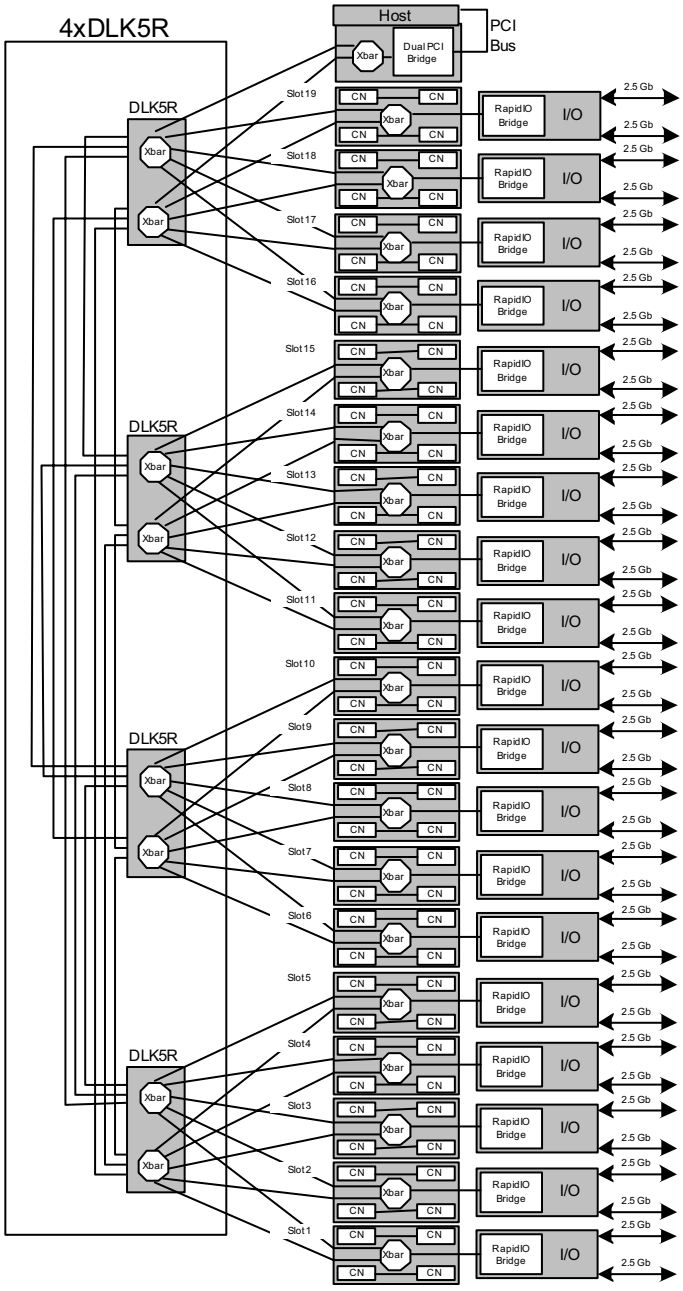
Figure 12-2 on page 129 is an overview of an entire system topology, showing the following elements of a system configured with 76 compute nodes:

- Up to four DLK5R RapidIO midplane interconnect assemblies, which each link the user-defined P4 connectors of five consecutive CompactPCI slots
- System midplane and three expansion midplanes slots 1-19, occupied by 19 MC4PK512H processor boards
- PCI bus and host/multicomputer interface, using the MCP6-DPRB dual-PCI-to-RapidIO bridge (Slot 20)
- Dual-channel fiber-optic I/O

Note: Connections in Figure 12-2 on page 129 between a rear I/O module and a processor board are pass-through; they are not routed over the midplane at all. The I/O module must be installed in the rear of the same slot as a processor or bridge module.

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Figure 12-2. Topology: 76-Node System Configuration

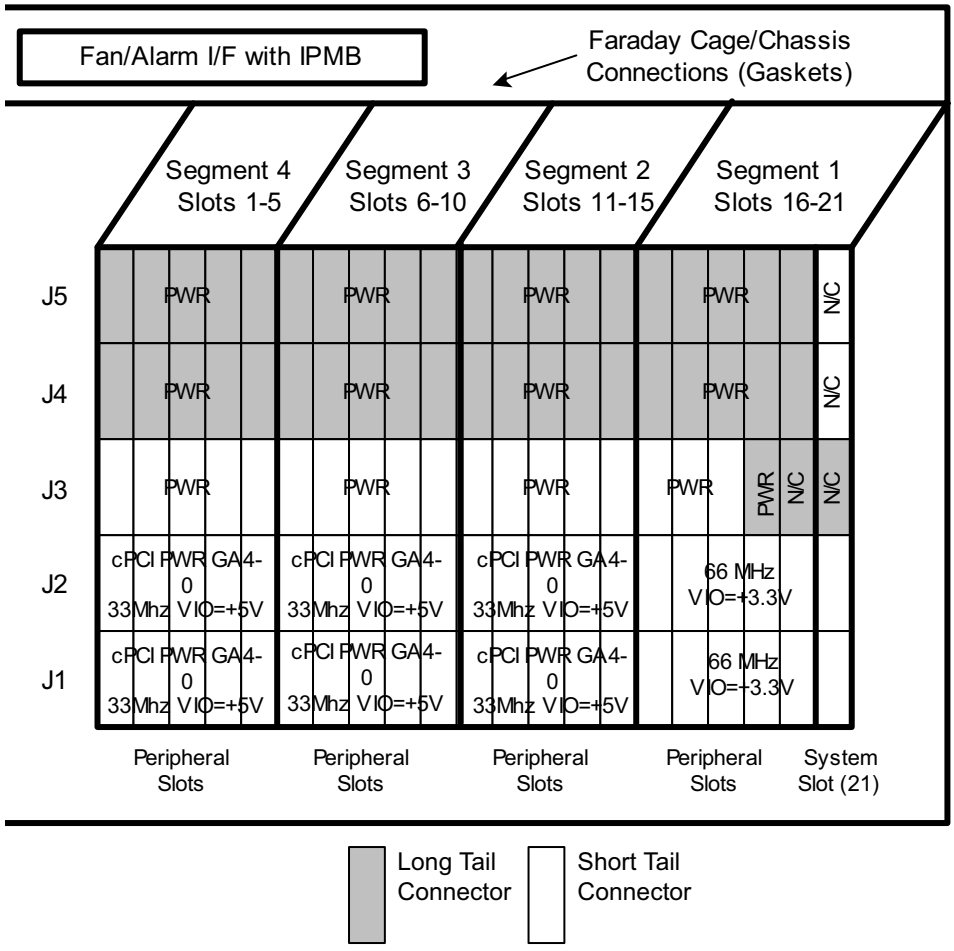


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Midplane

The system includes a 6-slot CompactPCI system midplane plus up to three 5-slot expansion midplanes with passive components. It accommodates up to 21 circuit boards and is designed to allow front and rear access. For future expansion, the midplane is divided into four separate cPCI midplanes, with six slots in segment 1 and five slots each in the other three segments (Figure 12-3). It should be noted that these CompactPCI segments are not bridged in any way, and that only segment 1 actually possesses a CompactPCI bus. Thus, PCI communications from modules in slots outside the first segment are not currently possible.

Figure 12-3. Midplane Architecture: cPCI Segmentation and Signal Blocks



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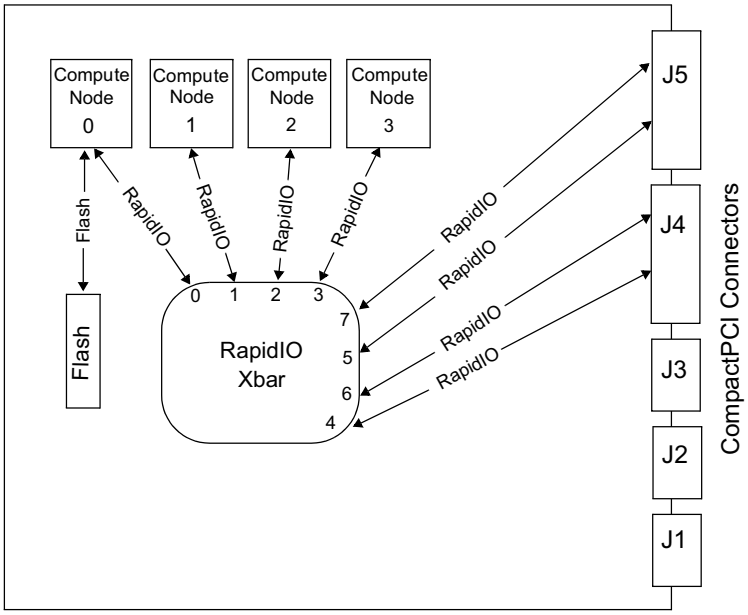
An optional, factory-set jumper on the power backplane ties frame ground to signal ground.

MC4PK Processing Module

The MC4PK processor module features four compute nodes, each comprising a PPC 7447A G4 microprocessor with embedded L2 cache, a GxCE compute node ASIC, and a DDR-SDRAM main memory subsystem. One compute node connects to a flash RAM device. Figure 12-4 provides an overview of the MC4PK processor module architecture.

An on-board RapidIO crossbar connects the GxCE RapidIO ports to four full duplex RapidIO ports. Two of these ports connect to the RapidIO fabric through the J4 connector. A third and fourth port support a rear transition module through the J5 connector.

Figure 12-4. MC4PK Processing Module



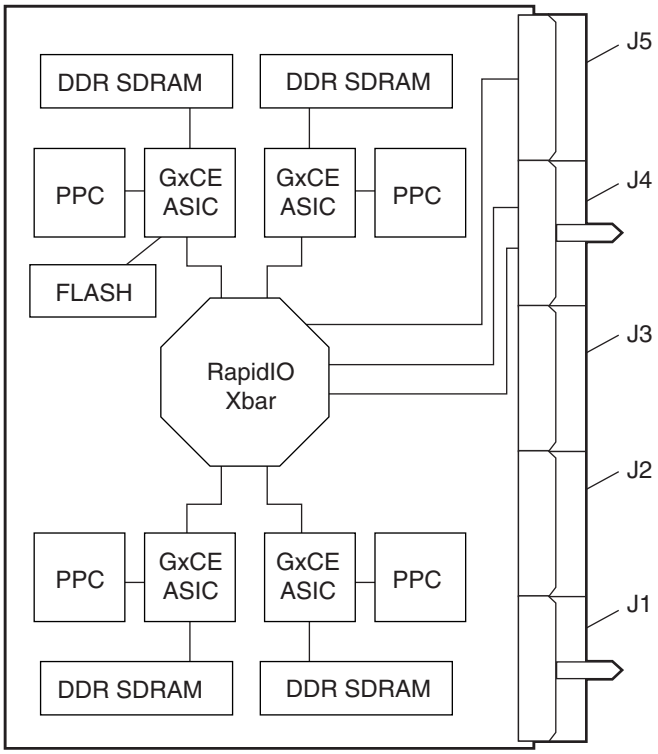
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MCP-P4K Processing Module

The MCP-P4K processor module features four compute nodes, each comprising a PPC 7445 G4 microprocessor with embedded L2 cache, a GxCE compute node ASIC, and a DDR-SDRAM main memory subsystem. One compute node connects to a flash RAM device. Figure 12-5 provides an overview of the MCP-P4K processor module architecture.

An on-board RapidIO crossbar connects the GxCE RapidIO ports to three full duplex RapidIO ports. Two of these ports connect to the RapidIO fabric via the J4 connector. A third port supports a rear transition module through the J5 connector.

Figure 12-5. MCP-P4K Processing Module

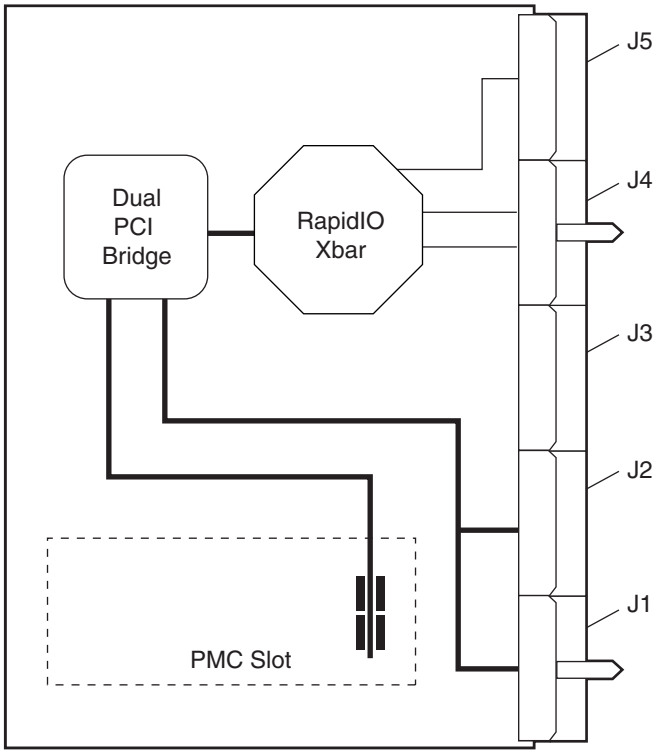


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MCP6-DPRB Bridge Module

The MCP6-DPRB module provides a bridge between PCI and RapidIO on a CompactPCI platform. The module's bridge component (DPRB) connects two PCI channels to one RapidIO port. One channel serves the midplane CompactPCI bus; the other serves a PCI mezzanine card site. An on-board RapidIO crossbar connects the DPRB RapidIO port to three full duplex RapidIO ports. Two of these ports connect to the RapidIO fabric via the J4 connector. A third port supports a rear transition module through the J5 connector. Figure 12-6 provides an overview of the bridge module architecture.

Figure 12-6. MCP6-DPRB Bridge Module

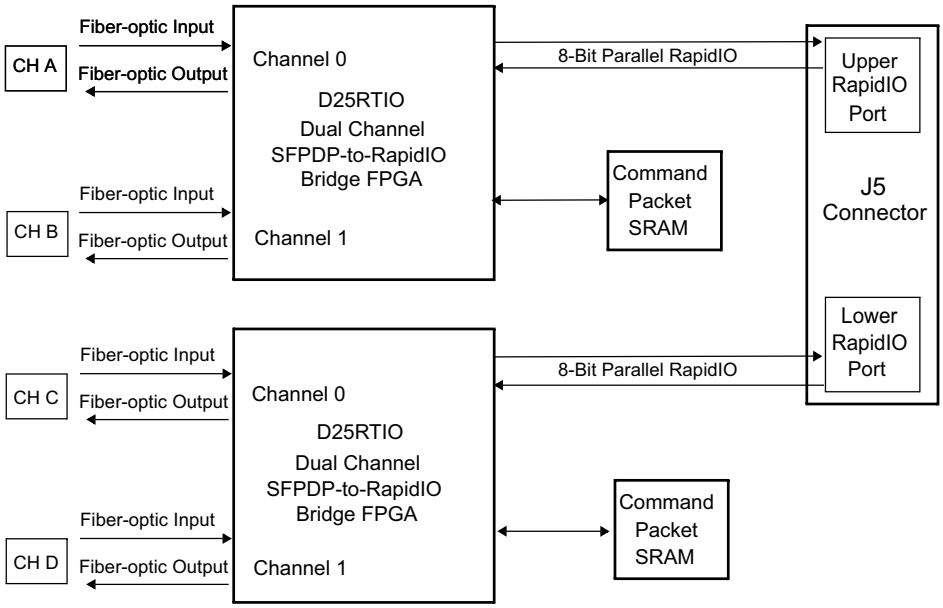


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TIO-4FGD I/O Module

The TIO-4FGD rear transition I/O module provides direct RapidIO connection to the processor module or the bridge module through the J5 connector. Four fiber-optic channels send and receive streaming data. Each pair (A and B or C and D) can be independently set to operate at 2.5 Gbaud or 1.0625 Gbaud. Two 8-bit, parallel RapidIO ports on the CompactPCI J5 connector provide an interface to the RapidIO fabric. Figure 12-7 provides an overview of the TIO-4FGD module architecture.

Figure 12-7. TIO-4FGD Module

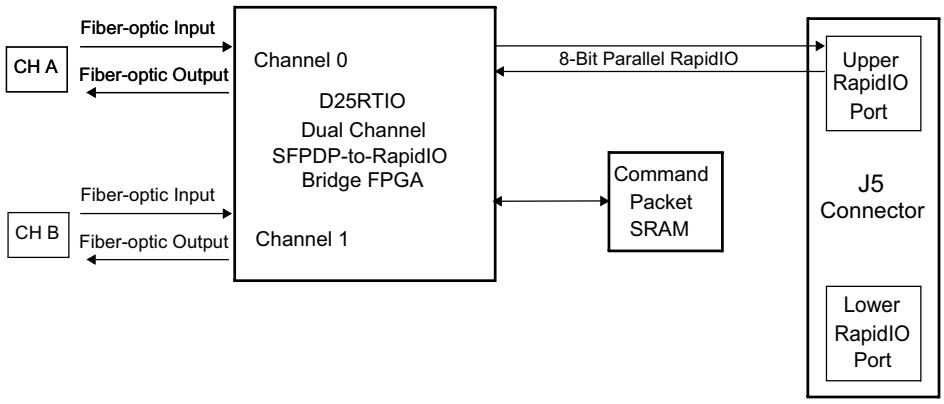


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TIO-2FGD I/O Module

The TIO-2FGD rear transition I/O module is a variation of the TIO-4FGD, providing two fiber-optic channels to send and receive streaming data. These channels can be set to operate at 2.5 or 1.0625 Gbaud. Two 8-bit parallel RapidIO ports on the J5 connector provide an interface to the RapidIO fabric. Figure 12-8 provides an overview of the TIO-2FGD module architecture.

Figure 12-8. TIO-2FGD Module

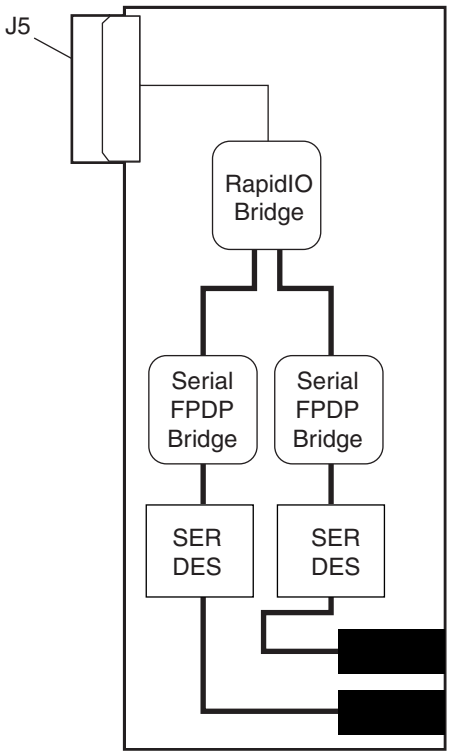


TIO-2FGR I/O Module

The TIO-2FGR rear transition I/O module provides direct RapidIO connection to the processor module or the bridge module through the J5 connector. Dual channels of 2.5 Gbaud fiber-optic I/O send and receive data to an 8-bit RapidIO port. The fiber-optic I/O stream uses the Serial FPDP transmission protocol. Figure 12-9 on page 136 provides an overview of the TIO-2FGR I/O module architecture.

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Figure 12-9. TIO-2FGR I/O Module

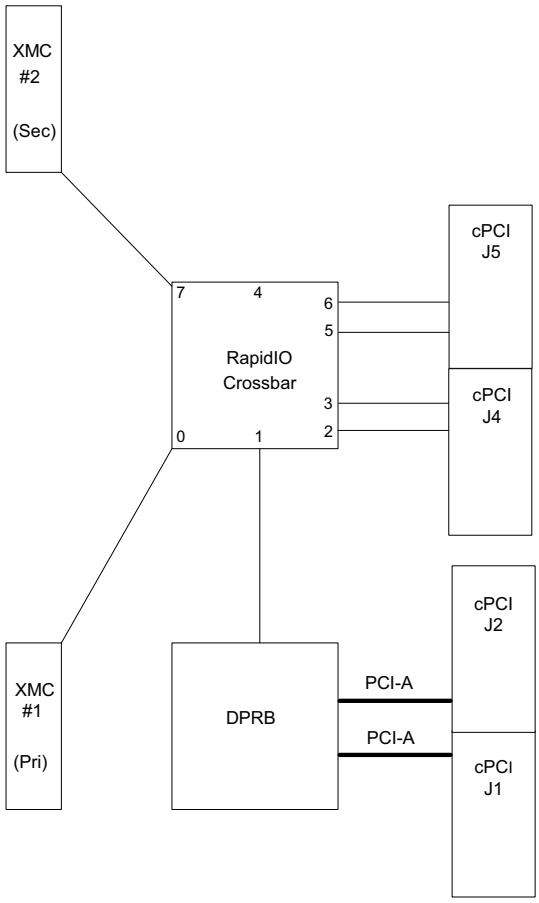


MCPIO-DPRC Module

Each mezzanine site on the MCPIO-DPRC module has a direct RapidIO connection to the 8-port crossbar ASIC. The module's PCI-to-RapidIO bridge component (DPRB) has a PCI channel, which connects to the backplane bus and links the bus to the RapidIO fabric. Two ports on the crossbar connect the on-board resources to the chassis RapidIO fabric through the J4 cPCI connector. Two more crossbar ports connect to the J5 cPCI connector to support a rear transition module. Figure 12-10 on page 137 illustrates the MCPIO-DPRC architecture.

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Figure 12-10. MCPIO-DPRC Module



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13

Removing and Installing Components

Removable Components

Replaceable components in the ImpactRT 3200S system chassis include power supply units, peripheral drives, fuses, blowers, and CompactPCI boards.

Table 13-1 lists the components that can be replaced by the user.

Table 13-1. Field Replaceable Units (FRUs)

Qty. per Chassis	Description
3, 6, or 9	Power supply
1	LCD display (2 x 16 text display, backlight)
1	Hard disk drive
1	Hard drive and CD carrier
1	SCSI CD-RW drive (12X/10X/32X, 5.25" wide)
0 or 1	Upper Blower assembly (Auxiliary Blower)
1	Lower Blower assembly (Main Blower)
1	Host single-board computer (SBC), with VGA card and SCSI PMC
1	Rear transition module for SBC
Variable	MC4PK RapidIO processing module
Variable	MCP-P4K RapidIO processing module
Variable	MCP6-DPRB-3R RapidIO bridge module
Variable	MCPIO-DPRC RapidIO bridge module
Variable	TIO-4FGD fiber-optic I/O module (rear transition module)

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Table 13-1. Field Replaceable Units (FRUs) *(continued)*

Qty. per Chassis	Description
Variable	TIO-2FGD fiber-optic I/O module (rear transition module)
Variable	TIO-2FGR fiber-optic I/O module (rear transition module)

Preparing for Installation or Removal

Tools Needed

Table 13-2 lists the tools required for removing and installing user-replaceable components.

Table 13-2. Removal and Replacement Tools

Task	Tools
Removing chassis covers or power supplies	Phillips screwdriver (no. 2)
Installing boards in card cage	Phillips screwdriver (no. 1)

Chassis Shutdown Procedures

To shut down the ImpactRT 3200S system, follow the procedure in this section and refer to Figure 13-1 on page 141.

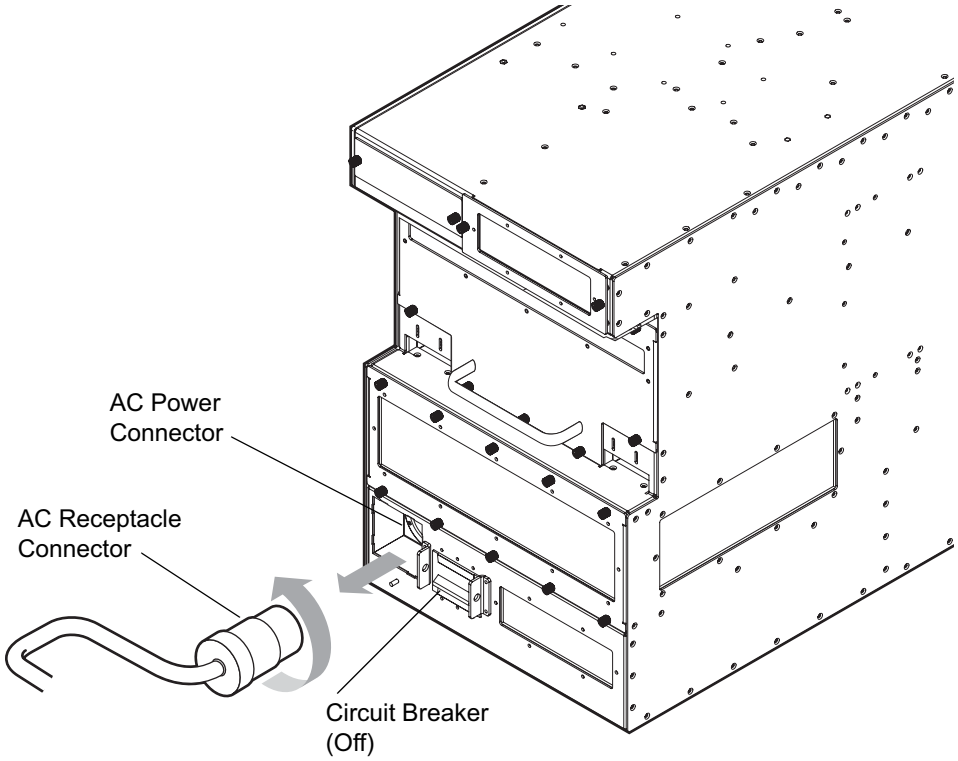
■ **To shut down the chassis:**

1. Shut down the operating system, as described in your OS documentation.
2. Turn the DC On/Off switch at the front of the chassis to the off position. (See Figure 1-2 on page 5.)
3. Turn off and lock out the circuit breaker at the rear of the chassis, to prevent accidental power activation. Figure 13-1 on page 141 shows the breaker in the off position. (See Table 2-4, “Lockout/Tagout Procedure” on page 11.)
4. Disconnect the power cord from the AC power connector at the bottom left rear of the chassis. Rotate the AC receptacle connector counter-clockwise, and pull it away from the chassis.

Warning: Audio levels as high as 78 dB(A) are possible at the rear of the chassis.

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Figure 13-1. Disconnecting Power Cable and Turning Off Circuit Breaker



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Replacing Power Supply Units

Each of the power supply units is replaceable. To replace an ImpactRT 3200S system power supply, follow the procedures in this section.

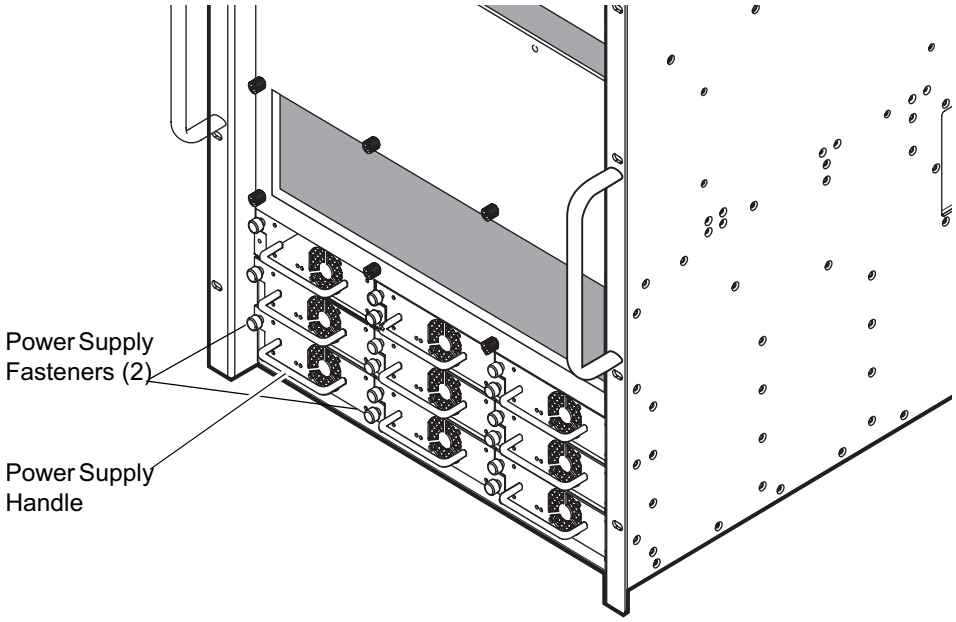
Tool Required: No. 2 Phillips screwdriver

Warning: To avoid danger of electric shock, turn the circuit breaker off prior to performing maintenance on the power supply (see "Chassis Shutdown Procedures" on page 140). Failing to completely isolate the chassis from input power creates a serious electrocution hazard.

- **To remove a power supply module (Figure 13-2):**

  1. Using a Phillips screwdriver, loosen the two knurled fasteners on the module faceplate.
  2. Pull the power supply handle to slide the module out.

Figure 13-2. Power Supply Module Removal



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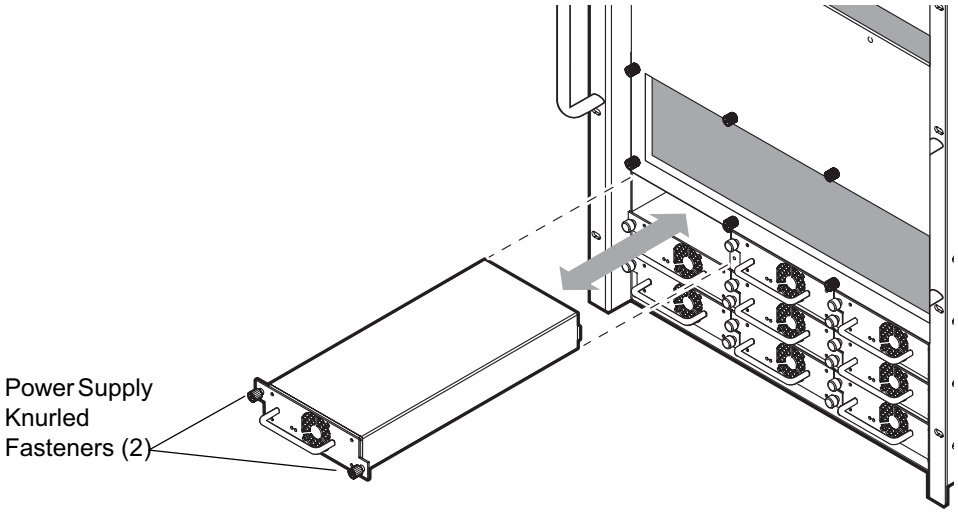
■ **To install a power supply module (Figure 13-3):**

1. Orient the module so that the rear connector is near the bottom.

Caution: Be sure that the orientation of the module is correct. Check to see that the main label on the power supply is facing down.

2. Slide the power supply into the chassis compartment until you feel the module connector seat in the backplane receptacle.
3. Using the Phillips screwdriver, tighten the two power supply fasteners.

Figure 13-3. Power Supply Module Installation



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Accessing the Internal Chassis Area for Cabling

To gain access to the ImpactRT 3200S system internal chassis area, remove the top rear cover. Follow the procedure in this section and refer to Figure 13-4 on page 144.

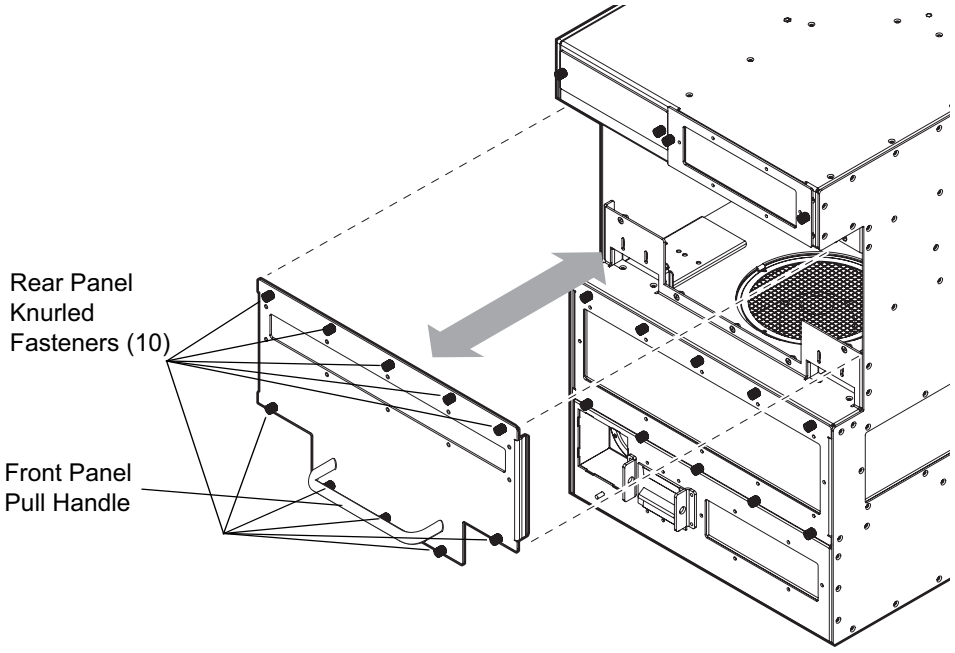
Warning: Turn off the circuit breaker located at the rear of the chassis. Failure to completely isolate the chassis from input power can cause electrical shock or damage to electrical components.

Tools Required: No. 2 Phillips screwdriver

■ **To remove the rear panel:**

1. Using the Phillips screwdriver, loosen the 10 rear panel knurled fasteners.
2. Using the handle, remove the rear panel from chassis, and set aside on a clean surface.

Figure 13-4. Rear Panel Removal



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Replacing the LCD Display

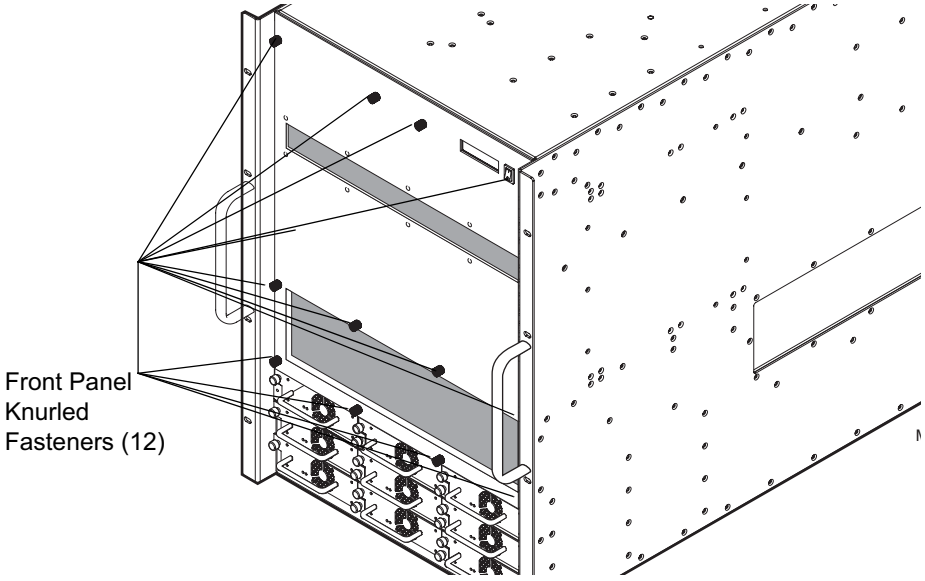
To replace the ImpactRT 3200S system LCD display, follow the procedures in this section and refer to Figure 13-5 on page 145, Figure 13-6 on page 146, and Figure 13-7 on page 147. The LCD display is located on the front panel at the top front of the unit (see Figure 13-6 on page 146).

Tools Required: No. 2 Phillips screwdriver

- **To access the LCD display:**

1. If the optional front panel is installed, remove it by loosening the 12 knurled fasteners. (See Figure 13-5 on page 145.)

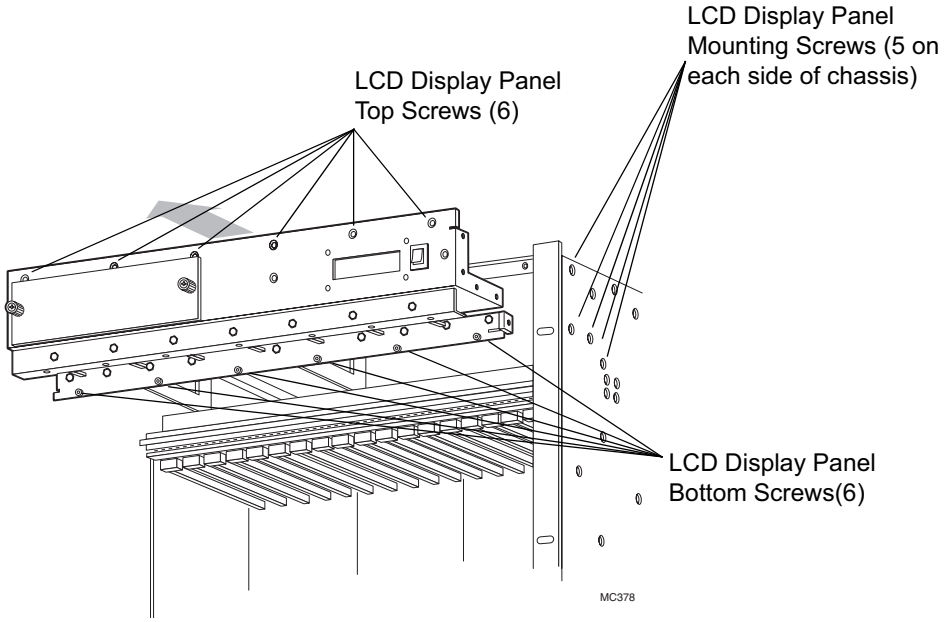
Figure 13-5. Front Panel Removal



2. Using the Phillips screwdriver, remove the five LCD display panel mounting screws on both the left and right sides of chassis. (See Figure 13-6 on page 146.)
3. Using the Phillips screwdriver, remove the six top LCD display panel screws. (See Figure 13-6 on page 146.)
4. Using the Phillips screwdriver, loosen the six bottom LCD display panel screws. (See Figure 13-6 on page 146.)
5. Slide the LCD display panel forward and fold it downward.

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Figure 13-6. LCD Display Panel Removal

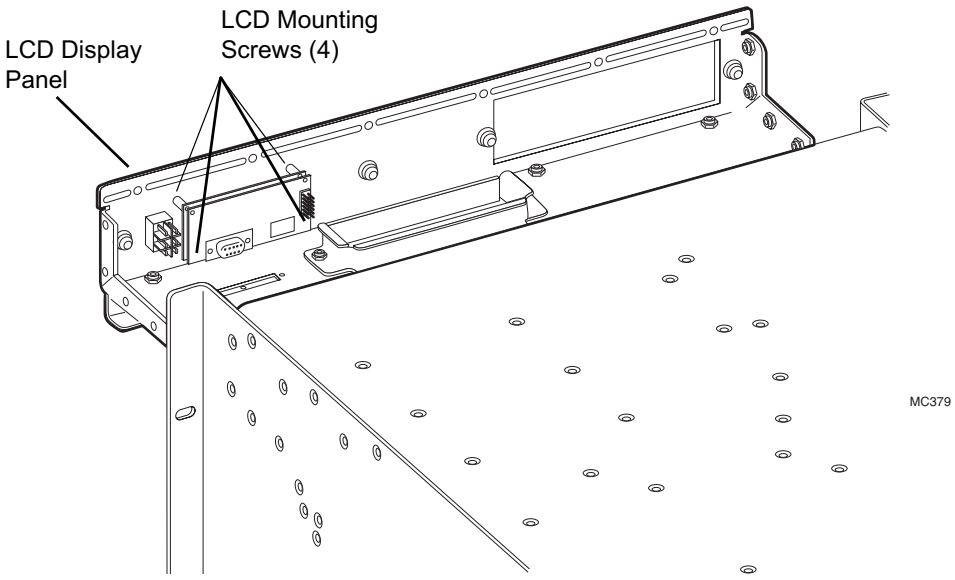


- **To remove the LCD display module:**

  1. Disconnect the LCD cable.
  2. Using the Phillips screwdriver, remove the four LCD mounting screws.

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Figure 13-7. Removing LCD From LCD Display Panel



- **To install the LCD display module:**

1. Position the LCD on the display panel. (See Figure 13-7.)
2. Using the Phillips screwdriver, secure the LCD to the LCD display panel with four screws.
3. Reconnect the LCD cable.
4. Slide the LCD display panel back into place.
5. Using the Phillips screwdriver, install the six top LCD display panel screws. (See Figure 13-6.)
6. Using the Phillips screwdriver, install the six bottom LCD display panel screws. (See Figure 13-6.)
7. Using the Phillips screwdriver, install the five LCD display panel mounting screws on both the left and right sides of the chassis. (See Figure 13-6.)
8. Using the Phillips screwdriver, install the front panel by tightening the twelve knurled fasteners. (See Figure 13-5.)

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Replacing the Drives

To replace the ImpactRT 3200S system hard drives, fuses, or CD-RW drive, follow the procedures in this section and refer to Figure 13-5 on page 145, Figure 13-6 on page 146, and Figure 13-7 on page 147. Replacing the hard drives, fuses, or CD-RW drive requires shutting down the system.

Caution: Removing drives while the system is running can cause data corruption.

Replacing a Hard Drive or CD-RW in the Drive Carrier

To remove or install a hard drive or CD-RW in the drive carrier in the rear of the chassis, refer to the following procedures and see Figure 13-4 on page 144, Figure 13-8 on page 149, and Figure 13-9 on page 150.

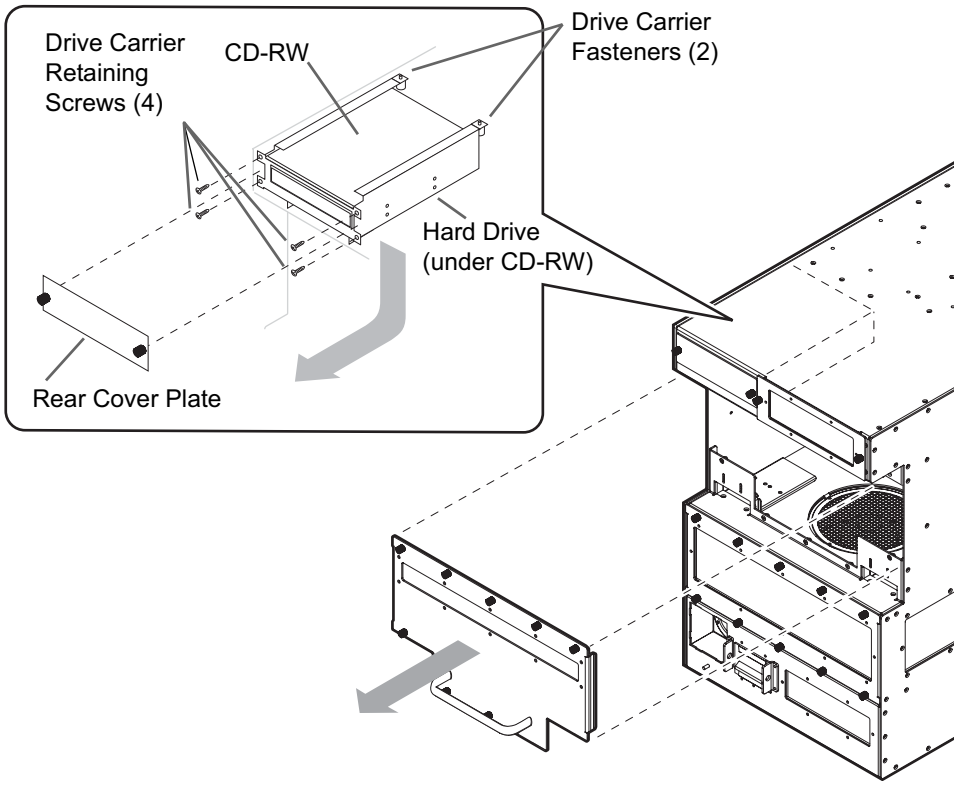
Tools Required: No. 2 Phillips screwdriver

- **To remove the drive carrier:**

1. Remove the rear panel. (See Figure 13-4 on page 144.)
   a. Using the Phillips screwdriver, loosen the rear panel fasteners.
   b. Use the handle to remove the rear panel from the chassis, and set it aside on a clean surface.
2. Using the Phillips screwdriver, loosen the two knurled screws on the CD-RW rear cover plate; remove the plate. (See Figure 13-8.)
3. Remove the drive carrier containing the hard drive and CD-RW drive as follows:
   a. Using the Phillips screwdriver, remove the four screws above and below the CD-RW drive in the rear of the drive carrier.
   b. From inside the chassis on the bottom side of drive carrier, use the Phillips screwdriver to loosen the two screws at the front end of the drive carrier. Let the front of the carrier rest on the top of the blower assembly.
   c. Disconnect all cables from the hard drive and CD-RW drive by reaching into the chassis through the open rear panel.
   d. Remove the drive carrier.

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Figure 13-8. Drive Carrier Removal and Installation



■ **To install the drive carrier:**

1. Connect the following cables to both the hard drive and the CD-RW drive:
   a. Power cables
   b. SCSI or IDE cables
2. Reposition the carrier in the chassis from the inside rear.
3. From inside the chassis on the bottom side, using the Phillips screwdriver, tighten the two knurled screws at the forward end of drive carrier.
4. Using the Phillips screwdriver, install the four screws above and below CD-RW drive in the rear of the drive carrier.
5. Using the Phillips screwdriver, install the rear CD-ROW cover plate and tighten the two knurled screws on the rear CD-RW cover plate.

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- **To install a CD-RW into the drive carrier:**

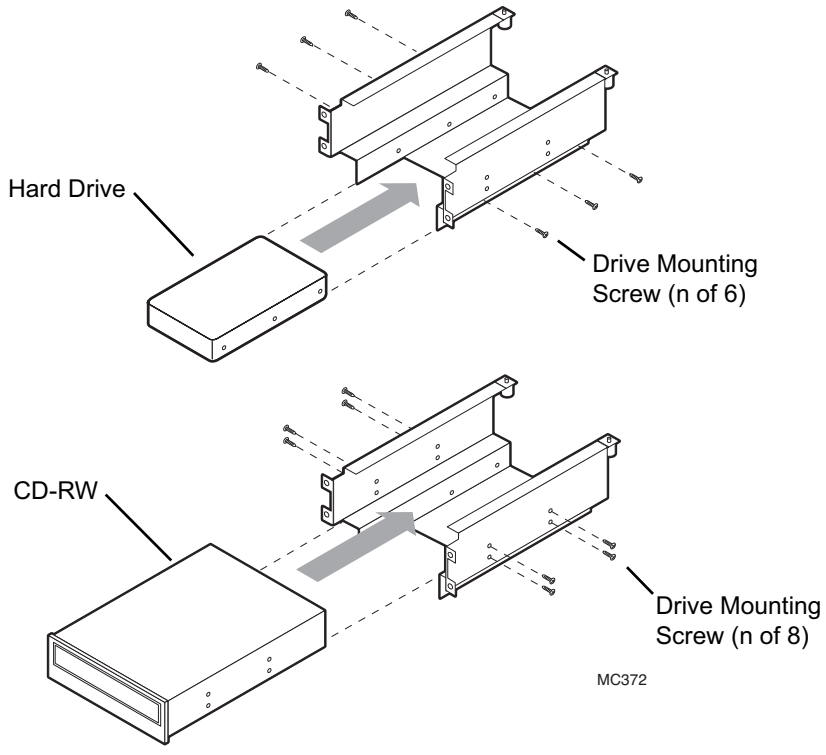
  1. Place the CD-RW in the carrier; align the mounting holes. (See Figure 13-9.)
  2. Using the Phillips screwdriver, install the mounting screws through the mounting holes into CD-RW.

- **To install a hard drive into the drive carrier:**

  1. Place the hard drive in the drive carrier; align the mounting holes. (See Figure 13-9.)
  2. Using the Phillips screwdriver, install the mounting screws through the mounting holes into the hard drive.

Note: If you remove both the hard drive and the CD-RW drive, you must reinstall the CD-RW drive before installing the hard drive. Otherwise, the CD-RW drive will not fit into the carrier.

Figure 13-9. Installing a Hard Drive and CD-RW into the Drive Carrier



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Replacing the Blowers

To replace the ImpactRT 3200S system main (lower) or auxiliary (upper) blower, follow the procedures in this section and refer to Figure 13-10 on page 152. Each blower has knurled fasteners to use for removal. Designations for each blower are shown in Figure 13-10.

Tools Required: No. 2 Phillips screwdriver

- **To remove a main (lower) blower assembly:**

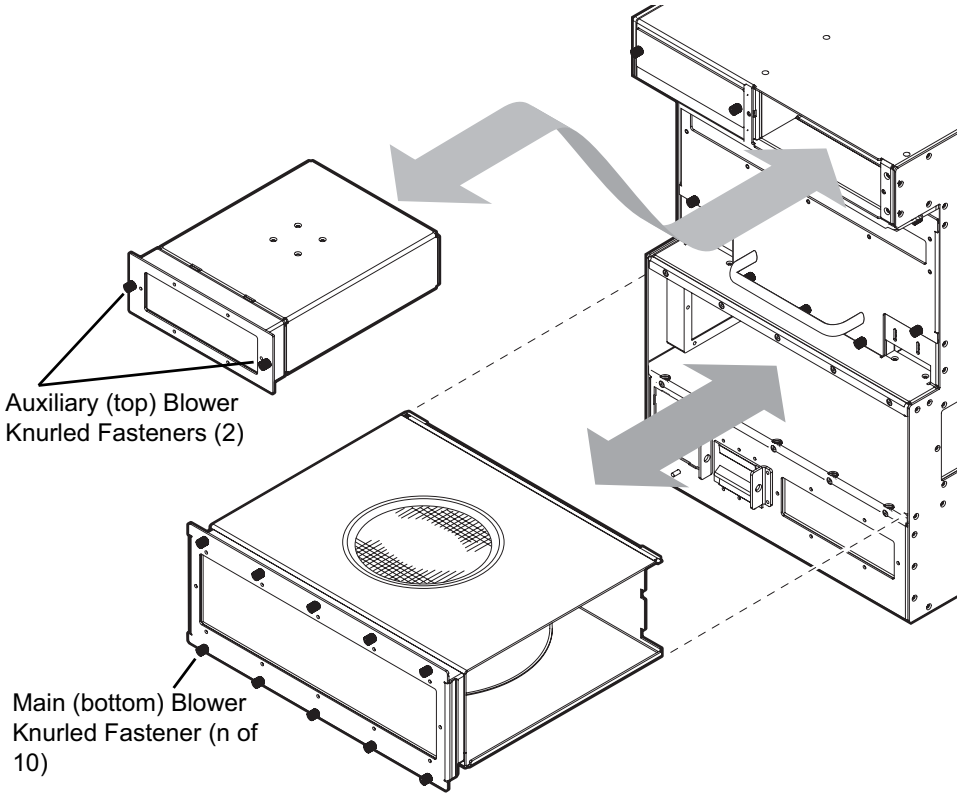
  1. Using the Phillips screwdriver, loosen the ten knurled fasteners across the top and bottom of blower assembly. (See Figure 13-10.)
  2. Pull on blower knurled fasteners to disengage connector on the rear of blower. (See Figure 13-10.)
  3. Remove main (lower) blower assembly.

- **To install a main (lower) blower assembly:**

  1. Align main blower with appropriate opening in chassis. (See Figure 13-10.)
  2. Slide blower into opening until it stops, making sure cabling does not get caught.
  3. Firmly press front of blower to engage connector at rear.
  4. Using the Phillips screwdriver, tighten the ten knurled fasteners across the top and bottom of the blower assembly. (See Figure 13-10.)

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Figure 13-10. Main and Auxiliary Blower Assemblies



- **To install an auxiliary (top) blower assembly:**

  1. Align auxiliary blower with appropriate opening in chassis. (See Figure 13-10.)
  2. Slide blower into opening until it stops, making sure cabling does not get caught.
  3. Firmly press front of the blower to engage connector at rear.
  4. Using the Phillips screwdriver, tighten the two knurled fasteners across the top and bottom of the blower assembly.(See Figure 13-10.)

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■ **To remove an auxiliary (top) blower assembly:**

1. Using the Phillips screwdriver, loosen the two knurled fasteners across the top and bottom of the blower assembly. (See Figure 13-10.)
2. Pull on the blower knurled fasteners to disengage the connector on the rear of the blower. (See Figure 13-10.)
3. Remove the auxiliary (top) blower assembly.

Replacing the SBC Module

To replace the ImpactRT 3200S system single-board computer (SBC) module, follow the procedures in this section. The host SBC is a standard CompactPCI module. The video card and the SCSI controller PMC cards are attached to the SBC. The SBC must be removed before either of the PMC cards can be replaced.

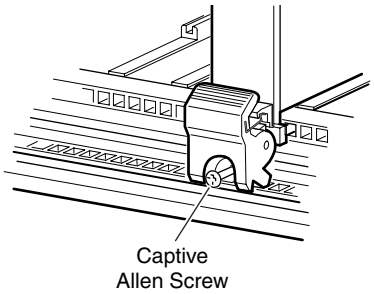
■ **To remove the SBC:**

1. Using the no. 2 Phillips screwdriver, remove the front door by loosening the twelve knurled fasteners. (See Figure 13-5 on page 145.)

Warning: Modules installed in the card cage must be securely seated and the ejector handles on the front panel firmly locked and secured with screws. Removing a module without properly shutting down the system can severely damage the module and can expose high-current components, creating a risk of electric shock.

2. Detach cabling from the module.
3. Extract the module:
   a. Use a no. 1 Phillips screwdriver to remove the captive screws at top and bottom (see Figure 13-11).

Figure 13-11. SBC Module (Detail)



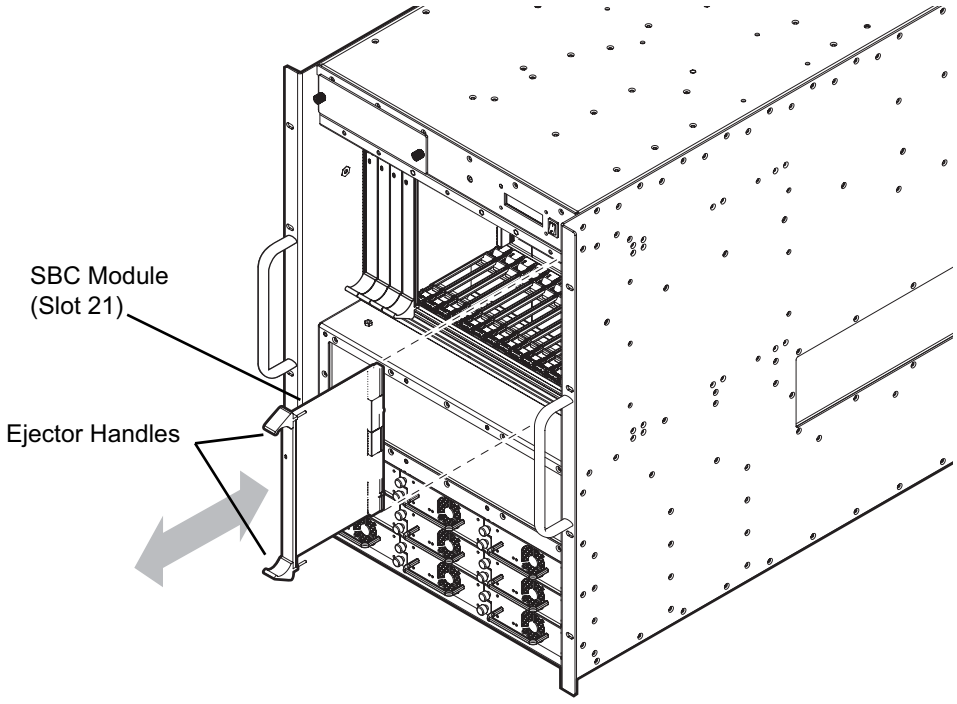
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b. Press the levers on the ejector handles and extract the module by pushing levers away from each other (top lever up; lower lever down; see Figure 13-12). For further information, please see the owner's manual for the SBC.

■ **To install the SBC:**

1. Align the module in the guides; slide it into the chassis. (See Figure 13-12.)
2. Firmly press the front of module into the backplane to engage the connectors.
3. Press the levers on the ejector handles inward to seat the modules. The levers complete the last 1/8 inch of connector engagement. Use a no. 1 Phillips screwdriver to fasten the screws at top and bottom. (See Figure 13-11 on page 153.)
4. Reattach cabling to the SBC module.
5. Using the Phillips screwdriver, reinstall the front panel by tightening the twelve knurled fasteners. (See Figure 13-5 on page 145.)

Figure 13-12. SBC Module



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Replacing the Rear Transition Board

To replace the ImpactRT 3200S system rear transition board (RTB), follow the procedures in this section and refer to Figure 13-4 on page 144 and Figure 13-13 on page 156. The RTB for the SBC is a standard CompactPCI card installed at the rear of the system. (See Figure 13-13 on page 156.)

- **To remove the rear panel:**

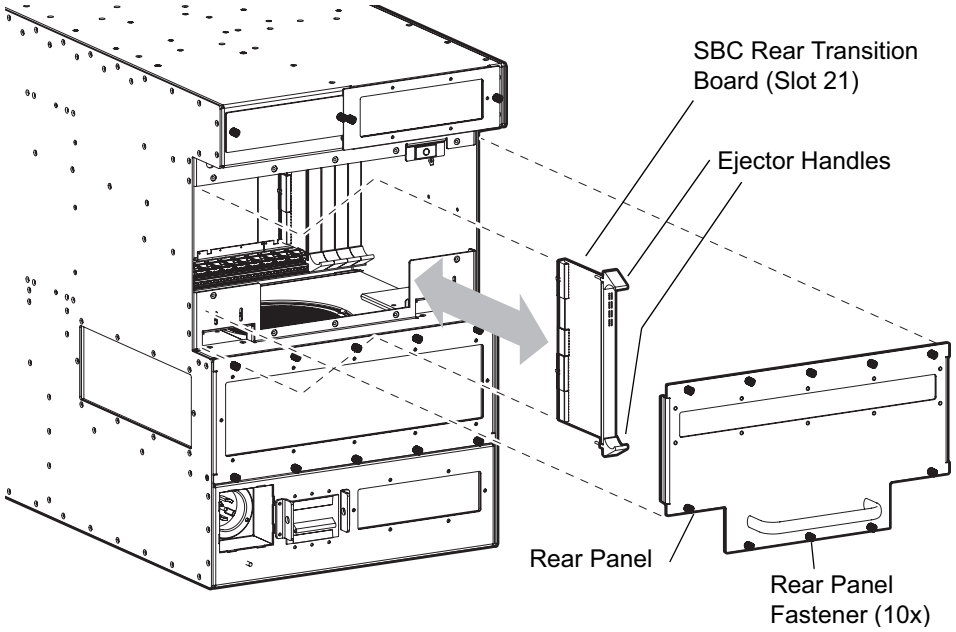
  1. Using the Phillips screwdriver, remove the ten knurled fasteners from the rear panel. (See Figure 13-13.)
  2. Using the handle, remove rear panel and set it aside on a clean surface.

- **To remove the RTB:**

  1. Detach cabling from the transition board. If the SCSI cable blocks access to the RTB, remove tie-wrap and move the cable aside.
  2. Remove the upper and lower mounting screws.
  3. Press the levers and extract the board by pushing the levers away from each other (top lever up; lower lever down).
  4. Slide the RTB out of its slot, then turn it horizontally to remove it from the chassis through the rear opening.

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Figure 13-13. Rear Transition Board



5. For further information, please see the owner's manual for the board.

■ **To install the RTB:**

1. Turn RTB horizontally to insert through the rear chassis opening, then turn RTB to a vertical position once it is inside chassis. (See Figure 13-13 on page 156.)
2. Align board in guides and slide into chassis.
3. Firmly press front of the board into midplane to engage connectors.
4. Tighten upper and lower mounting screws.
5. If necessary, reposition SCSI cable and replace tie-wrap.
6. Using the handle and the Phillips screwdriver, reinstall rear panel by tightening the 10 knurled fasteners. (See Figure 13-13.)

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Replacing a Mercury Module

To replace an ImpactRT 3200S Mercury module, follow the procedures in this section and refer to Figure 13-6 on page 146, Figure 13-14 on page 158, and Figure 13-15 on page 159. The connectors on the modules require considerable insertion force to fully seat the boards. Ejector handles on the front panels effectively seat and lock the boards into position.

Note: To replace a Mercury module, first remove the front door. For details, see Figure 13-6 on page 146.

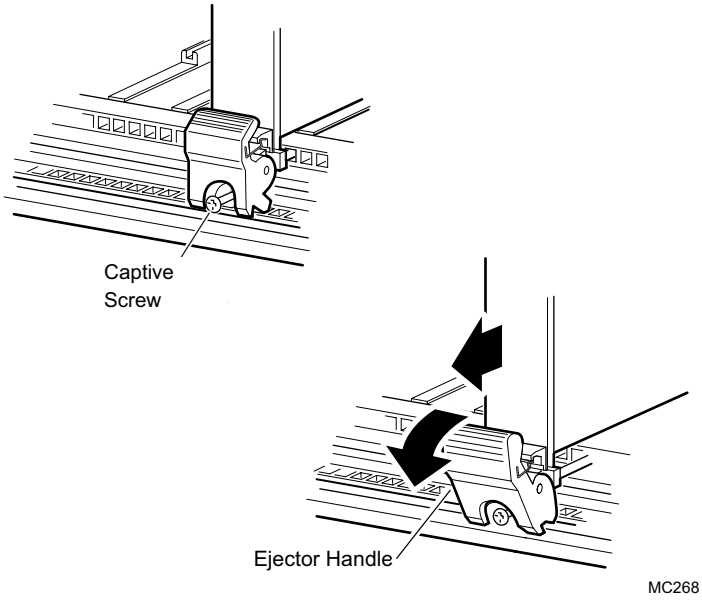
- **To remove a module:**

  1. Using the Phillips screwdriver, remove the front panel by loosening the twelve knurled fasteners. (See Figure 13-5 on page 145.)
  2. Disconnect any cables connected to the front panel.
  3. Loosen the captive screws at the top and bottom of the front panel, as shown in Figure 13-14.
  4. Disengage the board from the midplane by pulling the ejector handles outward, as shown in Figure 13-14.

     The ejector handle, shown in Figure 13-14, exerts the required force to disengage the board's connector pins.

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Figure 13-14. Removing a Module (Detail)



Caution: Clearance is limited between board components and the edges of the front panels of adjacent boards. Use care to avoid damaging components as you slide the boards out.

5. Pull out module, sliding it back along the card guide.

Installing a Module

Caution: Clearance is limited between a board's components and the edges of the adjacent board front panels. Use care to avoid damaging components as you slide the boards in.

■ **To install a module:**

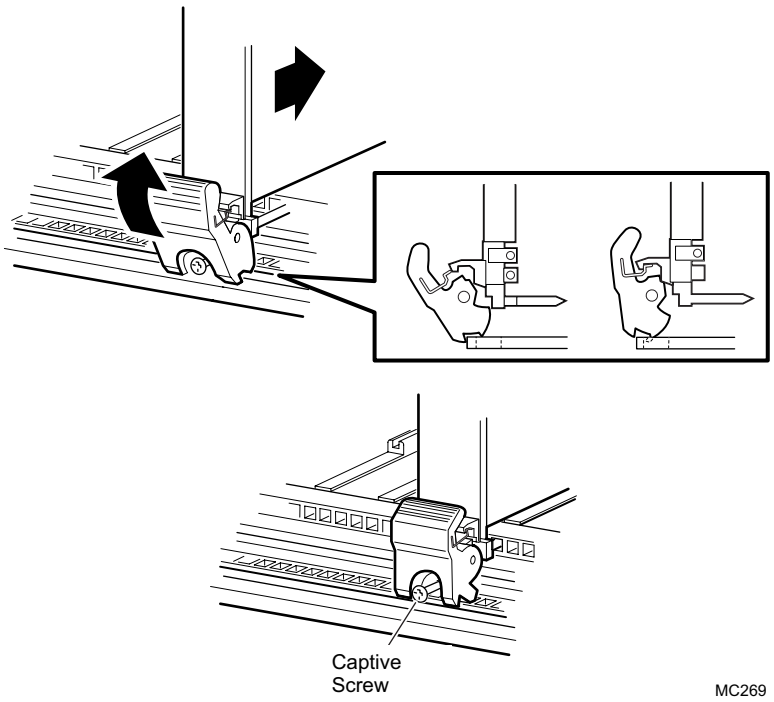
1. Position the module along the card guide; slide it in to engage midplane connectors. (See Figure 13-15 on page 159.)
2. Press the ejector handles inward to seat the board. Levers on the ejector handles are designed to grip the comb at the front end of the card guide.

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3. Using the Phillips screwdriver, reinstall the front panel by tightening the twelve knurled fasteners. (See Figure 13-6 on page 146.)

Caution: Be sure that the captive screw at the top of the module clears the comb at the front of the card cage. Engage the screw in the front panel threads and check its angle before pressing the ejector handles. Be sure that the board is level and slides in straight. Do not force boards into the card cage.

Figure 13-15. Installing a Module



Note: When the faceplate of the board is flush with the faceplate of the adjacent board, the board is fully seated.

Caution: Make sure the lever on the ejector handle is engaged as shown. If the board is not fully seated, the system might fail.

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4. Tighten the retaining screws to 4 in-lbs, top and bottom, on the module, as shown.
5. Reconnect any cables to the board.

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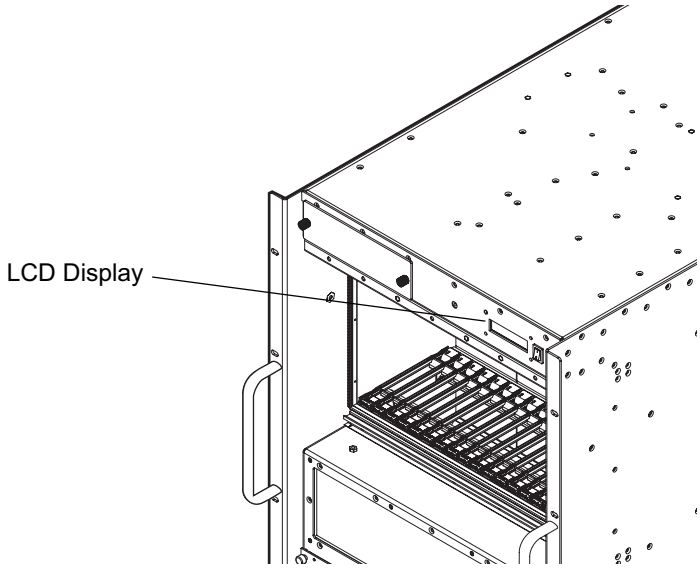
14

Troubleshooting the Chassis

Chassis Status Display

The monitor board, which monitors power supplies, temperature sensors, and blowers, displays chassis status using an alphanumeric LCD display on the chassis front panel (see Figure 14-1).

Figure 14-1. System Status Display



Troubleshooting information for the messages that can appear in the display area is provided in Table 14-1. Please note that not all messages have associated alarms.

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Table 14-1. LCD Display Messages

LCD Message	Problem	Description/Recommended Action
Matrix Orbital LK162-12		This message is displayed at power on if the Monitor Board is not communicating with the LCD display on the I^2C bus.
Mercury Computer Systems		Default display text. You can change the text of this message through the API.
	Power is off	Power Supplies are inhibited. Front Panel switch is OFF or Intrusion Switch is open.
NNNNN V FAIL=NN.NV	DC voltage failure	The indicated voltage is out of range, and the power supplies are turned on. This triggers a power down after the programmed shut-down delay of 30 seconds. Separate messages are displayed for each offending voltage. The NNNV voltages are: +5V = 5 volts to chassis boards +3.3V = 3.3 volts to chassis boards +12 = 12 volts -12V = -12 volts
FAN N FAIL	Top Fan Fail Bottom Fan Fail	The indicated blower has failed. This triggers a Power-Off alarm followed by a system shutdown after the programmed shutdown delay of 30 seconds.
EXHAUST TEMP FAIL = NN.NN°C INTAKE TEMP FAIL = NN.NN°C	Temperature fail	The air outlet or inlet temperature is too high. This fault triggers a Power-Off alarm followed by a system shutdown after the programmed shutdown delay of 30 seconds.

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