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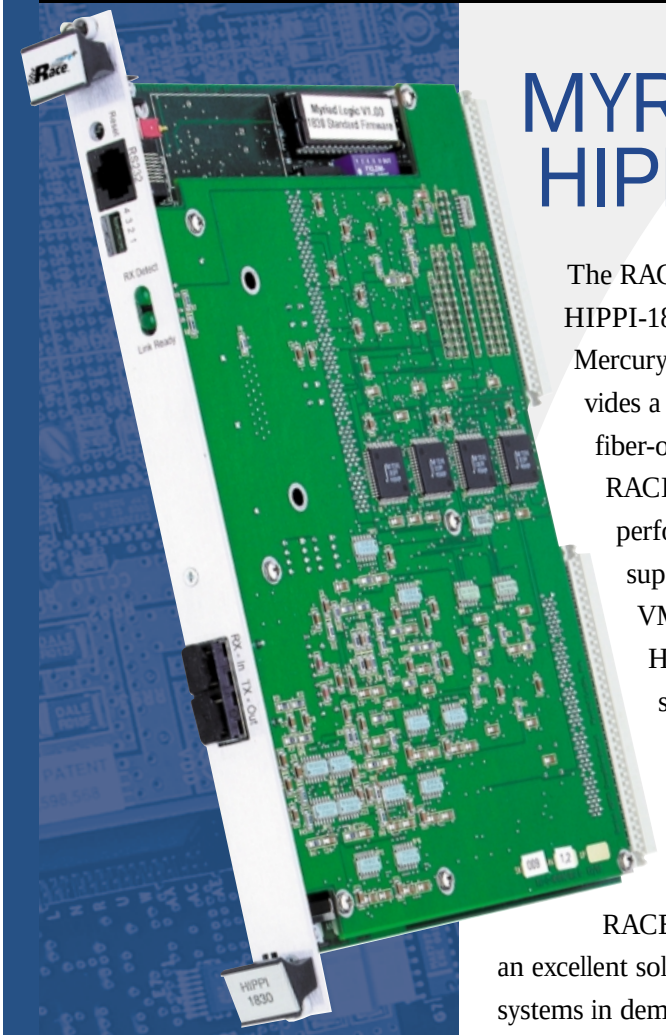
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Find the *Mercury Computer Systems / Myriad Logic HIPPI-1830* at our website: *Click HERE*

Computer Systems, Inc.
MERCURY

MYRIAD HIPPI-1830 Serial HIPPI Interface



The RACE++ Series MYRIAD™ HIPPI-1830 Serial Interface from Mercury Computer Systems provides a 100 MB/s, ANSI-standard, fiber-optic connection among RACE++® systems and high-performance workstations, supercomputers, and other VME systems. Low-overhead HIPPI protocols enable sustained transfer rates up to 95 MB/s using the RACE++ host interface.

Constructed from standard modules, the RACE++ Series HIPPI-1830 is an excellent solution for connecting systems in demanding real-time applications. It manages data transfer between system memory and the 100 MB/s fiber-optic communication channel. All communications intelligence and system interface functions are provided by the VRM-1630 foundation module. A low-profile daughtercard provides all serial HIPPI functions.

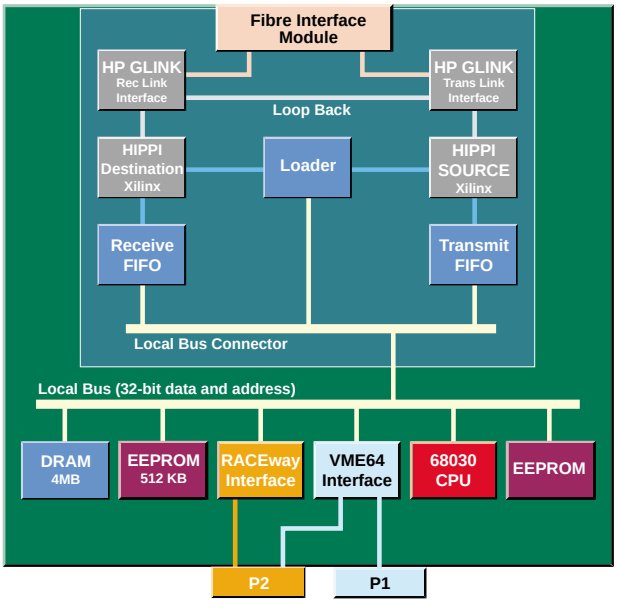
The HIPPI-1830 interface is optimized for real-time applications requiring high bandwidth and low latency. It provides ANSI X3T9.3-compliant, point-to-point, dual simplex channels compatible with a wide variety of high-performance workstations, supercomputers, and mass storage devices.

Serial HIPPI Daughtercard

Serial HIPPI is implemented on the low-profile daughtercard, which features:

- An optical transceiver module for electrical-to-optical translation
- Transmit/receive chipset to implement the Gbit protocol
- Xilinx 4000 family of field-programmable gate arrays (FPGAs) to implement the HIPPI protocol
- FIFO buffers.

RACE++ Series MYRIAD HIPPI-1830 Board Architecture



ANSI-Standard Fiber-Optic HIPPI Protocol with High-Density FPGAs

Sustained 95 MB/s System-to-System Transfers

160 MB/s Burst Data Transfers

Single-Mode Fiber Transmission up to 3 km

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The transceiver module can be supplied to support either single-mode or multi-mode fiber, providing transmission distances of 3 km and 300 meters, respectively. The transmit/receive chips provide serial-to-parallel and parallel-to-serial conversion as well as implement a robust Gbit/s serial transmission protocol that is the defined standard for serial HIPPI. They are configured to provide a loopback path, which allows a significant amount of built-in testing.

The HIPPI protocol is implemented in two high-density FPGAs, which are loaded by the onboard Motorola 68030 processor each time the board is reset. For applications that do not require or desire the serial HIPPI protocol, the FPGAs can be downloaded with a pass-through program. In this mode, data in VME or RACEway memory will be provided directly to the transmit/receive chip set for serialization and subsequent output.

The unit is software-compatible with the RACE++ Series MYRIAD HIPPI-830 parallel electrical interface, enabling simple upgrade from electrical to fiber-optic data transmission.

Foundation Module

The VRM-1630 foundation module supplies a full-featured VME64 master/slave interface (implemented with the Cypress Semiconductor VIC64 chipset) capable of sustaining 45 MB/s transfers in VME64 BLT mode. The VRM-1630's RACEway interface also provides full master/slave capability and has been benchmarked sustaining 95 MB/s transfers. An onboard Motorola 68030 processor operating at 40 MHz supports a VxWorks® kernel and a full-featured suite of HIPPI data transfer software that is compatible with the RACE++ Series MYRIAD HIPPI-830 electrical HIPPI product.

Contact Mercury for a product demonstration or for more information.

RACE++ MYRIAD

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The Ultimate Performance Machine

For more information, go to www.mc.com

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