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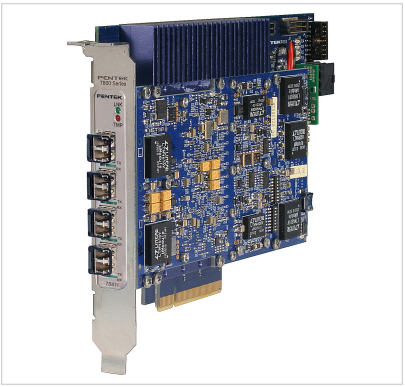
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Cobalt 78611

Quad serial FPDP interface PCIe board with Virtex-6 FPGA

Complete serial FPDP solution

- Fully compliant with VITA 17.1 specification
- Fibre optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O



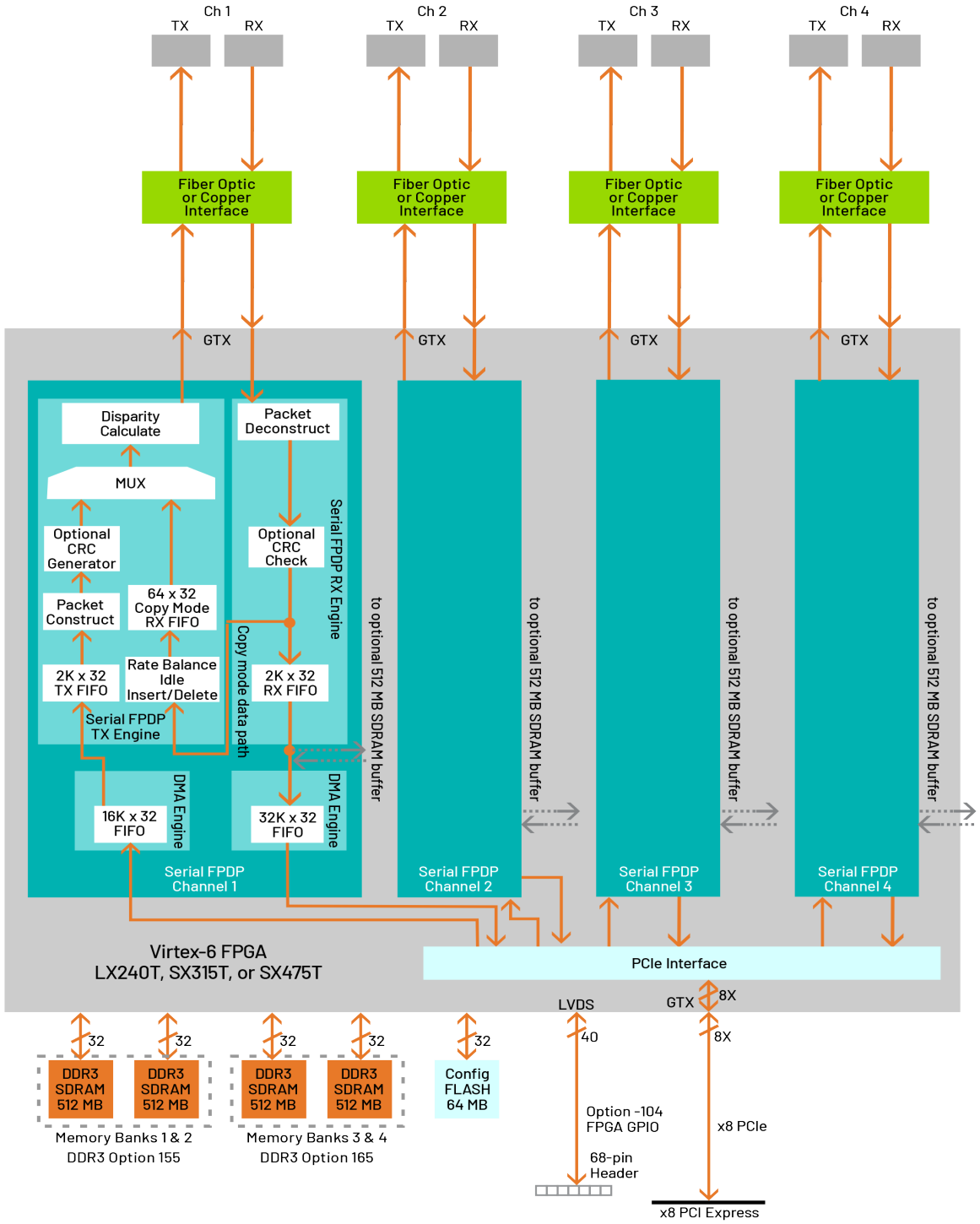
The 78611 is a multichannel, gigabit serial interface, ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link. The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 78611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the 78611 includes a general-purpose connector for application-specific I/O.

FEATURES

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fibre optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O

78611 BLOCK DIAGRAM



THE COBALT ARCHITECTURE

The Cobalt® Architecture features a Xilinx Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 71611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/ decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

SERIAL FPDP INTERFACE

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5,3.125, and 4.25 Gbaud link rates and the option for multimode and single-mode optical interfaces or copper interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

MEMORY RESOURCES

The 78611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI EXPRESS INTERFACE

The 78611 includes an industry standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

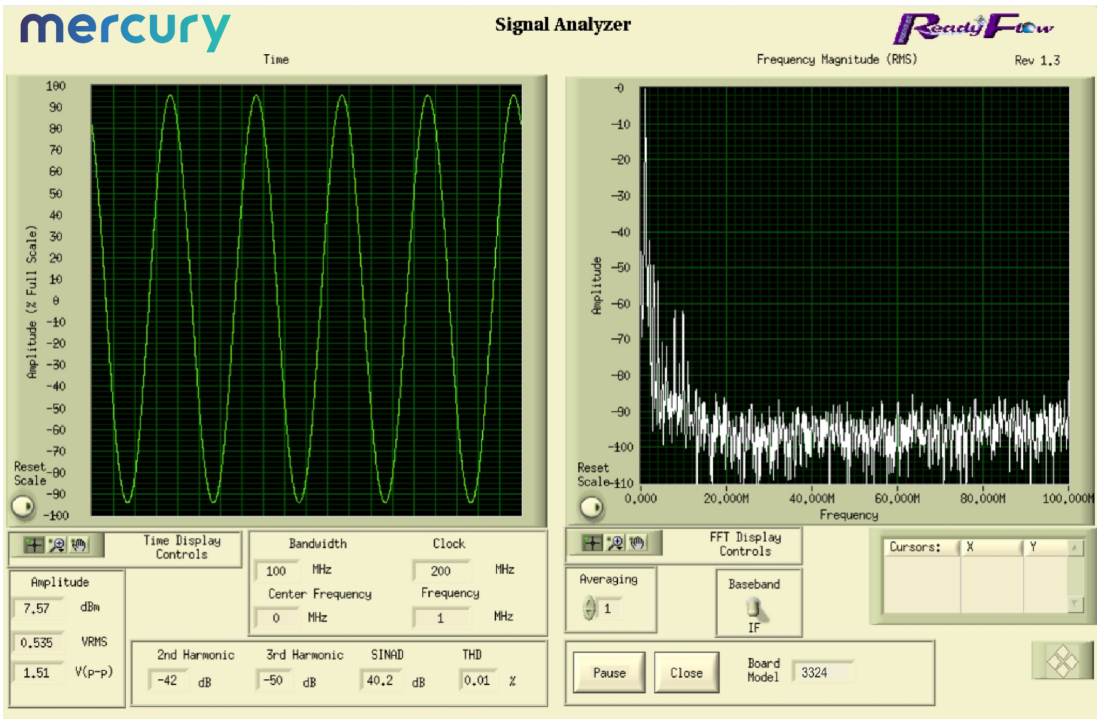
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

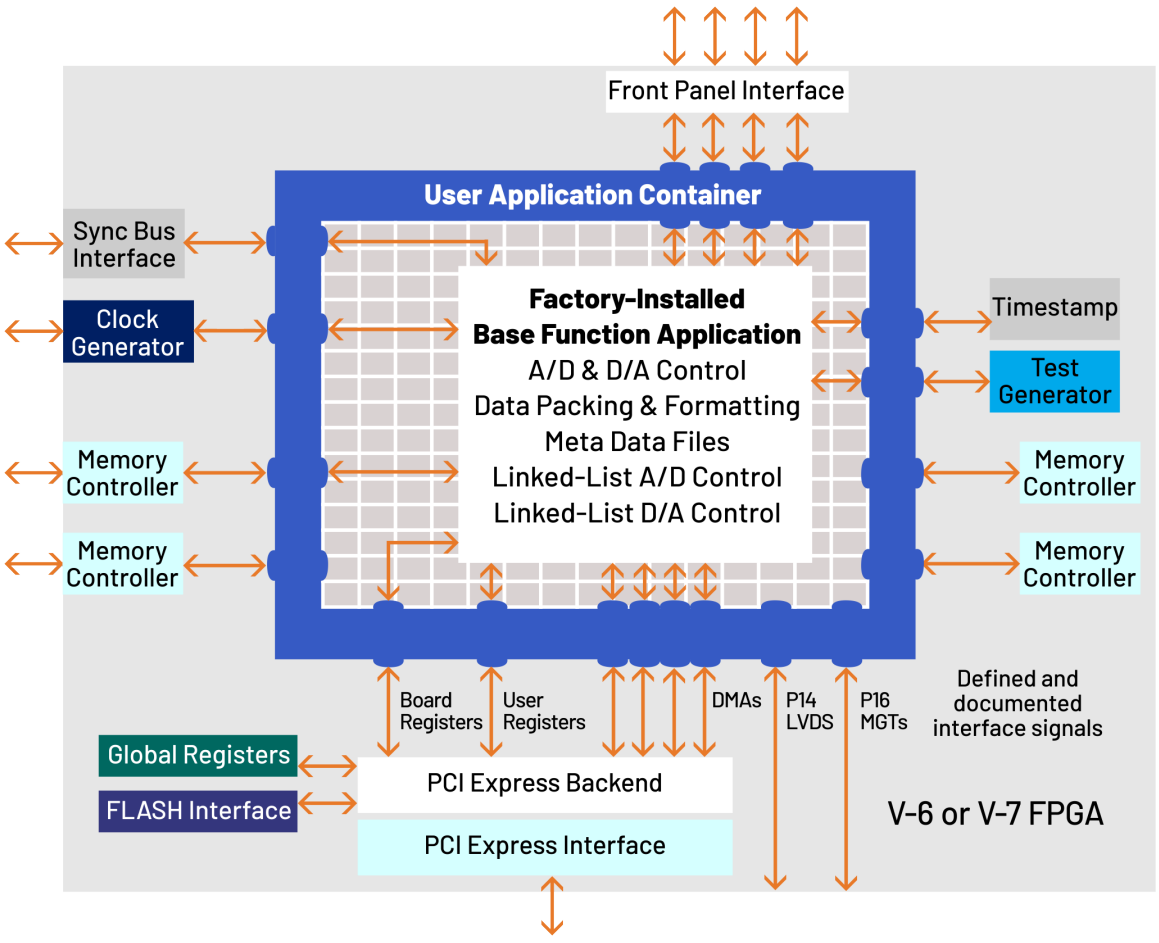
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

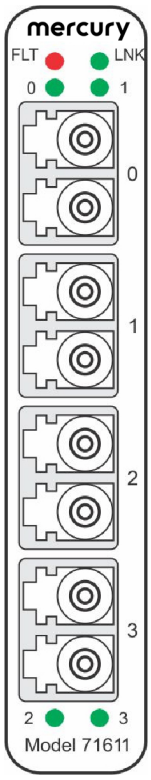
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FRONT PANEL CONNECTIONS

The XMC front panel provides four duplex input/output connectors. The front panel also includes six LEDs.



- **Fault LED:** The red **FLT** LED illuminates when an over-temperature or over-voltage condition is indicated by the temperature/voltage sensors on the PCB.
- **PCIe Link LED:** The green **LNK** LED illuminates when a valid link has been established over the PCIe interface.
- **SFPDP Port Link LEDs:** The four green SFPDP Port LEDs, two above the Port **0** connector, labeled **0** and **1** for SFPDP Ports **0** and **1** respectively, and two below the Port **3** connector, labeled **2** and **3** for SFPDF Posts **2** and **3** respectively. Each LED illuminates when a valid receive link has been established over the SFPDP interface for the Port.
- **SFPDF I/O Connectors:** Four duplex Serial FPDP (SFPDP) fiber-optic transceiver connectors, labeled **0** to **3** for SFPDP Ports **0** to **3** respectively, are provided.

SPECIFICATIONS

Front Panel Serial FPDP Inputs/Outputs

Number of Connectors: 4

Fiber Optic Connector Type: LC

Laser: 850 nm (standard, other options available)

Copper Connector Type: Micro Twinax

Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)

Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array

Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O

- Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory

- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: Half-length PCIe card

- Depth: 181 mm (7.13 in)
- Height: 111 mm (4.38 in) (including PCIe connectors)

Weight:

- PCIe Carrier: 110 grams (3.9 oz.)
- XMC Module: Approximately 14 oz. (400 grams)

ORDERING INFORMATION

Model	Description
78611	Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe

Options	Description
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280	Copper serial interfaces
-281	Multimode optical serial interfaces
-702	Air-cooled, Level 2

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71611 XMC (Quad Serial FPDP Interface with Virtex-6 FPGA) has the following variants:

Model	
52611	3U VPX board (single XMC)
57611	6U VPX board (single XMC)
58611	6U VPX board (dual XMC)
71611	XMC module
78611	PCIe board (single XMC)
7811	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

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MADE IN USA

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SERIAL FPDP VITA 17.1 COMPLIANCE

Mercury's Serial FPDP products fully comply with the VITA 17.1 specification as follows:

1. What Link Rate does the interface support?

✓ 1.0625 Gbaud ✓ 2.125 Gbaud ✓ 2.5 Gbaud ✓ 3.125 Gbaud ✓ 4.25 Gbaud

2. What Serial FPDP function does the interface support?

__Transmitter only __Receiver only ✓ Transmitter & Receiver

3. Does the Receiver support Flow Control (setting the STOP signal)?

__Always active __Not supported ✓ Optional (selectable)

4. Does the Transmitter support Flow Control (data transmission stops after a STOP signal)?

__Always active __Not supported ✓ Optional (selectable)

5. If the Transmitter supports Flow Control, after transmitting a STOP signal, how many 32-bit words can be received before a Receive FIFO overflow occurs?

✓ Programmable

6. Does the interface support CRC?

__Always active __Not supported ✓ Optional (selectable)

7. Does the Transmitter support Copy Master Mode (insertion of additional IDLE ordered sets)?

__Always active __Not supported ✓ Optional (selectable)

8. Does the Receiver support Copy Mode (re-transmission of data)?

✓ Yes __No

9. If Copy Mode is supported, what method is implemented (see VITA 17.1 Observation 6.1.4.4)?

__Method 1 ✓ Method 2

10. Does the Receiver support Copy/Loop Mode (re-transmit data and set Flow Control)?

✓ Yes __No

11. What type of media is supported?

✓ Short Wave Laser ✓ Long Wave Laser ✓ Copper

12. What type of media connectors are supported?

✓ LC __SC __ST ✓ Micro Twinax

13. Which fiber transmit data frames are supported in addition to Normal Data Fiber Frames (see VITA 17.1 Permission 7.3.3.1)?

✓ Sync without Data Fiber Frames ✓ Sync with Data Fiber Frames

14. Does the Serial FPDP Transmitter stop in response to the Serial FPDP Receiver sending NRDY True (see VITA 17.1 Observation 7.3.2.2)?

__Always __Never ✓ Optional (selectable)

15. Are status bits kept up to date when there is no data to transmit by sending empty Serial FPDP Normal Data Fiber (see VITA 17.1 Rule 7.3.3.8, Recommendation 7.3.3.2 and Suggestion 7.3.3.1)?

✓ Yes, empty frames transmitted __No, status is not updated when no data is transmitted

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