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MM6230

USERs GUIDE

MARCH 1989

HIGH PERFORMANCE EXPANSION MEMORY MODULE for the **VMEbus**

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation procedures of the **MM6230** Dynamic Random Access Memory Modules.

1.2 GENERAL DESCRIPTION

1.2.1 Configuration

The **MM6230** is compatible with **VMEbus** specifications (C.1). Inherent to the module are **VMEbus** options D32 (32 bit data path width) and A32 (32 bit address path width). The module also generates and stores an odd parity bit for each byte written on write cycles and checks parity for each byte read on read cycles. Then if a parity error is detected, the module responds by assertion of **BERR***. (see Figure 1.1).

The Memory Array is addressable as 8 bit bytes, 16 bit words, or 32 bit longwords. The **MM6230** can be configured for 4M or 8Megabytes capacity by populating it with 1024K industry standard CMOS DRAMs, such as the TC511000-12 devices. In addition, the **MM6230** Dynamic Memory Module may expanded to 16Megabytes with the addition of the **MM6235** 8Megabyte Expansion Memory Module (See Section 2.7). For Higher Performance applications, the **MM6230** Dynamic Memory Module is equipped with a **High Speed BLOCK Mode Transfer** capability. This allows the use of Block Mode Controllers, for increased system performance.

The **MM6230** is completely compatible with the MVME-133A and VME Bus Master Modules employing 68000, 68010, 68020, 68030 or N32xxx CPUs.

The **MM6230** base memory module is available in several options depending on the capacity required. Table 1.1 lists the optional part numbers for ordering purposes, the total memory capacity provided by each version.

Table 1.1 Memory Capacity Options

Option	Capacity
MM6230D/4M	4.0Megabytes
MM6230D/8M	8.0Megabytes
MM6230D/16M	8.0Megabytes
(W/MM6235/8M)	8.0Megabytes
Total	16.0Megabytes

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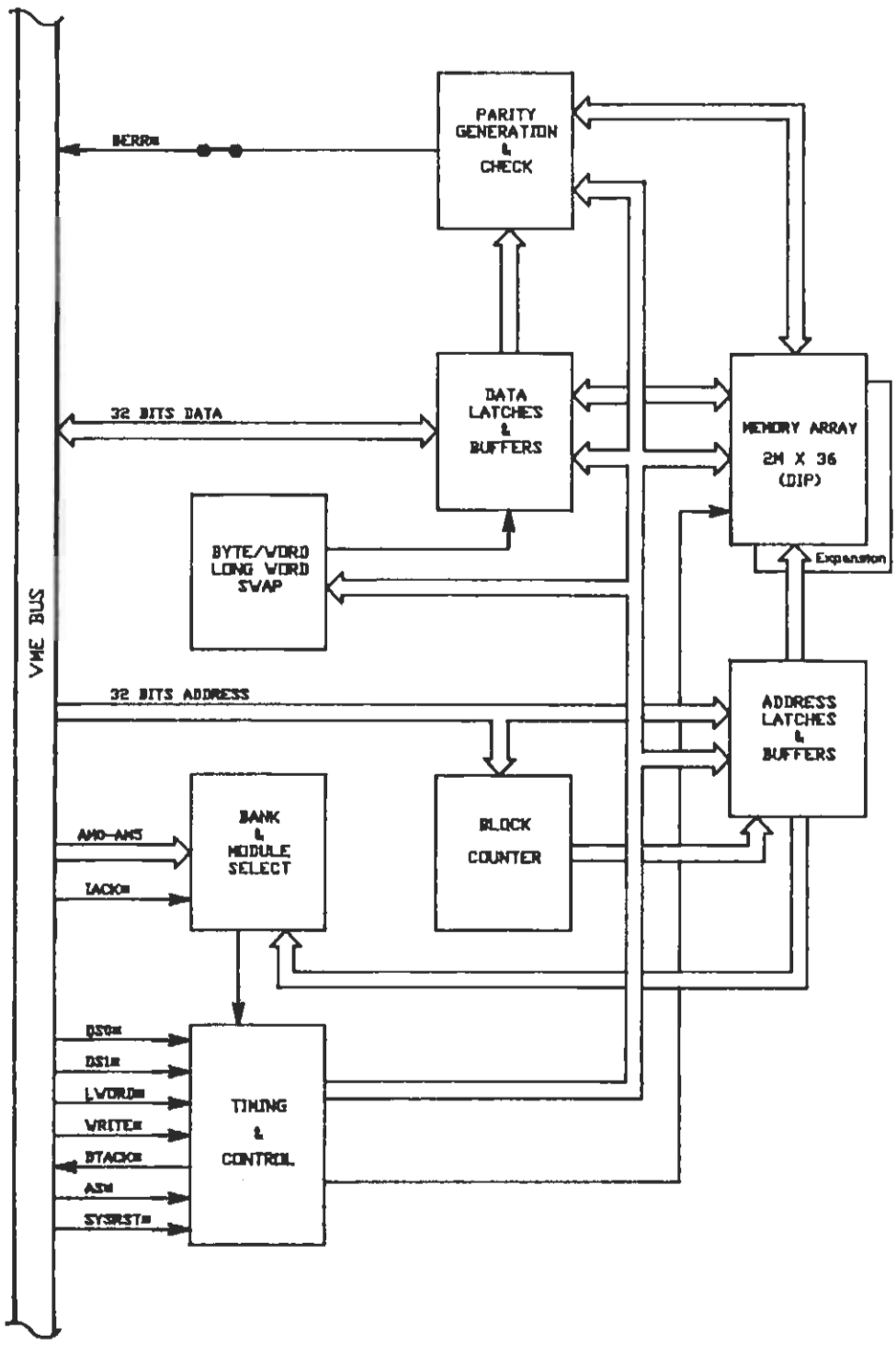


Figure 1.1 Functional Block Diagram

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1.2.2 OPERATIONAL FEATURES

The **MM6230** memory module contains its own address register and data buffers for total compatibility with the **VMEbus**.

Module selection for the **MM6230** resides on any 64K (10000 hex) bytes boundaries (A24/A32). The module may be mapped into one of the 16M byte banks, within the 4 G bytes of physical address space of the **VMEbus** (A32). The **MM6230**'s memory array is addressable as 8 bit bytes (D08),16 bit words (D16), or as 32 bit longwords (D32), using conventional read/write transfers, or HIGH Performance BLOCK Transfers (BLT).

The user must initialize the memory module to allow the parity generator to store ODD parity otherwise the module will assert BERR* for any subsequent read cycle. BERR* can be disconnected from the **VMEbus** by moving jumper E1-E2 to E2-E3 (see figure 1.2 for Jumper & Switch locations). (See Section 2.5.1 for Parity configuration).

The **MM6230** is configured to responds to various Address Modifier Codes (See Table 1.2). As shipped from the the factory the **MM6230** responds to A32 (using addresses A24-A31) only. Also shipped with the **MM6230** Dynamic Memory Module is an IFL to allow either an A32 (using addresses A24-A31) or A24 (ignoring addresses A24-A31). Other combinations are available, or by reprogramming the socketed IFL U15 (PLS153) (See Table 2.3 for IFL equations).

Table 1.2 Address Modifier Code

Hex Code	Address Modifier 5	4	3	2	1	0	Function
09	L	L	H	L	L	H	Extended Non-Privileged Data Access (32 Addr)
0A	L	L	H	L	H	L	Extended Non-Privileged Program Access (32 Addr)
0B	L	L	H	L	H	H	Extended Non-Privileged Block Transfer (32 Addr)
0D	L	L	H	H	L	H	Extended Supervisory Data Access (32 Addr)
0E	L	L	H	H	H	L	Extended Supervisory Program Access (32 Addr)
0F	L	L	H	H	H	H	Extended Supervisory Block Transfer (32 Addr)
39	H	H	H	L	L	H	Standard Non-Privileged Data Access (24 Addr)
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access (24 Addr)
3B	H	H	H	L	H	H	Standard Non-Privileged Block transfer (24 Addr)
3D	H	H	H	H	L	H	Standard Supervisory Data Access (24 Addr)
3E	H	H	H	H	H	L	Standard Supervisory Program Access (24 Addr)
3F	H	H	H	H	H	H	Standard Supervisory Block Transfer (24 Addr)

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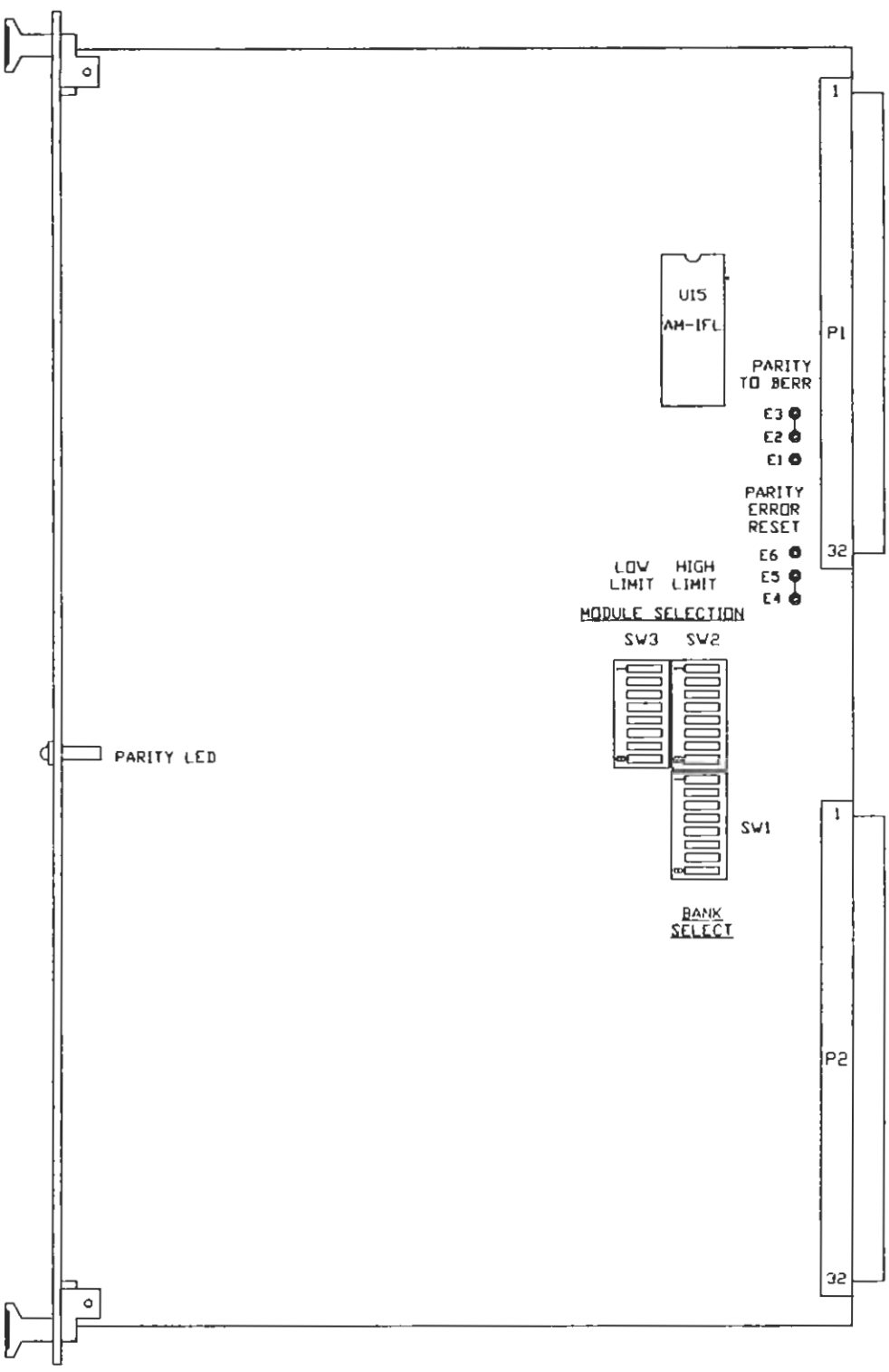


Figure 1.2 Jumper & Switch Locations

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1.3 GENERAL SPECIFICATIONS

Table 1.3 lists the general specifications for the **MM6230** DYNAMIC RAM Memory Module

Table 1.3 General Specifications

Characteristics	Specifications
Capacity	4M, 8M, 12M, or 16M,bytes
Cycle Time	250ns.
Access Time (Non-Blockmode)	190nsec Read (non-Block mode) 130nsec Write (Fast Write)
Access Time (Block Mode)	180nsec Read (Block mode) 130nsec Write (Fast Write)
Address	32 bits A32/A24/BLT/UAT VMEbus 32 bits A32/BLT/UAT VSBus
Data In/Data Out	8/16/24/32 bits bidirectional with three-state output D08/D16/D32
Modes of Operation	Read, Write, Read/Modify/Write (RMW), Block Transfers (BLT),
Un-aligned (UAT) Address Modifiers	6 bits, jumper selectable, or user programmable IFL
Parity	EVEN, 1 bit for each byte Generated on each WRITE Checked on each read
Module Selection	Memory selected on 1024K byte VMEbus and VSBus ($100000) boundary in any 16 Megabyte bank within a 4G byte address space.
Interface: Inputs	TTL-compatible
Outputs	48ma. Three-state, TTL-compatible
Operating Temperature	0 to 60 degrees C
Storage Temperature	-40 to +80 degrees C
Relative Humidity	Upto 95% without condensation
Power Requirements:	Standby Operate
+5V (fully-populated)	2.4A 2.6A
With **MM6235** Expansion	2.9A 3.1A

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Table 1.4 The VMEbus Interface Definition

NMEMONIC	TYPE	SIGNAL DESCRIPTION
ACFAIL*	O.C.	AC FAILURE - Indicates that the AC input to the power supply has been interrupted or that the necessary input voltage levels requirements are not being met.
AM0-AM5	3-S	ADDRESS MODIFIER (bits 0-5) - Master provides additional information about the address bus, such as size, cycle type, and/or dbt master identification.
AS*	3-S.	ADDRESS STROBE - Indicates that a valid address is on the address is oon the address bus.
A01-A31	3-S	ADDRESS bus (bits 1-31) - Specific physical memory address.
BBSY*	O.C.	BUS BUSY - Generated by the current DBT master to indicate that it is usion the bus.
BCLR*	3-S.	BUS CLEAR - Generated by the bus arbitrator to request release by the current DBT master for a higher level requesting master.
BERR*	O.C	BUSS ERROR - Generated by a slave to indicate that an unrecoverable error has occurred and that the bus cycle must be aborted.
BG0IN* BG3IN*	3-S.	BUS GRANT (0-3) IN - Together with BUS GRANT (0-3) OUT forms a daisy-chained bus grant. The BGxIN* signal indicates to this board that it may become the next DBT master.
BG0OUT- BG3OUT	3-S	BUS GRANT (0-3) OUT - Indicates to the next board in the daisy-chain that it may becomc the next master.
BR0*-BR3	O.C.	BUS REQUEST (0-3) - Indicates that a DBT master in the daisy-chain requires access to the (DBT) bus.
DS0*	3-S.	DATA STROBE 0 - Indicates that odd byte data is valid on the VME data transfer bus (D00-D07/D16-D23).
DS1*	3-S.	DATA STROBE 1 - Indicates that even byte data is valid on the VME data transfer bus (D08-D15/D24-D31).
DTACK*	O.C.	DATA TRANSFER ACKNOWLEDGE - Generated by a DBT slave. The leading (falling) edge indicates that read cycle data is valid or that data has been accepted during a write cycle.

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NMEMONIC	TYPE	DESCRIPTION
D00-D32	3-S	DATA BUS (bits 0 - 31) - Bidirectional data lines that provide a data path between the DTB master and slave.
GND		GROUND
IACK*	3-S./O.C.	INTERRUPT ACHNOWLEDGE - Generated by any master processing an interrupt request.
IACKIN*	3-S.	INTERRUPT ACKNOWLEDGE IN - Together with IACKOUT* forms a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	3-S.	INTERRUPT ACKNOWLEDGE OUT - Indicates to the next VME board in the daisy chain that an acknowledge cycle is in progress.
IRQ1*- IRQ7*	O.C.	INTERRUPT REQUEST (1-7) - Prioritized request for interrupt service, level 7 is the highest level, 1 is the lowest.
LWORD*	3-S.	LONG WORD - Indicates that the current data transfer is a 32 bit transfer.
SYSCLK	T.P.	SYSTEMS CLOCK - A constant 16 MHz clock that is independent of processor speed or timing.
SYSFAIL*	O.C.	SYSTEMS FAIL - Generated by any module on the VMEbus to indicate that a failure has occured in the system.
SYSRESET*	O.C.	SYSTEM RESET - When driven low, will cause a hardware system reset.
WRITE	3-S.	WRITE - When low, indicates that the data transfer cycle in progress is a write operation. When high during an address strobe, indicates a read operation is occuring.

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Table 1.5 VMEbus P1 Connector Assignment

Pin	A	B	C
1	D00	BBSY* **	D08
2	D01	BCLR* **	D09
3	D02	ACFAIL* **	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK **	BG3IN*	SYSFAIL* **
11	GND	BG3OUT*	BERR*
12	DS1*	BR0* **	SYSRESET*
13	DS0*	BR1* **	LWORD*
14	WRITE*	BR2* **	AM5
15	GND	BR3* **	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK **	A17
22	IACKOUT*	SERDAT **	A16
23	AM4	GND	A15
24	A07	IRQ7* **	A14
25	A06	IRQ6* **	A13
26	A05	IRQ5* **	A12
27	A04	IRQ4* **	A11
28	A03	IRQ3* **	A10
29	A02	IRQ2* **	A09
30	A01	IRQ1* **	A08
31	-12v **	+5vSTDBY **	+12v **
32	+5v	+5v	+5v

** - No Connection on MM6230D Memory Module

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Table 1.6 VMEbus P2 Pin Definition

Pin	A	B	C
1	USER I/O	+5v	USER I/O
2	USER I/O	GND	USER I/O
3	USER I/O	RESERVED	USER I/O
4	USER I/O	A24	USER I/O
5	USER I/O	A25	USER I/O
6	USER I/O	A26	USER I/O
7	USER I/O	A27	USER I/O
8	USER I/O	A28	USER I/O
9	USER I/O	A29	USER I/O
10	USER I/O	A30	USER I/O
11	USER I/O	A31	USER I/O
12	USER I/O	GND	USER I/O
13	USER I/O	+5v	USER I/O
14	USER I/O	D16	USER I/O
15	USER I/O	D17	USER I/O
16	USER I/O	D18	USER I/O
17	USER I/O	D19	USER I/O
18	USER I/O*	D20	USER I/O
19	USER I/O	D21	USER I/O
20	USER I/O	D22	USER I/O
21	USER I/O	D23	USER I/O
22	USER I/O	GND	USER I/O
23	USER I/O	D24	USER I/O
24	USER I/O	D25	USER I/O
25	USER I/O	D26	USER I/O
26	USER I/O	D27	USER I/O
27	USER I/O	D28	USER I/O
28	USER I/O	D29	USER I/O
29	USER I/O	D30	USER I/O
30	USER I/O	D31	USER I/O
31	USER I/O	GND	USER I/O
32	USER I/O	+5v	USER I/O

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1.4 INTERFACE TIMING

The **MM6230** memory modules are designed to accept Industry Standard 1024K x 1 DYNAMIC Random Access Memory Devices specified with an 120nsec typical access delay Time (ie. TC511000-12).

1.4.1 VMEbus Interface Timing

The Interface Timing Diagram (figure 1.3), illustrates the timing relationships on the Data Transfer bus,for Read and Write Cycles. Access delay time is measured from the leading edge of the Data strobes at the **VMEbus**. (see pg. 14 figure 1.3).

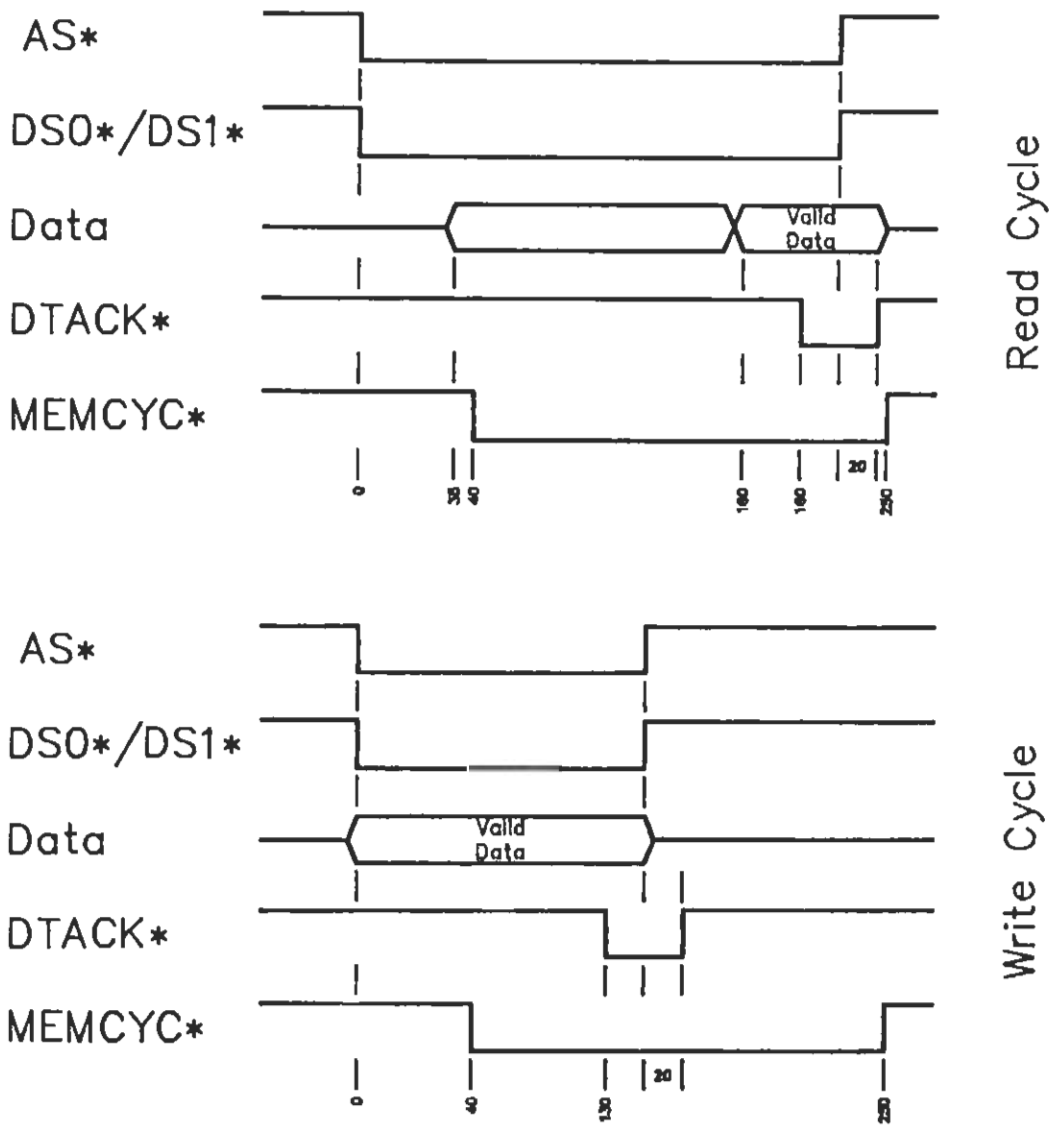


Figure 1.3 VMEbus Timing Diagram

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1.4.2 Refresh Timing

The refresh cycle timing is illustrated by figure 1.4. Refresh cycles are repeated once every 15usec. The cycle interval timing is handled by an onboard clock generator to provide a hidden refresh transparent to memory access cycles. (see pg.15 fig.1.4)

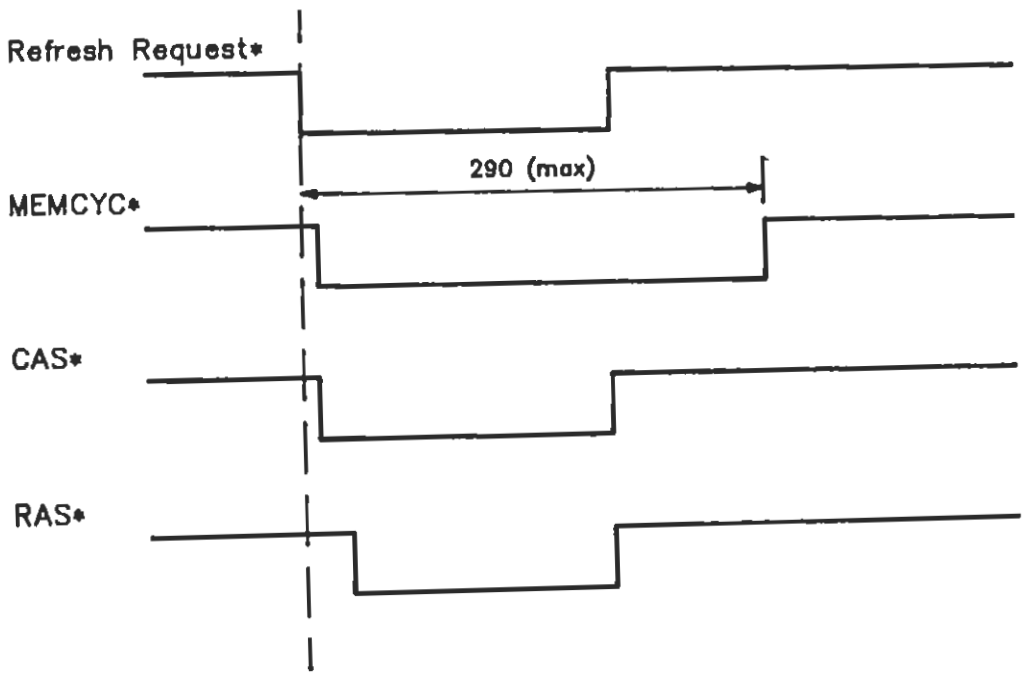


Figure 1.4 Refresh Timing Diagram

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1.5 MEMORY ARRAY ORGANIZATION

The memory array is partitioned into four 1024K x 36 bit segments. The minimum memory configuration would be 1024K x 36 bits, including the four parity bits DRAMs in segment zero. This would translate to 4 Megabytes minimum configuration for the **MM6230** Dynamic Memory Module

The **MM6230** Dynamic Memory Module is partitioned as two blocks of 36 bits each (32 plus 4 parity), however the system will only see 32 bits of data during memory references, as the parity is generated and checked transparent to the user. The 32 bits of data are divided into 4 bytes (8 bits each). While the memory reads and writes may be 8, 16 or 32 bits wide, the memory is organized as 32 bit wide locations with logic controlling which byte the user is reading or writing.

If the contents of the first 8 locations in memory are $01 $23 $45 $67 $89 $AB $CD $EF, determining which bits constitute what byte may be somewhat confusing. This can be cleared up by seeing the same data in the various formats used in most systems (IE: Byte, Word, and Longword).

BYTE Format WORD Format LONGWORD Format

```
Location Data    Location Data      Location Data
-------------------------------------------------
$00000000 $01 | $00000000 $0123 | $00000000 $01234567
$00000001 $23 | $00000002 $4567 | $00000004 $89ABCDEF
$00000002 $45 | $00000004 $89AB |
$00000003 $67 | $00000006 $CDEF |
$00000004 $89 |                 |
$00000005 $AB |                 |
$00000006 $CD |                 |
$00000007 $EF |                 |
```

BIT Organizations

LONGWORD

```
3                 1 1               0 3               1 1               0
1.............6 5.............0 1.............6 5.............0
-------------------------------------------------------------------------
```

WORD

```
1                 0 1               0 1               0 1               0
5.............0 5.............0 5.............0 5.............0
-------------------------------------------------------------------------
```

BYTE

```
0       00        0 0       00        0 0       00        0 0       00        0
7......07.......0 7......07.......0 7......07.......0 7......07.......0
00000001001000011 0100010101100111 1000100110101011 1100110111101111
$0 $1   $2  $3    $4  $5  $6  $7   $8  $9  $A  $B   $C  $D  $E  $F
```


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SECTION II
INSTALLATION

2.1 INTRODUCTION

This section details the step by step procedure to interface the **MM6230** Dynamic Memory Module with the VMEbus.

2.2 UNPACKING INSTRUCTIONS

Unpack module(s) from shipping carton. If carton is damaged upon receipt, request that the carrier's agent be present during unpacking and inspection of the equipment. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment. For repairs or replacement of a board damaged during shipment, contact Micro Memory Inc. to obtain a Return Authorization number and further instructions.

2.3 HARDWARE PREPARATION

The **MM6230** memory module should be inspected and prepared for jumper placement and switch settings prior to system installation. The following sections describe the proper jumper options and switch settings necessary for system operation. Figure 2.1 illustrates jumper and switch locations and should be referenced as necessary.

2.3.1 Handling Procedure

The **MM6230** Dynamic Memory Module uses MOS components that are susceptible to damage if exposed to static electrical charges. To avoid damage of these components during handling, testing or operation, the following procedure should be used.

- Device leads should contact conductive material to avoid building of any static charge, except during testing or operation.
- Soldering iron tips, metal fixtures, tools, and handling facilities used in preparing the module for operation should be grounded.
- Devices should never be removed or inserted while power is applied to the module because voltage transients may permanently damage the devices and/or module.
- **The memory module should never be plugged in or out of the cardcage while power is applied.**
- External signals should not be applied to device inputs while power is removed.
- Any memory module removed from the system should be transferred to either non-conductive foam or an anti-static plastic bag for storage or shipment.

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2.4 OPERATING AIRFLOW AND COOLING

An adequate airflow is required to maintain the operating temperature within specifications of the memory module.

2.5 JUMPER OPTIONS

There are several jumper options attainable on the **MM6230** Dynamic Memory Module, depending on the user application. Most of the available options are selected by installing or removing mini-jumpers on wire-wrap pins at 0.100 inch centers. See Figure 1.2 for jumper locations.

2.5.1 Reset Parity Error Selection.

The Parity Error L.E.D. will light upon detection of a parity error during a read cycle of **MM6230** Dynamic Memory Module, mini-jumpers E5-E6 allow for resetting the L.E.D. during the next cycle of the module. The **MM6230** Dynamic Memory Module as shipped, E4-E5, the Parity Error L.E.D. can ONLY be reset by **SYSRESET***.

2.5.2 Parity Reporting Selection.

As shipped, the **MM6230** Dynamic Memory Module will, upon detection of a PARITY ERROR, assert **BERR*** instead of **DTACK***. By moving E1-E2 to E2-E3, the **MM6230** Dynamic Memory Module will assert **DTACK*** regardless of the Parity status.

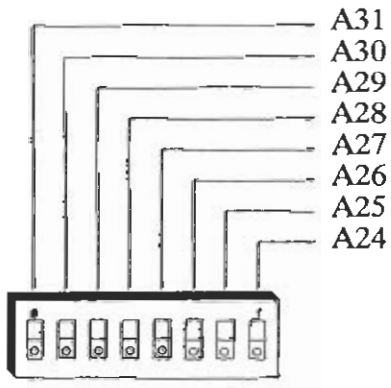
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2.6 BANK/MODULE SELECTION CONFIGURATION

Before the **MM6230** Dynamic Memory Module memory module can become truly operational, it must be mapped into an appropriate segment within the VMEbus (4G bytes) maximum address space. This can be accomplished by setting switches SW1 (bank select) & ,SW2 (upper limit) & SW3 (lower limit) See example below. (Note: The polarity of the BANK, and LIMIT switches, are REVERSED).

Table 2.1 BANK SELECTION Example

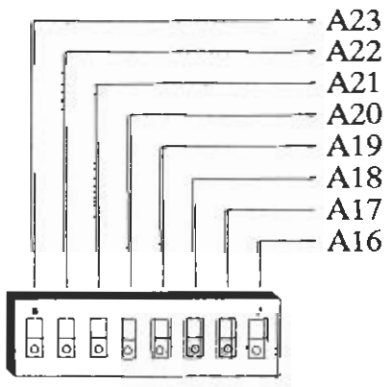
SW1 BANK SELECT ADDRESS



0 = CLOSED
1 = OPEN

SW2 UPPER LIMIT ADDRESS

SW3 LOWER LIMIT ADDRESS



1 = CLOSED
0 = OPEN

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2.7 Memory Expansion with the MM6235

The **MM6235** expansion memory module is a memory capacity expansion printed circuit board that is compatible and directly connectable to the **MM6230**'s auxiliary connector P3. Auxiliary connector P3 attaches the **MM6235** expansion module to the **MM6230**'s internal data transfer bus to provide an additional 8Megabytes of memory capacity without extending the overall height and VMEbus slot consumption of the basic **MM6230** Dynamic Memory Module.

The **MM6235** expansion memory module can be added at any future time as system demands expand.

Table 2.2 DRAM Device Locations for the MM6235 Module

BANK 3	PAR3	D24	D25	D26	D27	D28	D29	D30	D31
BANK 2	PAR3	D24	D25	D26	D27	D28	D29	D30	D31
BANK 3	PAR2	D16	D17	D18	D19	D20	D21	D22	D23
BANK 2	PAR2	D16	D17	D18	D19	D20	D21	D22	D23
BANK 3	PAR1	D08	D09	D10	D11	D12	D13	D14	D15
BANK 2	PAR1	D08	D09	D10	D11	D12	D13	D14	D15
BANK 3	PAR0	D00	D01	D02	D03	D04	D05	D06	D07
BANK 2	PAR0	D00	D01	D02	D03	D04	D05	D06	D07

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APPENDIX A

BANK SELECTION

(A24 - A31)

1 = Open
0 = Closed

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$00yyyyyy	0	0	0	0	0	0	0	0
$01yyyyyy	0	0	0	0	0	0	0	1
$02yyyyyy	0	0	0	0	0	0	1	0
$03yyyyyy	0	0	0	0	0	0	1	1
$04yyyyyy	0	0	0	0	0	1	0	0
$05yyyyyy	0	0	0	0	0	1	0	1
$06yyyyyy	0	0	0	0	0	1	1	0
$07yyyyyy	0	0	0	0	0	1	1	1
$08yyyyyy	0	0	0	0	1	0	0	0
$09yyyyyy	0	0	0	0	1	0	0	1
$0Ayyyyyy	0	0	0	0	1	0	1	0
$0Byyyyyy	0	0	0	0	1	0	1	1
$0Cyyyyyy	0	0	0	0	1	1	0	0
$0Dyyyyyy	0	0	0	0	1	1	0	1
$0Eyyyyyy	0	0	0	0	1	1	1	0
$0Fyyyyyy	0	0	0	0	1	1	1	1
$10yyyyyy	0	0	0	1	0	0	0	0
$11yyyyyy	0	0	0	1	0	0	0	1
$12yyyyyy	0	0	0	1	0	0	1	0
$13yyyyyy	0	0	0	1	0	0	1	1
$14yyyyyy	0	0	0	1	0	1	0	0
$15yyyyyy	0	0	0	1	0	1	0	1
$16yyyyyy	0	0	0	1	0	1	1	0
$17yyyyyy	0	0	0	1	0	1	1	1
$18yyyyyy	0	0	0	1	1	0	0	0
$19yyyyyy	0	0	0	1	1	0	0	1
$1Ayyyyyy	0	0	0	1	1	0	1	0
$1Byyyyyy	0	0	0	1	1	0	1	1
$1Cyyyyyy	0	0	0	1	1	1	0	0
$1Dyyyyyy	0	0	0	1	1	1	0	1
$1Eyyyyyy	0	0	0	1	1	1	1	0
$1Fyyyyyy	0	0	0	1	1	1	1	1

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$20yyyyyy	0	0	1	0	0	0	0	0
$21yyyyyy	0	0	1	0	0	0	0	1
$22yyyyyy	0	0	1	0	0	0	1	0
$23yyyyyy	0	0	1	0	0	0	1	1
$24yyyyyy	0	0	1	0	0	1	0	0
$25yyyyyy	0	0	1	0	0	1	0	1
$26yyyyyy	0	0	1	0	0	1	1	0
$27yyyyyy	0	0	1	0	0	1	1	1
$28yyyyyy	0	0	1	0	1	0	0	0
$29yyyyyy	0	0	1	0	1	0	0	1
$2Ayyyyyy	0	0	1	0	1	0	1	0
$2Byyyyyy	0	0	1	0	1	0	1	1
$2Cyyyyyy	0	0	1	0	1	1	0	0
$2Dyyyyyy	0	0	1	0	1	1	0	1
$2Eyyyyyy	0	0	1	0	1	1	1	0
$2Fyyyyyy	0	0	1	0	1	1	1	1
$30yyyyyy	0	0	1	1	0	0	0	0
$31yyyyyy	0	0	1	1	0	0	0	1
$32yyyyyy	0	0	1	1	0	0	1	0
$33yyyyyy	0	0	1	1	0	0	1	1
$34yyyyyy	0	0	1	1	0	1	0	0
$35yyyyyy	0	0	1	1	0	1	0	1
$36yyyyyy	0	0	1	1	0	1	1	0
$37yyyyyy	0	0	1	1	0	1	1	1
$38yyyyyy	0	0	1	1	1	0	0	0
$39yyyyyy	0	0	1	1	1	0	0	1
$3Ayyyyyy	0	0	1	1	1	0	1	0
$3Byyyyyy	0	0	1	1	1	0	1	1
$3Cyyyyyy	0	0	1	1	1	1	0	0
$3Dyyyyyy	0	0	1	1	1	1	0	1
$3Eyyyyyy	0	0	1	1	1	1	1	0
$3Fyyyyyy	0	0	1	1	1	1	1	1

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BANK SELECTION

(A24 - A31)

1 = Open
0 = Closed

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$40yyyyyy	0	1	0	0	0	0	0	0
$41yyyyyy	0	1	0	0	0	0	0	1
$42yyyyyy	0	1	0	0	0	0	1	0
$43yyyyyy	0	1	0	0	0	0	1	1
$44yyyyyy	0	1	0	0	0	1	0	0
$45yyyyyy	0	1	0	0	0	1	0	1
$46yyyyyy	0	1	0	0	0	1	1	0
$47yyyyyy	0	1	0	0	0	1	1	1
$48yyyyyy	0	1	0	0	1	0	0	0
$49yyyyyy	0	1	0	0	1	0	0	1
$4Ayyyyyy	0	1	0	0	1	0	1	0
$4Byyyyyy	0	1	0	0	1	0	1	1
$4Cyyyyyy	0	1	0	0	1	1	0	0
$4Dyyyyyy	0	1	0	0	1	1	0	1
$4Eyyyyyy	0	1	0	0	1	1	1	0
$4Fyyyyyy	0	1	0	0	1	1	1	1
$50yyyyyy	0	1	0	1	0	0	0	0
$51yyyyyy	0	1	0	1	0	0	0	1
$52yyyyyy	0	1	0	1	0	0	1	0
$53yyyyyy	0	1	0	1	0	0	1	1
$54yyyyyy	0	1	0	1	0	1	0	0
$55yyyyyy	0	1	0	1	0	1	0	1
$56yyyyyy	0	1	0	1	0	1	1	0
$57yyyyyy	0	1	0	1	0	1	1	1
$58yyyyyy	0	1	0	1	1	0	0	0
$59yyyyyy	0	1	0	1	1	0	0	1
$5Ayyyyyy	0	1	0	1	1	0	1	0
$5Byyyyyy	0	1	0	1	1	0	1	1
$5Cyyyyyy	0	1	0	1	1	1	0	0
$5Dyyyyyy	0	1	0	1	1	1	0	1
$5Eyyyyyy	0	1	0	1	1	1	1	0
$5Fyyyyyy	0	1	0	1	1	1	1	1

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$60yyyyyy	0	1	1	0	0	0	0	0
$61yyyyyy	0	1	1	0	0	0	0	1
$62yyyyyy	0	1	1	0	0	0	1	0
$63yyyyyy	0	1	1	0	0	0	1	1
$64yyyyyy	0	1	1	0	0	1	0	0
$65yyyyyy	0	1	1	0	0	1	0	1
$66yyyyyy	0	1	1	0	0	1	1	0
$67yyyyyy	0	1	1	0	0	1	1	1
$68yyyyyy	0	1	1	0	1	0	0	0
$69yyyyyy	0	1	1	0	1	0	0	1
$6Ayyyyyy	0	1	1	0	1	0	1	0
$6Byyyyyy	0	1	1	0	1	0	1	1
$6Cyyyyyy	0	1	1	0	1	1	0	0
$6Dyyyyyy	0	1	1	0	1	1	0	1
$6Eyyyyyy	0	1	1	0	1	1	1	0
$6Fyyyyyy	0	1	1	0	1	1	1	1
$70yyyyyy	0	1	1	1	0	0	0	0
$71yyyyyy	0	1	1	1	0	0	0	1
$72yyyyyy	0	1	1	1	0	0	1	0
$73yyyyyy	0	1	1	1	0	0	1	1
$74yyyyyy	0	1	1	1	0	1	0	0
$75yyyyyy	0	1	1	1	0	1	0	1
$76yyyyyy	0	1	1	1	0	1	1	0
$77yyyyyy	0	1	1	1	0	1	1	1
$78yyyyyy	0	1	1	1	1	0	0	0
$79yyyyyy	0	1	1	1	1	0	0	1
$7Ayyyyyy	0	1	1	1	1	0	1	0
$7Byyyyyy	0	1	1	1	1	0	1	1
$7Cyyyyyy	0	1	1	1	1	1	0	0
$7Dyyyyyy	0	1	1	1	1	1	0	1
$7Eyyyyyy	0	1	1	1	1	1	1	0
$7Fyyyyyy	0	1	1	1	1	1	1	1

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BANK SELECTION

(A24 - A31)

1 = Open
0 = Closed

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$80yyyyyy	1	0	0	0	0	0	0	0
$81yyyyyy	1	0	0	0	0	0	0	1
$82yyyyyy	1	0	0	0	0	0	1	0
$83yyyyyy	1	0	0	0	0	0	1	1
$84yyyyyy	1	0	0	0	0	1	0	0
$85yyyyyy	1	0	0	0	0	1	0	1
$86yyyyyy	1	0	0	0	0	1	1	0
$87yyyyyy	1	0	0	0	0	1	1	1
$88yyyyyy	1	0	0	0	1	0	0	0
$89yyyyyy	1	0	0	0	1	0	0	1
$8Ayyyyyy	1	0	0	0	1	0	1	0
$8Byyyyyy	1	0	0	0	1	0	1	1
$8Cyyyyyy	1	0	0	0	1	1	0	0
$8Dyyyyyy	1	0	0	0	1	1	0	1
$8Eyyyyyy	1	0	0	0	1	1	1	0
$8Fyyyyyy	1	0	0	0	1	1	1	1
$90yyyyyy	1	0	0	1	0	0	0	0
$91yyyyyy	1	0	0	1	0	0	0	1
$92yyyyyy	1	0	0	1	0	0	1	0
$93yyyyyy	1	0	0	1	0	0	1	1
$94yyyyyy	1	0	0	1	0	1	0	0
$95yyyyyy	1	0	0	1	0	1	0	1
$96yyyyyy	1	0	0	1	0	1	1	0
$97yyyyyy	1	0	0	1	0	1	1	1
$98yyyyyy	1	0	0	1	1	0	0	0
$99yyyyyy	1	0	0	1	1	0	0	1
$9Ayyyyyy	1	0	0	1	1	0	1	0
$9Byyyyyy	1	0	0	1	1	0	1	1
$9Cyyyyyy	1	0	0	1	1	1	0	0
$9Dyyyyyy	1	0	0	1	1	1	0	1
$9Eyyyyyy	1	0	0	1	1	1	1	0
$9Fyyyyyy	1	0	0	1	1	1	1	1

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$A0yyyyyy	1	0	1	0	0	0	0	0
$A1yyyyyy	1	0	1	0	0	0	0	1
$A2yyyyyy	1	0	1	0	0	0	1	0
$A3yyyyyy	1	0	1	0	0	0	1	1
$A4yyyyyy	1	0	1	0	0	1	0	0
$A5yyyyyy	1	0	1	0	0	1	0	1
$A6yyyyyy	1	0	1	0	0	1	1	0
$A7yyyyyy	1	0	1	0	0	1	1	1
$A8yyyyyy	1	0	1	0	1	0	0	0
$A9yyyyyy	1	0	1	0	1	0	0	1
$AAyyyyyy	1	0	1	0	1	0	1	0
$AByyyyyy	1	0	1	0	1	0	1	1
$ACyyyyyy	1	0	1	0	1	1	0	0
$ADyyyyyy	1	0	1	0	1	1	0	1
$AEyyyyyy	1	0	1	0	1	1	1	0
$AFyyyyyy	1	0	1	0	1	1	1	1
$B0yyyyyy	1	0	1	1	0	0	0	0
$B1yyyyyy	1	0	1	1	0	0	0	1
$B2yyyyyy	1	0	1	1	0	0	1	0
$B3yyyyyy	1	0	1	1	0	0	1	1
$B4yyyyyy	1	0	1	1	0	1	0	0
$B5yyyyyy	1	0	1	1	0	1	0	1
$B6yyyyyy	1	0	1	1	0	1	1	0
$B7yyyyyy	1	0	1	1	0	1	1	1
$B8yyyyyy	1	0	1	1	1	0	0	0
$B9yyyyyy	1	0	1	1	1	0	0	1
$B9yyyyyy	1	0	1	1	1	0	0	1
$BByyyyyy	1	0	1	1	1	0	1	1
$BCyyyyyy	1	0	1	1	1	1	0	0
$BDyyyyyy	1	0	1	1	1	1	0	1
$BEyyyyyy	1	0	1	1	1	1	1	0
$BFyyyyyy	1	0	1	1	1	1	1	1

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BANK SELECTION

(A24 - A31)

1 = Open
0 = Closed

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$C0yyyyyy	1	1	0	0	0	0	0	0
$C1yyyyyy	1	1	0	0	0	0	0	1
$C2yyyyyy	1	1	0	0	0	0	1	0
$C3yyyyyy	1	1	0	0	0	0	1	1
$C4yyyyyy	1	1	0	0	0	1	0	0
$C5yyyyyy	1	1	0	0	0	1	0	1
$C6yyyyyy	1	1	0	0	0	1	1	0
$C7yyyyyy	1	1	0	0	0	1	1	1
$C8yyyyyy	1	1	0	0	1	0	0	0
$C9yyyyyy	1	1	0	0	1	0	0	1
$CAyyyyyy	1	1	0	0	1	0	1	0
$CByyyyyy	1	1	0	0	1	0	1	1
$CCyyyyyy	1	1	0	0	1	1	0	0
$CDyyyyyy	1	1	0	0	1	1	0	1
$CEyyyyyy	1	1	0	0	1	1	1	0
$CFyyyyyy	1	1	0	0	1	1	1	1
$D0yyyyyy	1	1	0	1	0	0	0	0
$D1yyyyyy	1	1	0	1	0	0	0	1
$D2yyyyyy	1	1	0	1	0	0	1	0
$D3yyyyyy	1	1	0	1	0	0	1	1
$D4yyyyyy	1	1	0	1	0	1	0	0
$D5yyyyyy	1	1	0	1	0	1	0	1
$D6yyyyyy	1	1	0	1	0	1	1	0
$D7yyyyyy	1	1	0	1	0	1	1	1
$D8yyyyyy	1	1	0	1	1	0	0	0
$D9yyyyyy	1	1	0	1	1	0	0	1
$DAyyyyyy	1	1	0	1	1	0	1	0
$DByyyyyy	1	1	0	1	1	0	1	1
$DCyyyyyy	1	1	0	1	1	1	0	0
$DDyyyyyy	1	1	0	1	1	1	0	1
$DEyyyyyy	1	1	0	1	1	1	1	0
$DFyyyyyy	1	1	0	1	1	1	1	1

BANK SELECTED	SW 1 8	7	6	5	4	3	2	1
$E0yyyyyy	1	1	1	0	0	0	0	0
$E1yyyyyy	1	1	1	0	0	0	0	1
$E2yyyyyy	1	1	1	0	0	0	1	0
$E3yyyyyy	1	1	1	0	0	0	1	1
$E4yyyyyy	1	1	1	0	0	1	0	0
$E5yyyyyy	1	1	1	0	0	1	0	1
$E6yyyyyy	1	1	1	0	0	1	1	0
$E7yyyyyy	1	1	1	0	0	1	1	1
$E8yyyyyy	1	1	1	0	1	0	0	0
$E9yyyyyy	1	1	1	0	1	0	0	1
$EAyyyyyy	1	1	1	0	1	0	1	0
$EByyyyyy	1	1	1	0	1	0	1	1
$ECyyyyyy	1	1	1	0	1	1	0	0
$EDyyyyyy	1	1	1	0	1	1	0	1
$EEyyyyyy	1	1	1	0	1	1	1	0
$EFyyyyyy	1	1	1	0	1	1	1	1
$F0yyyyyy	1	1	1	1	0	0	0	0
$F1yyyyyy	1	1	1	1	0	0	0	1
$F2yyyyyy	1	1	1	1	0	0	1	0
$F3yyyyyy	1	1	1	1	0	0	1	1
$F4yyyyyy	1	1	1	1	0	1	0	0
$F5yyyyyy	1	1	1	1	0	1	0	1
$F6yyyyyy	1	1	1	1	0	1	1	0
$F7yyyyyy	1	1	1	1	0	1	1	1
$F8yyyyyy	1	1	1	1	1	0	0	0
$F9yyyyyy	1	1	1	1	1	0	0	1
$FAyyyyyy	1	1	1	1	1	0	1	0
$FByyyyyy	1	1	1	1	1	0	1	1
$FCyyyyyy	1	1	1	1	1	1	0	0
$FDyyyyyy	1	1	1	1	1	1	0	1
$FEyyyyyy	1	1	1	1	1	1	1	0
$FFyyyyyy	1	1	1	1	1	1	1	1

yyyyyy = Lower / Upper Limit Select Setting (See Appendix B)

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APPENDIX B

MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 3 8	7	6	5	4	3	2	1
$xx000000	0	0	0	0	0	0	0	0
$xx010000	0	0	0	0	0	0	0	1
$xx020000	0	0	0	0	0	0	1	0
$xx030000	0	0	0	0	0	0	1	1
$xx040000	0	0	0	0	0	1	0	0
$xx050000	0	0	0	0	0	1	0	1
$xx060000	0	0	0	0	0	1	1	0
$xx070000	0	0	0	0	0	1	1	1
$xx080000	0	0	0	0	1	0	0	0
$xx090000	0	0	0	0	1	0	0	1
$xx0A0000	0	0	0	0	1	0	1	0
$xx0B0000	0	0	0	0	1	0	1	1
$xx0C0000	0	0	0	0	1	1	0	0
$xx0D0000	0	0	0	0	1	1	0	1
$xx0E0000	0	0	0	0	1	1	1	0
$xx0F0000	0	0	0	0	1	1	1	1
$xx100000	0	0	0	1	0	0	0	0
$xx110000	0	0	0	1	0	0	0	1
$xx120000	0	0	0	1	0	0	1	0
$xx130000	0	0	0	1	0	0	1	1
$xx140000	0	0	0	1	0	1	0	0
$xx150000	0	0	0	1	0	1	0	1
$xx160000	0	0	0	1	0	1	1	0
$xx170000	0	0	0	1	0	1	1	1
$xx180000	0	0	0	1	1	0	0	0
$xx190000	0	0	0	1	1	0	0	1
$xx1A0000	0	0	0	1	1	0	1	0
$xx1B0000	0	0	0	1	1	0	1	1
$xx1C0000	0	0	0	1	1	1	0	0
$xx1D0000	0	0	0	1	1	1	0	1
$xx1E0000	0	0	0	1	1	1	1	0
$xx1F0000	0	0	0	1	1	1	1	1

UPPER LIMIT SELECTED	SW 2 8	7	6	5	4	3	2	1
$xx00FFFF	0	0	0	0	0	0	0	0
$xx01FFFF	0	0	0	0	0	0	0	1
$xx02FFFF	0	0	0	0	0	0	1	0
$xx03FFFF	0	0	0	0	0	0	1	1
$xx04FFFF	0	0	0	0	0	1	0	0
$xx05FFFF	0	0	0	0	0	1	0	1
$xx06FFFF	0	0	0	0	0	1	1	0
$xx07FFFF	0	0	0	0	0	1	1	1
$xx08FFFF	0	0	0	0	1	0	0	0
$xx09FFFF	0	0	0	0	1	0	0	1
$xx0AFFFF	0	0	0	0	1	0	1	0
$xx0BFFFF	0	0	0	0	1	0	1	1
$xx0CFFFF	0	0	0	0	1	1	0	0
$xx0DFFFF	0	0	0	0	1	1	0	1
$xx0EFFFF	0	0	0	0	1	1	1	0
$xx0FFFFF	0	0	0	0	1	1	1	1
$xx10FFFF	0	0	0	1	0	0	0	0
$xx11FFFF	0	0	0	1	0	0	0	1
$xx12FFFF	0	0	0	1	0	0	1	0
$xx13FFFF	0	0	0	1	0	0	1	1
$xx14FFFF	0	0	0	1	0	1	0	0
$xx15FFFF	0	0	0	1	0	1	0	1
$xx16FFFF	0	0	0	1	0	1	1	0
$xx17FFFF	0	0	0	1	0	1	1	1
$xx18FFFF	0	0	0	1	1	0	0	0
$xx19FFFF	0	0	0	1	1	0	0	1
$xx1AFFFF	0	0	0	1	1	0	1	0
$xx1BFFFF	0	0	0	1	1	0	1	1
$xx1CFFFF	0	0	0	1	1	1	0	0
$xx1DFFFF	0	0	0	1	1	1	0	1
$xx1EFFFF	0	0	0	1	1	1	1	0
$xx1FFFFF	0	0	0	1	1	1	1	1

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MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xx200000	0	0	1	0	0	0	0	0
$xx210000	0	0	1	0	0	0	0	1
$xz2Z0000	0	0	1	0	0	0	1	0
$xx220000	0	0	1	0	0	0	1	1
$xx230000	0	0	1	0	0	1	0	0
$xx24FFFF	0	0	1	0	0	1	0	1
$xx260000	0	0	1	0	0	1	1	0
$xx270000	0	0	1	0	0	1	1	1
$xx280000	0	0	1	0	1	0	0	0
$xx290000	0	0	1	0	1	0	0	1
$xx2A0000	0	0	1	0	1	0	1	0
$xx2B0000	0	0	1	0	1	0	1	1
$xx2C0000	0	0	1	0	1	1	0	0
$xx2D0000	0	0	1	0	1	1	0	1
$xx2E0000	0	0	1	0	1	1	1	0
$xx2F0000	0	0	1	0	1	1	1	1
$xx300000	0	0	1	1	0	0	0	0
$xx310000	0	0	1	1	0	0	0	1
$xx320000	0	0	1	1	0	0	1	0
$xx330000	0	0	1	1	0	0	1	1
$xx340000	0	0	1	1	0	1	0	0
$xx350000	0	0	1	1	0	1	0	1
$xx360000	0	0	1	1	0	1	1	0
$xx370000	0	0	1	1	0	1	1	1
$xx380000	0	0	1	1	1	0	0	0
$xx390000	0	0	1	1	1	0	0	1
$xx3A0000	0	0	1	1	1	0	1	0
$xx3B0000	0	0	1	1	1	0	1	1
$xx3C0000	0	0	1	1	1	1	0	0
$xx3D0000	0	0	1	1	1	1	0	1
$xx3E0000	0	0	1	1	1	1	1	0
$xx3F0000	0	0	1	1	1	1	1	1

UPPER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xx20FFFF	0	0	1	0	0	0	0	0
$xx21FFFF	0	0	1	0	0	0	0	1
$xx22FFFF	0	0	1	0	0	0	1	0
$xx23FFFF	0	0	1	0	0	0	1	1
$xx240000	0	0	1	0	0	1	0	0
$xx250000	0	0	1	0	0	1	0	1
$xx26FFFF	0	0	1	0	0	1	1	0
$xx27FFFF	0	0	1	0	0	1	1	1
$xx28FFFF	0	0	1	0	1	0	0	0
$xx29FFFF	0	0	1	0	1	0	0	1
$xx2AFFFF	0	0	1	0	1	0	1	0
$xx2BFFFF	0	0	1	0	1	0	1	1
$xx2VFFFF	0	0	1	0	1	1	0	0
$xx2DFFFF	0	0	1	0	1	1	0	1
$xx2EFFFF	0	0	1	0	1	1	1	0
$xx2FFFFF	0	0	1	0	1	1	1	1
$xx30FFFF	0	0	1	1	0	0	0	0
$xx31FFFF	0	0	1	1	0	0	0	1
$xx32FFFF	0	0	1	1	0	0	1	0
$xx33FFFF	0	0	1	1	0	0	1	1
$xx34FFFF	0	0	1	1	0	1	0	0
$xx35FFFF	0	0	1	1	0	1	0	1
$xx36FFFF	0	0	1	1	0	1	1	0
$xx37FFFF	0	0	1	1	0	1	1	1
$xx38FFFF	0	0	1	1	1	0	0	0
$xx39FFFF	0	0	1	1	1	0	0	1
$xx3AFFFF	0	0	1	1	1	0	1	0
$xx3BFFFF	0	0	1	1	1	0	1	1
$xx3CFFFF	0	0	1	1	1	1	0	0
$xx3DFFFF	0	0	1	1	1	1	0	1
$xx3EFFFF	0	0	1	1	1	1	1	0
$xx3FFFFF	0	0	1	1	1	1	1	1

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MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xx400000	0	1	0	0	0	0	0	0
$xx410000	0	1	0	0	0	0	0	1
$xx420000	0	1	0	0	0	0	1	0
$xx430000	0	1	0	0	0	0	1	1
$xx440000	0	1	0	0	0	1	0	0
$xx450000	0	1	0	0	0	1	0	1
$xx460000	0	1	0	0	0	1	1	0
$xx470000	0	1	0	0	0	1	1	1
$xx480000	0	1	0	0	1	0	0	0
$xx490000	0	1	0	0	1	0	0	1
$xx4A0000	0	1	0	0	1	0	1	0
$xx4B0000	0	1	0	0	1	0	1	1
$xx4C0000	0	1	0	0	1	1	0	0
$xx4D0000	0	1	0	0	1	1	0	1
$xx4E0000	0	1	0	0	1	1	1	0
$xx4F0000	0	1	0	0	1	1	1	1
$xx500000	0	1	0	1	0	0	0	0
$xx510000	0	1	0	1	0	0	0	1
$xx520000	0	1	0	1	0	0	1	0
$xx530000	0	1	0	1	0	0	1	1
$xx540000	0	1	0	1	0	1	0	0
$xx550000	0	1	0	1	0	1	0	1
$xx560000	0	1	0	1	0	1	1	0
$xx570000	0	1	0	1	0	1	1	1
$xx580000	0	1	0	1	1	0	0	0
$xx590000	0	1	0	1	1	0	0	1
$xx5A0000	0	1	0	1	1	0	1	0
$xx5B0000	0	1	0	1	1	0	1	1
$xx5C0000	0	1	0	1	1	1	0	0
$xx5D0000	0	1	0	1	1	1	0	1
$xx5E0000	0	1	0	1	1	1	1	0
$xx5F0000	0	1	0	1	1	1	1	1

UPPER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xx40FFFF	0	1	0	0	0	0	0	0
$xx41FFFF	0	1	0	0	0	0	0	1
$xx42FFFF	0	1	0	0	0	0	1	0
$xx43FFFF	0	1	0	0	0	0	1	1
$xx44FFFF	0	1	0	0	0	1	0	0
$xx45FFFF	0	1	0	0	0	1	0	1
$xx46FFFF	0	1	0	0	0	1	1	0
$xx47FFFF	0	1	0	0	0	1	1	1
$xx48FFFF	0	1	0	0	1	0	0	0
$xx49FFFF	0	1	0	0	1	0	0	1
$xx4AFFFF	0	1	0	0	1	0	1	0
$xx4BFFFF	0	1	0	0	1	0	1	1
$xx4CFFFF	0	1	0	0	1	1	0	0
$xx4DFFFF	0	1	0	0	1	1	0	1
$xx4EFFFF	0	1	0	0	1	1	1	0
$xx4FFFFF	0	1	0	0	1	1	1	1
$xx50FFFF	0	1	0	1	0	0	0	0
$xx51FFFF	0	1	0	1	0	0	0	1
$xx52FFFF	0	1	0	1	0	0	1	0
$xx53FFFF	0	1	0	1	0	0	1	1
$xx54FFFF	0	1	0	1	0	1	0	0
$xx55FFFF	0	1	0	1	0	1	0	1
$xx56FFFF	0	1	0	1	0	1	1	0
$xx57FFFF	0	1	0	1	0	1	1	1
$xx58FFFF	0	1	0	1	1	0	0	0
$xx59FFFF	0	1	0	1	1	0	0	1
$xx5AFFFF	0	1	0	1	1	0	0	1
$xx5BFFFF	0	1	0	1	1	0	1	1
$xx5CFFFF	0	1	0	1	1	1	0	0
$xx5DFFFF	0	1	0	1	1	1	0	1
$xx5EFFFF	0	1	0	1	1	1	1	0
$xx5FFFFF	0	1	0	1	1	1	1	1

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MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xx600000	0	1	1	0	0	0	0	0
$xx610000	0	1	1	0	0	0	0	1
$xx620000	0	1	1	0	0	0	1	0
$xx630000	0	1	1	0	0	0	1	1
$xx640000	0	1	1	0	0	1	0	0
$xx650000	0	1	1	0	0	1	0	1
$xx660000	0	1	1	0	0	1	1	0
$xx670000	0	1	1	0	0	1	1	1
$xx680000	0	1	1	0	1	0	0	0
$xx690000	0	1	1	0	1	0	0	1
$xx6A0000	0	1	1	0	1	0	1	0
$xx6B0000	0	1	1	0	1	0	1	1
$xx6C0000	0	1	1	0	1	1	0	0
$xx6D0000	0	1	1	0	1	1	0	1
$xx6E0000	0	1	1	0	1	1	1	0
$xx6F0000	0	1	1	0	1	1	1	1
$xx700000	0	1	1	1	0	0	0	0
$xx710000	0	1	1	1	0	0	0	1
$xx720000	0	1	1	1	0	0	1	0
$xx730000	0	1	1	1	0	0	1	1
$xx740000	0	1	1	1	0	1	0	0
$xx750000	0	1	1	1	0	1	0	1
$xx760000	0	1	1	1	0	1	1	0
$xx770000	0	1	1	1	0	1	1	1
$xx780000	0	1	1	1	1	0	0	0
$xx790000	0	1	1	1	1	0	0	1
$xx7A0000	0	1	1	1	1	0	1	0
$xx7B0000	0	1	1	1	1	0	1	1
$xx7C0000	0	1	1	1	1	1	0	0
$xx7D0000	0	1	1	1	1	1	0	1
$xx7E0000	0	1	1	1	1	1	1	0
$xx7F0000	0	1	1	1	1	1	1	1

UPPER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xx60FFFF	0	1	1	0	0	0	0	0
$xx61FFFF	0	1	1	0	0	0	0	1
$xx62FFFF	0	1	1	0	0	0	1	0
$xx63FFFF	0	1	1	0	0	0	1	1
$xx64FFFF	0	1	1	0	0	1	0	0
$xx65FFFF	0	1	1	0	0	1	0	1
$xx66FFFF	0	1	1	0	0	1	1	0
$xx67FFFF	0	1	1	0	0	1	1	1
$xx68FFFF	0	1	1	0	1	0	0	0
$xx69FFFF	0	1	1	0	1	0	0	1
$xx6AFFFF	0	1	1	0	1	0	1	0
$xx6BFFFF	0	1	1	0	1	0	1	1
$xx6CFFFF	0	1	1	0	1	1	0	0
$xx6DFFFF	0	1	1	0	1	1	0	1
$xx6EFFFF	0	1	1	0	1	1	1	0
$xx6FFFFF	0	1	1	0	1	1	1	1
$xx70FFFF	0	1	1	1	0	0	0	0
$xx71FFFF	0	1	1	1	0	0	0	1
$xx72FFFF	0	1	1	1	0	0	1	0
$xx73FFFF	0	1	1	1	0	0	1	1
$xx74FFFF	0	1	1	1	0	1	0	0
$xx75FFFF	0	1	1	1	0	1	0	1
$xx76FFFF	0	1	1	1	0	1	1	0
$xx77FFFF	0	1	1	1	0	1	1	1
$xx78FFFF	0	1	1	1	1	0	0	0
$xx79FFFF	0	1	1	1	1	0	0	1
$xx7AFFFF	0	1	1	1	1	0	1	0
$xx7BFFFF	0	1	1	1	1	0	1	1
$xx7CFFFF	0	1	1	1	1	1	0	0
$xx7DFFFF	0	1	1	1	1	1	0	1
$xx7EFFFF	0	1	1	1	1	1	1	0
$xx7FFFFF	0	1	1	1	1	1	1	1

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MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 3 8	7	6	5	4	3	2	1	UPPER LIMIT SELECTED	SW 2 8	7	6	5	4	3	2	1
$xx800000	1	0	0	0	0	0	0	0	$xx80FFFF	1	0	0	0	0	0	0	0
$xx810000	1	0	0	0	0	0	0	1	$xx81FFFF	1	0	0	0	0	0	0	1
$xx820000	1	0	0	0	0	0	1	0	$xx82FFFF	1	0	0	0	0	0	1	0
$xx830000	1	0	0	0	0	0	1	1	$xx83FFFF	1	0	0	0	0	0	1	1
$xx840000	1	0	0	0	0	1	0	0	$xx84FFFF	1	0	0	0	0	1	0	0
$xx850000	1	0	0	0	0	1	0	1	$xx85FFFF	1	0	0	0	0	1	0	1
$xx860000	1	0	0	0	0	1	1	0	$xx86FFFF	1	0	0	0	0	1	1	0
$xx870000	1	0	0	0	0	1	1	1	$xx87FFFF	1	0	0	0	0	1	1	1
$xx880000	1	0	0	0	1	0	0	0	$xx88FFFF	1	0	0	0	1	0	0	0
$xx890000	1	0	0	0	1	0	0	1	$xx89FFFF	1	0	0	0	1	0	0	1
$xx8A0000	1	0	0	0	1	0	1	0	$xx8AFFFF	1	0	0	0	1	0	1	0
$xx8B0000	1	0	0	0	1	0	1	1	$xx8BFFFF	1	0	0	0	1	0	1	1
$xx8C0000	1	0	0	0	1	1	0	0	$xx8CFFFF	1	0	0	0	1	1	0	0
$xx8D0000	1	0	0	0	1	1	0	1	$xx8DFFFF	1	0	0	0	1	1	0	1
$xx8E0000	1	0	0	0	1	1	1	0	$xx8EFFFF	1	0	0	0	1	1	1	0
$xx8F0000	1	0	0	0	1	1	1	1	$xx8FFFFF	1	0	0	0	1	1	1	1
$xx900000	1	0	0	1	0	0	0	0	$xx90FFFF	1	0	0	1	0	0	0	0
$xx910000	1	0	0	1	0	0	0	1	$xx91FFFF	1	0	0	1	0	0	0	1
$xx920000	1	0	0	1	0	0	1	0	$xx92FFFF	1	0	0	1	0	0	1	0
$xx930000	1	0	0	1	0	0	1	1	$xx93FFFF	1	0	0	1	0	0	1	1
$xx940000	1	0	0	1	0	1	0	0	$xx94FFFF	1	0	0	1	0	1	0	0
$xx950000	1	0	0	1	0	1	0	1	$xx95FFFF	1	0	0	1	0	1	0	1
$xx960000	1	0	0	1	0	1	1	0	$xx96FFFF	1	0	0	1	0	1	1	0
$xx970000	1	0	0	1	0	1	1	1	$xx97FFFF	1	0	0	1	0	1	1	1
$xx980000	1	0	0	1	1	0	0	0	$xx98FFFF	1	0	0	1	1	0	0	0
$xx990000	1	0	0	1	1	0	0	1	$xx99FFFF	1	0	0	1	1	0	0	1
$xx9A0000	1	0	0	1	1	0	1	0	$xx9AFFFF	1	0	0	1	1	0	1	0
$xx9B0000	1	0	0	1	1	0	1	1	$xx9BFFFF	1	0	0	1	1	0	1	1
$xx9C0000	1	0	0	1	1	1	0	0	$xx9CFFFF	1	0	0	1	1	1	0	0
$xx9D0000	1	0	0	1	1	1	0	1	$xx9DFFFF	1	0	0	1	1	1	0	1
$xx9E0000	1	0	0	1	1	1	1	0	$xx9EFFFF	1	0	0	1	1	1	1	0
$xx9F0000	1	0	0	1	1	1	1	1	$xx9FFFFF	1	0	0	1	1	1	1	1

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MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1	UPPER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xxA00000	1	0	1	0	0	0	0	0	$xxA0FFFF	1	0	1	0	0	0	0	0
$xxA10000	1	0	1	0	0	0	0	1	$xxA1FFFF	1	0	1	0	0	0	0	1
$xxA20000	1	0	1	0	0	0	1	0	$xxA2FFFF	1	0	1	0	0	0	1	0
$xxA30000	1	0	1	0	0	0	1	1	$xxA3FFFF	1	0	1	0	0	0	1	1
$xxA40000	1	0	1	0	0	1	0	0	$xxA40000	1	0	1	0	0	1	0	0
$xxA5FFFF	1	0	1	0	0	1	0	1	$xxA50000	1	0	1	0	0	1	0	1
$xxA60000	1	0	1	0	0	1	1	0	$xxA6FFFF	1	0	1	0	0	1	1	0
$xxA70000	1	0	1	0	0	1	1	1	$xxA7FFFF	1	0	1	0	0	1	1	1
$xxA80000	1	0	1	0	1	0	0	0	$xxA8FFFF	1	0	1	0	1	0	0	0
$xxA90000	1	0	1	0	1	0	0	1	$xxA9FFFF	1	0	1	0	1	0	0	1
$xxAA0000	1	0	1	0	1	0	1	0	$xxAAFFFF	1	0	1	0	1	0	1	0
$xxAB0000	1	0	1	0	1	0	1	1	$xxABFFFF	1	0	1	0	1	0	1	1
$xxAC0000	1	0	1	0	1	1	0	0	$xxACFFFF	1	0	1	0	1	1	0	0
$xxAD0000	1	0	1	0	1	1	0	1	$xxADFFFF	1	0	1	0	1	1	0	1
$xxAE0000	1	0	1	0	1	1	1	0	$xxAEFFFF	1	0	1	0	1	1	1	0
$xxAF0000	1	0	1	0	1	1	1	1	$xxAFFFFF	1	0	1	0	1	1	1	1
$xxB00000	1	0	1	1	0	0	0	0	$xxB0FFFF	1	0	1	1	0	0	0	0
$xxB10000	1	0	1	1	0	0	0	1	$xxB1FFFF	1	0	1	1	0	0	0	1
$xxB20000	1	0	1	1	0	0	1	0	$xxB2FFFF	1	0	1	1	0	0	1	0
$xxB30000	1	0	1	1	0	0	1	1	$xxB3FFFF	1	0	1	1	0	0	1	1
$xxB40000	1	0	1	1	0	1	0	0	$xxB4FFFF	1	0	1	1	0	1	0	0
$xxB50000	1	0	1	1	0	1	0	1	$xxB5FFFF	1	0	1	1	0	1	0	1
$xxB60000	1	0	1	1	0	1	1	0	$xxB6FFFF	1	0	1	1	0	1	1	0
$xxB70000	1	0	1	1	0	1	1	1	$xxB7FFFF	1	0	1	1	0	1	1	1
$xxB80000	1	0	1	1	1	0	0	0	$xxB8FFFF	1	0	1	1	1	0	0	0
$xxB90000	1	0	1	1	1	0	0	1	$xxB9FFFF	1	0	1	1	1	0	0	1
$xxBA0000	1	0	1	1	1	0	1	0	$xxBAFFFF	1	0	1	1	1	0	1	0
$xxBB0000	1	0	1	1	1	0	1	1	$xxBBFFFF	1	0	1	1	1	0	1	1
$xxBC0000	1	0	1	1	1	1	0	0	$xxBCFFFF	1	0	1	1	1	1	0	0
$xxBD0000	1	0	1	1	1	1	0	1	$xxBDFFFF	1	0	1	1	1	1	0	1
$xxBE0000	1	0	1	1	1	1	1	0	$xxBEFFFF	1	0	1	1	1	1	1	0
$xxBF0000	1	0	1	1	1	1	1	1	$xxBFFFFF	1	0	1	1	1	1	1	1

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MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xxC00000	1	1	0	0	0	0	0	0
$xxC10000	1	1	0	0	0	0	0	1
$xxC20000	1	1	0	0	0	0	1	0
$xxC30000	1	1	0	0	0	0	1	1
$xxC40000	1	1	0	0	0	1	0	0
$xxC50000	1	1	0	0	0	1	0	1
$xxC60000	1	1	0	0	0	1	1	0
$xxC70000	1	1	0	0	0	1	1	1
$xxC80000	1	1	0	0	1	0	0	0
$xxC90000	1	1	0	0	1	0	0	1
$xxCA0000	1	1	0	0	1	0	1	0
$xxCB0000	1	1	0	0	1	0	1	1
$xxCC0000	1	1	0	0	1	1	0	0
$xxCD0000	1	1	0	0	1	1	0	1
$xxCE0000	1	1	0	0	1	1	1	0
$xxCF0000	1	1	0	0	1	1	1	1
$xxD00000	1	1	0	1	0	0	0	0
$xxD10000	1	1	0	1	0	0	0	1
$xxD20000	1	1	0	1	0	0	1	0
$xxD30000	1	1	0	1	0	0	1	1
$xxD40000	1	1	0	1	0	1	0	0
$xxD50000	1	1	0	1	0	1	0	1
$xxD60000	1	1	0	1	0	1	1	0
$xxD70000	1	1	0	1	0	1	1	1
$xxD80000	1	1	0	1	1	0	0	0
$xxD90000	1	1	0	1	1	0	0	1
$xxDA0000	1	1	0	1	1	0	1	0
$xxDB0000	1	1	0	1	1	0	1	1
$xxDC0000	1	1	0	1	1	1	0	0
$xxDD0000	1	1	0	1	1	1	0	1
$xxDE0000	1	1	0	1	1	1	1	0
$xxDF0000	1	1	0	1	1	1	1	1

UPPER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xxC0FFFF	1	1	0	0	0	0	0	0
$xxC1FFFF	1	1	0	0	0	0	0	1
$xxC2FFFF	1	1	0	0	0	0	1	0
$xxC3FFFF	1	1	0	0	0	0	1	1
$xxC4FFFF	1	1	0	0	0	1	0	0
$xxC5FFFF	1	1	0	0	0	1	0	1
$xxC6FFFF	1	1	0	0	0	1	1	0
$xxC7FFFF	1	1	0	0	0	1	1	1
$xxC8FFFF	1	1	0	0	1	0	0	0
$xxC9FFFF	1	1	0	0	1	0	0	1
$xxCAFFFF	1	1	0	0	1	0	1	0
$xxCBFFFF	1	1	0	0	1	0	1	1
$xxCCFFFF	1	1	0	0	1	1	0	0
$xxCDFFFF	1	1	0	0	1	1	0	1
$xxCEFFFF	1	1	0	0	1	1	1	0
$xxCFFFFF	1	1	0	0	1	1	1	1
$xxD0FFFF	1	1	0	1	0	0	0	0
$xxD1FFFF	1	1	0	1	0	0	0	1
$xxD2FFFF	1	1	0	1	0	0	1	0
$xxD3FFFF	1	1	0	1	0	0	1	1
$xxD4FFFF	1	1	0	1	0	1	0	0
$xxD5FFFF	1	1	0	1	0	1	0	1
$xxD6FFFF	1	1	0	1	0	1	1	0
$xxD7FFFF	1	1	0	1	0	1	1	1
$xxD8FFFF	1	1	0	1	1	0	0	0
$xxD9FFFF	1	1	0	1	1	0	0	1
$xxDAFFFF	1	1	0	1	1	0	0	1
$xxDBFFFF	1	1	0	1	1	0	1	1
$xxDCFFFF	1	1	0	1	1	1	0	0
$xxDDFFFF	1	1	0	1	1	1	0	1
$xxDEFFFF	1	1	0	1	1	1	1	0
$xxDFFFFF	1	1	0	1	1	1	1	1

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MODULE SELECTION

(A16 - A23)

0 = Open
1 = Closed

LOWER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xxE00000	1	1	1	0	0	0	0	0
$xxE10000	1	1	1	0	0	0	0	1
$xxE20000	1	1	1	0	0	0	1	0
$xxE30000	1	1	1	0	0	0	1	1
$xxE40000	1	1	1	0	0	1	0	0
$xxE50000	1	1	1	0	0	1	0	1
$xxE60000	1	1	1	0	0	1	1	0
$xxE70000	1	1	1	0	0	1	1	1
$xxE80000	1	1	1	0	1	0	0	0
$xxE90000	1	1	1	0	1	0	0	1
$xxEA0000	1	1	1	0	1	0	1	0
$xxEB0000	1	1	1	0	1	0	1	1
$xxEC0000	1	1	1	0	1	1	0	0
$xxED0000	1	1	1	0	1	1	0	1
$xxEE0000	1	1	1	0	1	1	1	0
$xxEF0000	1	1	1	0	1	1	1	1
$xxF00000	1	1	1	1	0	0	0	0
$xxF10000	1	1	1	1	0	0	0	1
$xxF20000	1	1	1	1	0	0	1	0
$xxF30000	1	1	1	1	0	0	1	1
$xxF40000	1	1	1	1	0	1	0	0
$xxF50000	1	1	1	1	0	1	0	1
$xxF60000	1	1	1	1	0	1	1	0
$xxF70000	1	1	1	1	0	1	1	1
$xxF80000	1	1	1	1	1	0	0	0
$xxF90000	1	1	1	1	1	0	0	1
$xxFA0000	1	1	1	1	1	0	1	0
$xxFB0000	1	1	1	1	1	0	1	1
$xxFC0000	1	1	1	1	1	1	0	0
$xxFD0000	1	1	1	1	1	1	0	1
$xxFE0000	1	1	1	1	1	1	1	0
$xxFF0000	1	1	1	1	1	1	1	1

UPPER LIMIT SELECTED	SW 1 8	7	6	5	4	3	2	1
$xxE0FFFF	1	1	1	0	0	0	0	0
$xxE1FFFF	1	1	1	0	0	0	0	1
$xxE2FFFF	1	1	1	0	0	0	1	0
$xxE3FFFF	1	1	1	0	0	0	1	1
$xxE4FFFF	1	1	1	0	0	1	0	0
$xxE5FFFF	1	1	1	0	0	1	0	1
$xxE6FFFF	1	1	1	0	0	1	1	0
$xxE7FFFF	1	1	1	0	0	1	1	1
$xxE8FFFF	1	1	1	0	1	0	0	0
$xxE9FFFF	1	1	1	0	1	0	0	1
$xxEAFFFF	1	1	1	0	1	0	1	0
$xxEBFFFF	1	1	1	0	1	0	1	1
$xxECFFFF	1	1	1	0	1	1	0	0
$xxEDFFFF	1	1	1	0	1	1	0	1
$xxEEFFFF	1	1	1	0	1	1	1	0
$xxEFFFFF	1	1	1	0	1	1	1	1
$xxF0FFFF	1	1	1	1	0	0	0	0
$xxF1FFFF	1	1	1	1	0	0	0	1
$xxF2FFFF	1	1	1	1	0	0	1	0
$xxF3FFFF	1	1	1	1	0	0	1	1
$xxF4FFFF	1	1	1	1	0	1	0	0
$xxF5FFFF	1	1	1	1	0	1	0	1
$xxF6FFFF	1	1	1	1	0	1	1	0
$xxF7FFFF	1	1	1	1	0	1	1	1
$xxF8FFFF	1	1	1	1	1	0	0	0
$xxF9FFFF	1	1	1	1	1	0	0	1
$xxFAFFFF	1	1	1	1	1	0	1	0
$xxFBFFFF	1	1	1	1	1	0	1	1
$xxFCFFFF	1	1	1	1	1	1	0	0
$xxFDFFFF	1	1	1	1	1	1	0	1
$xxFEFFFF	1	1	1	1	1	1	1	0
$xxFFFFFF	1	1	1	1	1	1	1	1

xx = Bank Select Setting (See Appendix A)

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APPENDIX C

ADDRESS Modifier Equations IFL U15 (45661)

```
@DEVICE TYPE
PLS153
@DRAWING
1 of 1
@REVISION
C
@DATE
April 3, 1987
@SYMBOL
PN45661
@COMPANY
Micro Memory Inc.
9540 Vassar St.
Chatsworth, Ca. 91311
@NAME
ADDRMOD
@DESCRIPTION
Address Modifier qualifier
@COMMON PRODUCT TERM

AM09 = /AM5 * /AM4 *  AM3 * /AM2 * /AM1 *  AM0;
AM0A = /AM5 * /AM4 *  AM3 * /AM2 *  AM1 * /AM0;
AM0B = /AM5 * /AM4 *  AM3 * /AM2 *  AM1 *  AM0;
AM0D = /AM5 * /AM4 *  AM3 *  AM2 * /AM1 *  AM0;
AM0E = /AM5 * /AM4 *  AM3 *  AM2 *  AM1 * /AM0;
AM0F = /AM5 * /AM4 *  AM3 *  AM2 *  AM1 *  AM0;

AM39 =  AM5 *  AM4 *  AM3 * /AM2 * /AM1 *  AM0;
AM3A =  AM5 *  AM4 *  AM3 * /AM2 *  AM1 * /AM0;
AM3B =  AM5 *  AM4 *  AM3 * /AM2 *  AM1 *  AM0;
AM3D =  AM5 *  AM4 *  AM3 *  AM2 * /AM1 *  AM0;
AM3E =  AM5 *  AM4 *  AM3 *  AM2 *  AM1 * /AM0;
AM3F =  AM5 *  AM4 *  AM3 *  AM2 *  AM1 *  AM0;

@I/O DIRECTION
@OUTPUT POLARITY

X7,X8,X9 = 0;

@LOGIC EQUATION

SELECT  =          ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM39
        +          ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM3A
        +          ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM3B
        +          ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM3D
        +          ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM3E
        +          ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM3F
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM09
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0A
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0B
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0D
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0E
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0F
        +  SELECT * DBAS * BAS * /OVERFL * BLKMOD
        ;
```


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ADDRESS Modifier Equations IFL U15 (45661)

```
BLWORD   = /LWORD
         +  BLWORD * /MEMCYC-
         ;

BLKMOD   =  DBAS * BAS * AM3B
         +  DBAS * BAS * AM3F
         +  DBAS * BAS * AM0B
         +  DBAS * BAS * AM0F
         +  BLKMOD * DBAS * BAS
         ;
```


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ADDRESS Modifier Equations IFL U15 (45661-A32)

```
@DEVICE TYPE
PLS153
@DRAWING
1 of 1
@REVISION
A3.1 SPECIAL 32 BIT ONLY
@DATE
April 13, 1987
@SYMBOL
PN45661-A32
@COMPANY
Micro Memory Inc.
9540 Vassar St.
Chatsworth, Ca. 91311
@NAME
ADRMOD32
@DESCRIPTION
Address Modifier qualifier
@COMMON PRODUCT TERM

AM09 = /AM5 * /AM4 *  AM3 * /AM2 * /AM1 *  AM0;
AM0A = /AM5 * /AM4 *  AM3 * /AM2 *  AM1 * /AM0;
AM0B = /AM5 * /AM4 *  AM3 * /AM2 *  AM1 *  AM0;
AM0D = /AM5 * /AM4 *  AM3 *  AM2 * /AM1 *  AM0;
AM0E = /AM5 * /AM4 *  AM3 *  AM2 *  AM1 * /AM0;
AM0F = /AM5 * /AM4 *  AM3 *  AM2 *  AM1 *  AM0;

@I/O DIRECTION
@OUTPUT POLARITY

X7,X8,X9 = 0;

@LOGIC EQUATION

SELECT  = /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM09
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0A
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0B
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0D
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0E
        + /BANKS * ENABLE * /OVERFL * LLPGTQ * /HLSEL * DBAS * BAS * AM0F
        +  SELECT * DBAS * BAS * /OVERFL * BLKMOD
        ;

BLWORD  = /LWORD
        +  BLWORD * /MEMCYC-
        ;

BLKMOD  = DBAS * BAS * AM0B
        + DBAS * BAS * AM0F
        + BLKMOD * DBAS * BAS
        ;
```


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MICRO MEMORY. INC.	DATE 3/30/87	REV A
TITLE LIST OF MATERIALS MM-6230	NUMBER 91801	

PER DOCUMENT NO.

ORIGINATOR DATE

REVISIONS

REV	DESCRIPTION	E O	DATE	APPR
A	INITIAL RELEASE			

SIGNATURES	DATES
M/P ENGR	
MFG ENGR	
Q. C.	
ENGR MGR	

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SECURITY CLASSIFICATION			micro memory inc.		CODE IDENT. NO. 06481	LIST OF MATERIAL # 91801	A
			DRAWN			SHEET 2 OF 5	REV.
			CHECK				
			ENGR			TITLE: LIST OF MATERIALS MM-6230	
ART NO.	NEXT ASSY	MODEL NO.	PROJ				

QUANTITY REQ USED ON	QTY	ITEM NO.	PART OR IDENTIFYING NO.	MATERIAL OR DESCRIPTION	SPECIFICATION
	1	1	91811 A	Printed Wiring Board	
	1	2	91814	Front Panel Assembly	
	1	3	91104	Mtg. Bracket	
	2	4		Connector Panduit # 100-096-053 or equiv.	P1, P2
	72	5		Connector Pins Samtec # SS-132-G2	P3
		6			
	1	7	45660	Integrated Circuit PAL 20X8A	U1
	4	8		" " 74ALS646-1	U2,3,9,16
	3	9		" " 74LS682	U4,13,21
	2	10		" " 74F533	U5,6
	1	11		" " 74S38	U7
	3	12		" " 74LS240	U8,22,23
	2	13		" " 74F245	U10,11
	3	14		" " 74F74	U12,19,37
	1	15		" " 74F08	U14
	1	16	45661	" " PAL PLS153A	U15

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SECURITY CLASSIFICATION			Micro Memory Inc.		CODE IDENT. NO.	LIST OF MATERIAL #	
			DRAWN		06481	91801	A
			CHECK			SHEET 3 OF 5	REV.
			ENGR		TITLE: LIST OF MATERIALS MM-6230		
ART NO.	NEXT ASSY	MODEL NO.	PROJ				

QUANTITY REQ USED ON	QTY	ITEM NO.	PART OR IDENTIFYING NO.	MATERIAL OR DESCRIPTION	SPECIFICATION
	2	17		Integrated Circuit 74F64	U17,18
	1	18	45662	" " PAL 16L8B	U20
	2	19		" " 74F283	U23,24
	1	20	45663	" " PAL20L8B	U26
	1	21	45664	Integrated Circuit PAL 16L8B	U27
	1	22	45665	" " PAL PLS153	U28
	3	23		" " 74AS857	U29,30,31
	1	24		" " LM-555	U32
	3	25		" " 74AS1032	U34,35,36
	1	26		" " 74F04	U36
	1	27		" " 7474	U33
	1	28		" " 74F02	U39
	4	29		" " 74F280	U40,41,42,43
		30			
	1	31		Delay Line EP 8303 (PCA)	DL 1
	1	32		Delay Line EP 9206-020 (PCA)	DL 2

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SECURITY CLASSIFICATION			micro memory inc.		CODE IDENT. NO. 06481	LIST OF MATERIAL # 91801	A
			DRAWN			SHEET 4 OF 5	REV.
			CHECK				
			ENGR		TITLE: LIST OF MATERIALS MM-6230		
ART NO.	NEXT ASSY	MODEL NO.	PROJ				

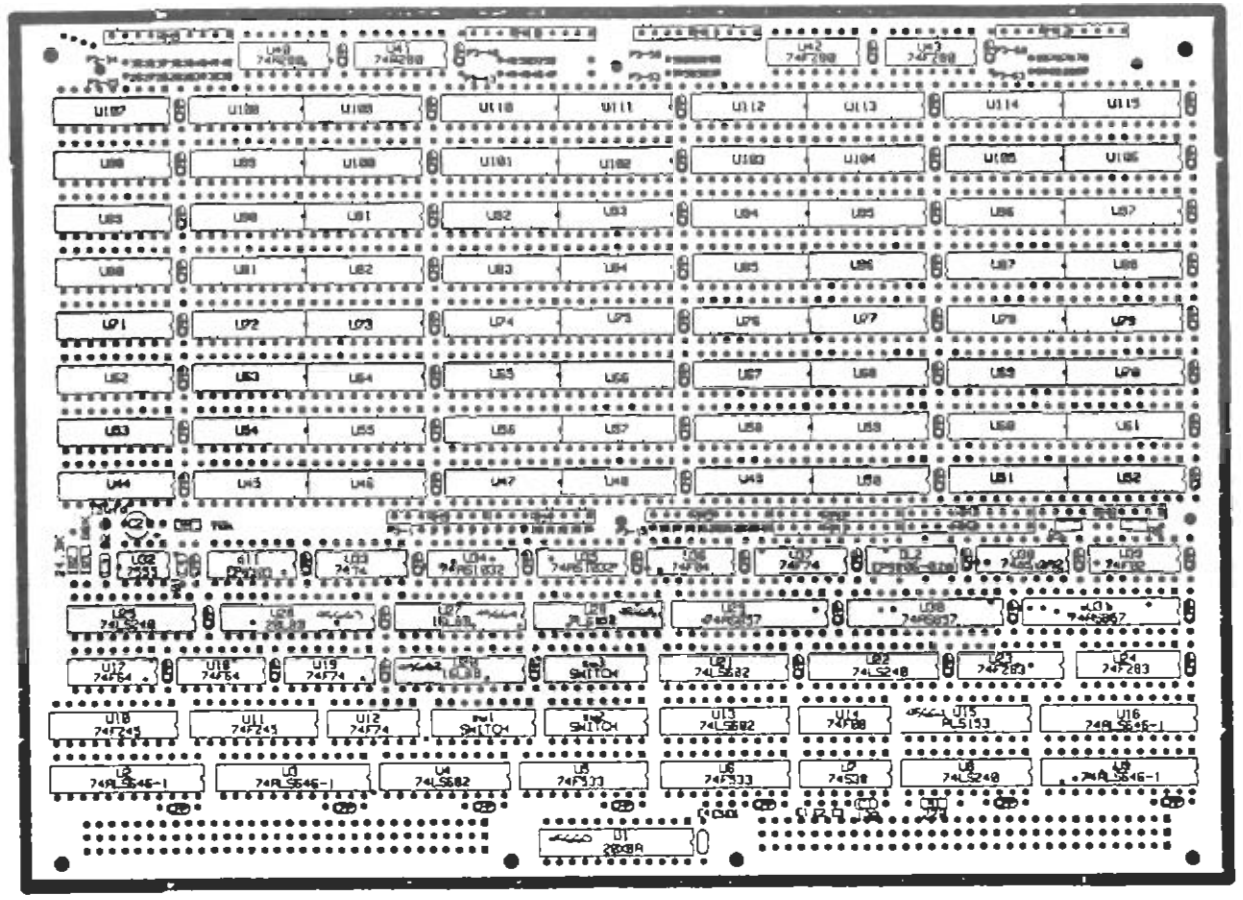
QUANTITY REQ USED ON	QTY	ITEM NO.	PART OR IDENTIFYING NO.	MATERIAL OR DESCRIPTION	SPECIFICATION
		33			
	3	34		Switch 8 pos Grayhill # 76SB08	SW 1,2,3
		35			
	72	36		Memory Chip 1 meg dynamic, 120, dip	U44 thru U115
		37		Toshiba P/N TC511000P12	
	72	38		Socket 18 pin Augat #218-ACB39D-C10	U44 thru U115
	4	39		Socket 20 pin Amp# 641612-3	U15,20,27,28
	2	40		Socket 24 pin Amp# 641933-1	U1,26
	6	41		Resistor Network 1K Bourns# 4610-101-102	RM1,2,9,10,11,12
	2	42		" " 22 ohm " # 4608-102-220	RM 3,4
	4	43		" " 22 ohm " # 4610-102-220	RM5,6,7,8
		44			
	1	45		Resistor 1/4 w ± 5 % 220 ohm	R 1
	1	46		" 1/4 w ± 1 % 24.3K	R 2
	1	47		" 1/4 w ± 1 % 68 K	R 3
	1	48		" 1/4 w ± 5 % 10K	R 4

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SECURITY CLASSIFICATION			Micro Memory Inc.		CODE IDENT. NO.	LIST OF MATERIAL #	
			DRAWN		06481	91801	A
			CHECK			SHEET 5 OF 5	REV.
			ENGR		TITLE: LIST OF MATERIALS MM-6230		
ART NO.	NEXT ASSY	MODEL NO.	PROJ				

QUANTITY REQ USED ON	QTY	ITEM NO.	PART OR IDENTIFYING NO.	MATERIAL OR DESCRIPTION	SPECIFICATION
	2	49		Resistor 1/4 w ± 5 % 1 K	R5,6
		50			
	1	51		Capacitor 100pf CK05BX102K	C 1
	1	52		" 15 ufd Jelly Bean	C 2
	1	53		" 82pf CK05BX820K	C 3
	1	54		" .01ufd CK05BX103K	C 4
	34	55		" .1ufd 50v, Kemet#C410C104M5UCA All Other	
		56			
	1	57		LED, Red Dialight #558-0102-003	LED 1
	6	58		Amp Pins .025 sq #11010	E1 thru E6
		59			
		60			
		61			
		62			
		63			
		64			

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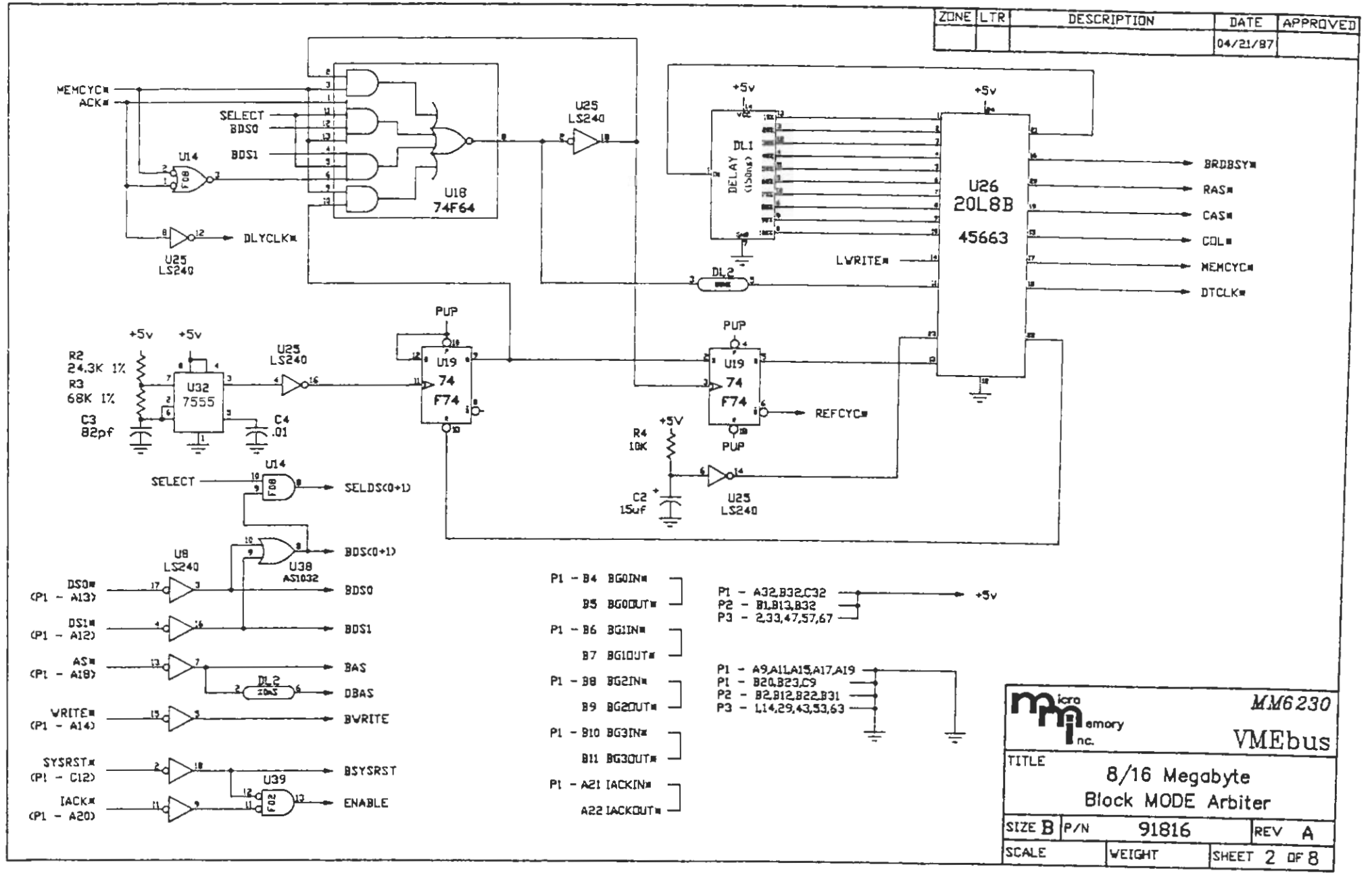
MICRO MEMORY, INC.

SCHEMATIC, SYSTEM MM-6230
COMPONENT LAYOUT

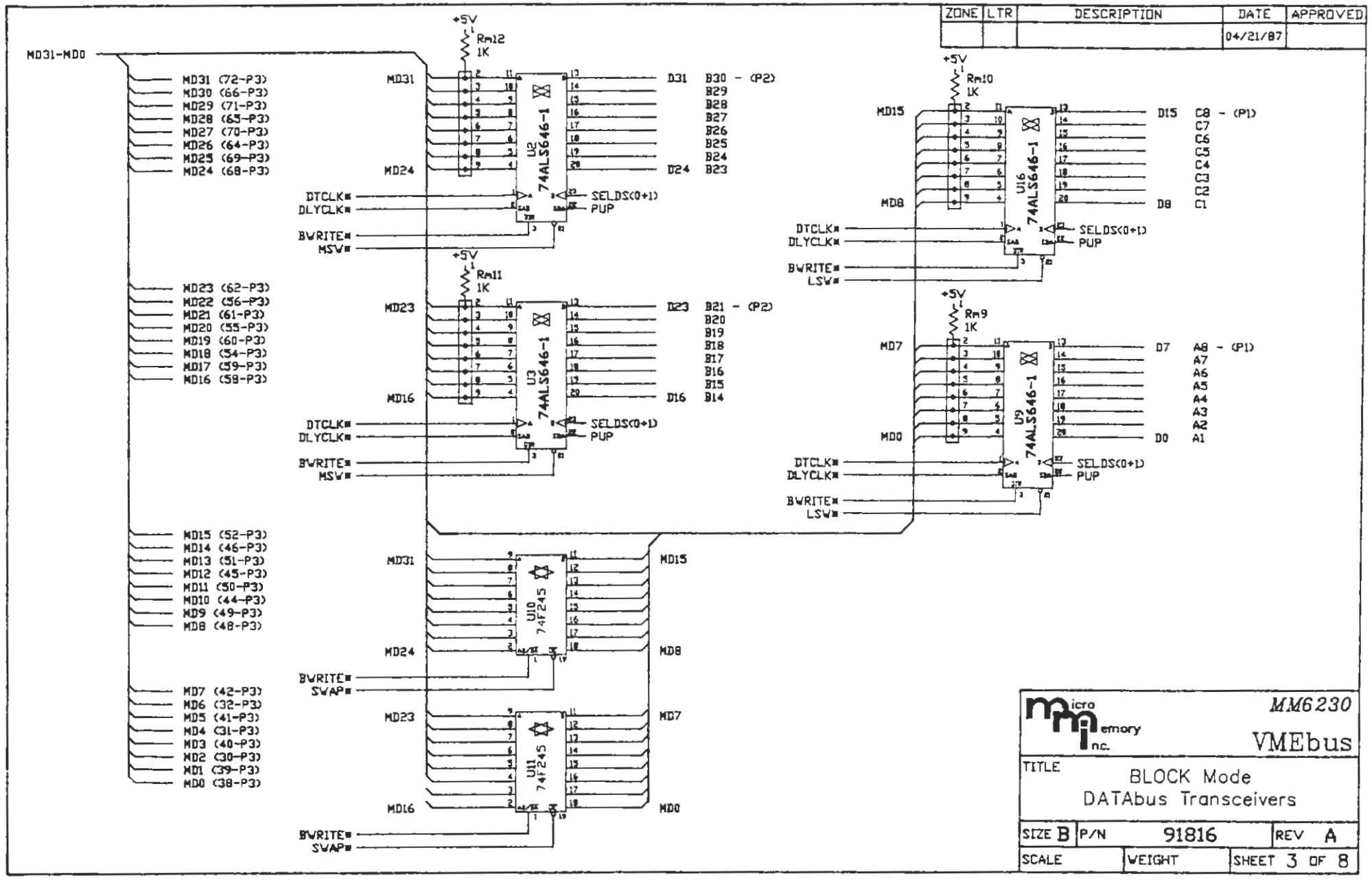
91816

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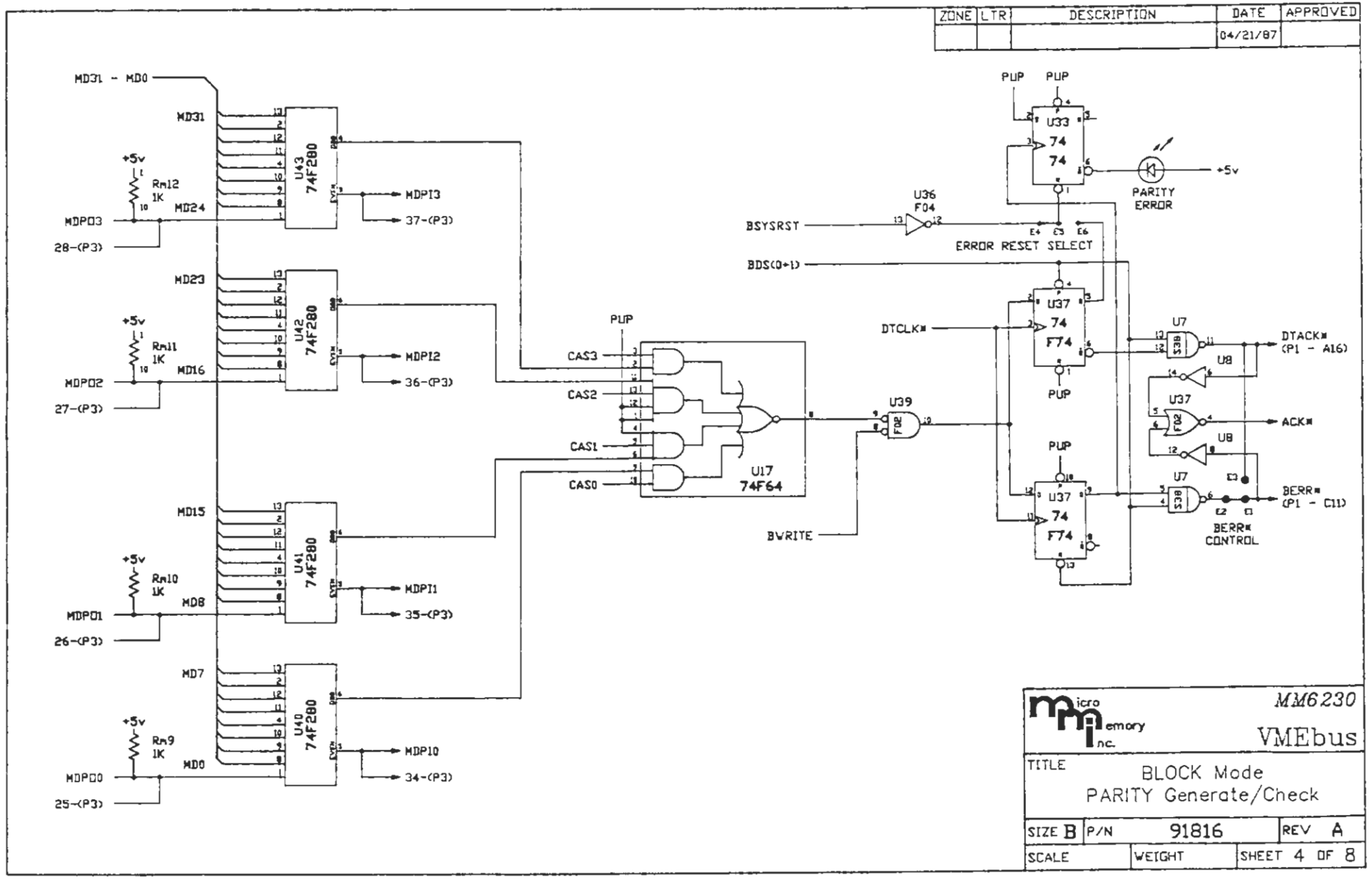


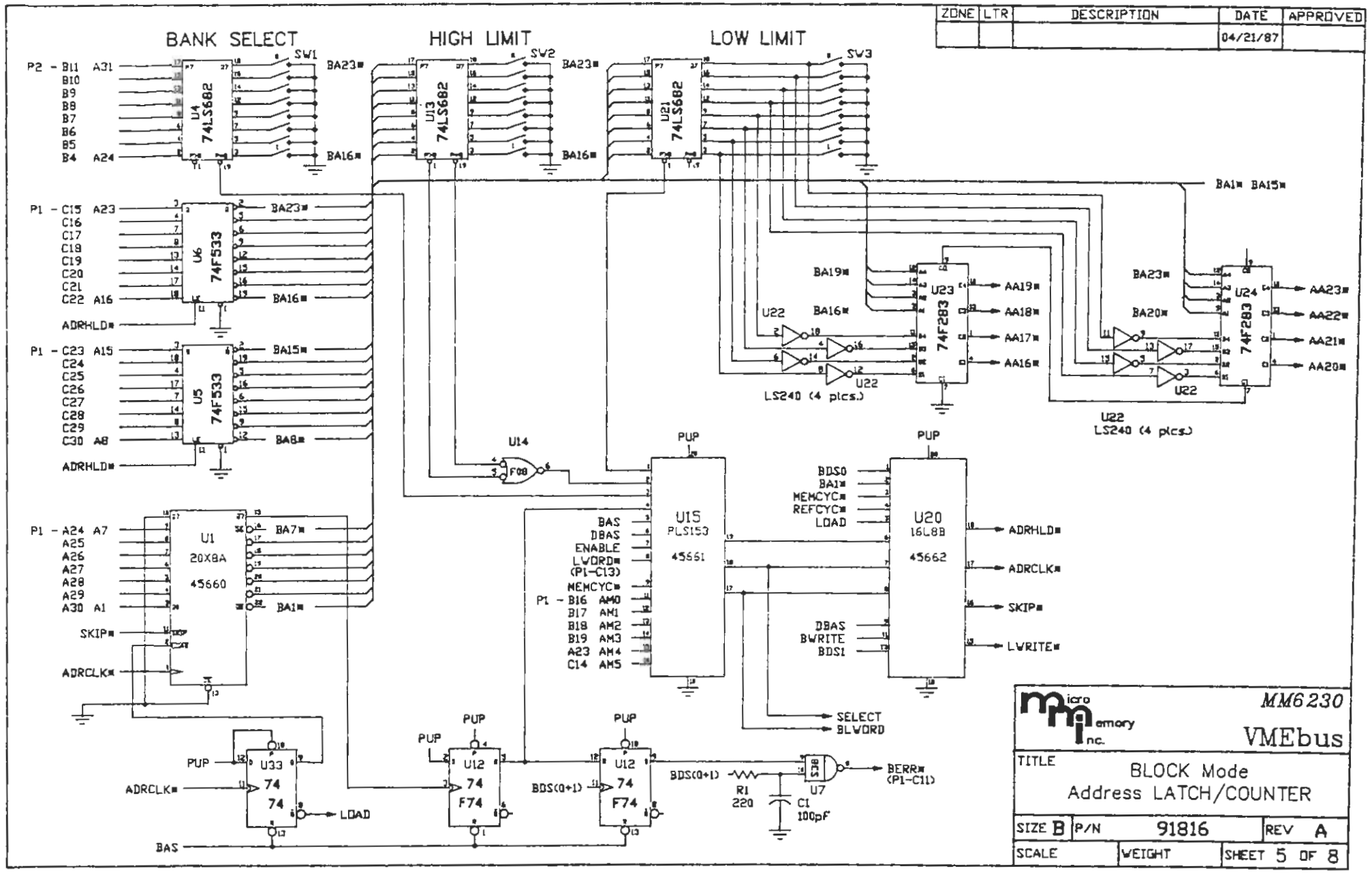
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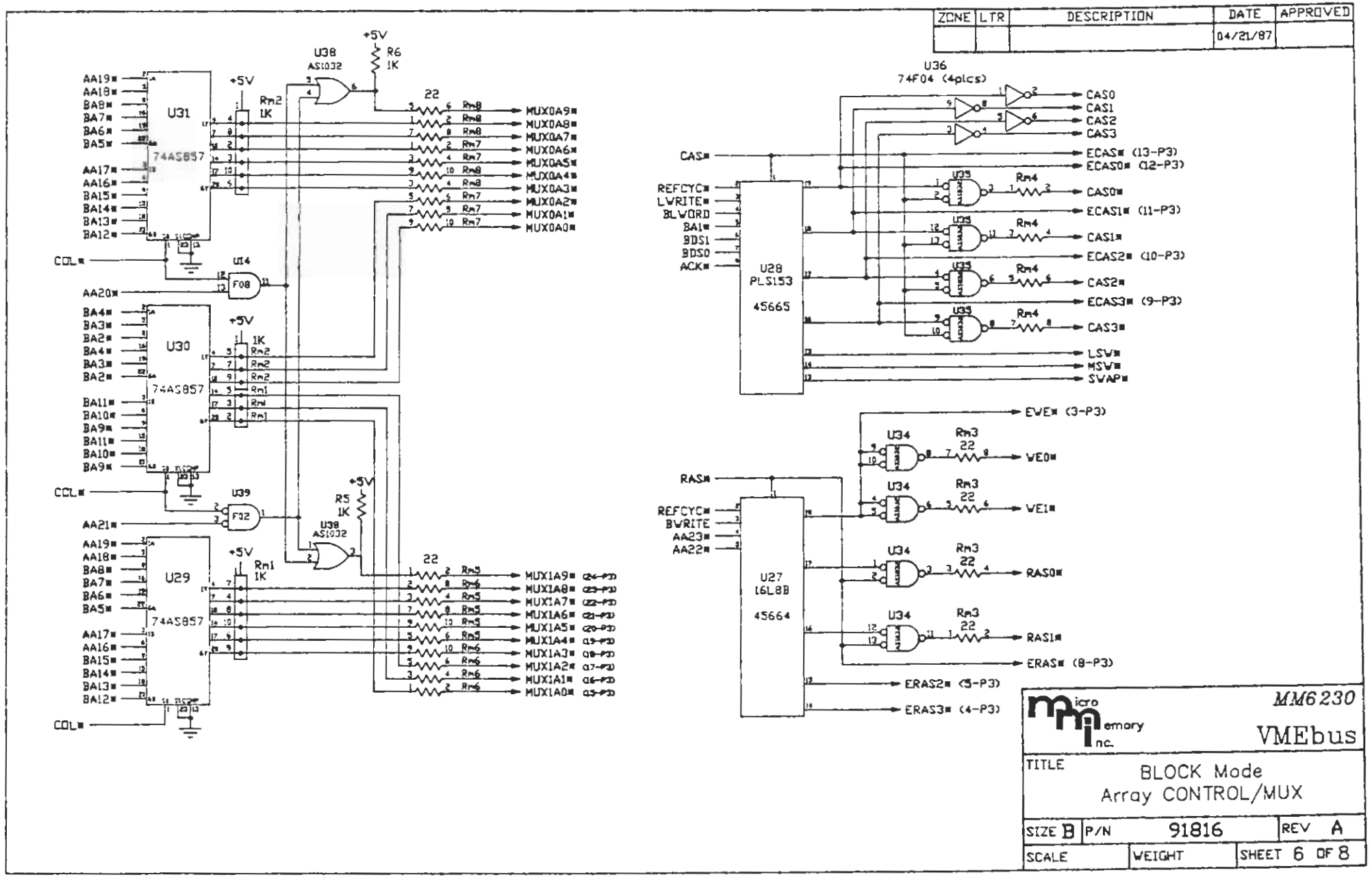
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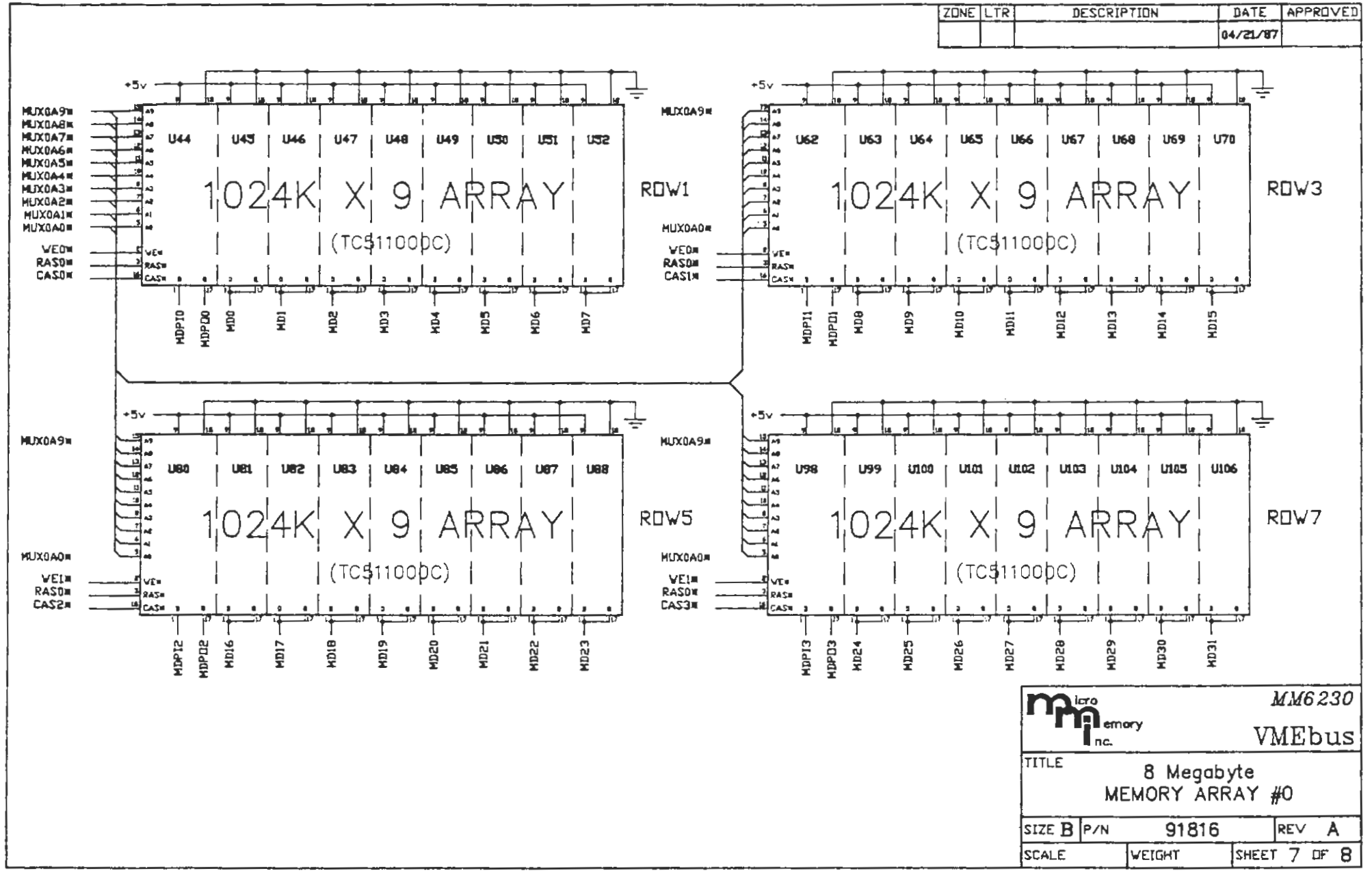


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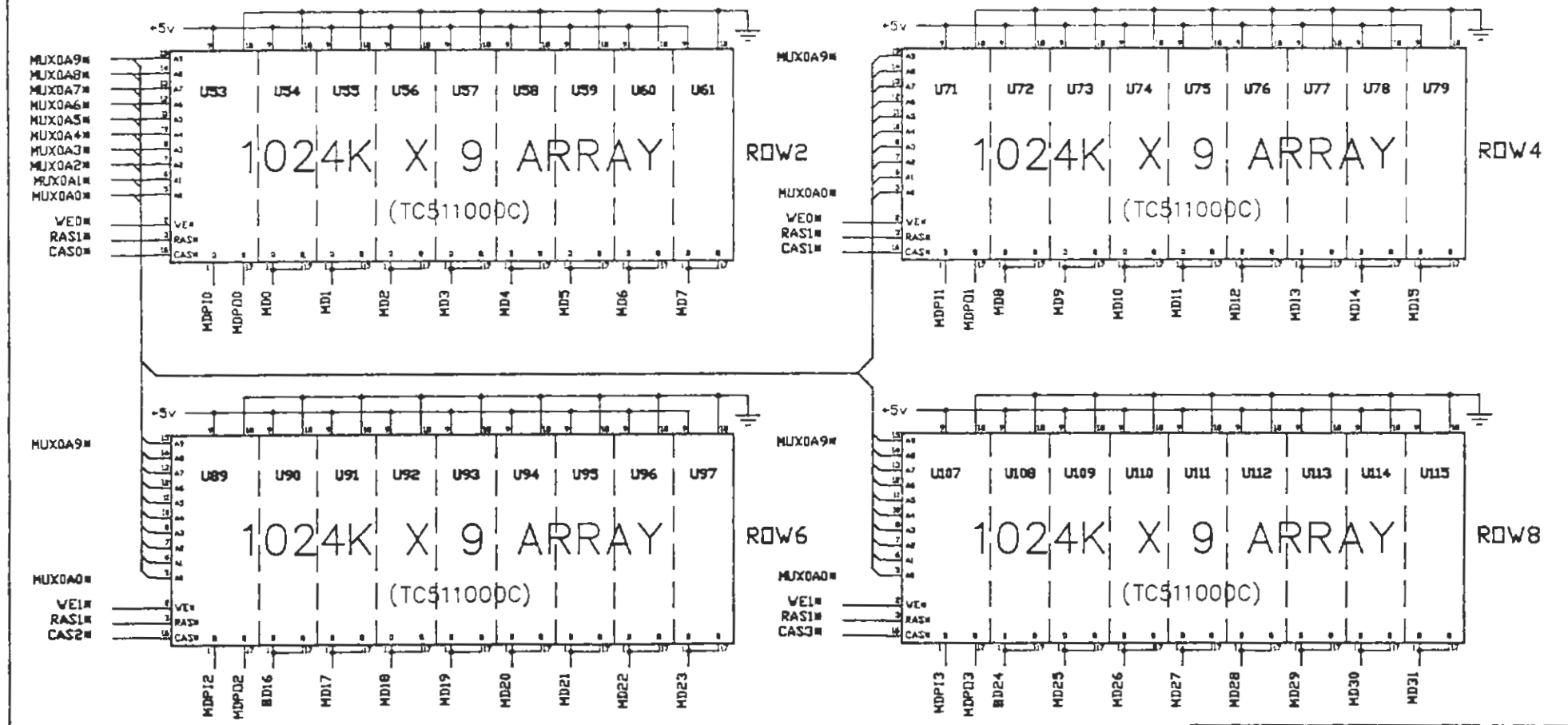
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ZONE	LTR	DESCRIPTION	DATE	APPROVED
			04/21/87	



micro memory inc.

MM6230

VMEbus

TITLE

8 Megabyte
MEMORY ARRAY #1

SIZE B	P/N 91816	REV A
SCALE	WEIGHT	SHEET 8 OF 8

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