MICRO MEMORY INC.
9540 VASSAR AVE.
CHATSWORTH, CALIF.
(818) 998-0070

MM-6300D

USERs GUIDE

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VMEbus DUAL port MEMORY MODULE for the VSBus & VMX32bus

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation procedures of the MM6300D Dual Port Dynamic Random Access Memory Module.

1.2 GENERAL DESCRIPTION

The MM6300D Dual Ported Memory is compatible with the VMEbus, VME Subsystem Bus (VSBus), and VMX32bus specifications. Inherent to the module are VMEbus options D32, D16 & D8 (32, 16 & 8 bit data path width), and A32, A24 (32, 24 bit address path width). The module also generates and stores an even parity bit for each byte written on write cycles and checks parity for each byte read on read cycles. Then if a parity error is detected, the module sets a Control Status Register (CSR) bit and may be programmed to assert the bus error signal on the requesting port. (see Section III for CSR programming)

While the MM6300D Dual Ported Memory was designed as a 32 bit wide (data path) memory board, the MM6300D Dual Ported Memory complies with VMEbus Specifications (Revision C.1) and VSBus Specifications (Revision A.1) and can be addressed as 8 bit bytes, 16 bit words, or 32 bit longwords. The MM6300D Dual Ported Memory can be configured for 1M and 2M, bytes capacity by populating it with 256K x 1 and 256K x 4 DRAMS.

The MM6300D Dual Ported Memory Control Status Register is software compatible with the Motorola MVME204 memory modules.

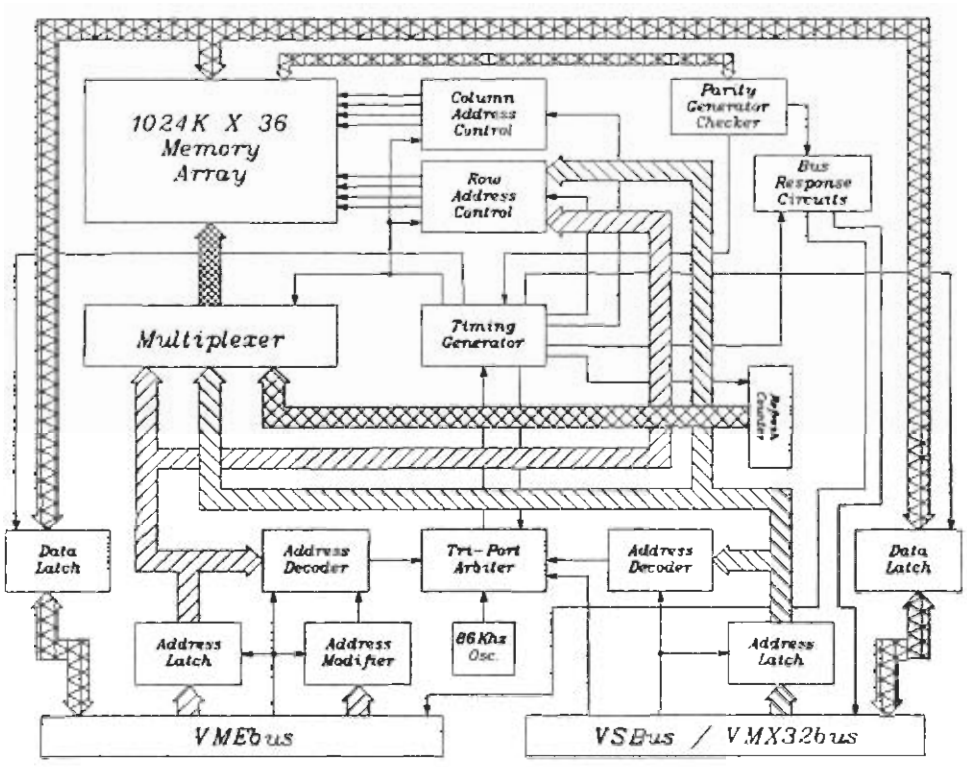
The MM6300D Dual Ported Memory memory modules are available in two options depending on the capacity required. Table 1.1 lists the optional part numbers for ordering purposes, the total memory capacity provided by each version.

TABLE 1.1

MEMORY CAPACITY OPTIONS

Table 1.1 summarizes the options with respect to storage capacity, available to MM6300D Dual Ported Memory user.

Option	Capacity
MM6300D/1M	1.0M Bytes
MM6300D/2M	2.0M Bytes



Functional Block Diagram Figure 1.1

1.2.2 OPERATIONAL FEATURES

The MM6300D Dual Ported Memory module contains its own address register and data buffers for each port for total compatibility with the VMEbus Specification (Rev. C.1) and VSBus Specification (Rev. A.1)

Module selection for the MM6300D Dual Ported Memory resides on 64K ($10000) byte boundaries. The module must be mapped in one of the 16Mega byte banks within the 4Giga bytes of physical address space, on each port, both the VMEbus and the VSBus or (VMX32bus).

The MM6300D Dual Ported Memory memory array can be addressed as 8 bit bytes, 16 bit words, or as 32 bit longwords. Memory cycle and Read/Write access times are 275nsec and 200/130nsec respectively.

The MM6300D Dual Ported Memory responds to various Address Modifier Codes. The codes are decoded by U1, Various combinations are available to the user (see Section II, jumpers).

The user may select to create his/her own Address Modifier code<s>, in this event the Address Modifier evaluation GAL (U1) can be replaced to accommodate the systems' requirements (see Section II, jumpers).

A Control Status Register (CSR) is available to allow various dynamic options to to be utilized by the software programmer. Included in the CSR are bits to make the MM6300D Dual Ported Memory a Private Bus only board (ie: VSBus only), or blocks of memory assigned to the VSBus only on a dynamic basis. A bit controls the response of the VSBus Cache lead. And a bit allows for Writing the Wrong Parity for dynamic diagnostics. The CSR is an A16 Slave and has separate address selection jumpers, and may be addressed on any ODD boundary in the VMEbus I/O address space. (See Section III for programming details).

1.3 GENERAL SPECIFICATIONS

Table 1.2 lists the general specifications for the MM6300D Dynamic Ram Memory Module.

TABLE 1.2

Characteristics	Specifications
Capacity	1M or 2M bytes
Cycle Time	275ns.
Read/Write Access Time	200ns./130ns. (fast write)
Address	24/32 bits VMEbus 32 bits VSBus
Address Modifiers	6 bits, jumper selectable, or user programmable GAL
Data In/Data Out	8/16/32 bits bidirectional with 48 ma. three-state output
Parity	EVEN, 1 bit for each byte Generated on each WRITE Checked on each read
Modes of Operation	Read, Write, Read-modify-Write Hidden refresh, Un-aligned
Module Selection VMEbus and VSBus	Memory selected on 64K byte ($10000) boundary in any 16 Megabyte bank within a 4G byte address space.
Control Status Register Selection	CSR Selected on any ODD address in the VMEbus 'A16' address space
Interface:	
Inputs	TTL-compatible
Outputs	48ma. Three-state, TTL-compatible
Operating Temperature	0 to 60 degrees C
Storage Temperature	-40 to +85 degrees C
Relative Humidity	95% without condensation
Power Requirements:	Standby Operate
+5V (fully-populated)	2.7A 3.2A

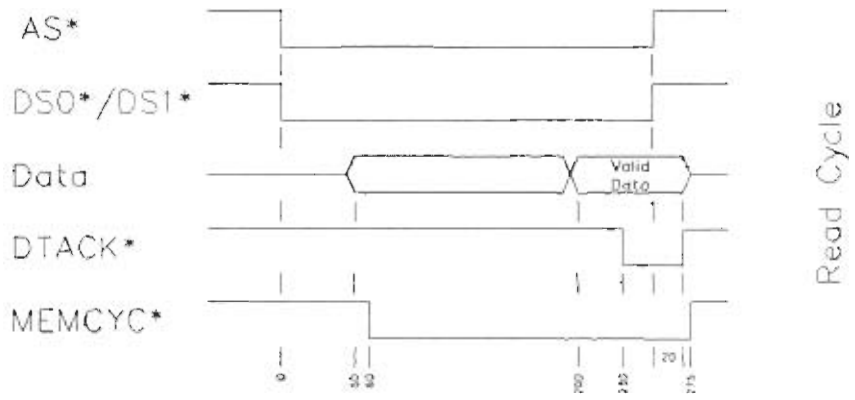
1.4 INTERFACE TIMING

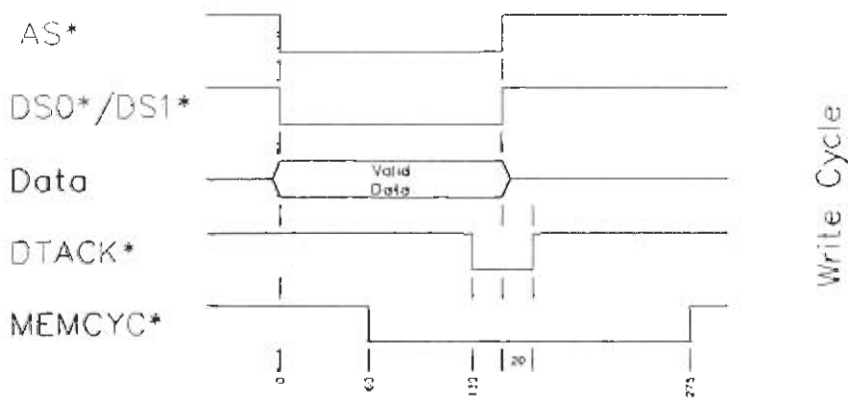
The MM6300D Dual Ported Memory memory modules are designed to accept Industry Standard 256K x 1 and 256K x 4 DRAMS with 120ns typical access times.

The VMEbus Interface Timing Diagram (Figure 1.2),illustrates the timing relationships on the Data Transfer bus, for Read and Write Cycles. Access delay time is measured from the leading edge of the Data strobes. (Figure 1.2).

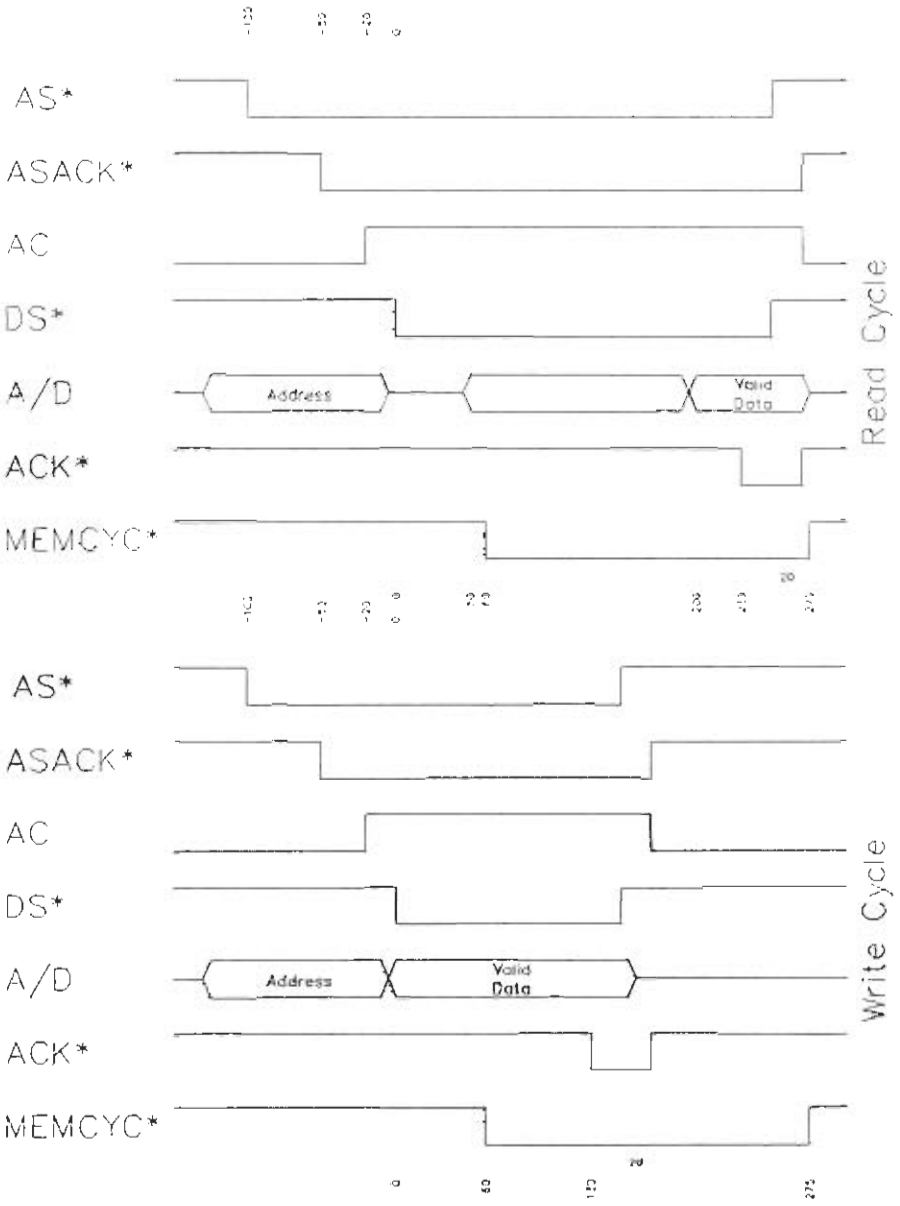
The VSBus Interface Timing Diagram (Figure 1.3), illustrates the timing relationships on the Data Transfer bus, for Read and Write Cycles. Access delay time is measured from the leading edge of the Data strobes. (Figure 1.3).

The refresh cycle timing is illustrated by Figure 1.4. Refresh cycles are repeated once every 15usec. The cycle interval timing is generated by a free running oscillator (U38) providing a refresh transparent to memory access cycles.

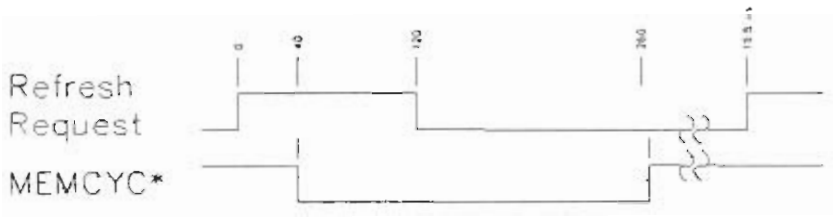




VMEbus Interface Timing Diagram Figure 1.2



VSBus Interface Timing Diagram Figure 1.3



Refresh Timing Diagram Figure 1.4

1.5 MEMORY ARRAY ORGANIZATION

The memory array is partitioned into two 256K x 36 bit segments. The minimum memory configuration would be 256K x 36 bits, including the four parity bits DRAMs in segment zero. This would translate to 1Megabytes minimum configuration for the MM6300D Dual Ported Memory.

The MM6300D Dual Ported Memory memory is partitioned as four blocks of 36 bits each (32 plus 4 parity), however the system will only see 32 bits of data during memory references, as the parity is generated and checked transparent to the user. The 32 bits of data are divided into 4 bytes (8 bits each). While the memory reads and writes may be 8, 16 or 32 bits wide, the memory is organized as 32 bit wide locations with logic controlling which byte<s> the user is reading or writing.

If the contents of the first 8 locations in memory are $01 $23 $45 $67 $89 $AB $CD $EF, determining which bits constitute what byte may be somewhat confusing. This can be cleared up by seeing the same data in the various formats used in most systems (IE: Byte, Word, and Longword).

BYTE Format		WORD Format		LONGWORD Format	
Location	Data	Location	Data	Location	Data
$00000000	$01	$00000000	$0123	$00000000	$01234567
$00000001	$23	$00000002	$4567	$00000004	$89ABCDEF
$00000002	$45	$00000004	$89AB		
$00000003	$67	$00000006	$CDEF		
$00000004	$89				
$00000005	$AB				
$00000006	$CD				
$00000007	$EF				

BIT Organizations

LONGWORD

```
3               1 1               0 3               1 1               0
1...............6 5...............0 1...............6 5...............0
```

WORD

```
1               0 1               0 1               0 1               0
5...............0 5...............0 5...............0 5...............0
```

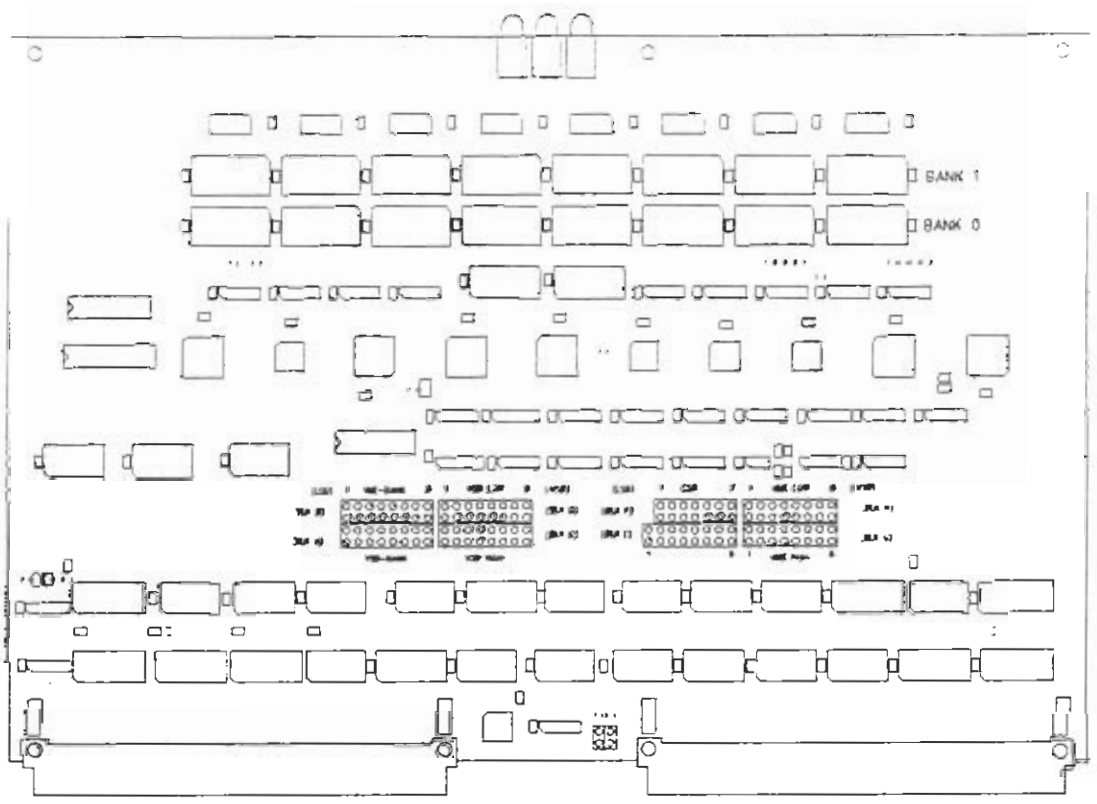
BYTE

```
0       00      0 0       00      0 0       00      0 0       00      0
7......07......0 7......07......0 7......07......0 7......07......0

0000000100100011 0100010101100111 1000100110101011 1100110111101111
 $0  $1  $2  $3   $4  $5  $6  $7   $8  $9  $A  $B   $C  $D  $E  $F
```

Table 1.5

DRAM Device locations for the MM6300D Dual Ported Memory



SECTION II

INSTALLATION

2.1 INTRODUCTION

This section details a step by step procedure to interface the MM6300D Dual Ported Memory to both the VMEbus and VSBus.

2.2 UNPACKING INSTRUCTIONS

Unpack module from shipping carton. If carton is damaged upon receipt, request that the carrier's agent be present during unpacking and inspection of the equipment. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment. For repairs or replacement of a board damaged during shipment, contact MICRO MEMORY, Inc. to obtain a Return Authorization number and further instructions.

2.3 HARDWARE PREPARATION

The memory module should be inspected and prepared for jumper placement prior to system installation. The following sections describe the proper jumper options necessary for system operation (see Section 2.5, for jumper options).

2.3.1 HANDLING PROCEDURE

The MM6300D Dual Ported Memory uses MOS components that are susceptible to damage if exposed to static electrical charges. To avoid damage of these components during handling, testing or operation, the following procedure should be used.

A. Device leads should contact conductive material to avoid building of any static charge, except during testing or operation.

B. Soldering iron tips, metal fixtures, tools, and handling facilities used in preparing the module for operation should be grounded.

C. Devices should never be removed or inserted while power is applied to the module because voltage transients may permanently damage the devices and/or module.

D. The memory module should never be plugged in or out of the cardcage while power is applied.

E. External signals should not be applied to device inputs while power is removed.

F. Any memory module removed from the system should be transferred to either non-conductive foam or an anti-static plastic bag for storage or shipment.

2.4 OPERATING ENVIRONMENT

The MM6300D Dual Ported Memory is an extremely High Density memory product. Containing, 64 bits of high current (48ma.) data bus drivers, numerous high speed components. And as a result, the environment into which the MM6300D Dual Ported Memory is placed, must be carefully considered.

2.4.1 AIRFLOW AND COOLING

Due to the extremely high component density of the MM6300D Dual Ported Memory, an adequate airflow is required to maintain the operating temperature within specifications of the memory module. Failure to adhere to these requirements may result in poor long term reliability.

2.4.2 POWER REQUIREMENTS

The power requirements of MM6300D Dual Ported Memory are such, that the module should never be operated while powered only by the P1 connector. Hence power should be applied to the appropriate pins (See Tables 1.3 & 1.4) of both the P1 and the P2 connector prior to operation of the MM6300D Dual Ported Memory.

2.5 JUMPER OPTIONS

There are several jumper options attainable on the MM6300D Dual Ported Memory memory module, depending on the user application. All of the available options are selected by installing or removing minijumpers on wirewrap pins on 0.100 inch centers. (see Figure G.1)

2.5.1 ADDRESS MODIFIER EVALUATION/SELECTION

The MM6300D Dual Ported Memory evaluates the Address Modifiers from the VMEbus to determine if they are to be responded to. As shipped from the factory, the MM6300D Dual Ported Memory responds to the common A24 (using only 24 address bits) & A32 (using all 32 address bits) Address Modifier codes. These Address Modifier codes are described in Appendix D. The user may select to replace the Address Modifier selection GAL (U1), to allow for some other combination or the creation of a special (user defined) code or codes. As shipped, when responding to the A24 Address Modifier code, the MM6300D Dual Ported Memory will only use A1 through A23 to evaluate the address. However this also is programmable by PAL (U14).

2.5.2 VSBUS ALTERNATE ADDRESS SPACE SELECTION (FACTORY, OPEN)

The MM6300D Dual Ported Memory normally is selected by the VSBus in the System Space, however the user may configure the MM6300D Dual Ported Memory to respond to the Alternate Space selection by shorting jumper E117 to E118. (See Figure G.1 for locations)

2.6 ADDRESS AND CONFIGURATION JUMPER SETTINGS

The MM6300D Dual Port Memory contains four (4) major jumper blocks and a single jumper pair that must be configured prior to installation before proper operation can be obtained. (See Figure G.1 for jumper locations)

Each port of the MM6300 Dual Port Memory must be addressed in it's four (4) Gigabyte address space. The VMEbus port is controlled by jumper blocks Blk B, Blk G & Blk H. While the VSBus port is controlled by blocks Blk A, Blk C & Blk D, also by jumpers E117-E118 Select Alternate Space (See Section 2.5.2). The installation (SHORTED) or removal (OPEN) of these mini-jumpers represent ones and zeros in the following examples.

2.6.1 BANK SELECTION

The MM6300 Dual Port Memory may be selected on any 64Kilobyte ($10000) boundary. However, due to the 24bit address mode required by A24 bus masters on the VMEbus, the MM6300 Dual Port Memory must reside wholly inside one of 256 16Megabyte banks. This is controlled by Blk B on the VMEbus and Blk A on the VSBus. (see Figure 2.1)

BANK SELECTION

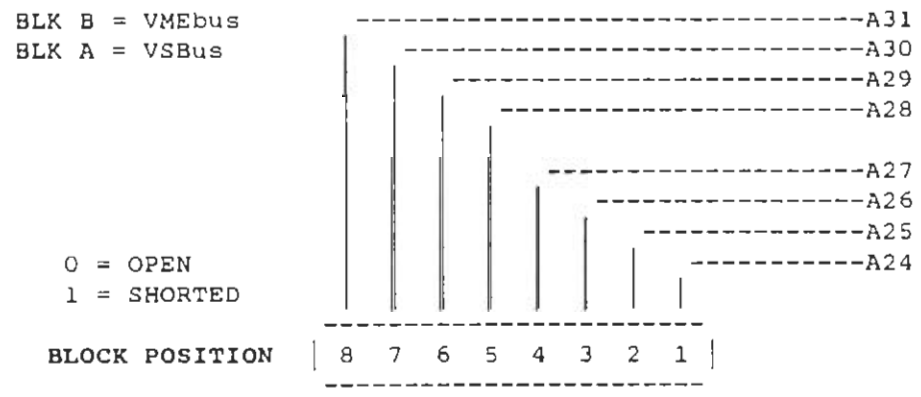


Figure 2.1 16Megabyte Bank selection

2.6.2 VMEBUS MODULE SELECTION

Selection of the VMEbus lower limit and upper limit on 64Kilobyte byte ($10000) boundaries within the selected bank is accomplished by installing (SHORTED) or removing (OPEN) the appropriate jumpers in blocks Blk H for lower limit and Blk G for upper limit, as illustrated in Figure 2.2. Position 1 is the least and position 8 is the most significant for both upper and lower limits.

2.6.3 VSBUS MODULE SELECTION

As with the VMEbus module selection, the VSBus lower limit and upper limit may be selected on any 64Kilobyte byte ($10000) boundaries within the selected bank is accomplished by installing (SHORTED) or removing (OPEN) the appropriate jumpers in blocks Blk D for lower limit and Blk C for upper limit, as illustrated in Figure 2.2. Position 1 is the least and position 8 is the most significant for both upper and lower limits.

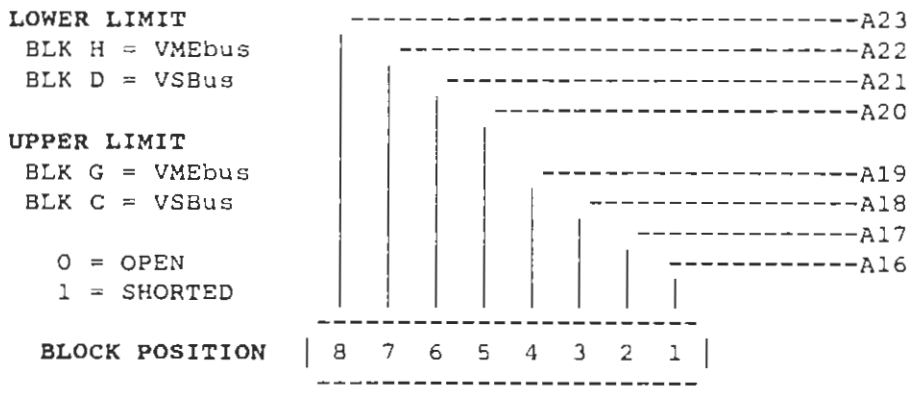


Figure 2.2 Upper & Lower Address selection

2.6.4 CONTROL / STATUS REGISTER ADDRESS SELECTION

Selection of the CSR address may be on any ODD address boundary, (ie: $0001, $0003, ..., $FFFF), within the VMEbus I/O space, by installing (SHORTED) or removing (OPEN) the appropriate jumpers in blocks Blk E for address bits A15 to A08, and Blk F for bits A07 to A01, as detailed in Figure 2.3.

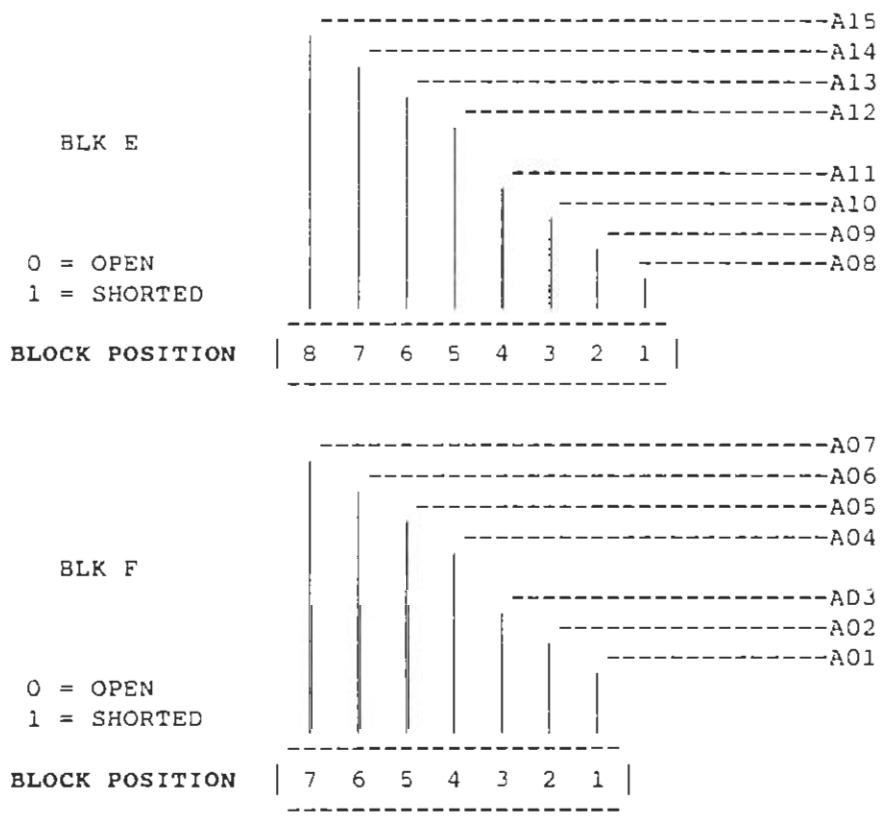


Figure 2.3 Control / Status Register Address selection

2.6.5 EXAMPLE ADDRESSING

To address the MM6300D Dual Ported Memory, the user must determine first where the MM6300D Dual Ported Memory is to be located. In this example I have chosen from 00100000 to $002FFFFF for the VMEbus and from $02000000 to $021FFFFF for the VSBus and an address of $0401 (VMEbus I/O space) for the CSR.

```
                 8                       1
                ------------------------
IF BLK B = |  0  0  0  0  0  0  0  0  |
                ------------------------
```

Then the VMEbus port would be selected or mapped into the first 16Megabyte bank ($00xxyyyy).

```
                 8                       1
                ------------------------
IF BLK H = |  0  0  0  1  0  0  0  0  |
                ------------------------
```

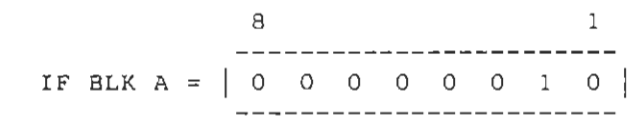
Then the VMEbus port would be selected, starting at location ($xx10yyyy).

```
                 8                       1
                ------------------------
IF BLK G = |  0  0  1  0  1  1  1  1  |
                ------------------------
```

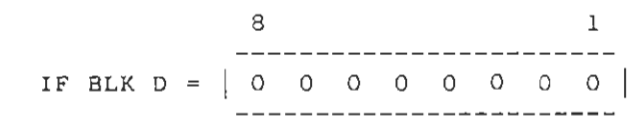
Then the VMEbus port would be selected upto (and including) location ($xx2Fyyyy).

(Note: the least significant 4 digits "yyyy" are ignored.)

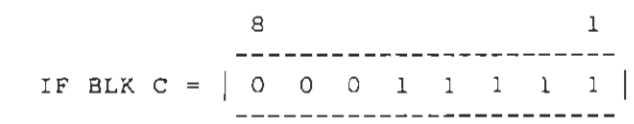
Figure 2.4 Example of VMEbus address selection:



Then the VSBus port would be selected or mapped into the third 16Megabyte bank ($02xxyyyy).



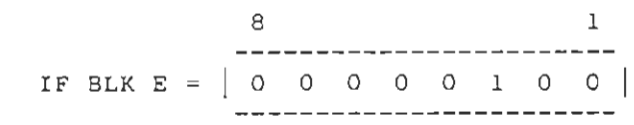
Then the VSBus port would be selected, starting at location ($xx00yyyy).

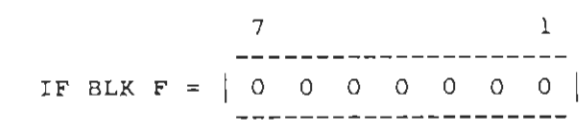


Then the VSBus port would be selected upto (and including) location ($xx1Fyyyy).

(Note: the least significant 4 digits "yyyy" are ignored.)

Figure 2.5 Example of VSBus addressing





Then the CSR would be selected at ($0401).

Figure 2.6 Example of CSR addressing

2.6.6 ADJUSTED ADDRESSING

In normal operation, the MM6300D Dual Ported Memory would be selected on a 2 Megabyte boundary. However, in some applications the user may wish to more accurately control the starting and ending addresses. An example would be when the user wants to start the memory immediately following some on-board memory (IE: 256 Kilobyte on-board memory). To keep both ports aligned (IE: first byte on VSBus port is first byte on VMEbus port), the addresses applied to the MM6300D Dual Ported Memory must be Adjusted, below 2 Megabyte increments. The MM6300D Dual Ported Memory allows the user to select an address on any 256 Kilobyte boundary, and still be fully aligned. If alignment is not necessary, the user may select on any 64 Kilobyte boundary.

2.7 INSTALLATION IN THE SYSTEM

After selecting the memory for the proper address locations by installing/removing the appropriate jumpers (see Section 2.6). And installing/removing the user defined option jumpers (see Section 2.5). And after following the guidelines set forth in Section 2.3, remove power, install the MM6300D Dual Ported Memory into the system, reapply power to the system.

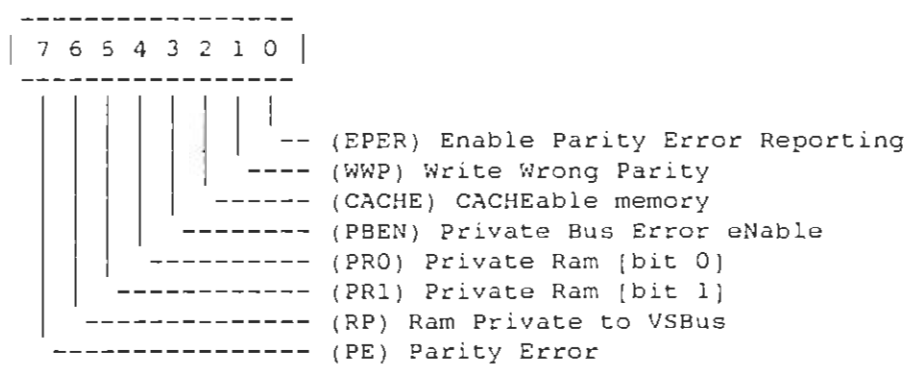
SECTION III

PROGRAMMING INFORMATION

3.1 CONTROL STATUS REGISTER

The Control Status Register (CSR) provides a VMEbus accessible resister to control and determine the status of the MM6300D Dual Ported Memory. In the following sections, the CSR bits are defined and their use is explained.

TABLE 3.1 C.S.R. BIT DEFINITIONS



3.2 PARITY ERROR DETECTION

The MM6300D Dual Ported Memory generates and checks for errors in the memory by calculating the parity of each byte in memory. During write cycles, the MM6300D Dual Ported Memory writes this bit into the array, and on read cycles it checks this bit against the bit in the array. If, during a read cycle, a difference is detected the CSR PE bit is set and if the CSR EPER bit is also set, the appropriate ERROR lead asserted. In the case of a VMEbus reference, the BERR* lead is asserted instead of the DTACK* lead. However on the VSBus, the ERR* is asserted along with the ACK* lead. The PE bit is cleared by reset or by writing a 0 into CSR bit 7.

3.3 THE PRIVATE BUS

There are two (2) methods to reserve memory for the VSBus, on the MM6300D Dual Ported Memory. Under software control, all or part may be reserved for exclusive use by the VSBus.

3.3.1 RP - RAM PRIVATE

The MM6300D Dual Ported Memory may be reserved in TOTAL, by setting the RP bit in the CSR to a 1. Any references made of the MM6300D Dual Ported Memory from the VMEbus port are ignored while this bit is set (see section 3.3.3 for exceptions).

3.3.2 PR1 & PR0 - PRIVATE RAM SEGMENTS

The PR0 & PR1 bits allocate the array to the VMEbus in 1Megabyte blocks (see Table 3.2). References made of the MM6300D Dual Ported Memory from the VMEbus port to segments not allocated to the VMEbus port are ignored (see section 3.3.3 for exceptions).

3.3.3 PBEN - PRIVATE BUS ERROR ENABLE

The RP, PR1 & PR0 bits control references made from the VMEbus port. Normally, references made by the VMEbus port are ignored, according to the allocations made (see sections 3.3.1 & 3.3.2). However the MM6300D Dual Ported Memory may be programmed to assert BERR* on the VMEbus instead of simply ignoring the reference. This often Speeds system performance by not having to wait for the Bus Timeout.

3.4 CACHEABLE MEMORY ENABLE

When set, this bit disables the CACHE* lead on the VSBus, indicating that the selected memory is NOT cacheable.

3.5 DIAGNOSTICS (WRITE WRONG PARITY)

The WWP bit, when set, causes the MM6300D Dual Ported Memory to generate the WRONG parity while writing to memory. This allows the system to test the parity bits of the MM6300D Dual Ported Memory during system diagnostics, by writing the wrong parity, and reading to see if the error is detected.

TABLE 3.2 PRIVATE MEMORY SEGMENTS

PR1	PR0	Memory Segment VMEbus accessible
0	0	3, 2, 1, 0
0	1	3, 2, 1
1	0	3, 2
1	1	3

Each segment contains 1 Mega bytes of memory.