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Find the *Curtiss-Wright / VMETRO / Micro Memory MM-6326/64M* at our website: *Click HERE*

MM-6326AD

64 MBYTE, DUAL-PORT, VME/VSB DRAM MEMORY MODULE

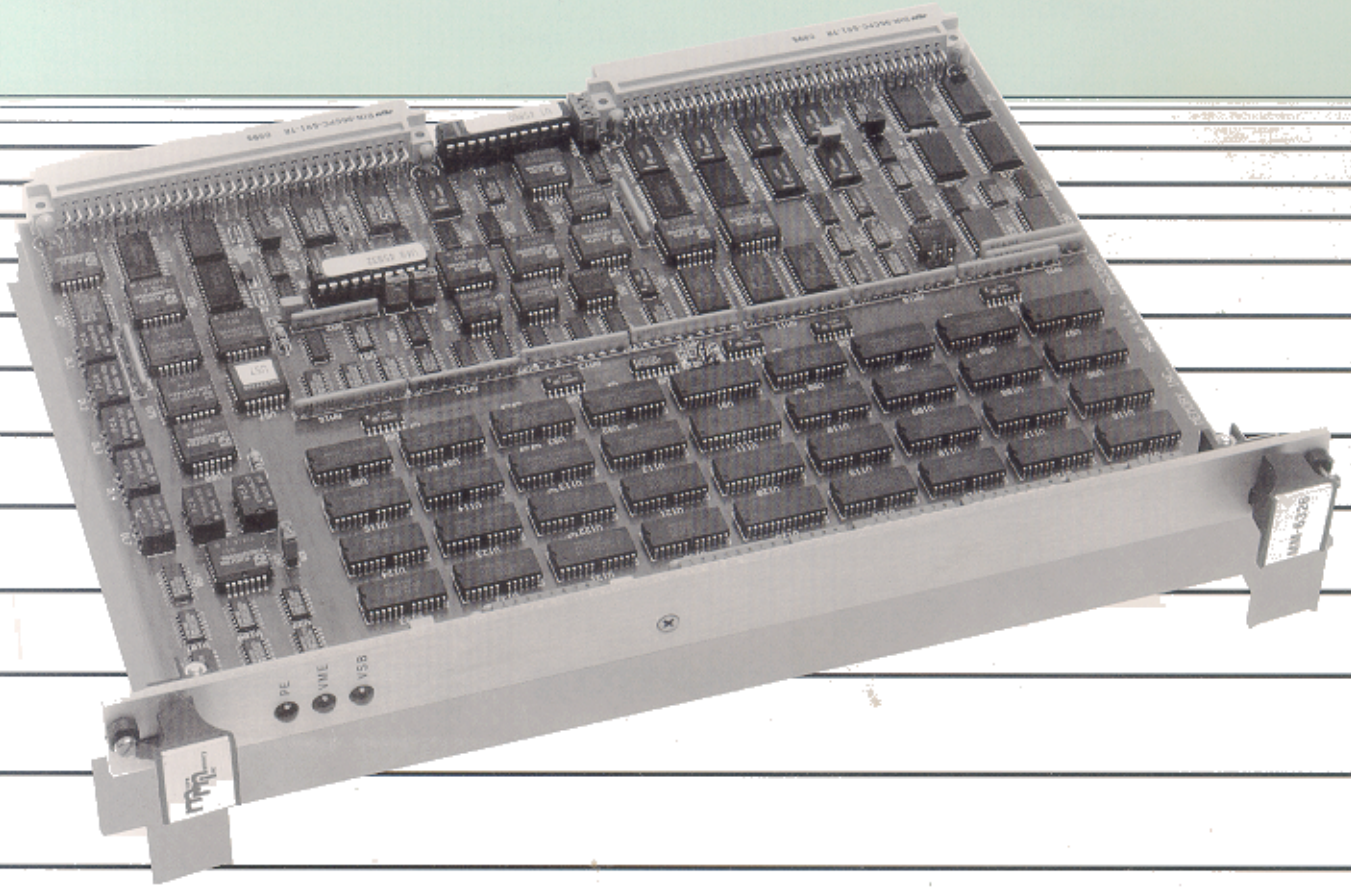
The MM-6326AD is a high speed, dual port, single card slot, high density memory module that provides up to 64 Mbytes for VME/VSB systems. It is intended for high performance applications employing Bank-Interleave, Page Mode and Block Transfer at data rates greater than 30 Mbytes/sec. It also supports sequential access (BLT) of 256 bytes on the VME and 64 K bytes on the VSB bus.

The Control Status Register (CSR), located in the short I/O address space, stores and reads byte-wide parity errors detected on the VME/VSB buses. The other bits enable Write-Wrong parity for diagnostics, disable VME-port and determine whether the memory is CACHEable on the VSB bus. Parity generation and checking are provided for each byte; parity status is stored and transmitted via BERR*.

Reliability is ensured by burn-in and running memory diagnostics that check operation for 48 hours while temperature-cycling boards from 0 to 60°C. Also, reliability is backed up by Micro Memory Inc.'s **Lifetime Warranty.**

FEATURES:

- Capacity: 32M and 64M bytes
- Cycle/Access Time (nsec): Read 125/75, Write 125/50 (Block Transfer-BLT, Page Mode and Bank-Interleave)
- Compatible with VMEbus Rev C.1 and VSBbus Rev C with A32/A24/D16/D8 (UAT) for VME and A32/D32 for VSB
- Block Transfer: VME=256 Bytes/Transfer
  VSB=64 Kbytes/Transfer
- Parity generation and checking for error detection on each byte
- Module selection on 1 Mbyte boundaries, jumper-selectable for lower and upper limits on each bus
- VMEbus Control Status Register (CSR) for parity reporting and control
- Write-Wrong parity for diagnostics
- Lifetime Warranty



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MM-6326AD SPECIFICATIONS

Parameter	Specification
Capacity	32M and 64M bytes
Cycle/Access Time (nsec)	Read: 125/75, Write: 125/50 (Block Transfer-BLT) Read: 200/150, Write: 200/90
Address	32 bits for VMEbus, 32 bits multiplexed with 32 data bits for the VSB bus
Data In/Data Out	8, 16, 32 bits (UAT) for VMEbus, 32 bits for VSB bus
Sequential Access	Block Transfer (BLT) of 256 bytes on VMEbus, 64K bytes on VSB bus
Address Modifiers	AM0-AM5 are decoded by socketed IFL with the following codes: A24: 39, 3A, 3D and 3E A32: 09, 0A, 0D and 0E A24 with BLT: 3B, 3F A32 with BLT: 0B, 0F
Parity Checking	Byte-wide parity generation and checking; parity output stored and transmitted via CSR; Write-Wrong parity for diagnostics
Control Status Register (CSR)	Read/Write, 8 bits wide, jumper-selectable, occupies one location in VME I/O space (A16)
CSR Format	D0 Enable Parity Out D1 Write-Wrong Parity D2 Memory CACHEable for VSB D6 VMEbus Disable D7 Parity Error Others: Don't Care
Interface	VME Rev C.1 and VSB Rev C
Modes of Operation	Read, write, read-modify-write, Page Mode in BLT, and refresh
Memory Selection	Two independent memory banks, switch-selectable on one Mbyte (100000H) boundaries for each port by setting the upper and lower limits
Operating Temperature	0 to +60°C
Storage Temperature	-40 to +85°C
Relative Humidity	Up to 95% without condensation
Power Requirements	5V @ 5.5 Amps

ORDERING INFORMATION

Part Number	Memory Capacity
MM-6326AD/XX	XX= 32M, 64M bytes (16 M bit Chips)

Specifications are subject to change without notice. Micro Memory Inc. reserves the right to make changes to improve reliability, function, or design. Micro Memory Inc. does not assume any liability arising from application of this product.

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