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MICRO MEMORY INC

9540 VASSAR AVE.

CHATSWORTH, CA. 91311

(818) 998-0070

MM-6400D

USERs GUIDE

NOVEMBER 1986

VMEbus DUAL port MEMORY MODULE for the VMXbus

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation procedures of the **MM6400D Dual Port Dynamic Random Access Memory Module**.

1.2 GENERAL DESCRIPTION

The **MM6400D Dual Ported Memory** is compatible with the **VMEbus**, VME Extended Bus (**VMXbus**) specifications. Inherent to the module are **VMEbus** options D32, D16 & D8 (32, 16 & 8 bit data path width), and A32, A24 (32, 24 bit address path width). The module also generates and stores an even parity bit for each byte written on write cycles and checks parity for each byte read on read cycles. Then if a parity error is detected, the module sets a **Control Status Register (CSR)** bit and may be programmed to assert the bus error signal on the requesting port. (see Section III for CSR programming)

While the **MM6400D Dual Ported Memory** was designed as a 32 bit wide (data path) memory board, the **MM6400D Dual Ported Memory** complies with **VMEbus** Specifications (**Revision C.1**) and **VMXbus** Specifications (**Revision B**) and can be addressed as 8 bit bytes, 16 bit words, or 32 bit longwords. The **MM6400D Dual Ported Memory** can be configured for 1M, 2M, 3M, and 4M bytes capacity by populating it with industry standard 256K X 9 NMOS DRAM Single-Inline-Packages (SIP) , such as the ASMD-1042 (120ns), or Texas Instruments TM4256EL9-12 NMOS DRAM modules.

The **MM6400D Dual Ported Memory** Control Status Register is software compatible with the **Motorola MVME204** memory modules.

The **MM6400D Dual Ported Memory** memory modules are available in several options depending on the capacity required. **Table 1.1** lists the optional part numbers for ordering purposes, the total memory capacity provided by each version.

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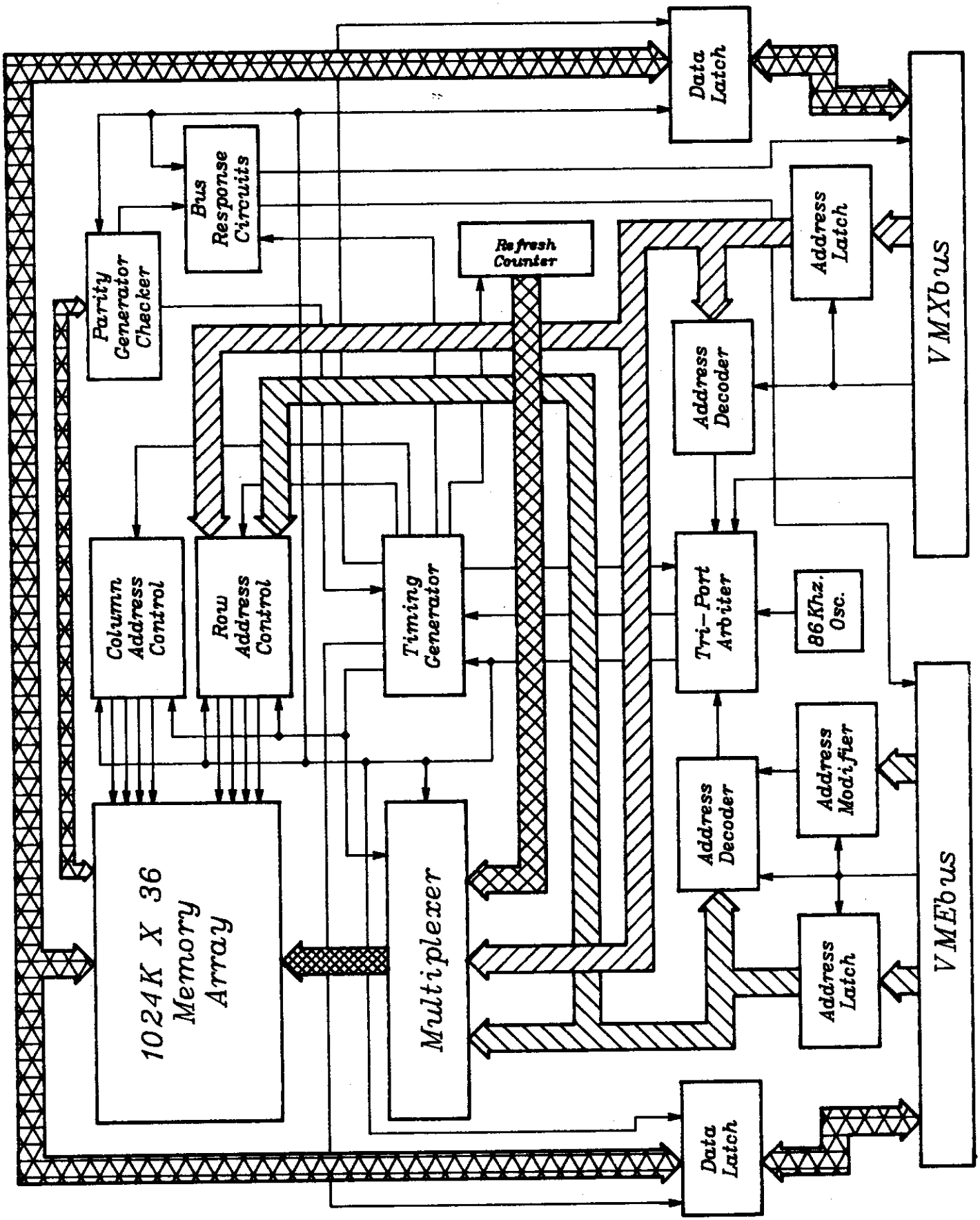
Table 1.1

Memory Capacity Options

Table 1.1 summarizes the options with respect to storage capacity, available to **MM6400D Dual Ported Memory** user.

Option	Capacity
MM6400D/1M	1.0M Bytes
MM6400D/2M	2.0M Bytes
MM6400D/3M	3.0M Bytes
MM6400D/4M	4.0M Bytes

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Functional Block Diagram Figure 1.1

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1.2.2 OPERATIONAL FEATURES

The **MM6400D Dual Ported Memory** module contains its own address register and data buffers for each port for total compatibility with the **VMEbus Specification (Rev. C.1)** and **VMXbus Specification (Rev. B)**

Module selection for the **MM6400D Dual Ported Memory** resides on 64K ($10000) byte boundaries. The module must be mapped in one of the 16Mega byte banks within the 4Giga bytes of physical address space, on each port, both the **VMEbus**.

The **MM6400D Dual Ported Memory** memory array can be addressed as 8 bit bytes, 16 bit words, or as 32 bit longwords. Memory cycle and Read/Write access times are 275nsec and 200/130nsec respectively.

The **MM6400D Dual Ported Memory** responds to various Address Modifier Codes. The codes are decoded by U14 (a socketed PAL), Various combinations are available to the user (see Section II, jumpers).

The user may select to create his/her own Address Modifier code<s>, in this event the Address Modifier evaluation PAL (U14) can be replaced to accommodate the systems' requirements (see Section II, jumpers).

A **Control Status Register (CSR)** is available to allow various dynamic options to to be utilized by the software programmer. Included in the **(CSR)** are bits to control the **Parity Error** output to requesting the bus, a bit allows for **Writing the Wrong Parity** for dynamic diagnostics. The **CSR** is an A16 Slave and has separate address selection jumpers, and may be addressed on any **ODD** boundary in the **VMEbus** I/O address space. (See Section III for programming details).

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1.3 GENERAL SPECIFICATIONS

Table 1.2 lists the general specifications for the **MM6400D** Dynamic Ram Memory Module.

Table 1.2

Characteristics	Specifications
Capacity	1M,2M,3M,or 4M,bytes
Cycle Time	275ns.
Read/Write Access Time	200ns./130ns. (fast write)
Address	24/32 bits **VMEbus** 24 bits **VMXbus**
Address Modifiers	6 bits, user programmable PAL
Data In/Data Out	8/16/32 bits bidirectional with 48 ma. three-state output
Parity	EVEN, 1 bit for each byte Generated on each WRITE Checked on each read
Modes of Operation	Read, Write, Read-modify-Write Hidden refresh, Un-aligned
Module Selection **VMEbus**	Memory selected on 64K byte ($10000) boundary in any 16 Megabyte bank within a 4G byte address space.
VMXbus	Memory selected on 64K byte ($10000) boundary within the 16 Megabyte **VMXbus** address space.
Control Status Register Selection	CSR Selected on any ODD address in the VMEbus 'A16' address space
Interface:	
Inputs	TTL-compatible
Outputs	48ma. Three-state, TTL-compatible
Operating Temperature	0 to 60 degrees C
Storage Temperature	-40 to +85 degrees C
Relative Humidity	95% without condensation
Power Requirements:	Standby Operate
+5V (fully-populated)	4.8A 5.0A

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Table 1.2
P1 Connector VMEbus Pin Assignments

PAGE NUMBER	ROWa SIGNAL MNEMONIC	ROWb SIGNAL MNEMONIC	ROWc SIGNAL MNEMONIC
1	D00	** BBSY*	D08
2	D01	** BCLR*	D09
3	D02	** ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	** SYSCLK	BG3IN*	** SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	** BR0*	SYSRESET*
13	DS0*	** BR1*	LWORD*
14	WRITE*	** BR2*	AM5
15	GND	** BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	** SERCLK(1)	A17
22	IACKOUT*	** SERDAT*(1)	A16
23	AM4	GND	A15
24	A07	** IRQ7*	A14
25	A06	** IRQ6*	A13
26	A05	** IRQ5*	A12
27	A04	** IRQ4*	A11
28	A03	** IRQ3*	A10
29	A02	** IRQ2*	A09
30	A01	** IRQ1*	A08
31	** -12v	** +5vSTDBY	** +12v
32	+5v	+5v	+5v

**** - No Connection on MM6400D Dual Ported Memory**

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Table 1.3
P2 Connector VMEbus/VMXbus Pin Assignments

PAGE NUMBER	ROWa SIGNAL MNEMONIC	ROWb SIGNAL MNEMONIC	ROWc SIGNAL MNEMONIC
1	DB00	+5v	DB01
2	DB02	GND	DB03
3	DB04	** RESERVED	DB05
4	DB06	A24	DB07
5	DB08	A25	DB09
6	DB10	A26	DB11
7	DB12	A27	DB13
8	DB14	A28	DB15
9	DB16	A29	DB17
10	DB18	A30	DB19
11	DB20	A31	DB21
12	DB22	GND	DB23
13	DB24	+5v	DB25
14	DB26	D16	DB27
15	DB28	D17	DB29
16	DB30	D18	DB31
17	WRITE*	D19	** RESERVED
18	** IRQ*	D20	** RESERVED
19	LWORD/A12	D21	** RESERVED
20	A02/A14	D22	A01/A13
21	A04/A16	D23	A03/A15
22	A06/A18	GND	A05/A17
23	A08/A20	D24	A07/A19
24	A10/A22	D25	A09/A21
25	** RESERVED	D26	A11/A23
26	** RESERVED	D27	LAS*
27	** RESERVED	D28	UAS*
28	** RESERVED	D29	UDS*
29	** RESERVED	D30	LDS*
30	** RESERVED	D31	DERR*
31	SMACKIN*	GND	ACK*
32	** SMRQ*	+5v	SMACKOUT*

** - No Connection on MM6400D Dual Ported Memory

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1.4 INTERFACE TIMING

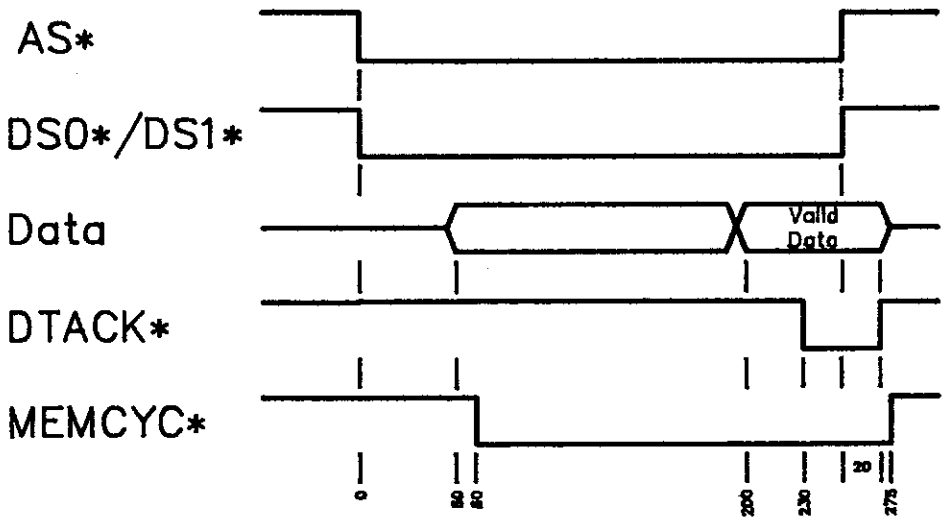
The **MM6400D Dual Ported Memory** memory modules are designed to accept Industry Standard 256K x 9 DYNAMIC Random Access Memory modules with a 120nsec typical access delay Time (ie: ASMD-1042).

The **VMEbus** Interface Timing Diagram (Figure 1.2), illustrates the timing relationships on the Data Transfer bus, for Read and Write Cycles. Access delay time is measured from the leading edge of the Data strobes. (Figure 1.2).

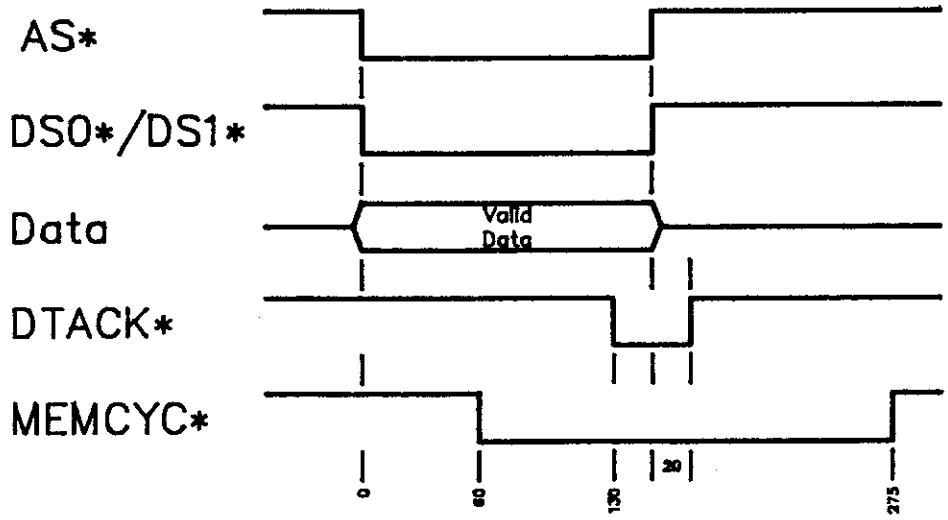
The **VMXbus** Interface Timing Diagram (Figure 1.3), illustrates the timing relationships on the Data Transfer bus, for Read and Write Cycles. Access delay time is measured from the leading edge of the Data strobes. (Figure 1.3).

The refresh cycle timing is illustrated by Figure 1.4. Refresh cycles are repeated once every 15usec. The cycle interval timing is generated by a free running oscillator (U68) providing a refresh transparent to memory access cycles.

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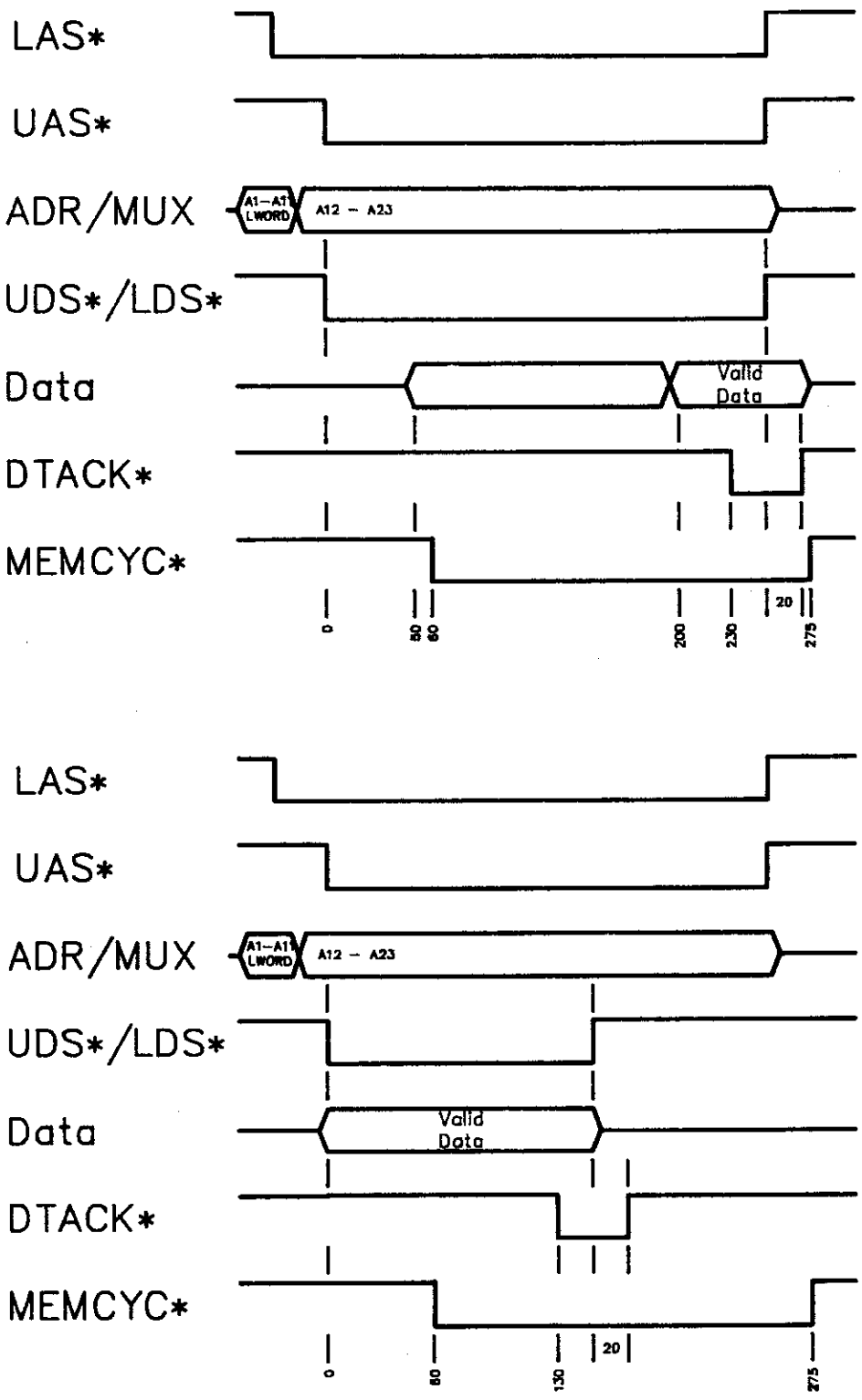
Read Cycle



Write Cycle

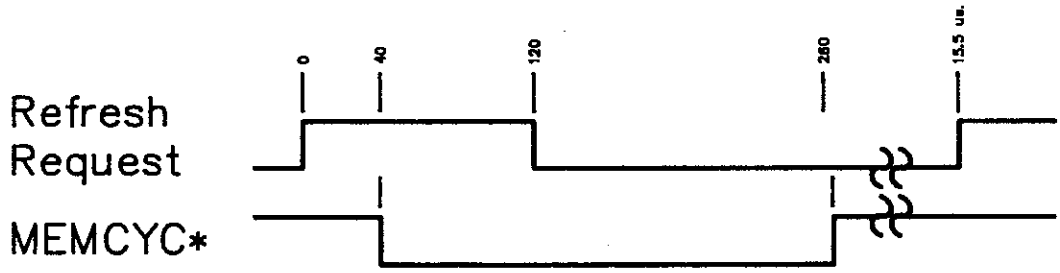
VMEbus Interface Timing Diagram Figure 1.2

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VMXbus Interface Timing Diagram Figure 1.3

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Refresh Timing Diagram Figure 1.4

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1.5 MEMORY ARRAY ORGANIZATION

The memory array is partitioned into four 256K x 36 bit segments. The minimum memory configuration would be 256K x 36 bits, including the four parity bits DRAMs in segment zero. This would translate to 1Megabytes minimum configuration for the **MM6400D Dual Ported Memory.**

The **MM6400D Dual Ported Memory** is partitioned as four blocks of 36 bits each (32 plus 4 parity), however the system will only see 32 bits of data during memory references, as the parity is generated and checked transparent to the user. The 32 bits of data are divided into 4 bytes (8 bits each). While the memory reads and writes may be 8, 16 or 32 bits wide, the memory is organized as 32 bit wide locations with logic controlling which byte<s> the user is reading or writing.

If the contents of the first 8 locations in memory are $01 $23 $45 $67 $89 $AB $CD $EF, determining which bits constitute what byte may be somewhat confusing. This can be cleared up by seeing the same data in the various formats used in most systems (IE: Byte, Word, and Longword).

BYTE Format		WORD Format		LONGWORD Format	
Location	Data	Location	Data	Location	Data
$00000000	$01	$00000000	$0123	$00000000	$01234567
$00000001	$23	$00000002	$4567	$00000004	$89ABCDEF
$00000002	$45	$00000004	$89AB		
$00000003	$67	$00000006	$CDEF		
$00000004	$89				
$00000005	$AB				
$00000006	$CD				
$00000007	$EF				

BIT Organizations

LONGWORD

```
3               1 1               0 3               1 1               0
1...............6 5...............0 1...............6 5...............0
```

WORD

```
1               0 1               0 1               0 1               0
5...............0 5...............0 5...............0 5...............0
```

BYTE

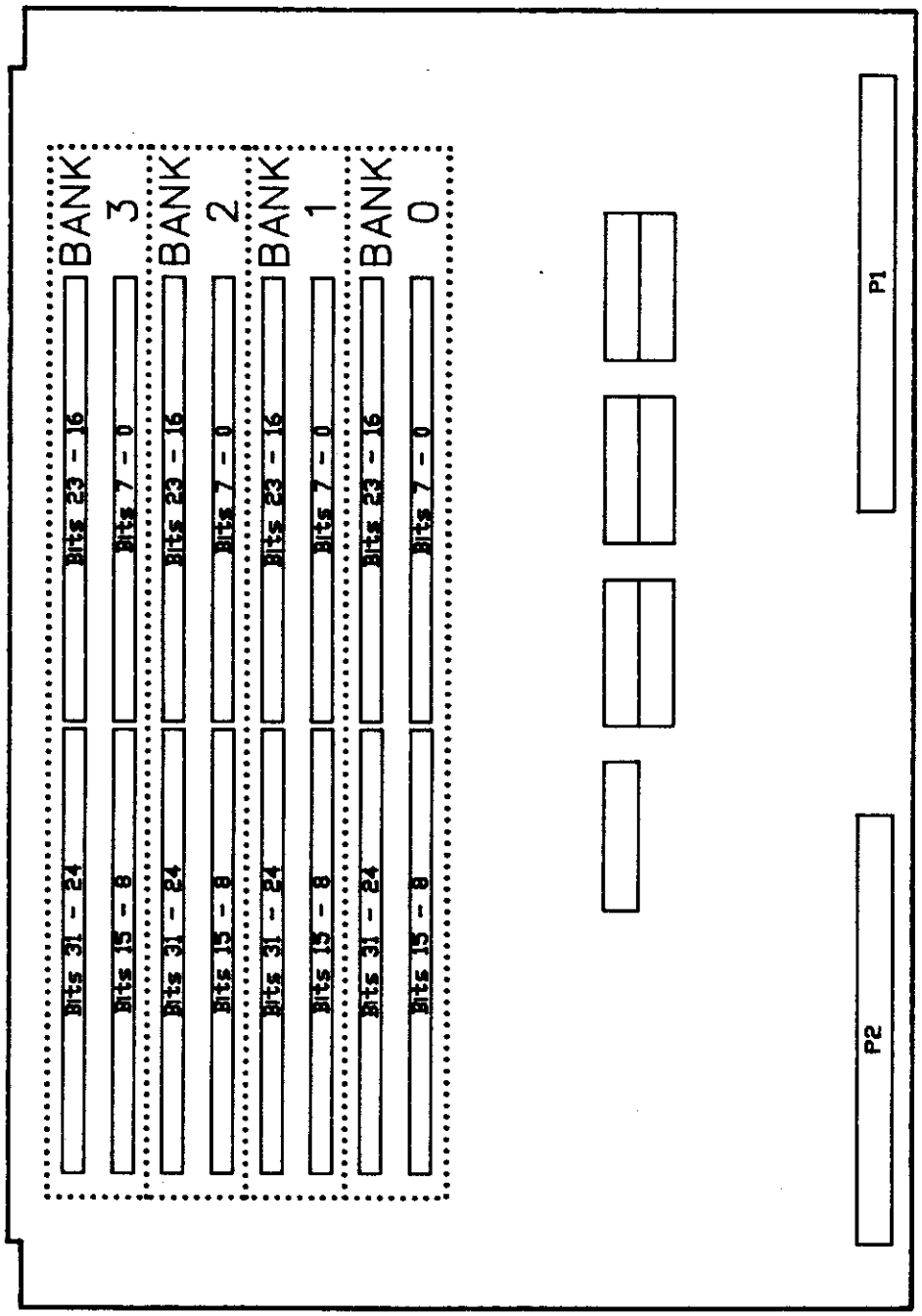
```
0       00      0 0       00      0 0       00      0 0       00      0
7......07......0 7......07......0 7......07......0 7......07......0

0000000100100011 0100010101100111 1000100110101011 1100110111101111
 $0  $1  $2  $3   $4  $5  $6  $7   $8  $9  $A  $B   $C  $D  $E  $F
```


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Table 1.5

DRAM Device locations for the MM6400D Dual Ported Memory



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SECTION II

INSTALLATION

2.1 INTRODUCTION

This section details a step by step procedure to interface the **MM6400D Dual Ported Memory** to both the **VMEbus** and **VMXbus**.

2.2 UNPACKING INSTRUCTIONS

Unpack module from shipping carton. If carton is damaged upon receipt, request that the carrier's agent be present during unpacking and inspection of the equipment. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment. For repairs or replacement of a board damaged during shipment, contact **MICRO MEMORY, Inc.** to obtain a Return Authorization number and further instructions.

2.3 HARDWARE PREPARATION

The memory module should be inspected and prepared for jumper placement prior to system installation. The following sections describe the proper jumper options necessary for system operation (see Section 2.5, for jumper options).

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2.3.1 Handling Procedure

The **MM6400D Dual Ported Memory** uses MOS components that are susceptible to damage if exposed to static electrical charges. To avoid damage of these components during handling, testing or operation, the following procedure should be used.

A. Device leads should contact conductive material to avoid building of any static charge, except during testing or operation.

B. Soldering iron tips, metal fixtures, tools, and handling facilities used in preparing the module for operation should be grounded.

C. Devices should never be removed or inserted while power is applied to the module because voltage transients may permanently damage the devices and/or module.

D. **The memory module should never be plugged in or out of the cardcage while power is applied.**

E. External signals should not be applied to device inputs while power is removed.

F. Any memory module removed from the system should be transferred to either non-conductive foam or an anti-static plastic bag for storage or shipment.

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2.4 OPERATING ENVIRONMENT

The **MM6400D Dual Ported Memory** is an extremely **High Density** memory product. Containing, 64 bits of high current (48ma.) data bus drivers, numerous high speed components. And as a result, the environment into which the **MM6400D Dual Ported Memory** is placed, must be carefully considered.

2.4.1 AIRFLOW AND COOLING

Due to the extremely high component density of the **MM6400D Dual Ported Memory**, an adequate airflow is required to maintain the operating temperature within specifications of the memory module. Failure to adhere to these requirements may result in poor long term reliability.

2.4.2 POWER REQUIREMENTS

The power requirements of **MM6400D Dual Ported Memory** are such, that the module should never be operated while powered only by the **P1** connector. Hence power should be applied to the appropriate pins (See Tables 1.3 & 1.4) of both the **P1** and the **P2** connector prior to operation of the **MM6400D Dual Ported Memory**.

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2.5 JUMPER OPTIONS

There are several jumper options attainable on the **MM6400D Dual Ported Memory** memory module, depending on the user application. All of the available options are selected by installing or removing mini-jumpers on wirewrap pins on 0.100 inch centers. (see Figure G.1)

2.5.1 Address Modifier Evaluation/Selection

The **MM6400D Dual Ported Memory** evaluates the Address Modifiers from the **VMEbus** to determine if they are to be responded to. As shipped from the factory, the **MM6400D Dual Ported Memory** responds to the common **A24** (using only 24 address bits) & **A32** (using all 32 address bits) Address Modifier codes. These Address Modifier codes are described in Appendix D. The user may select to replace the Address Modifier selection PAL (U14), to allow for some other combination or the creation of a special (user defined) code or codes. As shipped, when responding to the **A24** Address Modifier code, the **MM6400D Dual Ported Memory** will only use **A1** through **A23** to evaluate the address. However this also is programmable by PAL (U14).

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2.6 ADDRESS and CONFIGURATION JUMPER SETTINGS

The **MM6400D Dual Port Memory** contains four (4) major jumper blocks and a single jumper pair that must be configured prior to installation before proper operation can be obtained. (See Figure G.1 for jumper locations)

The **VMEbus** port of the **MM6400 Dual Port Memory** must be addressed in it's four (4) Gigabyte address space. While the **VMXbus** port need only selected within the 16Megabyte address space of the **VMXbus**. The **VMEbus** port is controlled by jumper blocks **Blk A, Blk B & Blk G**. While the **VMXbus** port is controlled by blocks **Blk C & Blk D**. The installation (**SHORTED**) or removal (**OPEN**) of these mini-jumpers represent ones and zeros in the following examples.

2.6.1 Bank Selection

The **MM6400 Dual Port Memory** may be selected on any 64Kilobyte ($10000) boundary. However, due to the 24bit address mode required by **A24** bus masters on the **VMEbus**, the **MM6400 Dual Port Memory** must reside wholly inside one of 256 16Megabyte banks. This is controlled by **Blk G** on the **VMEbus** (see Figure 2.1).

BANK SELECTION

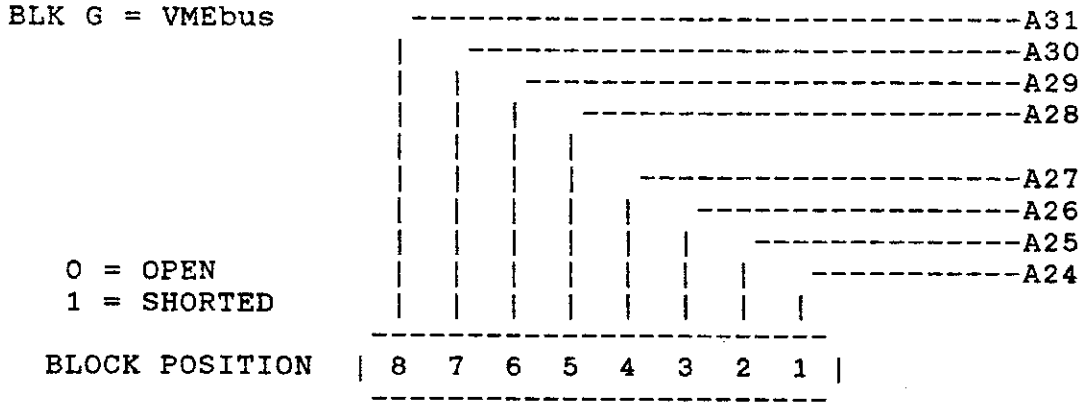


Figure 2.1 16Megabyte Bank selection

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2.6.2 VMEbus Module Selection

Selection of the **VMEbus** lower limit and upper limit on 64Kilobyte byte ($10000) boundaries within the selected bank is accomplished by installing (**SHORTED**) or removing (**OPEN**) the appropriate jumpers in blocks **Blk B** for lower limit and **Blk A** for upper limit, as illustrated in Figure 2.2. Position 1 is the least and position 8 is the most significant for both upper and lower limits.

2.6.3 VMXbus Module Selection

As with the **VMEbus** module selection, the **VMXbus** lower limit and upper limit may be selected on any 64Kilobyte byte ($10000) boundaries within the selected bank is accomplished by installing (**SHORTED**) or removing (**OPEN**) the appropriate jumpers in blocks **Blk D** for lower limit and **Blk C** for upper limit, as illustrated in Figure 2.2. Position 1 is the least and position 8 is the most significant for both upper and lower limits.

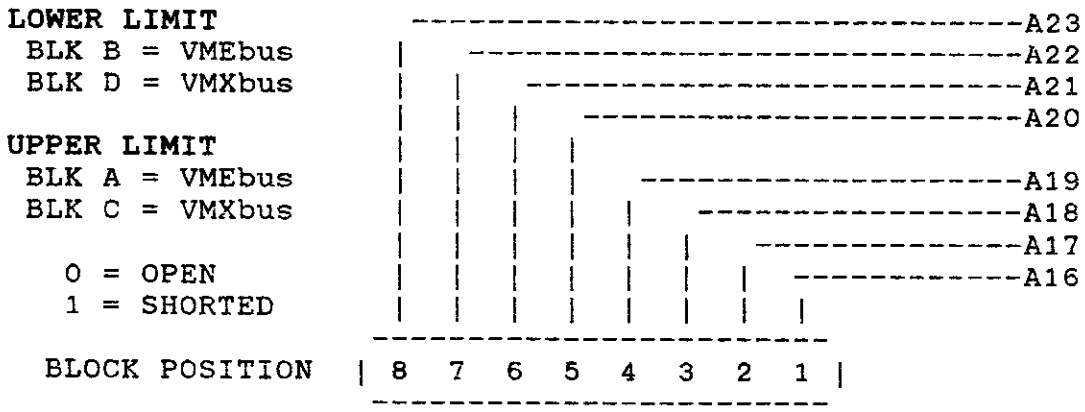


Figure 2.2 Upper & Lower Address selection

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2.6.4 Control / Status Register Address Selection

Selection of the **CSR** address may be on any **ODD** address boundary, (ie: $0001, $0003, ..., $FFFF), within the **VMEbus** I/O space, by installing (**SHORTED**) or removing (**OPEN**) the appropriate jumpers in blocks **Blk E** for address bits A15 to A08, and Blk H for bits A07 to A01, as detailed in Figure 2.3.

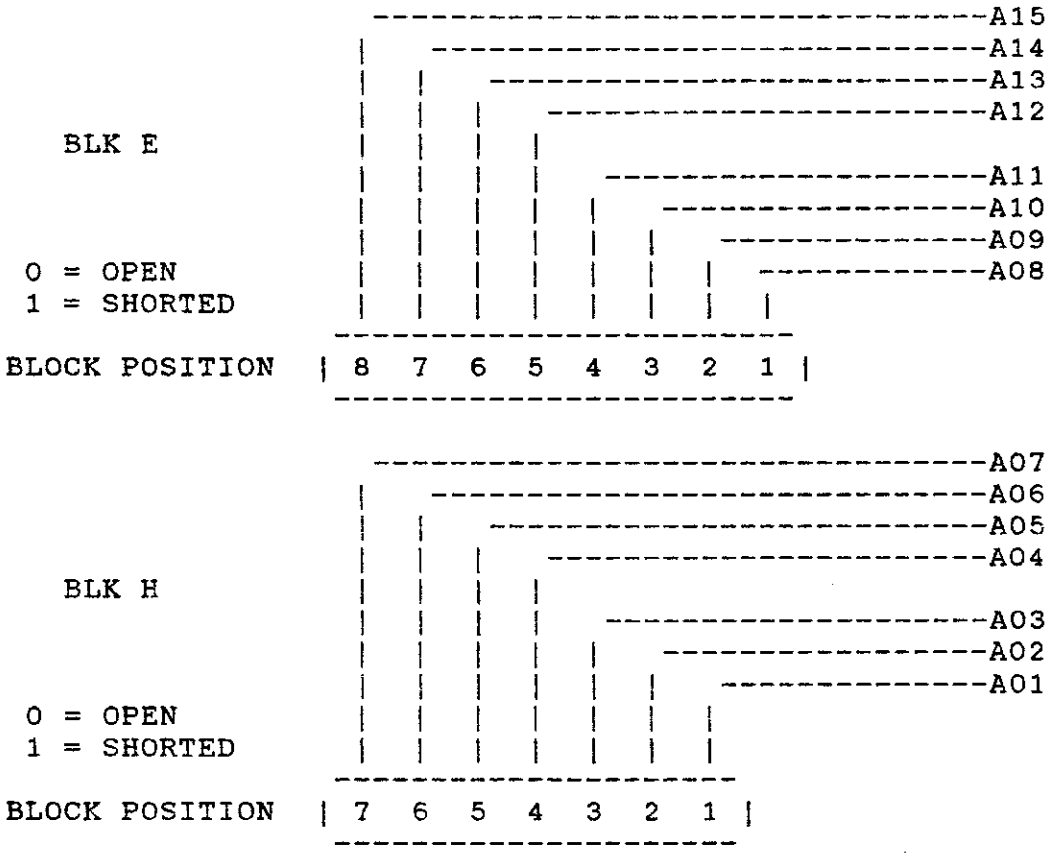


Figure 2.3 Control / Status Register Address selection

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2.6.5 Example Addressing

To address the **MM6400D Dual Ported Memory**, the user must determine first where the **MM6400D Dual Ported Memory** is to be located. In this example I have chosen from 00100000 to $004FFFFF for the **VMEbus** and from $000000 to $3FFFFF for the **VMXbus**. And an address of $0401 (**VMEbus** I/O space) for the **CSR**.

```
                 8                       1
                ------------------------
IF BLK G = | 0  0  0  0  0  0  0  0 |
                ------------------------
```

Then the **VMEbus** port would be selected or mapped into the first 16Megabyte bank ($00xxyyyy).

```
                 8                       1
                ------------------------
IF BLK B = | 0  0  0  1  0  0  0  0 |
                ------------------------
```

Then the **VMEbus** port would be selected, starting at location ($xx10yyyy).

```
                 8                       1
                ------------------------
IF BLK A = | 0  1  0  0  1  1  1  1 |
                ------------------------
```

Then the **VMEbus** port would be selected upto (and including) location ($xx4Fyyyy).

(Note: the least significant 4 digits "yyyy" are ignored.)

Figure 2.4 Example of VMEbus address selection:

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```
                 8                       1
                ------------------------
  IF BLK D = | 0  0  0  0  0  0  0  0 |
                ------------------------
```

Then the **VMXbus** port would be selected, starting at location ($00yyyy).

```
                 8                       1
                ------------------------
  IF BLK C = | 0  0  1  1  1  1  1  1 |
                ------------------------
```

Then the **VMXbus** port would be selected upto (and including) location ($3Fyyyy).

(Note: the least significant 4 digits "yyyy" are ignored.)

Figure 2.5 Example of VMXbus addressing

```
                 8                       1
                ------------------------
  IF BLK E = | 0  0  0  0  0  1  0  0 |
                ------------------------

                 7                    1
                ---------------------
  IF BLK H = | 0  0  0  0  0  0  0 |
                ---------------------
```

Then the **CSR** would be selected at ($0401).

Figure 2.6 Example of CSR addressing

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2.6.6 Adjusted Addressing

In normal operation, the **MM6400D Dual Ported Memory** would be selected on a 4 Megabyte boundary. However, in some applications the user may wish to more accurately control the starting and ending addresses. An example would be when the user wants to start the memory immediately following some on-board memory (IE: 256 Kilobyte on-board memory). To keep both ports aligned (IE: first byte on **VMXbus** port is first byte on **VMEbus** port), the addresses applied to the **MM6400D Dual Ported Memory** must be **Adjusted**, below 4 Megabyte increments. The **MM6400D Dual Ported Memory** allows the user to select an address on any 256 Kilobyte boundary, and still be fully aligned. If alignment is not necessary, the user may select on any 64 Kilobyte boundary.

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2.7 Installation in the system

After selecting the memory for the proper address locations by installing/removing the appropriate jumpers (see Section 2.6). And installing/removing the user defined option jumpers (see Section 2.5). And after following the guidelines set forth in Section 2.3, remove power, install the **MM6400D Dual Ported Memory** into the system, reapply power to the system.

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SECTION III

PROGRAMMING INFORMATION

3.1 Control Status Register

The **Control Status Register (CSR)** provides a **VMEbus** accessible resister to control and determine the status of the **MM6400D Dual Ported Memory**. In the following sections, the **CSR** bits are defined and their use is explained.

Table 3.1 C.S.R. Bit Definitions

```
 -----------------
| 7 6 5 4 3 2 1 0 |
 -----------------
  | | | | | | | |
  | | | | | | |  -- (EPER) Enable Parity Error Reporting
  | | | | | | ---- (WWP) Write Wrong Parity
  | | | | | ------ N/C
  | | | | --------- N/C
  | | | ----------- N/C
  | | -------------- N/C
  | ---------------- N/C
   ------------------ (PE) Parity Error
```


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3.2 Parity Error Detection

The **MM6400D Dual Ported Memory** generates and checks for errors in the memory by calculating the parity of each byte in memory. During write cycles, the **MM6400D Dual Ported Memory** writes this bit into the array, and on read cycles it checks this bit against the bit in the array. If, during a read cycle, a difference is detected the **CSR PE** bit is set and if the **CSR EPER** bit is also set, the appropriate **ERROR** lead asserted. In the case of a **VMEbus** reference, the **BERR*** lead is asserted instead of the **DTACK*** lead. However on the **VMXbus**, the **ERR*** is asserted along with the **ACK*** lead. The **PE** bit is cleared by reset or by writing a 0 into **CSR** bit 7.

3.3 Diagnostics (Write Wrong Parity)

The **WWP** bit, when set, causes the **MM6400D Dual Ported Memory** to generate the **WRONG** parity while writing to memory. This allows the system to test the parity bits of the **MM6400D Dual Ported Memory** during system diagnostics, by writing the wrong parity, and reading to see if the error is detected.

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TABLE A.1.1

BANK SELECTION
(A24 - A31)
(BLK G)

0 = Open
1 = Closed

BANK SELECTED	8	7	6	5	4	3	2	1
$00yyyyyy	0	0	0	0	0	0	0	0
$01yyyyyy	0	0	0	0	0	0	0	1
$02yyyyyy	0	0	0	0	0	0	1	0
$03yyyyyy	0	0	0	0	0	0	1	1
$04yyyyyy	0	0	0	0	0	1	0	0
$05yyyyyy	0	0	0	0	0	1	0	1
$06yyyyyy	0	0	0	0	0	1	1	0
$07yyyyyy	0	0	0	0	0	1	1	1
$08yyyyyy	0	0	0	0	1	0	0	0
$09yyyyyy	0	0	0	0	1	0	0	1
$0Ayyyyyy	0	0	0	0	1	0	1	0
$0Byyyyyy	0	0	0	0	1	0	1	1
$0Cyyyyyy	0	0	0	0	1	1	0	0
$0Dyyyyyy	0	0	0	0	1	1	0	1
$0Eyyyyyy	0	0	0	0	1	1	1	0
$0Fyyyyyy	0	0	0	0	1	1	1	1
$10yyyyyy	0	0	0	1	0	0	0	0
$11yyyyyy	0	0	0	1	0	0	0	1
$12yyyyyy	0	0	0	1	0	0	1	0
$13yyyyyy	0	0	0	1	0	0	1	1
$14yyyyyy	0	0	0	1	0	1	0	0
$15yyyyyy	0	0	0	1	0	1	0	1
$16yyyyyy	0	0	0	1	0	1	1	0
$17yyyyyy	0	0	0	1	0	1	1	1
$18yyyyyy	0	0	0	1	1	0	0	0
$19yyyyyy	0	0	0	1	1	0	0	1
$1Ayyyyyy	0	0	0	1	1	0	1	0
$1Byyyyyy	0	0	0	1	1	0	1	1
$1Cyyyyyy	0	0	0	1	1	1	0	0
$1Dyyyyyy	0	0	0	1	1	1	0	1
$1Eyyyyyy	0	0	0	1	1	1	1	0
$1Fyyyyyy	0	0	0	1	1	1	1	1

BANK SELECTED	8	7	6	5	4	3	2	1
$20yyyyyy	0	0	1	0	0	0	0	0
$21yyyyyy	0	0	1	0	0	0	0	1
$22yyyyyy	0	0	1	0	0	0	1	0
$23yyyyyy	0	0	1	0	0	0	1	1
$24yyyyyy	0	0	1	0	0	1	0	0
$25yyyyyy	0	0	1	0	0	1	0	1
$26yyyyyy	0	0	1	0	0	1	1	0
$27yyyyyy	0	0	1	0	0	1	1	1
$28yyyyyy	0	0	1	0	1	0	0	0
$29yyyyyy	0	0	1	0	1	0	0	1
$2Ayyyyyy	0	0	1	0	1	0	1	0
$2Byyyyyy	0	0	1	0	1	0	1	1
$2Cyyyyyy	0	0	1	0	1	1	0	0
$2Dyyyyyy	0	0	1	0	1	1	0	1
$2Eyyyyyy	0	0	1	0	1	1	1	0
$2Fyyyyyy	0	0	1	0	1	1	1	1
$30yyyyyy	0	0	1	1	0	0	0	0
$31yyyyyy	0	0	1	1	0	0	0	1
$32yyyyyy	0	0	1	1	0	0	1	0
$33yyyyyy	0	0	1	1	0	0	1	1
$34yyyyyy	0	0	1	1	0	1	0	0
$35yyyyyy	0	0	1	1	0	1	0	1
$36yyyyyy	0	0	1	1	0	1	1	0
$37yyyyyy	0	0	1	1	0	1	1	1
$38yyyyyy	0	0	1	1	1	0	0	0
$39yyyyyy	0	0	1	1	1	0	0	1
$3Ayyyyyy	0	0	1	1	1	0	1	0
$3Byyyyyy	0	0	1	1	1	0	1	1
$3Cyyyyyy	0	0	1	1	1	1	0	0
$3Dyyyyyy	0	0	1	1	1	1	0	1
$3Eyyyyyy	0	0	1	1	1	1	1	0
$3Fyyyyyy	0	0	1	1	1	1	1	1

yyyyyy = Lower / Upper Limit Select Setting (See Table B.1)

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TABLE A.1.2

BANK SELECTION
(A24 - A31)
(BLK G)

0 = Open
1 = Closed

BANK SELECTED	8	7	6	5	4	3	2	1
$40yyyyyy	0	1	0	0	0	0	0	0
$41yyyyyy	0	1	0	0	0	0	0	1
$42yyyyyy	0	1	0	0	0	0	1	0
$43yyyyyy	0	1	0	0	0	0	1	1
$44yyyyyy	0	1	0	0	0	1	0	0
$45yyyyyy	0	1	0	0	0	1	0	1
$46yyyyyy	0	1	0	0	0	1	1	0
$47yyyyyy	0	1	0	0	0	1	1	1
$48yyyyyy	0	1	0	0	1	0	0	0
$49yyyyyy	0	1	0	0	1	0	0	1
$4Ayyyyyy	0	1	0	0	1	0	1	0
$4Byyyyyy	0	1	0	0	1	0	1	1
$4Cyyyyyy	0	1	0	0	1	1	0	0
$4Dyyyyyy	0	1	0	0	1	1	0	1
$4Eyyyyyy	0	1	0	0	1	1	1	0
$4Fyyyyyy	0	1	0	0	1	1	1	1
$50yyyyyy	0	1	0	1	0	0	0	0
$51yyyyyy	0	1	0	1	0	0	0	1
$52yyyyyy	0	1	0	1	0	0	1	0
$53yyyyyy	0	1	0	1	0	0	1	1
$54yyyyyy	0	1	0	1	0	1	0	0
$55yyyyyy	0	1	0	1	0	1	0	1
$56yyyyyy	0	1	0	1	0	1	1	0
$57yyyyyy	0	1	0	1	0	1	1	1
$58yyyyyy	0	1	0	1	1	0	0	0
$59yyyyyy	0	1	0	1	1	0	0	1
$5Ayyyyyy	0	1	0	1	1	0	1	0
$5Byyyyyy	0	1	0	1	1	0	1	1
$5Cyyyyyy	0	1	0	1	1	1	0	0
$5Dyyyyyy	0	1	0	1	1	1	0	1
$5Eyyyyyy	0	1	0	1	1	1	1	0
$5Fyyyyyy	0	1	0	1	1	1	1	1
$60yyyyyy	0	1	1	0	0	0	0	0
$61yyyyyy	0	1	1	0	0	0	0	1
$62yyyyyy	0	1	1	0	0	0	1	0
$63yyyyyy	0	1	1	0	0	0	1	1
$64yyyyyy	0	1	1	0	0	1	0	0
$65yyyyyy	0	1	1	0	0	1	0	1
$66yyyyyy	0	1	1	0	0	1	1	0
$67yyyyyy	0	1	1	0	0	1	1	1
$68yyyyyy	0	1	1	0	1	0	0	0
$69yyyyyy	0	1	1	0	1	0	0	1
$6Ayyyyyy	0	1	1	0	1	0	1	0
$6Byyyyyy	0	1	1	0	1	0	1	1
$6Cyyyyyy	0	1	1	0	1	1	0	0
$6Dyyyyyy	0	1	1	0	1	1	0	1
$6Eyyyyyy	0	1	1	0	1	1	1	0
$6Fyyyyyy	0	1	1	0	1	1	1	1
$70yyyyyy	0	1	1	1	0	0	0	0
$71yyyyyy	0	1	1	1	0	0	0	1
$72yyyyyy	0	1	1	1	0	0	1	0
$73yyyyyy	0	1	1	1	0	0	1	1
$74yyyyyy	0	1	1	1	0	1	0	0
$75yyyyyy	0	1	1	1	0	1	0	1
$76yyyyyy	0	1	1	1	0	1	1	0
$77yyyyyy	0	1	1	1	0	1	1	1
$78yyyyyy	0	1	1	1	1	0	0	0
$79yyyyyy	0	1	1	1	1	0	0	1
$7Ayyyyyy	0	1	1	1	1	0	1	0
$7Byyyyyy	0	1	1	1	1	0	1	1
$7Cyyyyyy	0	1	1	1	1	1	0	0
$7Dyyyyyy	0	1	1	1	1	1	0	1
$7Eyyyyyy	0	1	1	1	1	1	1	0
$7Fyyyyyy	0	1	1	1	1	1	1	1

yyyyyy = Lower / Upper Limit Select Setting (See Table B.1)

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TABLE A.1.3

BANK SELECTION
(A24 - A31)
(BLK G)

0 = Open
1 = Closed

BANK SELECTED	8	7	6	5	4	3	2	1
$80yyyyyy	1	0	0	0	0	0	0	0
$81yyyyyy	1	0	0	0	0	0	0	1
$82yyyyyy	1	0	0	0	0	0	1	0
$83yyyyyy	1	0	0	0	0	0	1	1
$84yyyyyy	1	0	0	0	0	1	0	0
$85yyyyyy	1	0	0	0	0	1	0	1
$86yyyyyy	1	0	0	0	0	1	1	0
$87yyyyyy	1	0	0	0	0	1	1	1
$88yyyyyy	1	0	0	0	1	0	0	0
$89yyyyyy	1	0	0	0	1	0	0	1
$8Ayyyyyy	1	0	0	0	1	0	1	0
$8Byyyyyy	1	0	0	0	1	0	1	1
$8Cyyyyyy	1	0	0	0	1	1	0	0
$8Dyyyyyy	1	0	0	0	1	1	0	1
$8Eyyyyyy	1	0	0	0	1	1	1	0
$8Fyyyyyy	1	0	0	0	1	1	1	1
$90yyyyyy	1	0	0	1	0	0	0	0
$91yyyyyy	1	0	0	1	0	0	0	1
$92yyyyyy	1	0	0	1	0	0	1	0
$93yyyyyy	1	0	0	1	0	0	1	1
$94yyyyyy	1	0	0	1	0	1	0	0
$95yyyyyy	1	0	0	1	0	1	0	1
$96yyyyyy	1	0	0	1	0	1	1	0
$97yyyyyy	1	0	0	1	0	1	1	1
$98yyyyyy	1	0	0	1	1	0	0	0
$99yyyyyy	1	0	0	1	1	0	0	1
$9Ayyyyyy	1	0	0	1	1	0	1	0
$9Byyyyyy	1	0	0	1	1	0	1	1
$9Cyyyyyy	1	0	0	1	1	1	0	0
$9Dyyyyyy	1	0	0	1	1	1	0	1
$9Eyyyyyy	1	0	0	1	1	1	1	0
$9Fyyyyyy	1	0	0	1	1	1	1	1

BANK SELECTED	8	7	6	5	4	3	2	1
$A0yyyyyy	1	0	1	0	0	0	0	0
$A1yyyyyy	1	0	1	0	0	0	0	1
$A2yyyyyy	1	0	1	0	0	0	1	0
$A3yyyyyy	1	0	1	0	0	0	1	1
$A4yyyyyy	1	0	1	0	0	1	0	0
$A5yyyyyy	1	0	1	0	0	1	0	1
$A6yyyyyy	1	0	1	0	0	1	1	0
$A7yyyyyy	1	0	1	0	0	1	1	1
$A8yyyyyy	1	0	1	0	1	0	0	0
$A9yyyyyy	1	0	1	0	1	0	0	1
$AAyyyyyy	1	0	1	0	1	0	1	0
$AByyyyyy	1	0	1	0	1	0	1	1
$ACyyyyyy	1	0	1	0	1	1	0	0
$ADyyyyyy	1	0	1	0	1	1	0	1
$AEyyyyyy	1	0	1	0	1	1	1	0
$AFyyyyyy	1	0	1	0	1	1	1	1
$B0yyyyyy	1	0	1	1	0	0	0	0
$B1yyyyyy	1	0	1	1	0	0	0	1
$B2yyyyyy	1	0	1	1	0	0	1	0
$B3yyyyyy	1	0	1	1	0	0	1	1
$B4yyyyyy	1	0	1	1	0	1	0	0
$B5yyyyyy	1	0	1	1	0	1	0	1
$B6yyyyyy	1	0	1	1	0	1	1	0
$B7yyyyyy	1	0	1	1	0	1	1	1
$B8yyyyyy	1	0	1	1	1	0	0	0
$B9yyyyyy	1	0	1	1	1	0	0	1
$B9yyyyyy	1	0	1	1	1	0	0	1
$BByyyyyy	1	0	1	1	1	0	1	1
$BCyyyyyy	1	0	1	1	1	1	0	0
$BDyyyyyy	1	0	1	1	1	1	0	1
$BEyyyyyy	1	0	1	1	1	1	1	0
$BFyyyyyy	1	0	1	1	1	1	1	1

yyyyyy = Lower / Upper Limit Select Setting (See Table B.1)

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TABLE A.1.4

BANK SELECTION
(A24 - A31)
(BLK G)

0 = Open
1 = Closed

BANK SELECTED	8	7	6	5	4	3	2	1
$C0yyyyyy	1	1	0	0	0	0	0	0
$C1yyyyyy	1	1	0	0	0	0	0	1
$C2yyyyyy	1	1	0	0	0	0	1	0
$C3yyyyyy	1	1	0	0	0	0	1	1
$C4yyyyyy	1	1	0	0	0	1	0	0
$C5yyyyyy	1	1	0	0	0	1	0	1
$C6yyyyyy	1	1	0	0	0	1	1	0
$C7yyyyyy	1	1	0	0	0	1	1	1
$C8yyyyyy	1	1	0	0	1	0	0	0
$C9yyyyyy	1	1	0	0	1	0	0	1
$CAyyyyyy	1	1	0	0	1	0	1	0
$CByyyyyy	1	1	0	0	1	0	1	1
$CCyyyyyy	1	1	0	0	1	1	0	0
$CDyyyyyy	1	1	0	0	1	1	0	1
$CEyyyyyy	1	1	0	0	1	1	1	0
$CFyyyyyy	1	1	0	0	1	1	1	1
$D0yyyyyy	1	1	0	1	0	0	0	0
$D1yyyyyy	1	1	0	1	0	0	0	1
$D2yyyyyy	1	1	0	1	0	0	1	0
$D3yyyyyy	1	1	0	1	0	0	1	1
$D4yyyyyy	1	1	0	1	0	1	0	0
$D5yyyyyy	1	1	0	1	0	1	0	1
$D6yyyyyy	1	1	0	1	0	1	1	0
$D7yyyyyy	1	1	0	1	0	1	1	1
$D8yyyyyy	1	1	0	1	1	0	0	0
$D9yyyyyy	1	1	0	1	1	0	0	1
$DAyyyyyy	1	1	0	1	1	0	1	0
$DByyyyyy	1	1	0	1	1	0	1	1
$DCyyyyyy	1	1	0	1	1	1	0	0
$DDyyyyyy	1	1	0	1	1	1	0	1
$DEyyyyyy	1	1	0	1	1	1	1	0
$DFyyyyyy	1	1	0	1	1	1	1	1

BANK SELECTED	8	7	6	5	4	3	2	1
$E0yyyyyy	1	1	1	0	0	0	0	0
$E1yyyyyy	1	1	1	0	0	0	0	1
$E2yyyyyy	1	1	1	0	0	0	1	0
$E3yyyyyy	1	1	1	0	0	0	1	1
$E4yyyyyy	1	1	1	0	0	1	0	0
$E5yyyyyy	1	1	1	0	0	1	0	1
$E6yyyyyy	1	1	1	0	0	1	1	0
$E7yyyyyy	1	1	1	0	0	1	1	1
$E8yyyyyy	1	1	1	0	1	0	0	0
$E9yyyyyy	1	1	1	0	1	0	0	1
$EAyyyyyy	1	1	1	0	1	0	1	0
$EByyyyyy	1	1	1	0	1	0	1	1
$ECyyyyyy	1	1	1	0	1	1	0	0
$EDyyyyyy	1	1	1	0	1	1	0	1
$EEyyyyyy	1	1	1	0	1	1	1	0
$EFyyyyyy	1	1	1	0	1	1	1	1
$F0yyyyyy	1	1	1	1	0	0	0	0
$F1yyyyyy	1	1	1	1	0	0	0	1
$F2yyyyyy	1	1	1	1	0	0	1	0
$F3yyyyyy	1	1	1	1	0	0	1	1
$F4yyyyyy	1	1	1	1	0	1	0	0
$F5yyyyyy	1	1	1	1	0	1	0	1
$F6yyyyyy	1	1	1	1	0	1	1	0
$F7yyyyyy	1	1	1	1	0	1	1	1
$F8yyyyyy	1	1	1	1	1	0	0	0
$F9yyyyyy	1	1	1	1	1	0	0	1
$FAyyyyyy	1	1	1	1	1	0	1	0
$FByyyyyy	1	1	1	1	1	0	1	1
$FCyyyyyy	1	1	1	1	1	1	0	0
$FDyyyyyy	1	1	1	1	1	1	0	1
$FEyyyyyy	1	1	1	1	1	1	1	0
$FFyyyyyy	1	1	1	1	1	1	1	1

YYYYYY = Lower / Upper Limit Select Setting (See Table B.1)

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TABLE B.1.1

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A) (VMXbus = BLK D & BLK C)

LOWER LIMITS	BLK B / BLK D 8 7 6 5 4 3 2 1	UPPER LIMITS	BLK A / BLK C 8 7 6 5 4 3 2 1
$xx000000	0 0 0 0 0 0 0 0	$xx00FFFF	0 0 0 0 0 0 0 0
$xx010000	0 0 0 0 0 0 0 1	$xx01FFFF	0 0 0 0 0 0 0 1
$xx020000	0 0 0 0 0 0 1 0	$xx02FFFF	0 0 0 0 0 0 1 0
$xx030000	0 0 0 0 0 0 1 1	$xx03FFFF	0 0 0 0 0 0 1 1
$xx040000	0 0 0 0 0 1 0 0	$xx04FFFF	0 0 0 0 0 1 0 0
$xx050000	0 0 0 0 0 1 0 1	$xx05FFFF	0 0 0 0 0 1 0 1
$xx060000	0 0 0 0 0 1 1 0	$xx06FFFF	0 0 0 0 0 1 1 0
$xx070000	0 0 0 0 0 1 1 1	$xx07FFFF	0 0 0 0 0 1 1 1
$xx080000	0 0 0 0 1 0 0 0	$xx08FFFF	0 0 0 0 1 0 0 0
$xx090000	0 0 0 0 1 0 0 1	$xx09FFFF	0 0 0 0 1 0 0 1
$xx0A0000	0 0 0 0 1 0 1 0	$xx0AFFFF	0 0 0 0 1 0 1 0
$xx0B0000	0 0 0 0 1 0 1 1	$xx0BFFFF	0 0 0 0 1 0 1 1
$xx0C0000	0 0 0 0 1 1 0 0	$xx0CFFFF	0 0 0 0 1 1 0 0
$xx0D0000	0 0 0 0 1 1 0 1	$xx0DFFFF	0 0 0 0 1 1 0 1
$xx0E0000	0 0 0 0 1 1 1 0	$xx0EFFFF	0 0 0 0 1 1 1 0
$xx0F0000	0 0 0 0 1 1 1 1	$xx0FFFFF	0 0 0 0 1 1 1 1
$xx100000	0 0 0 1 0 0 0 0	$xx10FFFF	0 0 0 1 0 0 0 0
$xx110000	0 0 0 1 0 0 0 1	$xx11FFFF	0 0 0 1 0 0 0 1
$xx120000	0 0 0 1 0 0 1 0	$xx12FFFF	0 0 0 1 0 0 1 0
$xx130000	0 0 0 1 0 0 1 1	$xx13FFFF	0 0 0 1 0 0 1 1
$xx140000	0 0 0 1 0 1 0 0	$xx14FFFF	0 0 0 1 0 1 0 0
$xx150000	0 0 0 1 0 1 0 1	$xx15FFFF	0 0 0 1 0 1 0 1
$xx160000	0 0 0 1 0 1 1 0	$xx16FFFF	0 0 0 1 0 1 1 0
$xx170000	0 0 0 1 0 1 1 1	$xx17FFFF	0 0 0 1 0 1 1 1
$xx180000	0 0 0 1 1 0 0 0	$xx18FFFF	0 0 0 1 1 0 0 0
$xx190000	0 0 0 1 1 0 0 1	$xx19FFFF	0 0 0 1 1 0 0 1
$xx1A0000	0 0 0 1 1 0 1 0	$xx1AFFFF	0 0 0 1 1 0 1 0
$xx1B0000	0 0 0 1 1 0 1 1	$xx1BFFFF	0 0 0 1 1 0 1 1
$xx1C0000	0 0 0 1 1 1 0 0	$xx1CFFFF	0 0 0 1 1 1 0 0
$xx1D0000	0 0 0 1 1 1 0 1	$xx1DFFFF	0 0 0 1 1 1 0 1
$xx1E0000	0 0 0 1 1 1 1 0	$xx1EFFFF	0 0 0 1 1 1 1 0
$xx1F0000	0 0 0 1 1 1 1 1	$xx1FFFFF	0 0 0 1 1 1 1 1

xx = Bank Select Setting (See Table A.1)

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TABLE B.1.2

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A)

LOWER LIMITS	BLK B / BLK D 8	7	6	5	4	3	2	1
$xx200000	0	0	1	0	0	0	0	0
$xx210000	0	0	1	0	0	0	0	1
$xx220000	0	0	1	0	0	0	1	0
$xx230000	0	0	1	0	0	0	1	1
$xx240000	0	0	1	0	0	1	0	0
$xx250000	0	0	1	0	0	1	0	1
$xx260000	0	0	1	0	0	1	1	0
$xx270000	0	0	1	0	0	1	1	1
$xx280000	0	0	1	0	1	0	0	0
$xx290000	0	0	1	0	1	0	0	1
$xx2A0000	0	0	1	0	1	0	1	0
$xx2B0000	0	0	1	0	1	0	1	1
$xx2C0000	0	0	1	0	1	1	0	0
$xx2D0000	0	0	1	0	1	1	0	1
$xx2E0000	0	0	1	0	1	1	1	0
$xx2F0000	0	0	1	0	1	1	1	1
$xx300000	0	0	1	1	0	0	0	0
$xx310000	0	0	1	1	0	0	0	1
$xx320000	0	0	1	1	0	0	1	0
$xx330000	0	0	1	1	0	0	1	1
$xx340000	0	0	1	1	0	1	0	0
$xx350000	0	0	1	1	0	1	0	1
$xx360000	0	0	1	1	0	1	1	0
$xx370000	0	0	1	1	0	1	1	1
$xx380000	0	0	1	1	1	0	0	0
$xx390000	0	0	1	1	1	0	0	1
$xx3A0000	0	0	1	1	1	0	1	0
$xx3B0000	0	0	1	1	1	0	1	1
$xx3C0000	0	0	1	1	1	1	0	0
$xx3D0000	0	0	1	1	1	1	0	1
$xx3E0000	0	0	1	1	1	1	1	0
$xx3F0000	0	0	1	1	1	1	1	1

(VMXbus = BLK D & BLK C)

UPPER LIMITS	BLK A / BLK C 8	7	6	5	4	3	2	1
$xx20FFFF	0	0	1	0	0	0	0	0
$xx21FFFF	0	0	1	0	0	0	0	1
$xx22FFFF	0	0	1	0	0	0	1	0
$xx23FFFF	0	0	1	0	0	0	1	1
$xx24FFFF	0	0	1	0	0	1	0	0
$xx25FFFF	0	0	1	0	0	1	0	1
$xx26FFFF	0	0	1	0	0	1	1	0
$xx27FFFF	0	0	1	0	0	1	1	1
$xx28FFFF	0	0	1	0	1	0	0	0
$xx29FFFF	0	0	1	0	1	0	0	1
$xx2AFFFF	0	0	1	0	1	0	1	0
$xx2BFFFF	0	0	1	0	1	0	1	1
$xx2CFFFF	0	0	1	0	1	1	0	0
$xx2DFFFF	0	0	1	0	1	1	0	1
$xx2EFFFF	0	0	1	0	1	1	1	0
$xx2FFFFF	0	0	1	0	1	1	1	1
$xx30FFFF	0	0	1	1	0	0	0	0
$xx31FFFF	0	0	1	1	0	0	0	1
$xx32FFFF	0	0	1	1	0	0	1	0
$xx33FFFF	0	0	1	1	0	0	1	1
$xx34FFFF	0	0	1	1	0	1	0	0
$xx35FFFF	0	0	1	1	0	1	0	1
$xx36FFFF	0	0	1	1	0	1	1	0
$xx37FFFF	0	0	1	1	0	1	1	1
$xx38FFFF	0	0	1	1	1	0	0	0
$xx39FFFF	0	0	1	1	1	0	0	1
$xx3AFFFF	0	0	1	1	1	0	1	0
$xx3BFFFF	0	0	1	1	1	0	1	1
$xx34FFFF	0	0	1	1	1	1	0	0
$xx3DFFFF	0	0	1	1	1	1	0	1
$xx3EFFFF	0	0	1	1	1	1	1	0
$xx3FFFFF	0	0	1	1	1	1	1	1

xx = Bank Select Setting (See Table A.1)

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TABLE B.1.3

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A) (VMXbus = BLK D & BLK C)

LOWER LIMITS	BLK B / BLK D 8 7 6 5 4 3 2 1
$xx400000	0 1 0 0 0 0 0 0
$xx410000	0 1 0 0 0 0 0 1
$xx420000	0 1 0 0 0 0 1 0
$xx430000	0 1 0 0 0 0 1 1
$xx440000	0 1 0 0 0 1 0 0
$xx450000	0 1 0 0 0 1 0 1
$xx460000	0 1 0 0 0 1 1 0
$xx470000	0 1 0 0 0 1 1 1
$xx480000	0 1 0 0 1 0 0 0
$xx490000	0 1 0 0 1 0 0 1
$xx4A0000	0 1 0 0 1 0 1 0
$xx4B0000	0 1 0 0 1 0 1 1
$xx4C0000	0 1 0 0 1 1 0 0
$xx4D0000	0 1 0 0 1 1 0 1
$xx4E0000	0 1 0 0 1 1 1 0
$xx4F0000	0 1 0 0 1 1 1 1
$xx500000	0 1 0 1 0 0 0 0
$xx510000	0 1 0 1 0 0 0 1
$xx520000	0 1 0 1 0 0 1 0
$xx530000	0 1 0 1 0 0 1 1
$xx540000	0 1 0 1 0 1 0 0
$xx550000	0 1 0 1 0 1 0 1
$xx560000	0 1 0 1 0 1 1 0
$xx570000	0 1 0 1 0 1 1 1
$xx580000	0 1 0 1 1 0 0 0
$xx590000	0 1 0 1 1 0 0 1
$xx5A0000	0 1 0 1 1 0 1 0
$xx5B0000	0 1 0 1 1 0 1 1
$xx5C0000	0 1 0 1 1 1 0 0
$xx5D0000	0 1 0 1 1 1 0 1
$xx5E0000	0 1 0 1 1 1 1 0
$xx5F0000	0 1 0 1 1 1 1 1

UPPER LIMITS	BLK A / BLK C 8 7 6 5 4 3 2 1
$xx40FFFF	0 1 0 0 0 0 0 0
$xx41FFFF	0 1 0 0 0 0 0 1
$xx42FFFF	0 1 0 0 0 0 1 0
$xx43FFFF	0 1 0 0 0 0 1 1
$xx44FFFF	0 1 0 0 0 1 0 0
$xx45FFFF	0 1 0 0 0 1 0 1
$xx46FFFF	0 1 0 0 0 1 1 0
$xx47FFFF	0 1 0 0 0 1 1 1
$xx48FFFF	0 1 0 0 1 0 0 0
$xx49FFFF	0 1 0 0 1 0 0 1
$xx4AFFFF	0 1 0 0 1 0 1 0
$xx4BFFFF	0 1 0 0 1 0 1 1
$xx4CFFFF	0 1 0 0 1 1 0 0
$xx4DFFFF	0 1 0 0 1 1 0 1
$xx4EFFFF	0 1 0 0 1 1 1 0
$xx4FFFFF	0 1 0 0 1 1 1 1
$xx50FFFF	0 1 0 1 0 0 0 0
$xx51FFFF	0 1 0 1 0 0 0 1
$xx52FFFF	0 1 0 1 0 0 1 0
$xx53FFFF	0 1 0 1 0 0 1 1
$xx54FFFF	0 1 0 1 0 1 0 0
$xx55FFFF	0 1 0 1 0 1 0 1
$xx56FFFF	0 1 0 1 0 1 1 0
$xx57FFFF	0 1 0 1 0 1 1 1
$xx58FFFF	0 1 0 1 1 0 0 0
$xx59FFFF	0 1 0 1 1 0 0 1
$xx5AFFFF	0 1 0 1 1 0 1 0
$xx5BFFFF	0 1 0 1 1 0 1 1
$xx5CFFFF	0 1 0 1 1 1 0 0
$xx5DFFFF	0 1 0 1 1 1 0 1
$xx5EFFFF	0 1 0 1 1 1 1 0
$xx5FFFFF	0 1 0 1 1 1 1 1

xx = Bank Select Setting (See Table A.1)

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TABLE B.1.4

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A) LOWER LIMITS	BLK B / BLK D 8 7 6 5 4 3 2 1	(VMXbus = BLK D & BLK C) UPPER LIMITS	BLK A / BLK C 8 7 6 5 4 3 2 1
$xx600000	0 1 1 0 0 0 0 0	$xx60FFFF	0 1 1 0 0 0 0 0
$xx610000	0 1 1 0 0 0 0 1	$xx61FFFF	0 1 1 0 0 0 0 1
$xx620000	0 1 1 0 0 0 1 0	$xx62FFFF	0 1 1 0 0 0 1 0
$xx630000	0 1 1 0 0 0 1 1	$xx63FFFF	0 1 1 0 0 0 1 1
$xx640000	0 1 1 0 0 1 0 0	$xx64FFFF	0 1 1 0 0 1 0 0
$xx650000	0 1 1 0 0 1 0 1	$xx65FFFF	0 1 1 0 0 1 0 1
$xx660000	0 1 1 0 0 1 1 0	$xx66FFFF	0 1 1 0 0 1 1 0
$xx670000	0 1 1 0 0 1 1 1	$xx67FFFF	0 1 1 0 0 1 1 1
$xx680000	0 1 1 0 1 0 0 0	$xx68FFFF	0 1 1 0 1 0 0 0
$xx690000	0 1 1 0 1 0 0 1	$xx69FFFF	0 1 1 0 1 0 0 1
$xx6A0000	0 1 1 0 1 0 1 0	$xx6AFFFF	0 1 1 0 1 0 1 0
$xx6B0000	0 1 1 0 1 0 1 1	$xx6BFFFF	0 1 1 0 1 0 1 1
$xx6C0000	0 1 1 0 1 1 0 0	$xx6CFFFF	0 1 1 0 1 1 0 0
$xx6D0000	0 1 1 0 1 1 0 1	$xx6DFFFF	0 1 1 0 1 1 0 1
$xx6E0000	0 1 1 0 1 1 1 0	$xx6EFFFF	0 1 1 0 1 1 1 0
$xx6F0000	0 1 1 0 1 1 1 1	$xx6FFFFF	0 1 1 0 1 1 1 1
$xx700000	0 1 1 1 0 0 0 0	$xx70FFFF	0 1 1 1 0 0 0 0
$xx710000	0 1 1 1 0 0 0 1	$xx71FFFF	0 1 1 1 0 0 0 1
$xx720000	0 1 1 1 0 0 1 0	$xx72FFFF	0 1 1 1 0 0 1 0
$xx730000	0 1 1 1 0 0 1 1	$xx73FFFF	0 1 1 1 0 0 1 1
$xx740000	0 1 1 1 0 1 0 0	$xx74FFFF	0 1 1 1 0 1 0 0
$xx750000	0 1 1 1 0 1 0 1	$xx75FFFF	0 1 1 1 0 1 0 1
$xx760000	0 1 1 1 0 1 1 0	$xx76FFFF	0 1 1 1 0 1 1 0
$xx770000	0 1 1 1 0 1 1 1	$xx77FFFF	0 1 1 1 0 1 1 1
$xx780000	0 1 1 1 1 0 0 0	$xx78FFFF	0 1 1 1 1 0 0 0
$xx790000	0 1 1 1 1 0 0 1	$xx79FFFF	0 1 1 1 1 0 0 1
$xx7A0000	0 1 1 1 1 0 1 0	$xx7AFFFF	0 1 1 1 1 0 1 0
$xx7B0000	0 1 1 1 1 0 1 1	$xx7BFFFF	0 1 1 1 1 0 1 1
$xx7C0000	0 1 1 1 1 1 0 0	$xx7CFFFF	0 1 1 1 1 1 0 0
$xx7D0000	0 1 1 1 1 1 0 1	$xx7DFFFF	0 1 1 1 1 1 0 1
$xx7E0000	0 1 1 1 1 1 1 0	$xx7EFFFF	0 1 1 1 1 1 1 0
$xx7F0000	0 1 1 1 1 1 1 1	$xx7FFFFF	0 1 1 1 1 1 1 1

xx = Bank Select Setting (See Table A.1)

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TABLE B.1.5

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A) LOWER LIMITS	BLK B / BLK D 8 7 6 5 4 3 2 1	(VMXbus = BLK D & BLK C) UPPER LIMITS	BLK A / BLK C 8 7 6 5 4 3 2 1
$xx800000	1 0 0 0 0 0 0 0	$xx80FFFF	1 0 0 0 0 0 0 0
$xx810000	1 0 0 0 0 0 0 1	$xx81FFFF	1 0 0 0 0 0 0 1
$xx820000	1 0 0 0 0 0 1 0	$xx82FFFF	1 0 0 0 0 0 1 0
$xx830000	1 0 0 0 0 0 1 1	$xx83FFFF	1 0 0 0 0 0 1 1
$xx840000	1 0 0 0 0 1 0 0	$xx84FFFF	1 0 0 0 0 1 0 0
$xx850000	1 0 0 0 0 1 0 1	$xx85FFFF	1 0 0 0 0 1 0 1
$xx860000	1 0 0 0 0 1 1 0	$xx86FFFF	1 0 0 0 0 1 1 0
$xx870000	1 0 0 0 0 1 1 1	$xx87FFFF	1 0 0 0 0 1 1 1
$xx880000	1 0 0 0 1 0 0 0	$xx88FFFF	1 0 0 0 1 0 0 0
$xx890000	1 0 0 0 1 0 0 1	$xx89FFFF	1 0 0 0 1 0 0 1
$xx8A0000	1 0 0 0 1 0 1 0	$xx8AFFFF	1 0 0 0 1 0 1 0
$xx8B0000	1 0 0 0 1 0 1 1	$xx8BFFFF	1 0 0 0 1 0 1 1
$xx8C0000	1 0 0 0 1 1 0 0	$xx8CFFFF	1 0 0 0 1 1 0 0
$xx8D0000	1 0 0 0 1 1 0 1	$xx8DFFFF	1 0 0 0 1 1 0 1
$xx8E0000	1 0 0 0 1 1 1 0	$xx8EFFFF	1 0 0 0 1 1 1 0
$xx8F0000	1 0 0 0 1 1 1 1	$xx8FFFFF	1 0 0 0 1 1 1 1
$xx900000	1 0 0 1 0 0 0 0	$xx90FFFF	1 0 0 1 0 0 0 0
$xx910000	1 0 0 1 0 0 0 1	$xx91FFFF	1 0 0 1 0 0 0 1
$xx920000	1 0 0 1 0 0 1 0	$xx92FFFF	1 0 0 1 0 0 1 0
$xx930000	1 0 0 1 0 0 1 1	$xx93FFFF	1 0 0 1 0 0 1 1
$xx940000	1 0 0 1 0 1 0 0	$xx94FFFF	1 0 0 1 0 1 0 0
$xx950000	1 0 0 1 0 1 0 1	$xx95FFFF	1 0 0 1 0 1 0 1
$xx960000	1 0 0 1 0 1 1 0	$xx96FFFF	1 0 0 1 0 1 1 0
$xx970000	1 0 0 1 0 1 1 1	$xx97FFFF	1 0 0 1 0 1 1 1
$xx980000	1 0 0 1 1 0 0 0	$xx98FFFF	1 0 0 1 1 0 0 0
$xx990000	1 0 0 1 1 0 0 1	$xx99FFFF	1 0 0 1 1 0 0 1
$xx9A0000	1 0 0 1 1 0 1 0	$xx9AFFFF	1 0 0 1 1 0 1 0
$xx9B0000	1 0 0 1 1 0 1 1	$xx9BFFFF	1 0 0 1 1 0 1 1
$xx9C0000	1 0 0 1 1 1 0 0	$xx9CFFFF	1 0 0 1 1 1 0 0
$xx9D0000	1 0 0 1 1 1 0 1	$xx9DFFFF	1 0 0 1 1 1 0 1
$xx9E0000	1 0 0 1 1 1 1 0	$xx9EFFFF	1 0 0 1 1 1 1 0
$xx9F0000	1 0 0 1 1 1 1 1	$xx9FFFFF	1 0 0 1 1 1 1 1

xx = Bank Select Setting (See Table A.1)

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TABLE B.1.6

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A) LOWER LIMITS	BLK B / BLK D 8 7 6 5 4 3 2 1	(VMXbus = BLK D & BLK C) UPPER LIMITS	BLK A / BLK C 8 7 6 5 4 3 2 1
$xxA00000	1 0 1 0 0 0 0 0	$xxA0FFFF	1 0 1 0 0 0 0 0
$xxA10000	1 0 1 0 0 0 0 1	$xxA1FFFF	1 0 1 0 0 0 0 1
$xxA20000	1 0 1 0 0 0 1 0	$xxA2FFFF	1 0 1 0 0 0 1 0
$xxA30000	1 0 1 0 0 0 1 1	$xxA3FFFF	1 0 1 0 0 0 1 1
$xxA40000	1 0 1 0 0 1 0 0	$xxA4FFFF	1 0 1 0 0 1 0 0
$xxA50000	1 0 1 0 0 1 0 1	$xxA5FFFF	1 0 1 0 0 1 0 1
$xxA60000	1 0 1 0 0 1 1 0	$xxA6FFFF	1 0 1 0 0 1 1 0
$xxA70000	1 0 1 0 0 1 1 1	$xxA7FFFF	1 0 1 0 0 1 1 1
$xxA80000	1 0 1 0 1 0 0 0	$xxA8FFFF	1 0 1 0 1 0 0 0
$xxA90000	1 0 1 0 1 0 0 1	$xxA9FFFF	1 0 1 0 1 0 0 1
$xxAA0000	1 0 1 0 1 0 1 0	$xxAAFFFF	1 0 1 0 1 0 1 0
$xxAB0000	1 0 1 0 1 0 1 1	$xxABFFFF	1 0 1 0 1 0 1 1
$xxAC0000	1 0 1 0 1 1 0 0	$xxACFFFF	1 0 1 0 1 1 0 0
$xxAD0000	1 0 1 0 1 1 0 1	$xxADFFFF	1 0 1 0 1 1 0 1
$xxAE0000	1 0 1 0 1 1 1 0	$xxAEFFFF	1 0 1 0 1 1 1 0
$xxAF0000	1 0 1 0 1 1 1 1	$xxAFFFFF	1 0 1 0 1 1 1 1
$xxB00000	1 0 1 1 0 0 0 0	$xxB0FFFF	1 0 1 1 0 0 0 0
$xxB10000	1 0 1 1 0 0 0 1	$xxB1FFFF	1 0 1 1 0 0 0 1
$xxB20000	1 0 1 1 0 0 1 0	$xxB2FFFF	1 0 1 1 0 0 1 0
$xxB30000	1 0 1 1 0 0 1 1	$xxB3FFFF	1 0 1 1 0 0 1 1
$xxB40000	1 0 1 1 0 1 0 0	$xxB4FFFF	1 0 1 1 0 1 0 0
$xxB50000	1 0 1 1 0 1 0 1	$xxB5FFFF	1 0 1 1 0 1 0 1
$xxB60000	1 0 1 1 0 1 1 0	$xxB6FFFF	1 0 1 1 0 1 1 0
$xxB70000	1 0 1 1 0 1 1 1	$xxB7FFFF	1 0 1 1 0 1 1 1
$xxB80000	1 0 1 1 1 0 0 0	$xxB8FFFF	1 0 1 1 1 0 0 0
$xxB90000	1 0 1 1 1 0 0 1	$xxB9FFFF	1 0 1 1 1 0 0 1
$xxBA0000	1 0 1 1 1 0 1 0	$xxBAFFFF	1 0 1 1 1 0 1 0
$xxBB0000	1 0 1 1 1 0 1 1	$xxBBFFFF	1 0 1 1 1 0 1 1
$xxBC0000	1 0 1 1 1 1 0 0	$xxBCFFFF	1 0 1 1 1 1 0 0
$xxBD0000	1 0 1 1 1 1 0 1	$xxBDFFFF	1 0 1 1 1 1 0 1
$xxBE0000	1 0 1 1 1 1 1 0	$xxBEFFFF	1 0 1 1 1 1 1 0
$xxBF0000	1 0 1 1 1 1 1 1	$xxBFFFFF	1 0 1 1 1 1 1 1

xx = Bank Select Setting (See Table A.1)

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TABLE B.1.7

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A) (VMXbus = BLK D & BLK C)

LOWER LIMITS	BLK B / BLK D 8 7 6 5 4 3 2 1	UPPER LIMITS	BLK A / BLK C 8 7 6 5 4 3 2 1
$xxC00000	1 1 0 0 0 0 0 0	$xxC0FFFF	1 1 0 0 0 0 0 0
$xxC10000	1 1 0 0 0 0 0 1	$xxC1FFFF	1 1 0 0 0 0 0 1
$xxC20000	1 1 0 0 0 0 1 0	$xxC2FFFF	1 1 0 0 0 0 1 0
$xxC30000	1 1 0 0 0 0 1 1	$xxC3FFFF	1 1 0 0 0 0 1 1
$xxC40000	1 1 0 0 0 1 0 0	$xxC4FFFF	1 1 0 0 0 1 0 0
$xxC50000	1 1 0 0 0 1 0 1	$xxC5FFFF	1 1 0 0 0 1 0 1
$xxC60000	1 1 0 0 0 1 1 0	$xxC6FFFF	1 1 0 0 0 1 1 0
$xxC70000	1 1 0 0 0 1 1 1	$xxC7FFFF	1 1 0 0 0 1 1 1
$xxC80000	1 1 0 0 1 0 0 0	$xxC8FFFF	1 1 0 0 1 0 0 0
$xxC90000	1 1 0 0 1 0 0 1	$xxC9FFFF	1 1 0 0 1 0 0 1
$xxCA0000	1 1 0 0 1 0 1 0	$xxCAFFFF	1 1 0 0 1 0 1 0
$xxCB0000	1 1 0 0 1 0 1 1	$xxCBFFFF	1 1 0 0 1 0 1 1
$xxCC0000	1 1 0 0 1 1 0 0	$xxCCFFFF	1 1 0 0 1 1 0 0
$xxCD0000	1 1 0 0 1 1 0 1	$xxCDFFFF	1 1 0 0 1 1 0 1
$xxCE0000	1 1 0 0 1 1 1 0	$xxCEFFFF	1 1 0 0 1 1 1 0
$xxCF0000	1 1 0 0 1 1 1 1	$xxCFFFFF	1 1 0 0 1 1 1 1
$xxD00000	1 1 0 1 0 0 0 0	$xxD0FFFF	1 1 0 1 0 0 0 0
$xxD10000	1 1 0 1 0 0 0 1	$xxD1FFFF	1 1 0 1 0 0 0 1
$xxD20000	1 1 0 1 0 0 1 0	$xxD2FFFF	1 1 0 1 0 0 1 0
$xxD30000	1 1 0 1 0 0 1 1	$xxD3FFFF	1 1 0 1 0 0 1 1
$xxD40000	1 1 0 1 0 1 0 0	$xxD4FFFF	1 1 0 1 0 1 0 0
$xxD50000	1 1 0 1 0 1 0 1	$xxD5FFFF	1 1 0 1 0 1 0 1
$xxD60000	1 1 0 1 0 1 1 0	$xxD6FFFF	1 1 0 1 0 1 1 0
$xxD70000	1 1 0 1 0 1 1 1	$xxD7FFFF	1 1 0 1 0 1 1 1
$xxD80000	1 1 0 1 1 0 0 0	$xxD8FFFF	1 1 0 1 1 0 0 0
$xxD90000	1 1 0 1 1 0 0 1	$xxD9FFFF	1 1 0 1 1 0 0 1
$xxDA0000	1 1 0 1 1 0 1 0	$xxDAFFFF	1 1 0 1 1 0 1 0
$xxDB0000	1 1 0 1 1 0 1 1	$xxDBFFFF	1 1 0 1 1 0 1 1
$xxDC0000	1 1 0 1 1 1 0 0	$xxDCFFFF	1 1 0 1 1 1 0 0
$xxDD0000	1 1 0 1 1 1 0 1	$xxDDFFFF	1 1 0 1 1 1 0 1
$xxDE0000	1 1 0 1 1 1 1 0	$xxDEFFFF	1 1 0 1 1 1 1 0
$xxDF0000	1 1 0 1 1 1 1 1	$xxDFFFFF	1 1 0 1 1 1 1 1

xx = Bank Select Setting (See Table A.1)

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TABLE B.1.8

MODULE SELECTION
(A16 - A23)

0 = Open
1 = Closed

(VMEbus = BLK B & BLK A) LOWER LIMITS	BLK B / BLK D 8 7 6 5 4 3 2 1	(VMXbus = BLK D & BLK C) UPPER LIMITS	BLK A / BLK C 8 7 6 5 4 3 2 1
$xxE00000	1 1 1 0 0 0 0 0	$xxE0FFFF	1 1 1 0 0 0 0 0
$xxE10000	1 1 1 0 0 0 0 1	$xxE1FFFF	1 1 1 0 0 0 0 1
$xxE20000	1 1 1 0 0 0 1 0	$xxE2FFFF	1 1 1 0 0 0 1 0
$xxE30000	1 1 1 0 0 0 1 1	$xxE3FFFF	1 1 1 0 0 0 1 1
$xxE40000	1 1 1 0 0 1 0 0	$xxE4FFFF	1 1 1 0 0 1 0 0
$xxE50000	1 1 1 0 0 1 0 1	$xxE5FFFF	1 1 1 0 0 1 0 1
$xxE60000	1 1 1 0 0 1 1 0	$xxE6FFFF	1 1 1 0 0 1 1 0
$xxE70000	1 1 1 0 0 1 1 1	$xxE7FFFF	1 1 1 0 0 1 1 1
$xxE80000	1 1 1 0 1 0 0 0	$xxE8FFFF	1 1 1 0 1 0 0 0
$xxE90000	1 1 1 0 1 0 0 1	$xxE9FFFF	1 1 1 0 1 0 0 1
$xxEA0000	1 1 1 0 1 0 1 0	$xxEAFFFF	1 1 1 0 1 0 1 0
$xxEB0000	1 1 1 0 1 0 1 1	$xxEBFFFF	1 1 1 0 1 0 1 1
$xxEC0000	1 1 1 0 1 1 0 0	$xxECFFFF	1 1 1 0 1 1 0 0
$xxED0000	1 1 1 0 1 1 0 1	$xxEDFFFF	1 1 1 0 1 1 0 1
$xxEE0000	1 1 1 0 1 1 1 0	$xxEEFFFF	1 1 1 0 1 1 1 0
$xxEF0000	1 1 1 0 1 1 1 1	$xxEFFFFF	1 1 1 0 1 1 1 1
$xxF00000	1 1 1 1 0 0 0 0	$xxF0FFFF	1 1 1 1 0 0 0 0
$xxF10000	1 1 1 1 0 0 0 1	$xxF1FFFF	1 1 1 1 0 0 0 1
$xxF20000	1 1 1 1 0 0 1 0	$xxF2FFFF	1 1 1 1 0 0 1 0
$xxF30000	1 1 1 1 0 0 1 1	$xxF3FFFF	1 1 1 1 0 0 1 1
$xxF40000	1 1 1 1 0 1 0 0	$xxF4FFFF	1 1 1 1 0 1 0 0
$xxF50000	1 1 1 1 0 1 0 1	$xxF5FFFF	1 1 1 1 0 1 0 1
$xxF60000	1 1 1 1 0 1 1 0	$xxF6FFFF	1 1 1 1 0 1 1 0
$xxF70000	1 1 1 1 0 1 1 1	$xxF7FFFF	1 1 1 1 0 1 1 1
$xxF80000	1 1 1 1 1 0 0 0	$xxF8FFFF	1 1 1 1 1 0 0 0
$xxF90000	1 1 1 1 1 0 0 1	$xxF9FFFF	1 1 1 1 1 0 0 1
$xxFA0000	1 1 1 1 1 0 1 0	$xxFAFFFF	1 1 1 1 1 0 1 0
$xxFB0000	1 1 1 1 1 0 1 1	$xxFBFFFF	1 1 1 1 1 0 1 1
$xxFC0000	1 1 1 1 1 1 0 0	$xxFCFFFF	1 1 1 1 1 1 0 0
$xxFD0000	1 1 1 1 1 1 0 1	$xxFDFFFF	1 1 1 1 1 1 0 1
$xxFE0000	1 1 1 1 1 1 1 0	$xxFEFFFF	1 1 1 1 1 1 1 0
$xxFF0000	1 1 1 1 1 1 1 1	$xxFFFFFF	1 1 1 1 1 1 1 1

xx = Bank Select Setting (See Table A.1)

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Address Modifier Evaluation PAL

```
@DEVICE TYPE
82S153
@DRAWING
x of y
@REVISION
A3
@DATE
July 11,1986
@SYMBOL
PN455XX
@COMPANY
Micro Memory inc.
Chatsworth, Ca.
@NAME
ADDRMOD
@DESCRIPTION
MM6400 Address Modifier and CSR controller
@COMMON PRODUCT TERM

AM09 = /AM5 * /AM4 *  AM3 * /AM2 * /AM1 *  AM0 ;
AM0A = /AM5 * /AM4 *  AM3 * /AM2 *  AM1 * /AM0 ;
AM0D = /AM5 * /AM4 *  AM3 *  AM2 * /AM1 *  AM0 ;
AM0E = /AM5 * /AM4 *  AM3 *  AM2 *  AM1 * /AM0 ;
AM29 =  AM5 * /AM4 *  AM3 * /AM2 * /AM1 *  AM0 ;
AM2D =  AM5 * /AM4 *  AM3 *  AM2 * /AM1 *  AM0 ;
AM39 =  AM5 *  AM4 *  AM3 * /AM2 * /AM1 *  AM0 ;
AM3A =  AM5 *  AM4 *  AM3 * /AM2 *  AM1 * /AM0 ;
AM3D =  AM5 *  AM4 *  AM3 *  AM2 * /AM1 *  AM0 ;
AM3E =  AM5 *  AM4 *  AM3 *  AM2 *  AM1 * /AM0 ;

@I/O DIRECTION
@OUTPUT POLARITY

X7,X8 = 1 ;
X9 = 0 ;
```


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```
@LOGIC EQUATION

AMSEL = /EBANK- * RST- * IACK- * AM09
      + /EBANK- * RST- * IACK- * AM0A
      + /EBANK- * RST- * IACK- * AM0D
      + /EBANK- * RST- * IACK- * AM0E
      +           RST- * IACK- * AM39
      +           RST- * IACK- * AM3A
      +           RST- * IACK- * AM3D
      +           RST- * IACK- * AM3E
      + AMSEL * /BEAS-
      ;

CSRRE- = /( RST- * IACK- * AM29 *
           /MSB- * /LSB- * /BEAS- * /EDS0- *  EWRITE-
       +    RST- * IACK- * AM2D *
           /MSB- * /LSB- * /BEAS- * /EDS0- *  EWRITE-
          ) ;

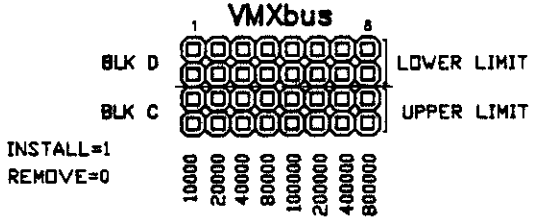
CSRWE- = /( RST- * IACK- * AM29 *
           /MSB- * /LSB- * /BEAS- * /EDS0- * /EWRITE-
       +    RST- * IACK- * AM2D *
           /MSB- * /LSB- * /BEAS- * /EDS0- * /EWRITE-
          ) ;
```


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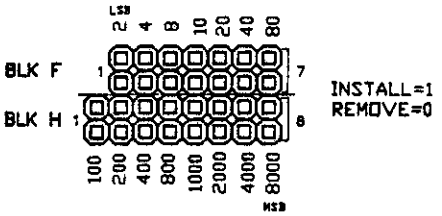
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ZONE	LTR	DESCRIPTION	DATE	APPROVED

VMXbus

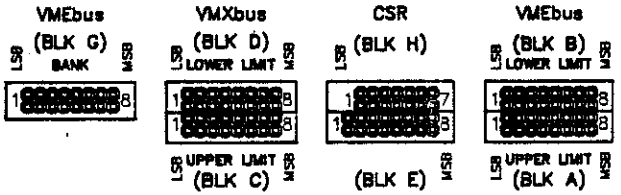


CSR



MEMORY ARRAY

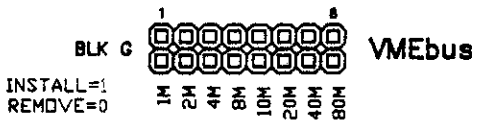
(4 MBYTES)



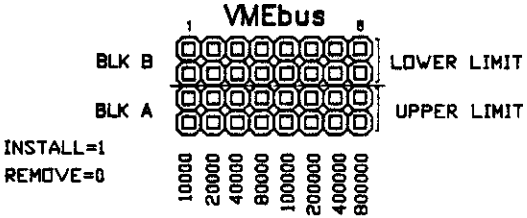
P2

P1

Bank Selection



VMEbus



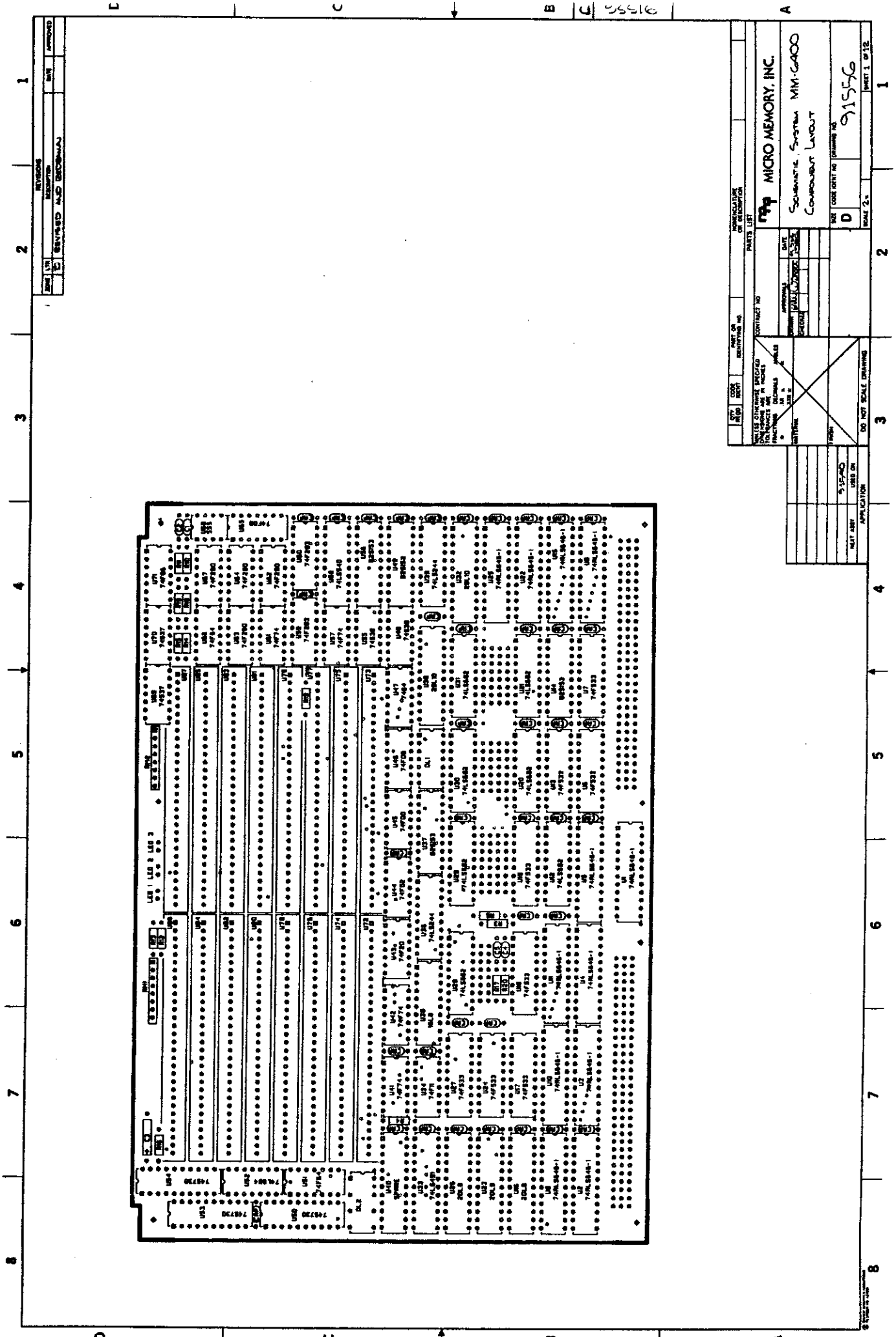
Micro Memory Inc.

MM6400D

VME/VMXbus

TITLE: APPENDIX G
Block & Jumper
Locations

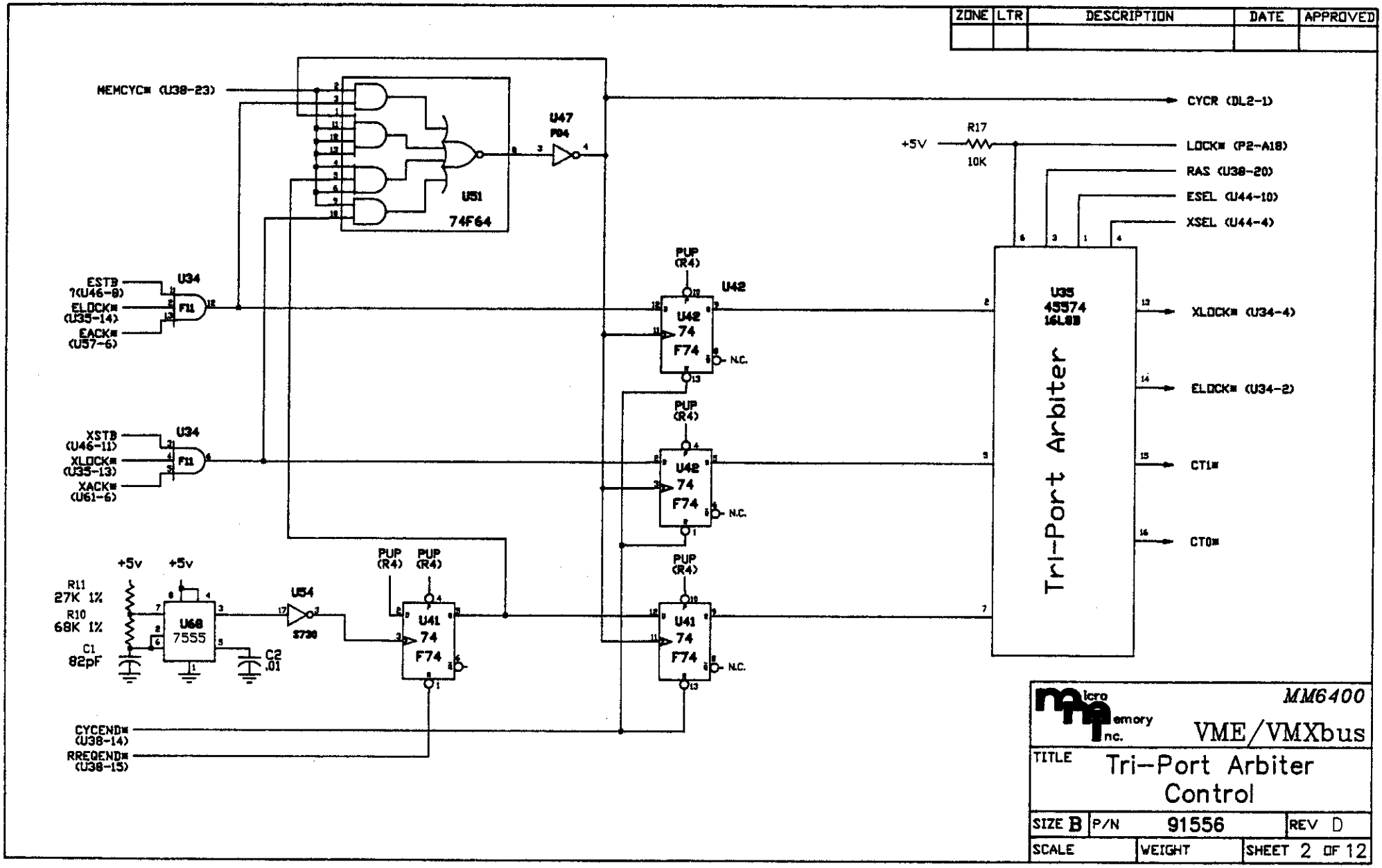
SIZE B	P/N 91556	REV B
SCALE	WEIGHT	SHEET 1 OF 1



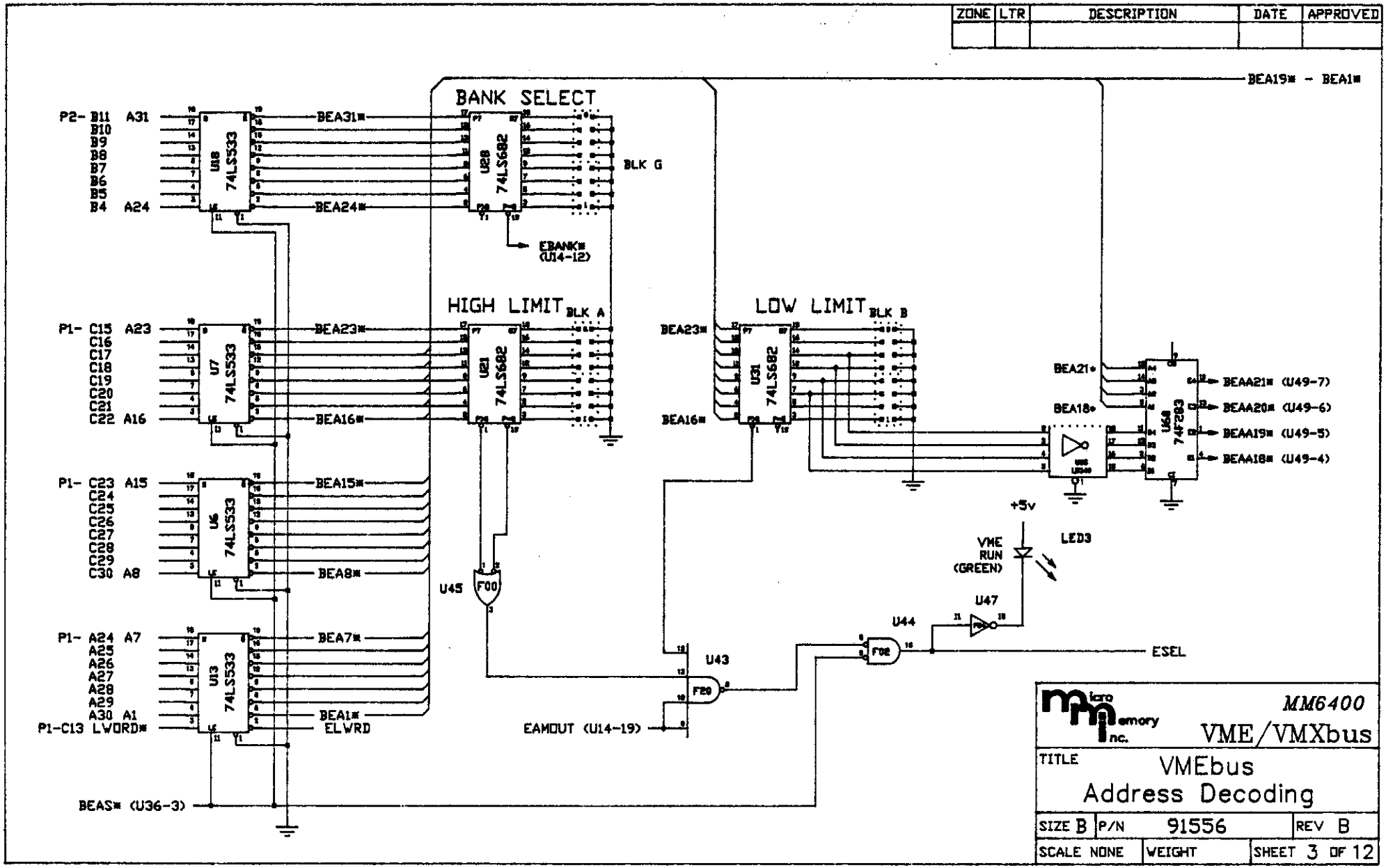
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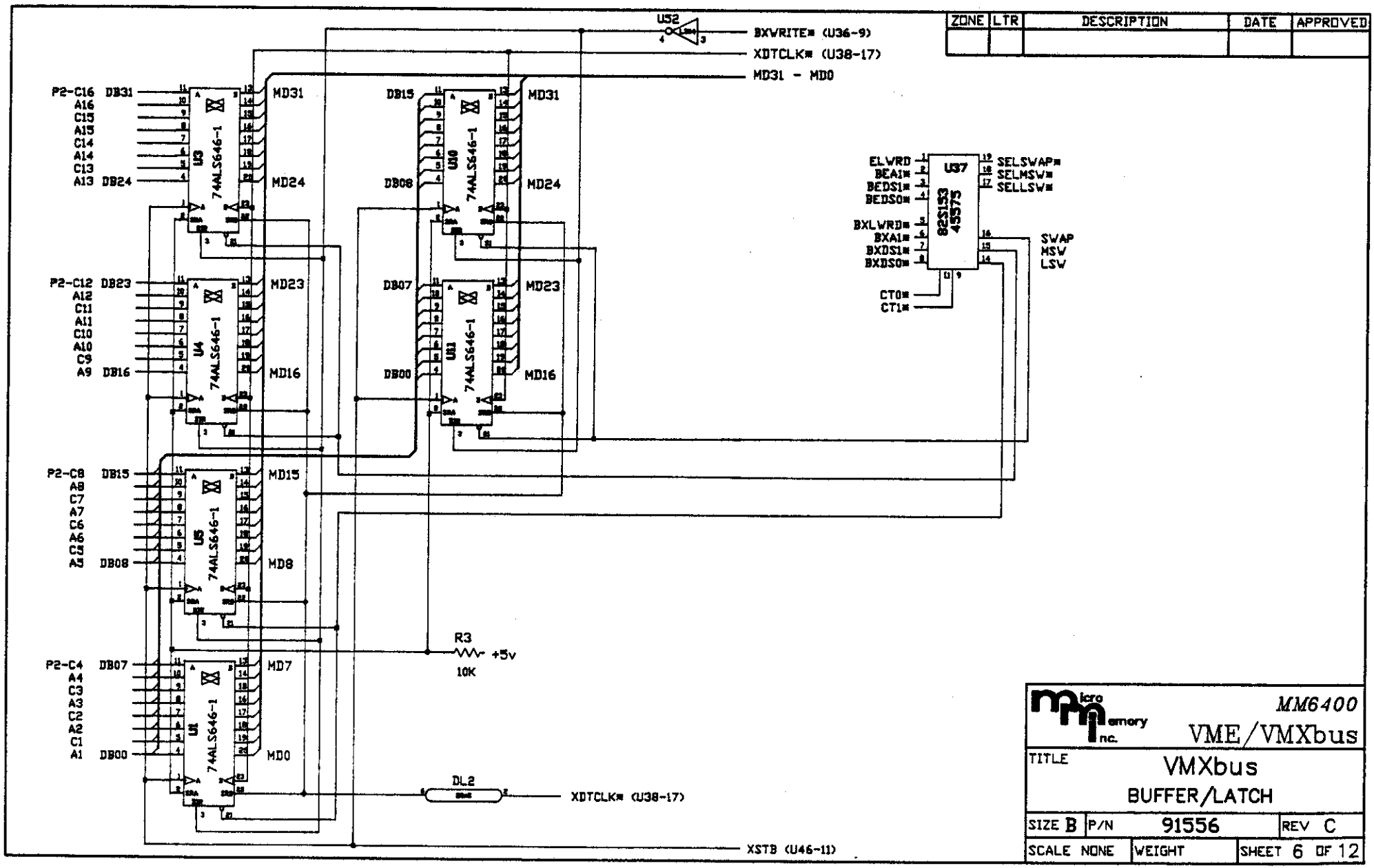
ZONE	LTR	DESCRIPTION	DATE	APPROVED



micro memory inc.			MM6400
			VME/VMXbus
TITLE	Tri-Port Arbiter Control		
SIZE B	P/N 91556		REV D
SCALE	WEIGHT		SHEET 2 OF 12



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ZONE	LTR	DESCRIPTION	DATE	APPROVED

micro memory inc.

MM6400

VME/VMXbus

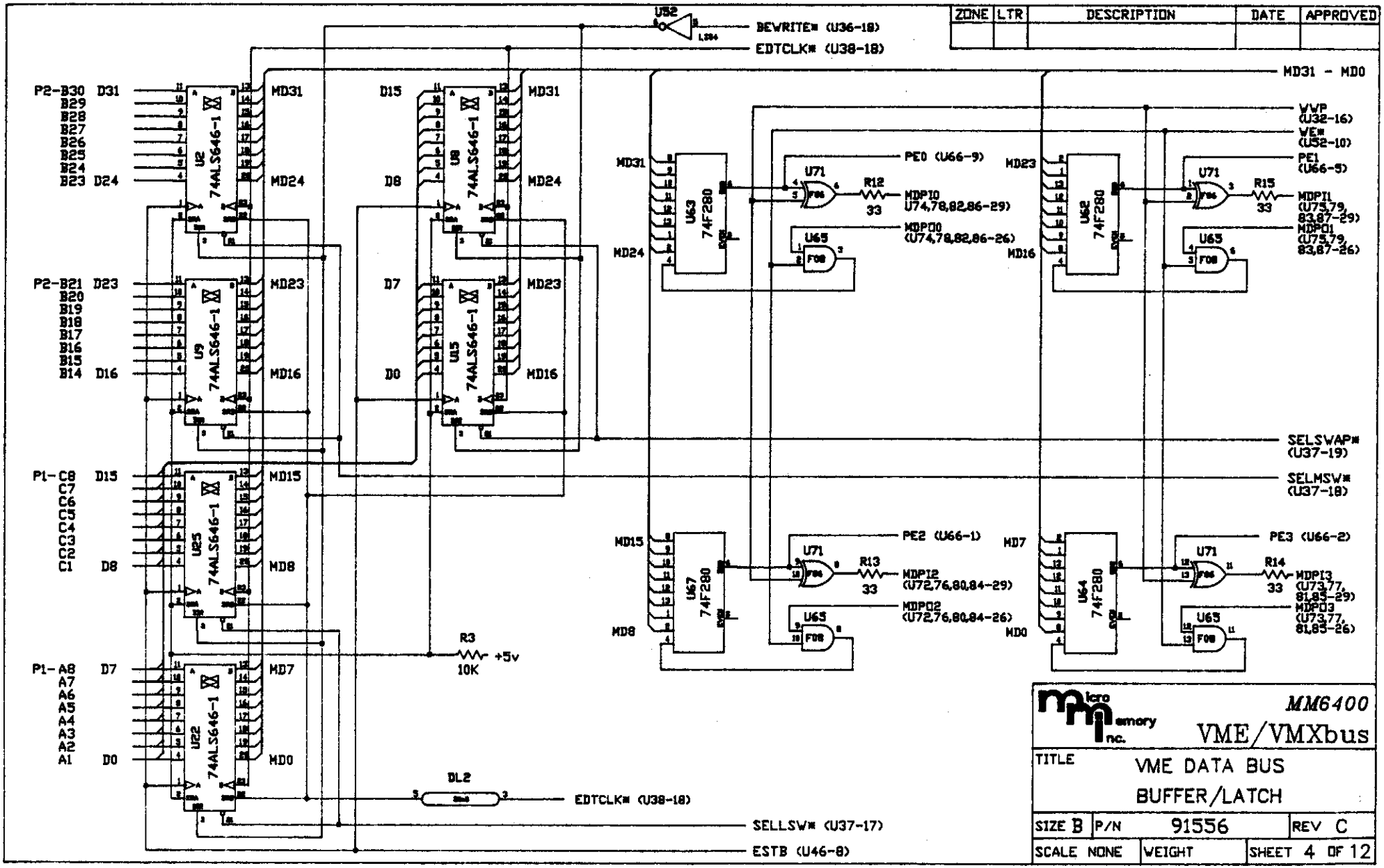
TITLE

VMXbus

BUFFER/LATCH

SIZE B	P/N 91556	REV C
SCALE NONE	WEIGHT	SHEET 6 OF 12

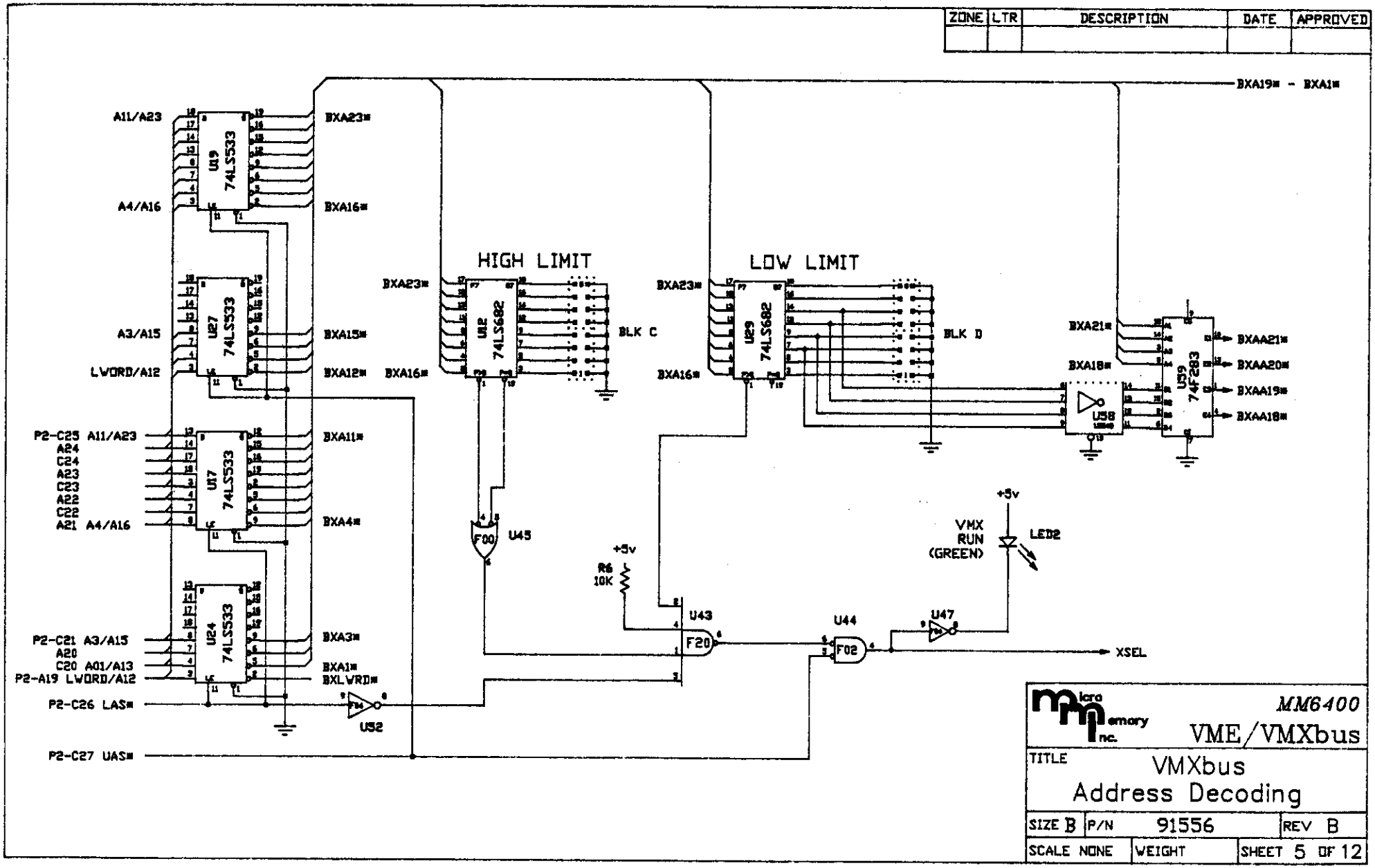
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ZONE	LTR	DESCRIPTION	DATE	APPROVED



Micro Memory Inc.

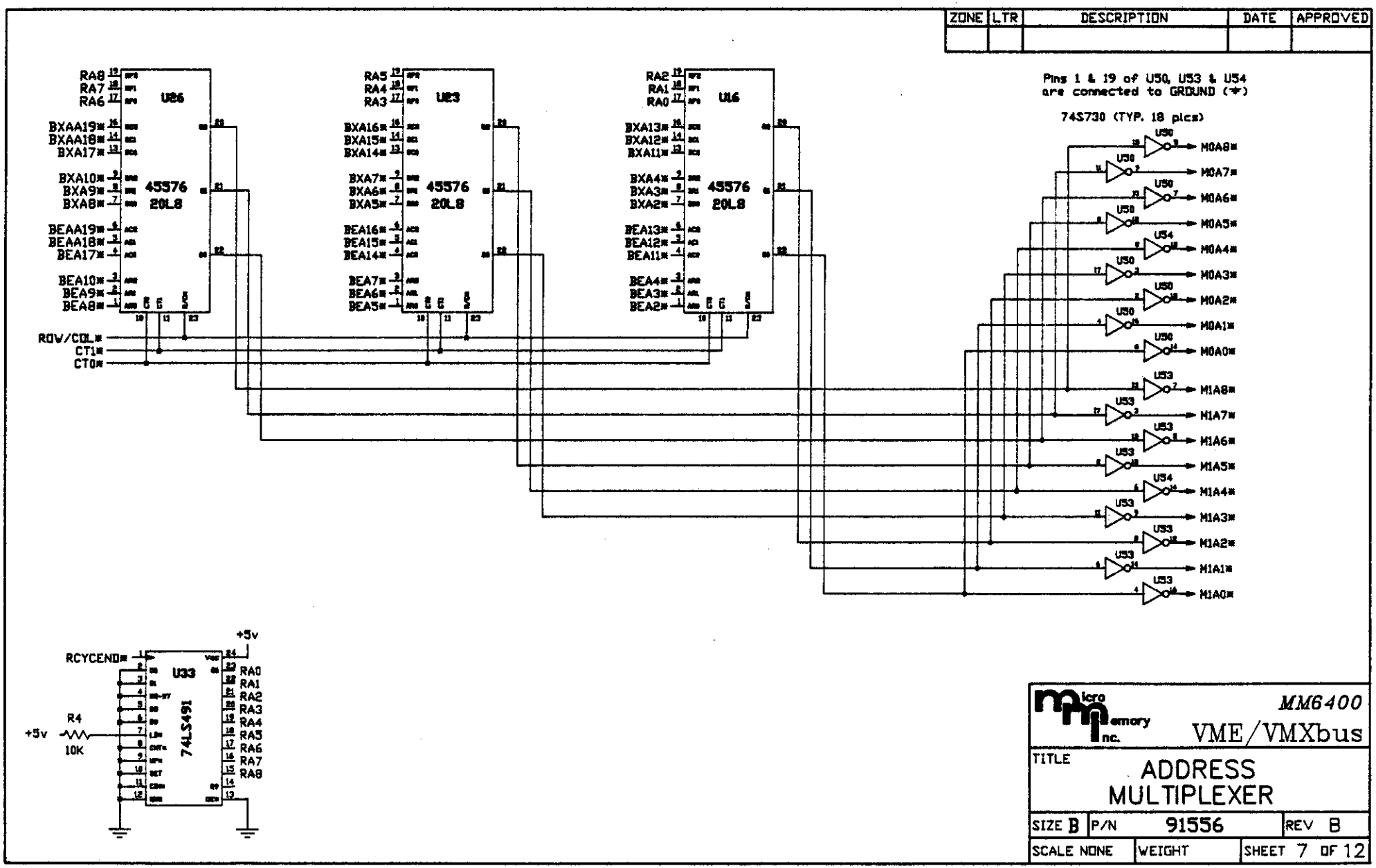
MM6400

VME/VMXbus

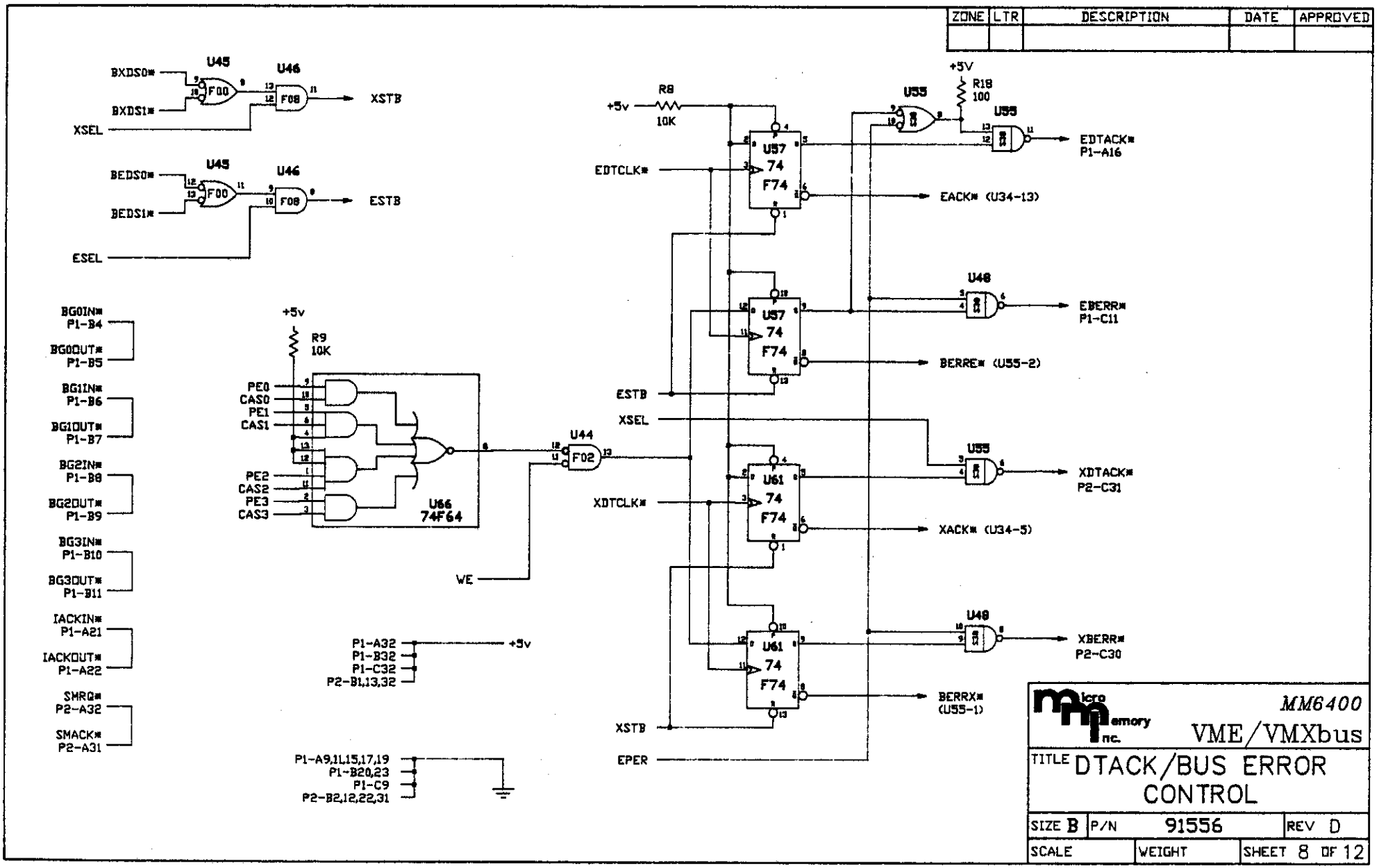
TITLE

VMXbus
Address Decoding

SIZE B	P/N 91556	REV B
SCALE NONE	WEIGHT	SHEET 5 OF 12



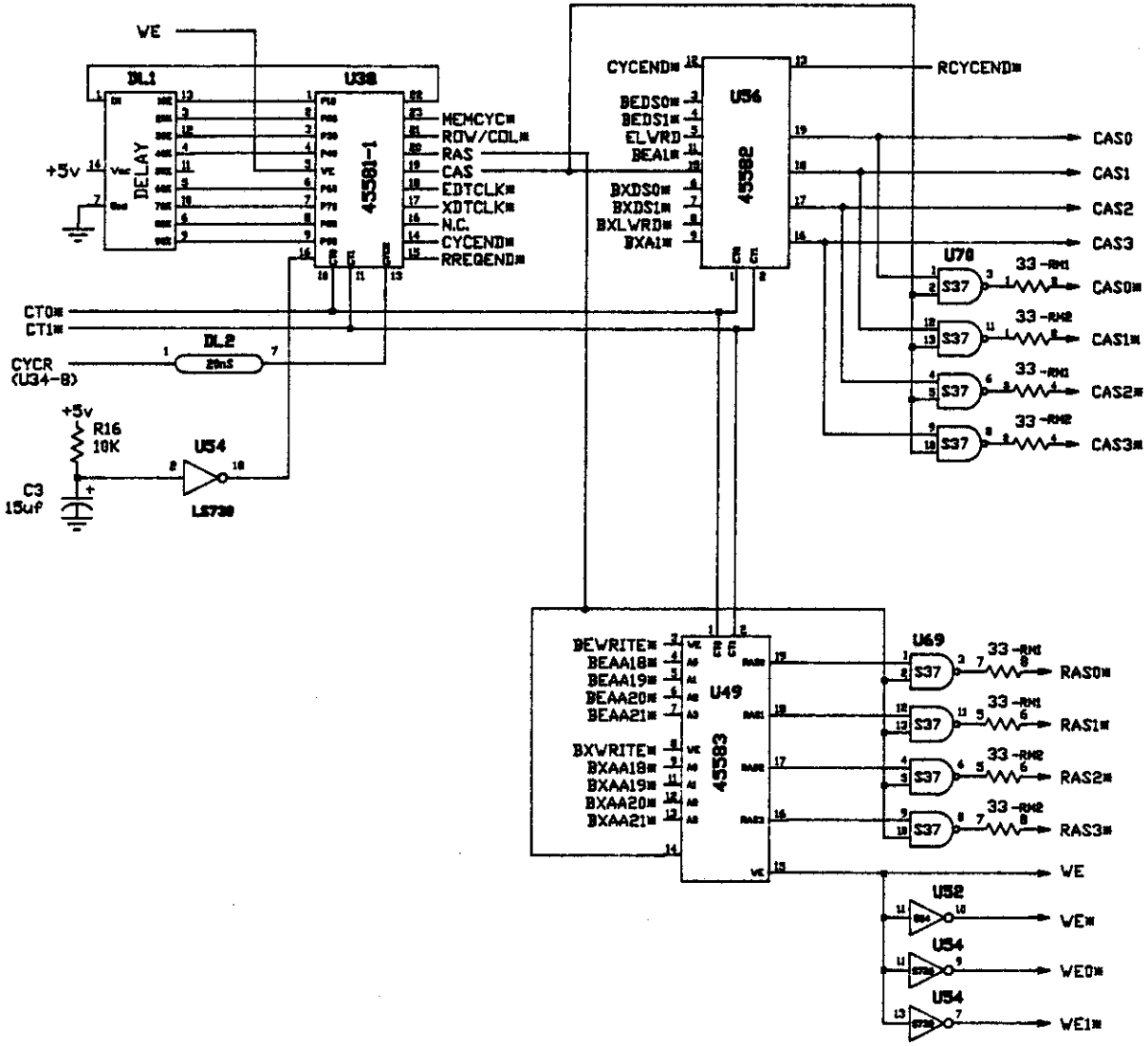
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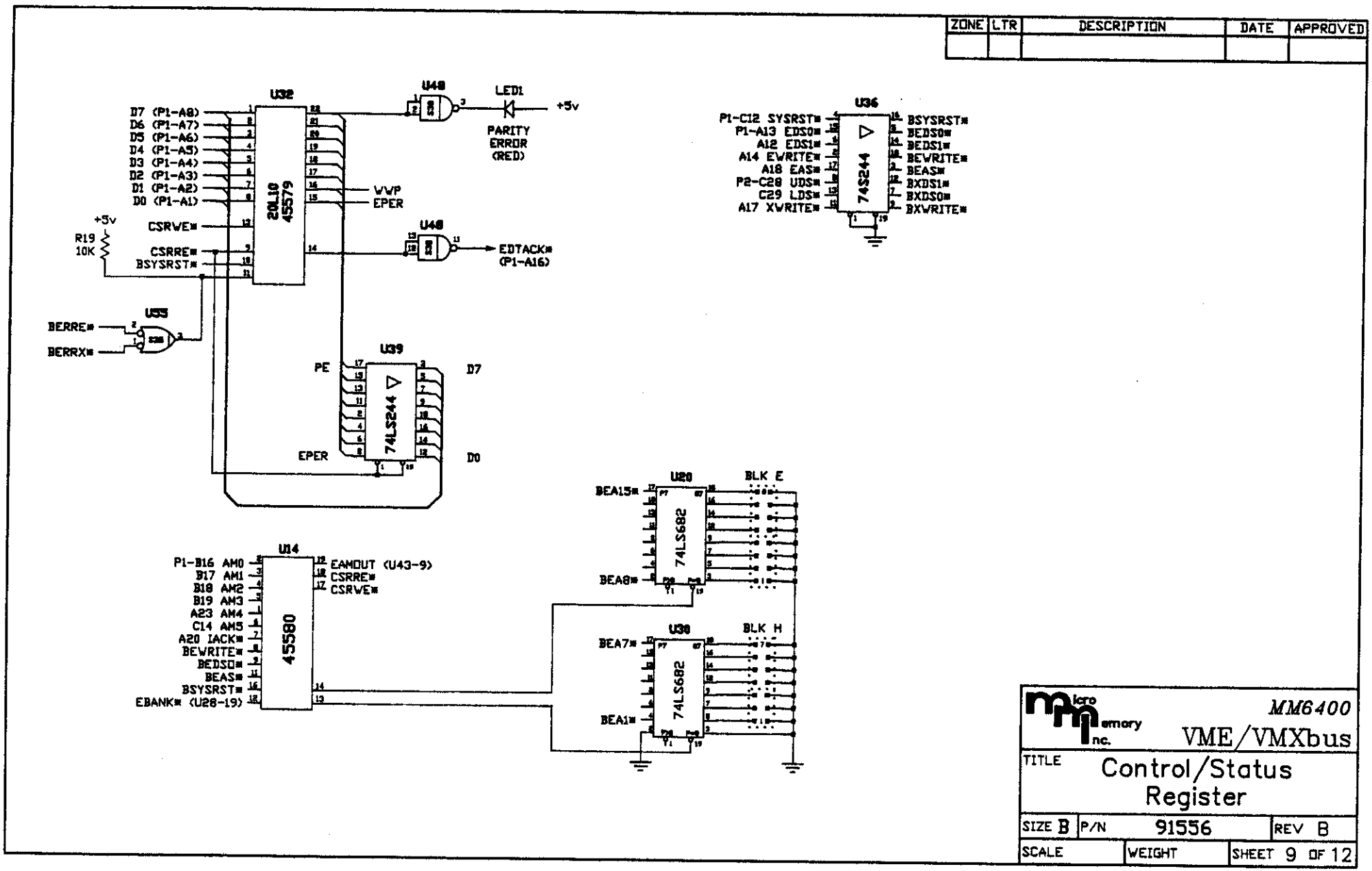
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ZONE	LTR	DESCRIPTION	DATE	APPROVED



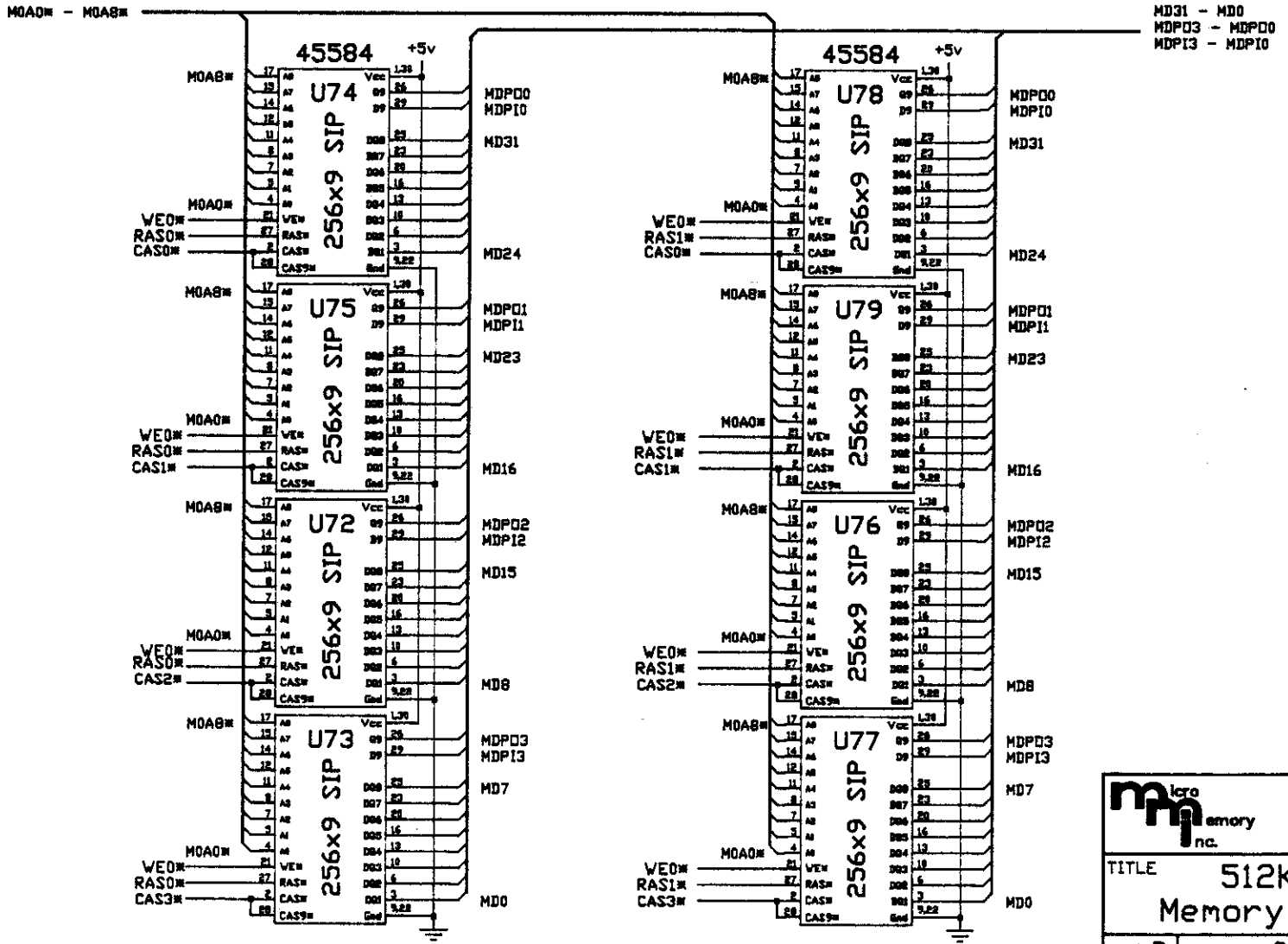
Micro Memory Inc.	*MM6400* VME/VMXbus	
TITLE	DYNAMIC MEMORY CONTROL	
SIZE B	P/N 91556	REV C
SCALE NONE	WEIGHT	SHEET 10 OF 12



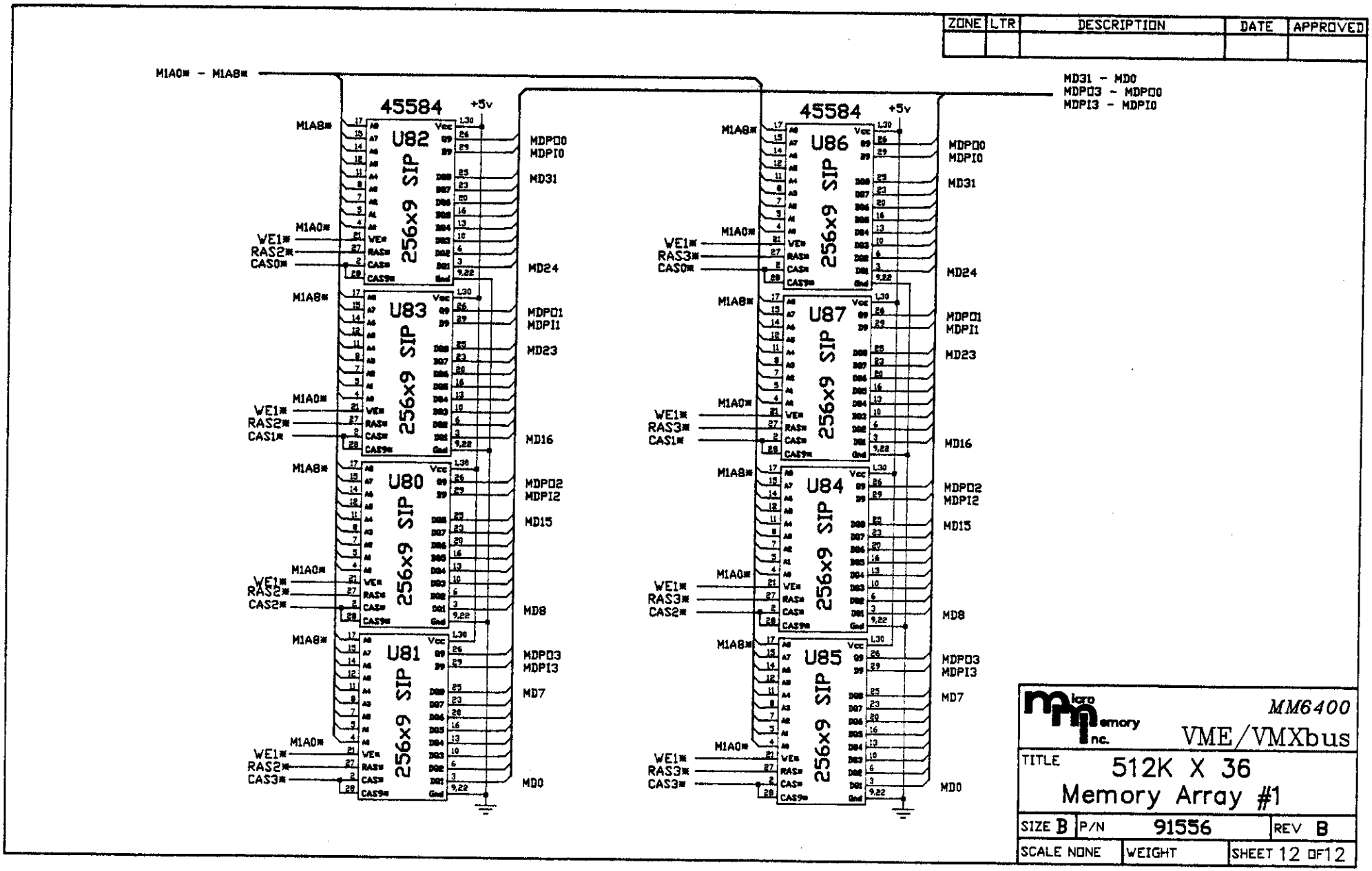
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ZONE	LTR	DESCRIPTION	DATE	APPROVED



micro memory inc.			*MM6400* VME/VMXbus
TITLE	512K X 36 Memory Array #0		
SIZE B	P/N 91556		REV B
SCALE NONE	WEIGHT		SHEET 11 OF12



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