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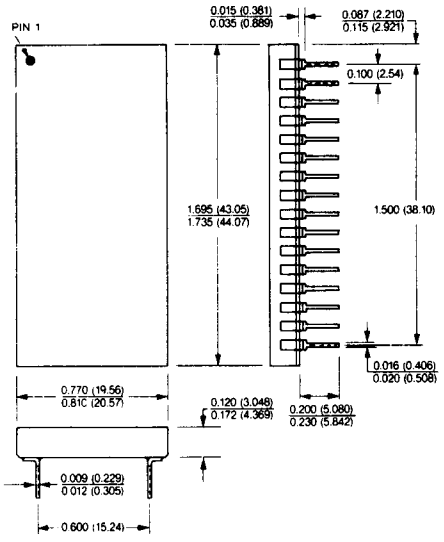
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FEATURES

- 16-Bit Resolution
- 14-Bit Performance Guaranteed Over Temperature
- 40μsec Max Conversion Time
- ±0.003% FSR Maximum Linearity Error
- Serial and Parallel Outputs
- 6 User-Selectable Input Ranges
- 1080mW Max Power Consumption
- Standard 32-Pin DIP
- Full Mil Operation −55°C to +125°C
- MIL-PRF-38534 Screening Optional

32 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN5290 and MN5291 are high-performance, dual-in-line packaged, 40μsec, 16-bit A/D converters specifically designed for use in military/aerospace and industrial applications that demand fully guaranteed high-resolution performance over extended operating temperature ranges. These successive approximation A/D converters exploit the stability and tracking advantages of both SiCr and NiCr thin-film resistor technologies. Fully assembled devices are functionally laser trimmed before and after a proprietary resistor stabilization process that made MN5290 and MN5291 the industry's first 16-bit A/D's to fully guarantee performance from −55°C to +125°C. Recently, the Micro Networks MN5295/5296 (17μsec conversion time) have joined MN5290/5291 as the only true military 16-bit A/D's.

MN5290 and MN5291 are packaged in industry-standard, hermetically sealed, 32-pin, ceramic, dual-in-line packages. Each is complete with internal clock and reference and has 6 user-selectable input ranges. Output data is straight binary coded for unipolar input ranges and offset binary coded for bipolar input ranges and is available in both serial and parallel formats.

MN5290 and MN5291 are ideal for applications requiring true 14- and 13-bit performance over extended temperature ranges. Applications will be found in military instrumentation, ATE and servo systems and in industrial robotic position sensing systems. MN5290H/B and MN5291H/B are available with Environmental Stress Screening while MN5290H/B CH and MN5291H/B CH are screened in accordance with MIL-PRF-38534.

Model Number	Temperature Range for Guaranteed No Missing Codes	
MN5290	14 Bits	0°C to +70°C
MN5290H	14 Bits	−55°C to +125°C
MN5290H/B	14 Bits	−55°C to +125°C
MN5290H/B CH	14 Bits	−55°C to +125°C
MN5291	13 Bits	0°C to +70°C
MN5291H	13 Bits	−55°C to +125°C
MN5291H/B	13 Bits	−55°C to +125°C
MN5291H/B CH	13 Bits	−55°C to +125°C

MN5290 MN5291 HIGH-RESOLUTION A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5290, MN5291	0°C to +70°C
MN5290H, H/B; MN5291H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 27)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 23)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pin 29)	0 to +7 Volts
Analog Inputs (Pins 8 and 9)	±22 Volts
Digital Inputs (Pins 30 and 32)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5290 H/B CH

- Select MN5290 or MN5291 model.
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{dd} = +5V unless otherwise indicated) (Note 1)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Bipolar		0 to +5, 10, 20 ±2.5, 5, 10		Volts Volts
Input Impedance (Note 2): 0 to +5V, ±2.5V 0 to +10V, ±5V ±10V		2.5 5 10		kΩ kΩ kΩ
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			+40 −1.6	μA mA
TRANSFER CHARACTERISTICS (Note 3)				
Resolution		16		Bits
Integral Linearity Error (Note 4): Initial (+25°C): MN5290 MN5291 Over Temperature (Note 5): MN5290 MN5291		 ±0.0015 ±0.003 ±0.003 ±0.006	 ±0.003 ±0.006 ±0.006 ±0.012	 %FSR %FSR %FSR %FSR
Differential Linearity Error (Note 4): MN5290 MN5291		±0.003 ±0.006	±0.006 ±0.012	%FSR %FSR
Temperature Range for Guaranteed No Missing Codes MN5290 (14 bits), MN5291 (13 bits) MN5290H (14 bits), MN5291H (13 bits)	 0 −55		 +70 +125	 °C °C
Full Scale Absolute Accuracy Error (Note 6): Unipolar: Initial (+25°C) Over Temperature (Note 5) Bipolar: Initial (+25°C) Over Temperature (Note 5)		 ±0.075 ±0.15 ±0.1 ±0.2	 ±0.15 ±0.3 ±0.2 ±0.4	 %FSR %FSR %FSR %FSR
Unipolar Offset Error (Notes 7, 8): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.1 ±0.2 ±15	%FSR %FSR ppm of FSR/°C
Bipolar Zero Error (Notes 7, 9): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.12 ±0.2 ±15	%FSR %FSR ppm of FSR/°C
Gain Error (Notes 7, 10): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.1 ±0.2 ±20	% % ppm/°C
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 11): Unipolar Ranges Bipolar Ranges		SB OB		
Logic Levels: Logic "1" (I_{SOURCE} ≤ 320μA) Logic "0" (I_{SINK} ≤ 3.2mA)	+2.4		 +0.4	Volts Volts
REFERENCE OUTPUT				
Internal Reference: Voltage Accuracy Tempco (Note 2) External Current (Notes 2,12)		+10.000 ±0.025 ±5	 ±0.1 1	Volts % ppm/°C mA
DYNAMIC CHARACTERISTICS				
Conversion Time (14 Bits/16 Bits) (Note 13)		34/38	36/40	μsec

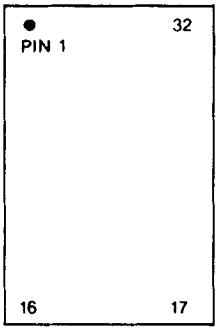
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: ±15V Supplies +5V Logic Supply	±14.55 +4.75	±15 +5	±15.45 +5.25	Volts Volts
Power Supply Rejection (Note 14): +15V Supply −15V Supply +5V Logic Supply		±0.005 ±0.005 ±0.001	±0.02 ±0.02 ±0.01	%FSR/%Supply %FSR/% Supply %FSR/% Supply
Current Drains: +15V Supply −15V Supply +5V Logic Supply		+30 −20 +12	+37 −29 +18	mA mA mA
Power Consumption		810	1080	mW

SPECIFICATION NOTES:

1. Listed specifications apply for all part numbers unless specifically indicated. Detailed timing specifications appear in the Timing sections of this data sheet.
2. These parameters are listed for reference only and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for 0 to +20V or ±10V operation has a 20V FSR. A unit connected for 0 to +10V or ±5V operation has a 10V FSR etc. 1 LSB for 16 bits is equivalent to 0.00153%FSR. 1 LSB for 14 bits is equivalent to 0.0061%FSR.
4. ±0.003%FSR is equivalent to ±½ LSB for 14 bits. ±0.006%FSR is equivalent to ±½ LSB for 13 bits.
5. Listed specifications apply over the 0°C to +70°C temperature range for standard products and over the −55°C to +125°C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Initial unipolar offset (bipolar zero) and gain errors are adjustable to zero with the use of external potentiometers.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN5290/5291 on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN5290/5291 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
10. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 1111 to 1111 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0000 0001 to 0000 0000 0000 0000.
11. SB = straight binary. OB = offset binary. See table of transition voltages in section labeled Digital Output Coding.
12. In addition to supplying 1mA of current for bipolar offsetting purposes (pin 7 connected to pin 24), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
13. Conversion is initiated on the falling edge of the start convert command, and conversion time is defined as the width of the status (end of conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14-bit conversions. See Timing Diagram.
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

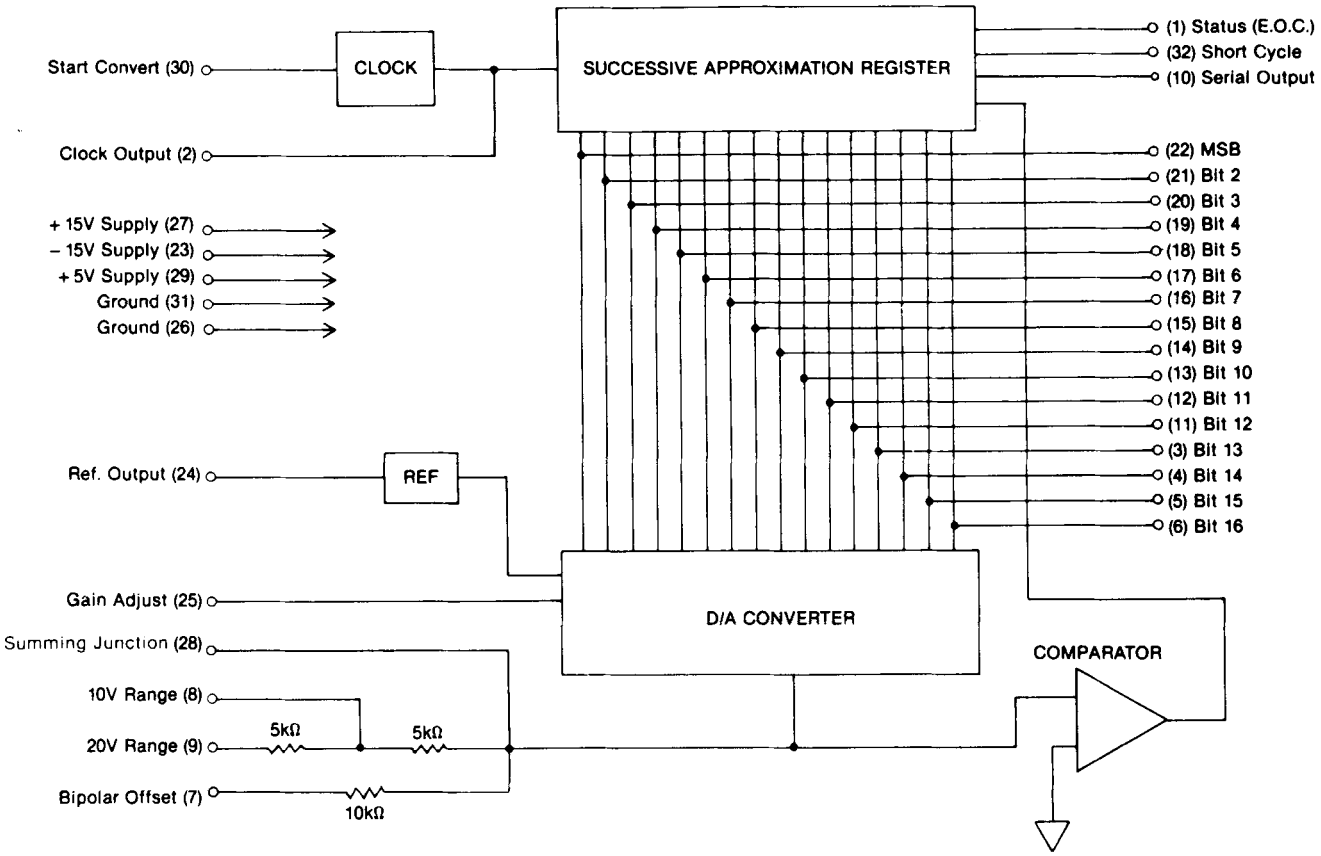
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	Status (E.O.C.)	32	Short Cycle
2	Clock Output	31	Ground
3	Bit 13	30	Start Convert
4	Bit 14	29	+5V Supply (+V_{dd})
5	Bit 15	28	Summing Junction
6	Bit 16 (LSB)	27	+15V Supply (+V_{cc})
7	Bipolar Offset	26	Ground
8	10V Input Range	25	Gain Adjust
9	20V Input Range	24	Reference Output (+10V)
10	Serial Output	23	−15V Supply (−V_{cc})
11	Bit 12	22	Bit 1 (MSB)
12	Bit 11	21	Bit 2
13	Bit 10	20	Bit 3
14	Bit 9	19	Bit 4
15	Bit 8	18	Bit 5
16	Bit 7	17	Bit 6

BLOCK DIAGRAM



APPLICATIONS INFORMATION

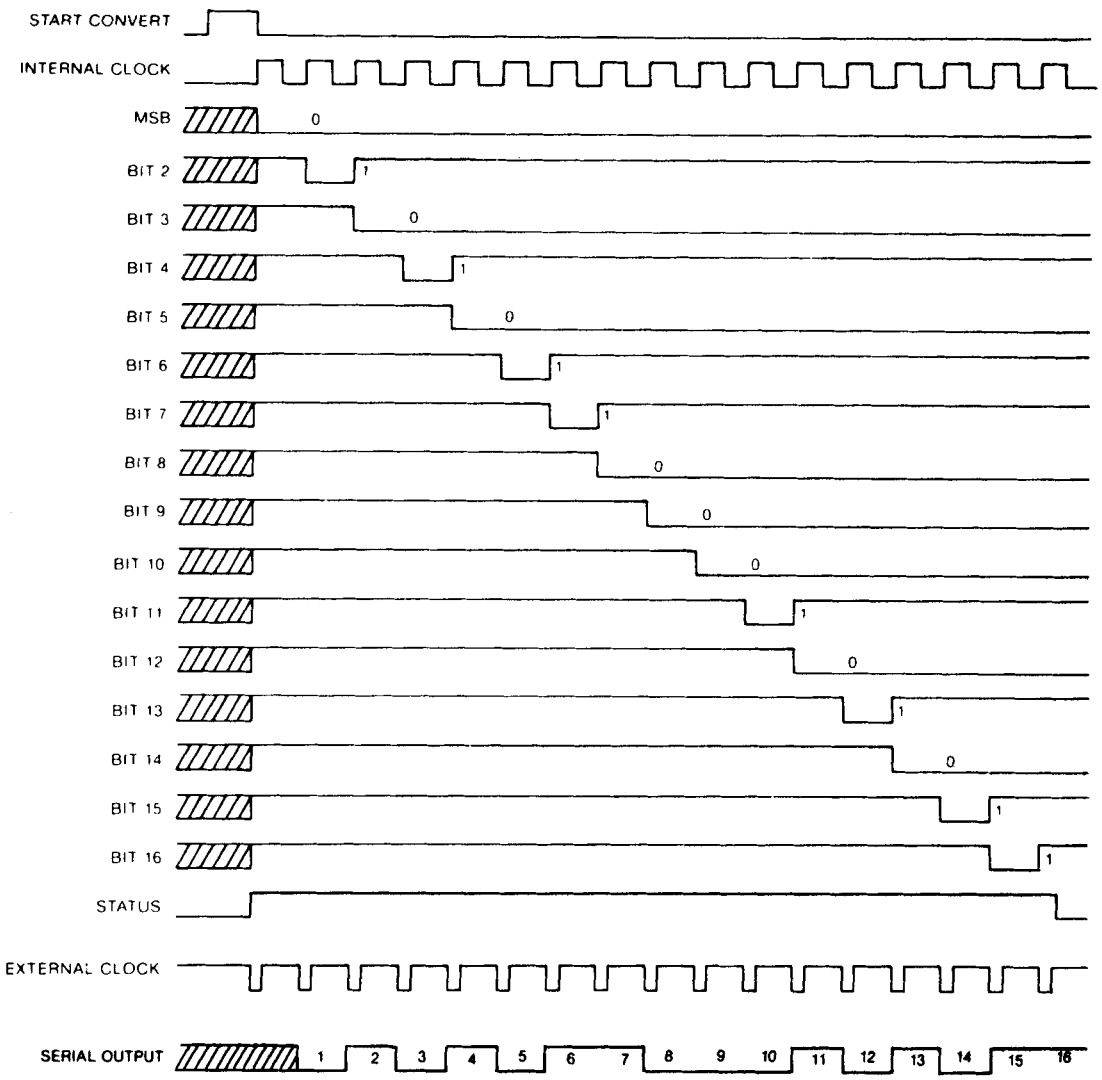
DESCRIPTION OF OPERATION—See Block Diagram. The successive approximation register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the analog-to-digital converter (A/D) and the digital drive for the A/D's internal digital-to-analog converter (D/A). The falling edge of a start convert pulse applied to pin 30 turns on the A/D's internal clock and resets the SAR. In this state, the output of the MSB flip flop is set to logic "0"; the outputs of the other bit flip flops are set to a logic "1"; and the Status (pin 1) is set to logic "1" (see Timing Diagram). The Start Convert must now remain low for the conversion to continue.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after Start Convert has gone low, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 16) also drops the Status Output to a "0" signaling that the conversion is complete and turning off the internal clock. Output data is now valid and will remain so until another conversion is started.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5290 and MN5291. The units' two ground pins (pins 26 and 31) are not connected to each other internally. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a nonpolarized 0.01μF ceramic bypass capacitor should be connected between pins 26 and 31 as close to the unit as possible and wide conductor runs employed.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 7 (Bipolar Offset), 8 and 9 (Analog Inputs), 28 (Summing Junction) and 25 (Gain Adjust) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when using these inputs. Input signal lines should be as short as possible. In bipolar operation, where pin 7 is connected to pin 24, a short jumper should be used. If bipolar offsetting is not used, pin 7 should be grounded to pin 26. For external offset adjustment, the 1.8 megohm resistor should be located as close to pin 28 as possible. A 0.01μF ceramic capacitor should be connected between pin 25 and analog ground as close to the package as possible.

TIMING DIAGRAM



SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise specified)

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (14 Bits/16 Bits)		34/38	36/40	µsec
Internal Clock Frequency (Note 8)		420		kHz
Start Convert Positive Pulse Width (Note 8)	50			nsec
Delay Falling Edge of Start to (Note 8): Status = "1"		50	80	nsec
Clock Output = "1"		20	50	nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8)	20	120	200	nsec
Delay LSB Valid to Falling Edge of Status (Note 8)	20	60		nsec

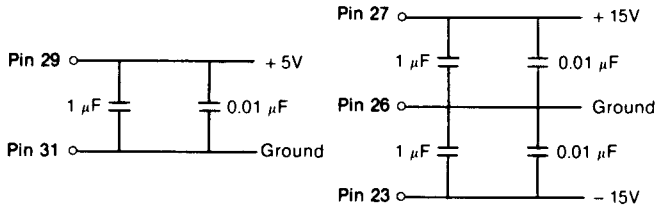
TIMING DIAGRAM NOTES

1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. Data will be valid 60nsec before the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
5. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock.
6. When the converter is initially "powered up", it may come on at any point in the conversion cycle.
7. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14 bit conversions.
8. These parameters are listed for reference only and are not tested.

Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN5290 and MN5291. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagram below.

If short cycling is not used, the Short Cycle pin (pin 32) must be connected to +5V (pin 29).

POWER SUPPLY DECOUPLING



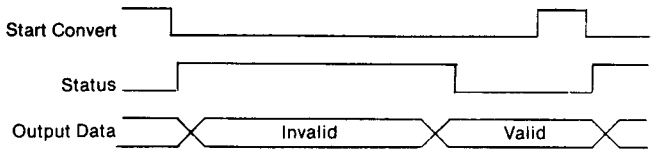
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

SHORT CYCLING—For applications requiring fewer than 16 bits of resolution, the MN5290 and MN5291 can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle pin (pin 32). For example, to truncate at 14 bits, connect pin 5 (Bit 15) to pin 32; converting will stop and Status will go low after bit 14 has been set. For any length conversion, the falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs.

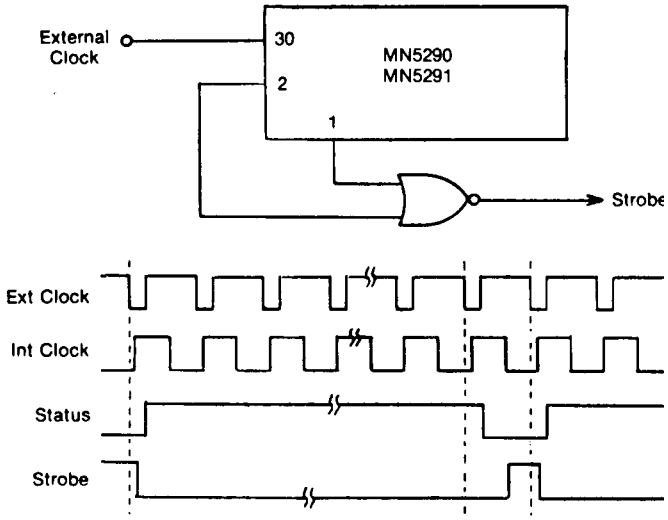
EXTERNAL CLOCK—An external clock may be connected to the Start Convert input. This external clock must consist of negative-going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 17 clock cycles. The internal clock will be disabled whenever Start Convert is held high. When using an external clock, a Start Convert command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after Status has gone low signaling the end of the previous conversion. When continuously converting in this manner, Status will go low for one external clock period following the completion of each conversion.

SERIAL OUTPUT—Serial data is available only during the conversion process. Format is NRZ with the MSB occurring first. Serial data is coded the same as parallel output data, and it is synchronous with the internal clock as shown in the Timing Diagram. Each data bit becomes valid typically 120nsec after each rising clock edge and remains valid for the full clock period. Therefore, falling clock edges can be used to strobe serial data into output registers.

STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert signal; will remain high during conversion; and will drop to a logic "0" when conversion is complete. The falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs. If parallel data is to be latched into external registers, this delay should be long enough to accomodate the set-up time requirements of the latch such that Status can be used to strobe the latch. If the delay is not long enough, the Status can be delayed with gate delays or the latch can be strobed with the leading edge of the next start convert pulse. See diagram below.

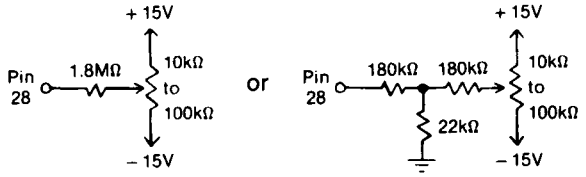


If continuously converting with an external clock, Status can be NORed with the internal clock, as shown below, to produce a positive strobe pulse approximately ½ period wide approximately ½ period after Status has gone low. The rising edge of this pulse can be used to latch data after each conversion. Recall that the falling edges of the external clock pulses generate rising edges of the internal clock and that these two clocks appear 180 degrees out of phase. The delay from the rising edge of the internal clock to the rising edge of Status is typically 120nsec. See Timing Diagram and the section labeled External Clock.



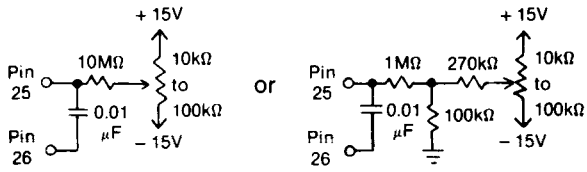
INTERNAL REFERENCE—The MN5290 and MN5291 contain an internal, low-drift 10V reference that is laser trimmed to an initial accuracy of ±0.1%. The reference is pinned out on pin 24 and can supply up to 1mA beyond the current required for bipolar operation (pin 24 connected to pin 7). If the external load is expected to vary during converter operation or if the internal reference is to be used to drive external circuitry at elevated temperatures, the reference output should be buffered externally.

OPTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS — Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 28 should be connected as described in the Range Selection section.



ZERO ADJUSTMENT—Connect the zero adjust potentiometer as shown. For unipolar ranges, apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "0" and the LSB "flickers" on and off. For bipolar ranges, apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits "flicker" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off.



DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+ F.S.	+ F.S.	1111 1111 1111 1111
+ F.S. – 3/2 LSB	+ F.S. – 3/2 LSB	1111 1111 1111 111Ø*
+ 1/2 F.S. + 1/2 LSB	+ 1/2 LSB	1000 0000 0000 000Ø*
+ 1/2 F.S. – 1/2 LSB	– 1/2 LSB	ØØØØ ØØØØ ØØØØ ØØØØ*
+ 1/2 F.S. – 3/2 LSB	– 3/2 LSB	0111 1111 1111 111Ø*
+ 1/2 LSB	– F.S. + 1/2 LSB	0000 0000 0000 000Ø*
0	– F.S.	0000 0000 0000 0000

CODING NOTES:

1. For 10 Volts FSR, 1LSB for 16 Bits = 152.6μV. 1LSB for 14 Bits = 610.4μV.
2. For 20 Volts FSR, 1LSB for 16 Bits = 305.2μV. 1LSB for 14 Bits = 1.22mV.
3. For unipolar ranges, the coding is straight binary.
4. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5290/MN5291 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE					
	0 to + 5V	0 to + 10V	0 to + 20V	± 2.5V	± 5V	± 10V
Connect Pin 7 to Pin	26	26	26	24	24	24
Connect Pin 9 to Pin	28	Open	Input	28	Open	Input
Connect Pin 28 to Pin	9	Open	Open	9	Open	Open
Connect Input to Pin	8	8	9	8	8	9
Input Impedance (KΩ)	2.5	5	10	2.5	5	10

EXAMPLE: For the ± 10V range, the transition from output code 1111 1111 1111 1111 to output code 1111 1111 1111 1110 (or vice versa) will ideally occur at an input of + 9.999542V (+ F.S. – 3/2LSB). Subsequently, any voltage greater than + 9.999542V will give a digital output of all "1's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of – 0.000153 volts. The 0000 0000 0000 0000 to 0000 0000 0000 0001 transition will occur at – 9.999847V. An input more negative than this level will give all "0's."

USING TRACK-HOLD AMPLIFIERS WITH MN5290 AND MN5291 CONVERTERS

Successive approximation type A/D converters cannot accurately digitize analog signals whose slew rates produce amplitude changes (ΔV) greater than ± 1/2LSB during the A/D conversion time (Δt). If such signals are to be accurately digitized, a sample/hold (S/H) or track/hold (T/H) amplifier will be required in front of the A/D to hold input signals constant during the conversion period. For an MN5290 operating on its ± 10V input range and short cycled for 14-bit conversions, 1/2LSB (ΔV) is equivalent to 0.61mV, and the maximum conversion time (Δt) is 36μsec. Therefore, the analog-signal slew-rate limit beyond which an MN5290 requires a T/H is equal to $\Delta V/\Delta t = 0.61mV/36\mu sec = 16.94$ V/sec. If one prefers to think in terms of sinusoidal bandwidths, one concludes that a 36μsec, 14-bit A/D cannot accurately digitize a sinewave whose instantaneous slew rate exceeds 16.94V/sec. For a given sine wave $v(t) = A\sin\omega t$, the maximum slew rate will equal $\Delta V/\Delta t$ (max) $= A\omega = 2\pi Af$. If A = 10V and $\Delta V/\Delta t$ (max) = 16.94V/sec, then f(max) = 0.27Hz. In summary, the MN5290 or any similar successive approximation type A/D operated without a T/H (S/H) cannot be expected to accurately and linearly digitize a ± 10V sine wave with a frequency above 0.27Hz. The A/D will exhibit accuracy and linearity errors around the max slew rate point (zero crossing) of the sine wave. A properly selected T/H (S/H) in front of a given A/D converter will increase the permitted slew rate (bandwidth) by a factor equa to the ratio of the A/D conversion time divided by the T/H aperture jitter. The T/H may reduce system throughput however, since T/H acquisition and transient settling times will have to be added to A/D conversion time to determine how often digital output data can be updated.

There are four major considerations when choosing a T/H to operate with the MN5290 or MN5291. The T/H must have an input/output linearity commensurate with that of the chosen A/D. The T/H must be capable of and clearly specify acquisition and track-to-hold transient settling times to ± 0.003%FSR (± 1/2LSB for MN5290 short-cycled to 14 bits) or to ± 0.006%FSR (± 1/2LSB for MN5291 short-cycled to 13 bits). The T/H's output droop in the hold mode must be low enough so the held signal does not change more than ± 1/2LSB during the A/D conversion time. For an MN5290 operating on its ± 10V range and short cycled to 14 bits, this droop limit is 0.61mV/36μsec = 16.94μV/μsec. For an MN5291 operating on its ± 10V range and short cycled to 13 bits, this droop limit is 1.22mV/34μsec = 36μV/μsec. Lastly, the T/H

feedthrough attenuation must be such that no more than ± ½LSB of changing input signal feeds through during the conversion period. For use with a 14-bit MN5290, the T/H should have at least 84dB of feedthrough attenuation at appropriate frequencies. For use with a 13-bit MN5291, the T/H should have at least 78dB of feedthrough attenuation.

When actually implementing the T/H-A/D connection, there are two important timing considerations. When commanded to the signal acquisition mode (track mode) the T/H must be given enough time to acquire a new signal to within ± ½LSB of final value, and when commanded back to the hold mode, the T/H must be given enough time to permit its output transient to settle to within ± ½LSB of final value before initiating a conversion. This second consideration is often overlooked. When a T/H or S/H is commanded from the signal acquisition mode to the hold mode, a transient (glitch) invariably occurs, and the transient should be allowed to decay sufficiently before an A/D conversion is initiated. The relevant T/H specification may be called Track to Hold Transient Settling Time, Transient Settling Time or simply Settling Time. It is important to recall that for most successive approximation type A/D converters, the MSB is not set to its final value until 1 full clock period after a conversion has been initiated, and the transient must have decayed before that time. In the MN5290 for example (see Timing Diagram), the MSB is not set to its final value until 1 full clock period (2.4μsec typical) after the falling edge of the start convert command. If the transient of the selected T/H decays to within ± ½LSB of the appropriate resolution in less than 2.4μsec, the falling edge of the convert command can be used to drive the T/H into the hold mode.

Figure 1 (below) shows just such a configuration. When the start command is high, the T/H is in the tracking (signal acquisition) mode. The falling edge of the start command puts the T/H into the hold mode and simultaneously initiates the conversion operation. The MSB is set to its final value 1 clock period later, and the switching transient of the selected T/H must decay sufficiently during that time. The duration of the start convert command must be long enough to accommodate the acquisition time of the chosen T/H.

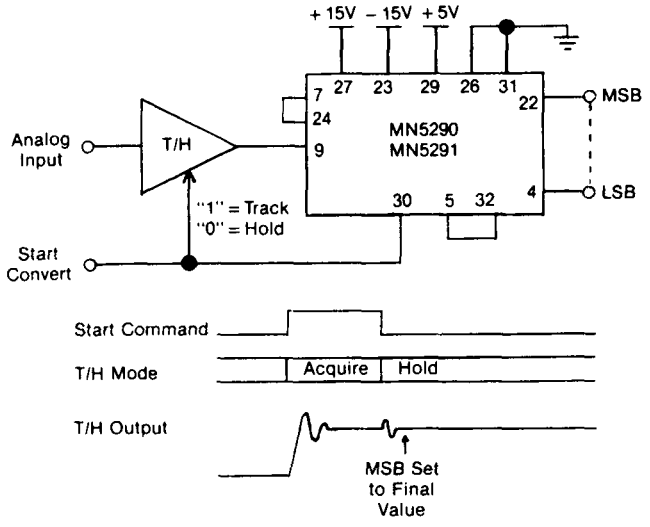


Figure 1. If controlling the T/H with the converter start pulse, the pulse must be wide enough to accomodate the acquisition time of the chosen T/H.

Another popular technique is to control the T/H's operation with the A/D converter's status line. This is demonstrated in Figure 2 below. For the MN5290 and MN5291, the status output is high during a conversion and drops low when a conversion is complete. The rising edge of status at the beginning of a conversion is used to command the T/H into the hold mode. As before, the T/H transient will have to decay before the A/D makes its MSB decision. The falling edge of status at the end of a conversion drives the T/H back into the track mode. The time between the falling edge of status and the falling edge of the next start convert pulse (the rising edge of the next status pulse) must be long enough to accomodate the acquisition time of the selected T/H.

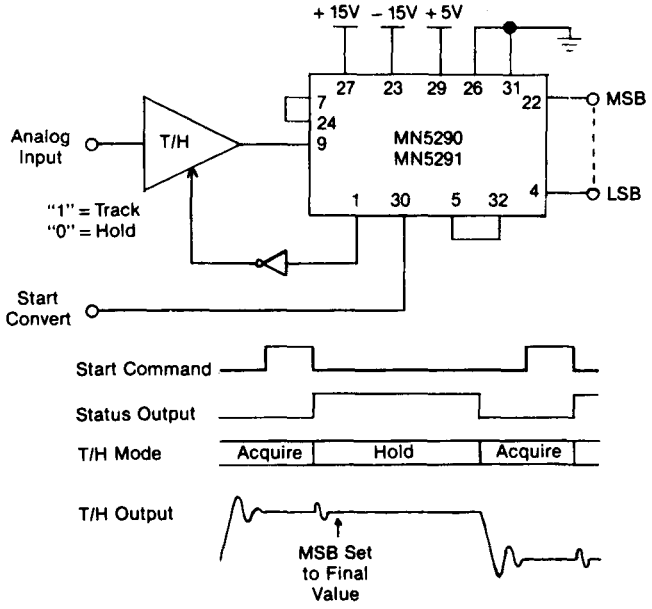


Figure 2. If controlling the T/H with the converter status output, the time between conversions must be long enough to accomodate the acquisition time of the chosen T/H.

If the MN5290 or MN5291 is to be operated in a continuously converting mode, there will not be enough time between conversions for most T/H's to acquire a new signal to the appropriate accuracy. In this situation, the falling edge of status at the end of each conversion can be used to fire a one-shot whose output can be both the start convert and T/H command signals. The duration of the one-shot must be long enough to accomodate the acquisition time of the chosen T/H.

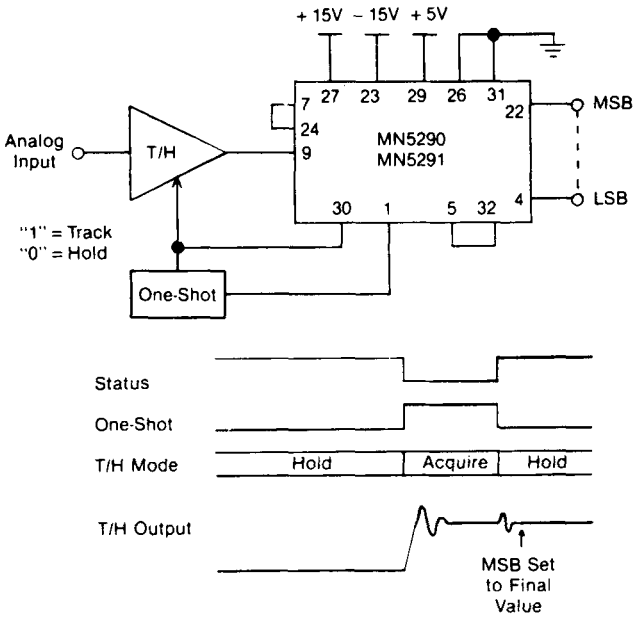


Figure 3. If continuously converting, a one-shot may be required to generate the start and T/H command pulses.

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