

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*



Chip-Scale Atomic Clock (CSAC)
SA.45s
User's Guide

© 2020-2021 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication is provided for the sole purpose of designing with and using Microchip products. Information regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL OR CONSEQUENTIAL LOSS, DAMAGE, COST OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackeTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2020-2021, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-7484-5

© 2020-2021 Microchip Technology Inc.

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXXXXA", where "XXXXXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics, to open a list of available online help files.

PURPOSE OF THIS GUIDE

The CSAC user guide provides basic recommendations for designing products to use Microchip's Chip-Scale Atomic Clock (CSAC) SA.45s. The guidelines in the document are generic because specific product requirements vary from one application to the other.

This material consists of a brief description of CSAC design supported by block diagrams, description of environmental issues, installation guidelines, and unit operation.

WHO SHOULD READ THIS GUIDE

This document is intended for engineers and telecommunications professionals who are designing, installing, operating, or maintaining time, frequency, and synchronization systems having a requirement for a low profile and highly precise frequency generator.

To use this document effectively, you should have a good understanding of digital telecommunications technologies and analog frequency generation and synthesis techniques.

DOCUMENT LAYOUT

This guide contains the following sections:

- **Chapter 1. "Product Overview"**: Provides an overview of the product, describes the major hardware and software features, and lists the system specifications.
- **Chapter 2. "Functional Description"**: Contains the Principle of Operation, Start-Up Sequence, and aspects related to first power-up.
- **Chapter 3. "Programmer's Reference"**: Provides an overview of the telemetry interface and command structure.
- **Chapter 4. "Developer's Kit"**: Describes the package contents, evaluation board information, and how to use the CSACdemo software.
- **Chapter 5. "Design Guide"**: Contains information about disciplining, heat sinking, soldering, and additional notes about the evaluation board.

© 2020-2021 Microchip Technology Inc.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

WARNINGS, CAUTIONS, RECOMMENDATIONS, AND NOTES

Warnings, Cautions, Recommendations, and Notes attract attention to essential or critical information in this guide. The types of information included in each are displayed in a style consistent with the examples below.

WARNING

To avoid serious personal injury or death, do not disregard warnings. All warnings use this style. Warnings are installation, operation, or maintenance procedures, practices, or statements, that if not strictly observed, may result in serious personal injury or even death.

CAUTION

To avoid personal injury, do not disregard cautions. All cautions use this style. Cautions are installation, operation, or maintenance procedures, practices, conditions, or statements, that if not strictly observed, may result in damage to, or destruction of, the equipment. Cautions are also used to indicate a long-term health hazard.

Note: All notes use this style. Notes contain installation, operation, or maintenance procedures, practices, conditions, or statements that alert you to important information, which may make your task easier or increase your understanding.

WHERE TO FIND ANSWERS TO PRODUCT AND DOCUMENT QUESTIONS

For additional information about the products described in this guide, please contact your Microchip representative or your local sales office. You can also contact us on the web at www.microsemi.com/ftdsupport.

When this manual is updated the latest version will be available for downloading from Microchip's web site. Manuals are provided in PDF format for ease of use. After downloading, you can view the manual on a computer or print it using Adobe Acrobat Reader.

Manual updates are available at: www.microsemi.com/ftdsupport

RELATED DOCUMENTS AND INFORMATION

See your Microchip representative or sales office for a complete list of available documentation. To order any accessory, contact the Microchip Sales Department. See www.microsemi.com/sales-contacts/0 for sales support contact information. If you encounter any difficulties installing or using the product, contact Microchip Frequency and Time Systems (FTS) Services and Support:

U.S.A. Call Center: including Americas, Asia and Pacific Rim

Frequency and Time Systems

3870 N 1st St.

San Jose, CA 95134

Toll-free in North America: 1-888-367-7966

Telephone: 408-428-7907

Fax: 408-428-7998

© 2020-2021 Microchip Technology Inc.

email: ftd.support@microsemi.com

Internet: www.microsemi.com/ftdsupport

Europe, Middle East, and Africa (EMEA)

Microchip FTS Services and Support EMEA

Altlaufstrasse 42

85635 Hoehenkirchen-Siegertsbrunn

Germany

Telephone: +49 700 3288 6435

Fax: +49 8102 8961 533

email: ftd.emeasupport@microsemi.com

email: ftd.emea_sales@microsemi.com

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
http://www.microchip.com/support.

© 2020-2021 Microchip Technology Inc.

DOCUMENT REVISION HISTORY

Revision A (September 2020)

- Initial release of this document as Microchip DS50003041A. Updated mechanical drawing per EC14514.
  - Under Microsemi's literature system, this document is number 098-00055-000, Rev. E.

Revision B (January 2021)

- Updated Alarm Limit values for 0x0010 and 0x0020 in Table 3-5 and added corresponding note.
- Updated drawing for Figure 5-3 for clarity.

Table of Contents

Preface **3**
Purpose of This Guide 3
Who Should Read This Guide 3
Document Layout 3
Conventions Used in this Guide 4
Warnings, Cautions, Recommendations, and Notes 5
Where to Find Answers to Product and Document Questions 5
Related Documents and Information 5
The Microchip Website 6
Customer Support 6
Document Revision History 7

Chapter 1. Product Overview
1.1 Introduction 10
1.2 SA.45s Overview 10
1.2.1 Packaging 11
1.2.2 Absolute Minimum and Maximum Ratings 11
1.2.3 Mechanical Interface and Mounting Considerations 12
1.2.4 Recommended Operating Characteristics 13

Chapter 2. Functional Description
2.1 Principle of Operation 14
2.2 Start-Up Sequence 15
2.3 Built-In Test Equipment (BITE) 15
2.4 RF Output Characteristics 16
2.5 What to Expect During First Power-Up 16
2.6 Frequency Steering 16
2.6.1 Frequency Calibration 18
2.7 1PPS Output 19
2.8 1PPS Synchronization 19
2.8.1 Manual Synchronization 19
2.8.2 Automatic Synchronization 20
2.9 1PPS Disciplining 20
2.9.1 Cable Length Compensation 21
2.10 Time-of-Day 22
2.11 Analog Tuning 23
2.12 Ultra-Low Power Operating Mode 24
2.13 1PPS Phase Measurement Mode 26

© 2020-2021 Microchip Technology Inc.

Chapter 3. Operation

3.1 Overview of Telemetry Interface 28
3.1.1 Checksum (Error-Checking Option for Telemetry Interface Communications) 28
3.1.2 How to Calculate the Checksum 29
3.2 Command Summary 29
3.3 Detailed Command Descriptions 30
3.3.1 Telemetry (6 and ^) 30
3.3.2 Frequency Adjustment (F) 32
3.3.3 Set/Clear Operating Modes (M) 33
3.3.4 1PPS Synchronization (S) 34
3.3.5 Set 1PPS Disciplining Time Constant (D) 35
3.3.6 Set 1PPS Disciplining Cable Length Compensation (DC) 35
3.3.7 Set Ultra-Low Power Mode Parameters (U) 35
3.3.8 Time-of-Day (TOD) 36
3.3.9 Set 1PPS Phase Threshold for Discipline Status OK Check (m) 37
3.3.10 Set 1PPS Out Pulse Width as an Integer Multiple of Default Width (>) 37
3.3.11 Deferred Command (@) 38
3.3.12 Help (?) 38

Chapter 4. Developer's Kit

4.1 Package Contents 40
4.2 Evaluation Board Overview 40
4.3 Installing the CSAC on the Test Fixture 41
4.4 Cabling 41
4.5 CSACdemo Software Installation 42
4.6 CSACdemo Operation 42
4.6.1 Initial Power-On 42
4.6.2 Establishing Communication 42
4.6.3 Monitoring Communications 43
4.6.4 Observing Acquisition 43
4.7 Data Acquisition with CSACdemo 44

Chapter 5. Design Guide

5.1 The Art of Disciplining 46
5.2 Heat Sink 47
5.3 Notes on Soldering 47
5.4 Notes on the Evaluation Board 48
5.5 Time Error of a CSAC 49
5.6 Writes to NVRAM 49

Worldwide Sales and Service 51

© 2020-2021 Microchip Technology Inc.

Chapter 1. Product Overview

1.1 INTRODUCTION

The Microchip Model SA.45s Chip-Scale Atomic Clock (CSAC) is the world's smallest, lowest power atomic clock technology. This user's reference guide provides the basic guidelines and recommendations for designing products with the CSAC reference. These are generic, and should be tailored for each application.

This document is intended for engineers, technicians, and technologists who are designing, installing, operating or maintaining time, frequency, and synchronization systems. The CSAC is a low profile, highly precise frequency generator. To use this document effectively, an understanding of digital communication technologies is required. It is advantageous to have a background in frequency generation and synthesis techniques.

1.2 SA.45S OVERVIEW

The Microchip CSAC SA.45s is the world's first commercially available chip-scale atomic clock, providing the accuracy and stability of atomic clock technology while achieving true breakthroughs in reduced size, weight, and power consumption. The small size (less than 17 cc) and low power consumption of the CSAC (less than 125 mW) enables atomic timing accuracy in portable, battery-powered applications.



FIGURE 1-1: *Microchip SA.45s Chip-Scale Atomic Clock (CSAC).*

The CSAC provides RF and 1PPS outputs at standard CMOS levels. It accepts a 1PPS input to synchronize the output to within 100 ns of a reference clock. It can also discipline its phase and frequency to within 1 ns and 1×10^{-12}, respectively.

This user guide provides engineering information for use of the CSAC. It also provides supporting information for use of the Developer's Kit (p/n 990-00123-00x). Furthermore, the design details of the developer's kit can be used to assist with host system design (for example, power conditioning or signal buffering). This guide must be used in conjunction with the current data sheet for CSAC SA.45s, which is available on the Microchip web site at www.microchip.com.

© 2020-2021 Microchip Technology Inc.

CAUTION

To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC.

1.2.1 Packaging

Retain the original CSAC ESD-safe packaging material in the event that the device needs to be returned to Microchip for service.

1.2.2 Absolute Minimum and Maximum Ratings

The following table indicates the absolute minimum and maximum ratings to which the CSAC can be subjected without permanent unrecoverable damage.

Note: The CSAC cannot be expected to perform normally when operated outside of the recommended operating conditions. All ratings apply at 25°C, unless otherwise noted.

TABLE 1-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Supply Voltage (V_{CC})	0V to +4.1V
Analog Tuning Voltage	0V to V_{CC}
Maximum Current Draw	1PPS input, RS-232, BITE: ±2 mA
	1PPS output, RF output, ±20 mA
Storage Temperature	–55°C to +85°C

Note: Refer to the product data sheet for updated parameters.

© 2020-2021 Microchip Technology Inc.

1.2.3 Mechanical Interface and Mounting Considerations

The physical dimensions of the CSAC are 1.6" x 1.4" x 0.45" H. The following illustration shows the detailed dimensions of CSAC. The CSAC baseplate and cover are 80% nickel-iron magnetic alloy per ASTM A753, Type 4 (Mu-Metal or Hy-Mu80™).

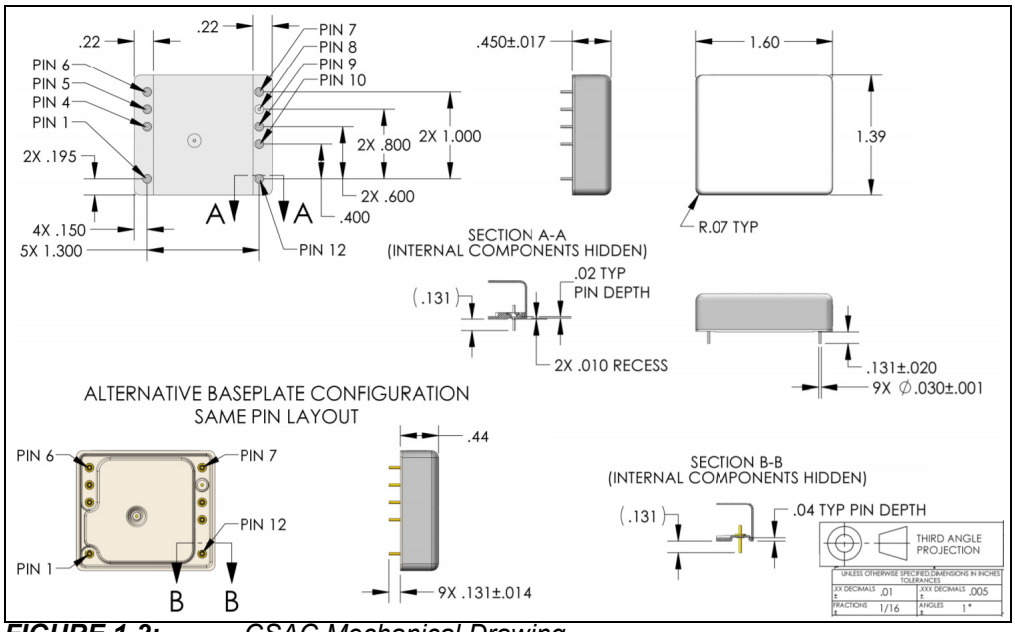
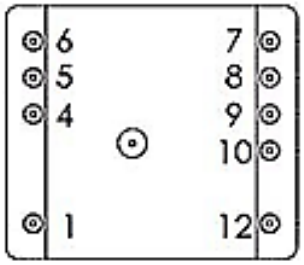


FIGURE 1-2: *CSAC Mechanical Drawing.*

The following table shows the pinout of the CSAC.

TABLE 1-2: CSAC SA.45S PINOUT

Pin	I.D.	Pinout Diagram
1	Tune	
2	N/A	
3	N/A	
4	BITE	
5	Tx	
6	Rx	
7	VCC	
8	GND	
9	1PPS Input	
10	1PPS Output	
11	N/A	
12	RF Output	

Note: Pins labeled “N/A” are not present in the CSAC.

1.2.4 Recommended Operating Characteristics

The CSAC pinout is shown in Table 1-2. The electrical function of each pin is shown in the following table.

TABLE 1-3: RECOMMENDED OPERATING CHARACTERISTICS

Pin	Function	Level	Reference Section
1	Analog tuning input (Note 1)	0V to 2.5V	**Section 2.11 "Analog Tuning"**
4	Built-In Test Equipment (BITE) (Note 2)	LogicH > 2.8V LogicL < 0.3V	**Section 2.3 "Built-In Test Equipment (BITE)"**
5, 6	RS-232	2.8V < LogicH < VCC 0V < LogicL < 0.3V	**Chapter 3. "Programmer's Reference"**
7	VCC	3.3VDC ±0.1VDC	—
8	Ground	—	—
9	1PPS In (Note 3)	2.5V < LogicH < VCC 0V < LogicL < 0.5V	—
10	1PPS Out (Note 4, Note 5)	2.8V < LogicH < VCC 0V < LogicL < 0.3V	**Section 2.7 "1PPS Output"**
12	RF Out	2.8V < LogicH < VCC 0V < LogicL < 0.3V	**Section 2.4 "RF Output Characteristics"**

Note 1: Analog Tuning Sensitivity is $\Delta f/f = (V_{TUNE} - 1250\ mV) \times 1.77 \times 10^{-11}/mV$.

2: Built-In Test Equipment: 0 = Normal operation, 1 = Unlock condition.

3: Timing reference is rising edge of input pulse on pin 9.

4: Output 1PPS is 100 µs in duration for option 001. Refer to the data sheet for other options. (400 µs for firmware versions 1.06 and earlier).

5: Timing reference is the rising edge of pin 10. Rise time <10 ns at a load capacitance of 10 pF.

6: See the CSAC SA.45s data sheet for updated parameters.

© 2020-2021 Microchip Technology Inc.

Chapter 2. Functional Description

The following is a functional description of the CSAC.

2.1 PRINCIPLE OF OPERATION

The CSAC is a passive atomic clock, incorporating the interrogation technique of coherent population trapping (CPT) and operating on the D1 optical resonance of atomic cesium. A complete description of passive atomic clocks, CPT, and the CSAC architecture is beyond the scope of this user guide. The following illustration shows a simplified block diagram of the CSAC.

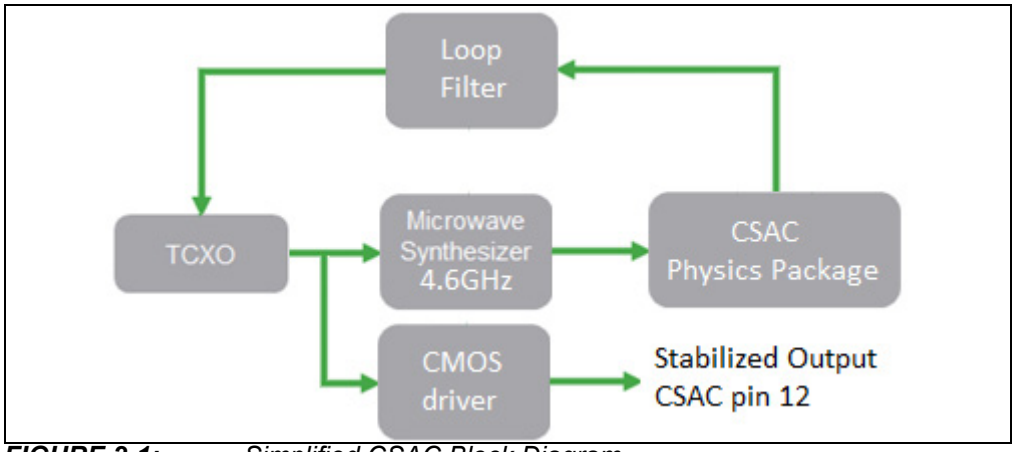


FIGURE 2-1: *Simplified CSAC Block Diagram.*

The principal RF output from the CSAC is provided by a temperature-compensated crystal oscillator (TCXO), which is buffered by a CMOS logic gate and provided on the CSAC output pin 12. In normal operation, the frequency of the TCXO is continuously compared and corrected to ground state hyperfine frequency of the cesium atoms, contained in the physics package, which thereby improves the stability and environmental sensitivity of the TCXO by four to five orders of magnitude. In addition to the TCXO and the physics package (Note 1), the essential components of the CSAC are the microwave synthesizer and the microprocessor (Note 2). The microwave synthesizer generates 4596.3x MHz with microprocessor-controlled tuning resolution of approximately 1×10^{-12}. The microprocessor serves multiple functions, including implementation of the frequency-lock loop filter for the TCXO, optimization of physics package operation, state-of-health monitoring, and command and control through communications port.

When the CSAC is initially powered on, it performs an acquisition sequence, which includes stabilizing the temperature of the physics package, optimizing physics package operating parameters, and acquiring frequency lock to the atomic resonance. The acquisition process may be monitored through the status field of the telemetry (see **Section 3.3.1 "Telemetry (6 and ^)"**). On power-up, the status begins at 8 (oven warm-up). The status value decrements numerically through the acquisition until normal operation (status = 0) is achieved. On rare occasions, the status countdown will reset during the acquisition. This is normal behavior if it does not disrupt the warm-up specification time.

© 2020-2021 Microchip Technology Inc.

Note 1: R. Lutwak, et. al., The Chip-Scale Atomic Clock - Low-Power Physics Package, Proceedings of the 36th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting, December 7–9, 2004, Washington, DC.

2: R. Lutwak, et. al., The MAC - A Miniature Atomic Clock, Proceedings of the 2005 Joint IEEE International Frequency Control Symposium and Precise Time & Time Interval Systems & Applications Meeting, August 29–31, 2005, Vancouver, BC.

2.2 START-UP SEQUENCE

CAUTION

To avoid severe damage to the unit, do not apply power to the incorrect terminals. The CSAC does not have reverse voltage protection.

When power is connected to pin 7, the CSAC unit begins its warm-up cycle. A signal appears at the output once power is applied to the unit. This output signal is not stable until the oscillator is locked (indicated by the BITE pin at CMOS_low).

After 3 minutes, the CSAC achieves Lock and BITE = 0 (**Section 2.3 "Built-In Test Equipment (BITE)"**). Power consumption during warm-up is greater than during normal operation; it is specified on the CSAC data sheet.

It is recommended to always allow CSAC to remain powered on for >102 seconds after it acquires LOCK. 102 seconds is the minimum amount of time necessary to save CSAC set points to memory. Otherwise, upon the next power up, the unit may go in to a mode of operation where it re-acquires all of its set points; warm-up time will then be out of specification.

2.3 BUILT-IN TEST EQUIPMENT (BITE)

CSAC state-of-health can be monitored electronically on pin 4 (BITE) of the CSAC. Frequency lock is indicated both by status = 0 in the status field of telemetry and by the electrical state of the BITE output pin, which is high (logic 1) upon initial power-on and whenever status ≠ 0. The BITE pin is a high impedance CMOS logic output.

Note: When not locked, BITE = 1 and also status ≠ 0 in the status field of the telemetry output string.

At the conclusion of the acquisition sequence (status = 0), BITE remains high for an additional 5 seconds in order to avoid false indication in the event of acquisition failure. Subsequently, BITE provides an immediate (within 1 second) indication of lock failure or alarm.

© 2020-2021 Microchip Technology Inc.

2.4 RF OUTPUT CHARACTERISTICS

The buffered CMOS RF output is provided on pin 12 of the CSAC. The output series impedance is 200Ω. For reference, the output driver circuit of the CSAC is shown in the following illustration.

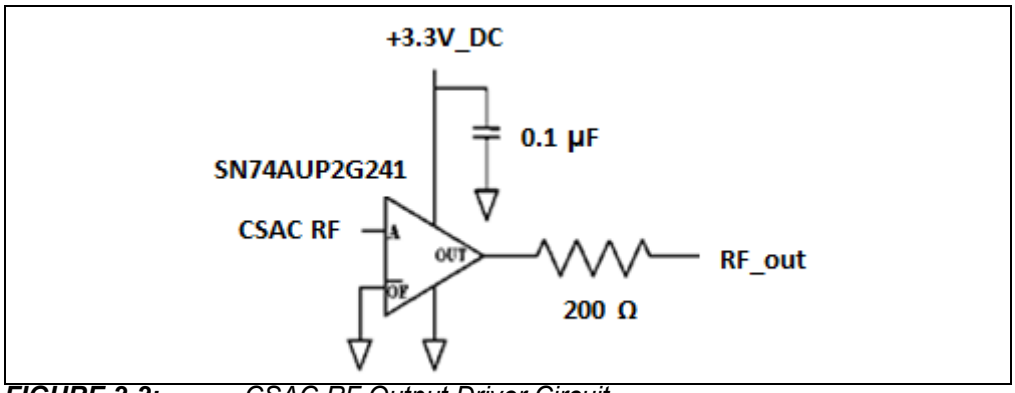


FIGURE 2-2: *CSAC RF Output Driver Circuit.*

The CSAC is designed for embedded low-power applications. It is expected to drive a high impedance input, not a 50Ω measurement instrument or transmission line.

> **Note:** Driving a 50Ω line at 13 dBm consumes nearly as much power as the CSAC itself. If a high-level (high-power) output driver is required, a driver circuit must be implemented external to the CSAC, such as the one implemented on the Evaluation Board (see **Section 5.4 "Notes on the Evaluation Board"**).

The RF output appears on pin 12 after the CSAC is powered ON and is always present, regardless of the lock status. When the CSAC is out of lock (BITE = 1, status ≠ 0), the output frequency is provided by the free-running TCXO, which has frequency accuracy specification of $\pm 20 \times 10^{-6}$ and temperature sensitivity of $\approx \pm 30 \times 10^{-9}$/°C. Typically, the unlocked frequency accuracy during acquisition is significantly better than this ($<1 \times 10^{-8}$) as the CSAC memorizes its last-known-good tuning voltage and restores this voltage upon power-up and/or subsequent recovery from loss-of-lock.

2.5 WHAT TO EXPECT DURING FIRST POWER-UP

All CSACs have their output frequency re-centered prior to shipment. However, the shipment conditions will affect the absolute frequency offset when received by the end-user (temperature excursions, vibration, duration of transit, and so on). Therefore, some unknown frequency offset should be expected when the CSAC is first powered on by the user. Offsets may be corrected, as explained in the following section.

2.6 FREQUENCY STEERING

> **Note:** CSACdemo is a graphical interface used to communicate and for limited control of a CSAC. To display the functionality of CSAC, screen shots of CSACdemo are included in the sections that follow. For more information on CSACdemo, see **Section 4.6 "CSACdemo Operation"**. For full functionality and control of a CSAC, use of a hyperterminal or similar interface is the preferred method.

For external steering and/or calibration, the CSAC internal microwave synthesizer may be adjusted by the user through the `!F` command (see **Section 3.3.2 "Frequency Adjustment (F)"**). Steering values are entered in (integer) units of 1×10^{-15}, though

the resolution realized by the CSAC hardware is approximately 1×10^{-12}. Steering commands may be entered as either absolute steers (`!FA`) or as relative steers (`!FD`). In the case of an absolute steer, the contents of the steer register are replaced with the new value. In the case of a relative steer, the new value is summed with the existing value in the steer register. The maximum steer that can be entered in a single `!FD` command is $\pm 2 \times 10^{-8}$ ($\pm 20000000 \times 10^{-15}$). The maximum steer that can be entered in a single `!FA` command is approximately $\pm 2 \times 10^{-6}$ ($\pm 2000000000 \times 10^{-15}$). If a larger value is sent to the CSAC, the maximum allowed steer is applied.

CAUTION

It is recommended to limit steering commands to <±2 × 10^{-8} increments, to allow the CSAC to slowly adjust. A larger steer may cause the CSAC to unlock. Do not allow steering to accumulate beyond the stated data sheet limit.

To overcome the software limit ($\pm 2 \times 10^{-8}$) imposed by the `!FD` command, the latch command (`!FL`) will need to be employed (for more information, see **Section 2.6.1 "Frequency Calibration"**). Ultimately, the CSAC steering capability is physically limited by the TCXO tuning voltage. An alarm will trigger when this voltage is breached. Generally, steering the CSAC far from its nominal output frequency is undesirable as it will make disciplining difficult, therefore increasing the likelihood of unlock.

Note: Steering commands may be entered during acquisition (Status ≠ 0) but will not take effect until lock is achieved.

Frequency steering is volatile. Upon reboot, the CSAC returns to its nominal (calibrated) frequency setting. To update the non-volatile calibration, use the Frequency Latch command (**Section 3.3.2 "Frequency Adjustment (F)"**).

The current steering value appears in the telemetry string as `Steer`.

Note: Steer reports the actual hardware steering, in units of $\times 10^{-12}$, even though the software registers maintain resolution of $\times 10^{-15}$, so that many small relative corrections may be applied. As a result, the reported value may appear to disagree with the applied correction by one unit or so due to roundoff error. An example is provided in **Section 3.3.2 "Frequency Adjustment (F)"**.

To apply a frequency correction from the main panel of CSACdemo, select relative or absolute from the pull down menu and enter the desired steering into the Adjust field in $\times 10^{-15}$.

The following screen shot shows an example where an absolute correction of -100000×10^{-15} is entered. The correction is applied to the CSAC when **Apply** is selected.

© 2020-2021 Microchip Technology Inc.

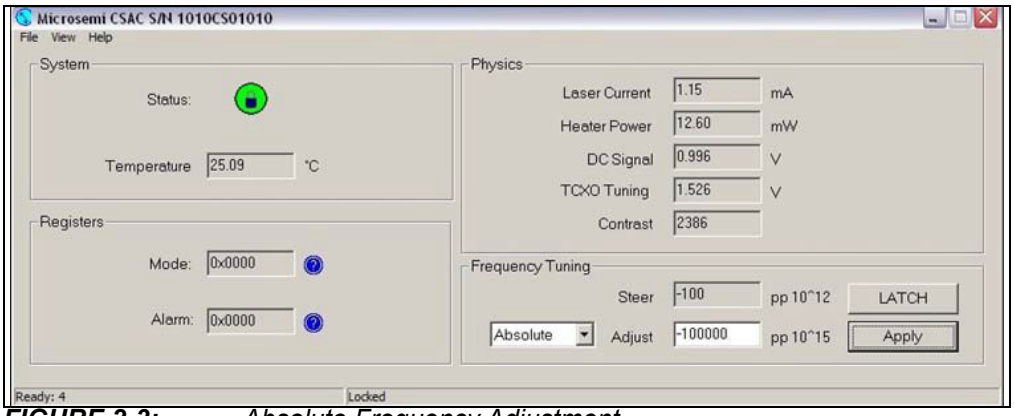


FIGURE 2-3: *Absolute Frequency Adjustment.*

As shown in the previous screen shot, after **Apply** is clicked, the correction is applied to the CSAC and the value of `Steer` changes (on the next polling update) to indicate the internal correction of -100×10^{-12}.

The following screen shot shows an example of relative frequency tuning after absolute steer is reset to 0. In this example, each time **Apply** is clicked, an additional correction of -100000×10^{-15} is applied to the CSAC. In this screen shot, **Apply** is clicked a total of four times. The resultant value of Steer is -400×10^{-12}.

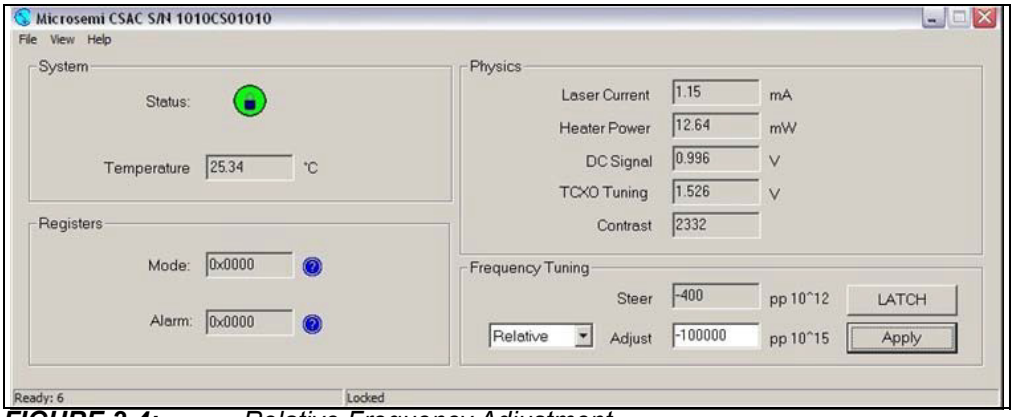


FIGURE 2-4: *Relative Frequency Adjustment.*

2.6.1 Frequency Calibration

The internal frequency calibration of the CSAC is set prior to shipment. It is sometimes desirable (and likely) that the calibration needs to be updated from time to time to remove cumulative frequency aging offsets.

Calibration of the CSAC is a two-step process. First, the CSAC is steered onto frequency, either through an external `!F` command (see **Section 2.6 "Frequency Steering"**), through 1PPS disciplining (see **Section 2.9 "1PPS Disciplining"**), or with analog tuning (see **Section 2.11 "Analog Tuning"**). Second, the present value of Steer is summed into the non-volatile calibration register through the Frequency Latch command (see **Section 3.3.2 "Frequency Adjustment (F)"**). Following a Latch command, the value of Steer is reset to zero.

Note:	The Latch command is only valid when the CSAC is locked (Status = 0).

To latch the current steer value to non-volatile storage from CSACdemo, click **LATCH**.

Note: It may be tempting, particularly in disciplining applications, to frequently latch the steering value into calibration in the event of unforeseen power outage. This is highly discouraged for the following reason. The lifetime of the CSAC's NV memory is finite; updating it >20,000 times will damage it and render the CSAC inoperable.

2.7 1PPS OUTPUT

A CMOS level 1 pulse-per-second (1PPS) output is available on pin 10 upon power-up. The output series impedance is 200Ω. The output driver circuit is similar to that of the RF output (see Figure 2-2). Nominal levels are 0VDC to 3.3VDC. For synchronization purposes, the on-time point is the rising edge of pin 10.

The 1PPS output is derived by digital division of the RF reference frequency. The frequency stability and accuracy of the 1PPS output reflects that of the RF output. Consequently, when unlocked (BITE = 1, status ≠ 0), the 1PPS stability reflects that of the free-running TCXO.

2.8 1PPS SYNCHRONIZATION

The 1PPS output is synchronous with one rising edge of the RF output (pin 12). The 1PPS output may be synchronized with a particular cycle of the RF by applying a synchronization pulse to pin 9. When synchronized, the counters are reset such that the 1PPS output occurs on the RF rising edge, which is nearest to the externally-applied rising edge. In this way, the CSAC 1PPS can be synchronized to within one clock cycle (±100 ns) of the external reference.

The CSAC provides two modes for 1PPS synchronization, Manual and Automatic, which are selected through a bit in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**).

Note: The configuration of the mode register is non-volatile (preserved across power cycles).

2.8.1 Manual Synchronization

In Manual Synchronization mode (default), the CSAC ignores any signal present on the 1PPS input line (pin 9) until commanded. When a synchronization command is received (see **Section 3.3.4 "1PPS Synchronization (S)"**), the CSAC 1PPS is synchronized to the next rising edge to appear on pin 9.

This mode is applicable to configurations where the CSAC is embedded in a system where a 1PPS signal is always present, but not always reliably accurate or stable (such as a GPS receiver). The host microprocessor may command the CSAC to synchronize after it has verified the state-of-health of the 1PPS reference source (for example, after querying lock state of the GPS receiver).

To perform manual synchronization from CSACdemo, open the **1PPS…** panel from the **View** menu. The 1PPS panel is shown in the following screen shot.

© 2020-2021 Microchip Technology Inc.

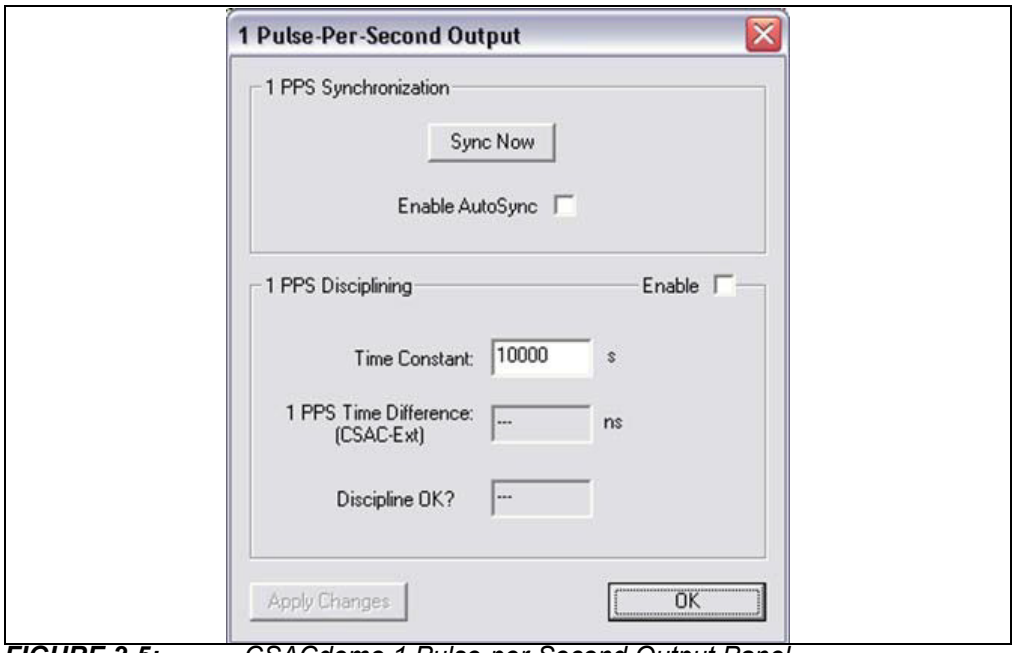


FIGURE 2-5: *CSACdemo 1 Pulse-per-Second Output Panel.*

To manually synchronize the CSAC from CSACdemo, make sure that a valid 1PPS reference is connected to the 1PPS reference input and click **Sync Now** on the 1PPS panel. The CSAC synchronizes to the next rising edge detected on the 1PPS reference input.

2.8.2 Automatic Synchronization

In Automatic Synchronization mode, the CSAC synchronizes its 1PPS output to every rising edge that appears on pin 9. In this mode, synchronization may be performed by connecting a reference 1PPS signal to pin 9 without needing to issue the synchronization command. Automatic synchronization can be enabled/disabled through bit 3 (0x0008) in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**).

This mode can be useful, for example, in cases where the host system does not communicate with the CSAC or in which the host system has no method or need to determine the state-of-health of the reference source.

Note:	Automatic Synchronization mode and Disciplining mode (see **Section 2.9 "1PPS Disciplining"**) are mutually exclusive. Enabling either in the mode register disables the other.

To enable Automatic Synchronization from CSACdemo, select the **Enable Autosync** checkbox on the 1PPS panel and click **Apply Changes** (see Figure 2-5).

2.9 1PPS DISCIPLINING

A high-resolution phase meter is implemented within the CSAC for improved synchronization (<100 ns) as well as for frequency calibration of the CSAC. The phase meter measures the time difference between the internal CSAC 1PPS (pin 10) and the externally applied reference 1PPS (pin 9). The phase meter measures the relative phase between the CSAC and the reference once per second with a resolution of 450 ps.

Based on the measurements of the phase meter, the disciplining algorithms adjust the CSAC's microwave synthesizer through the digital tuning value (`steer`, observed from the telemetry string). The algorithm will simultaneously steer both the phase and fre-

© 2020-2021 Microchip Technology Inc.

quency to that of the external reference, ultimately achieving accuracies of <5 ns and 5×10^{-13}, respectively. Note that, unlike the `!FA` and `!FD` commands, there is no software limitation upon the value of steer.

Disciplining can be enabled/disabled through bit 4 (0x0010) in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**). The time constant of the steering algorithm is user selectable through the ID command (see **Section 3.3.5 "Set 1PPS Disciplining Time Constant (D)"**).

> **Note:** Both mode setting and time constant are non-volatile, that is, preserved across power cycles.

Prior to the onset of steering, the disciplining algorithms first perform an initialization sequence in which the variables of the steering algorithm are reset to defaults and a 1PPS synchronization operation (see **Section 3.3.4 "1PPS Synchronization (S)"**) is executed to bring the 1PPS output within 100 ns of the reference. Initialization is performed when Disciplining is first enabled in the mode register and, in the case where Disciplining is already enabled after the CSAC achieves frequency lock (BITE = 0, status = 0).

In the event that the 1PPS reference is removed from pin 9 while Disciplining, the CSAC remains in holdover and preserves the most recent steering value. If the 1PPS reference subsequently reappears, Disciplining continues where it left off, without reinitializing. The notable exception to this is the case in which the CSAC 1PPS has drifted significantly in phase (>1 µs) from the reference 1PPS during the outage. In this case a synchronization is performed, though the Disciplining variables are not reinitialized.

If it is necessary to force re-initialization of the disciplining variables, perhaps because the reference source is deemed untrustworthy and subsequently recovers, this can be accomplished by disabling and re-enabling Disciplining in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**).

When Disciplining is enabled, the most recent phase meter measurement, rounded to the nearest nanosecond, is reported in the standard telemetry (see **Section 3.3.1 "Telemetry (6 and ^)"**). The sign of the reported value reflects the measurement of (1PPS_EXT–1PPS_CSAC), that is, if the CSAC 1PPS rising edge occurs after the external 1PPS rising edge, then the sign is negative.

The status of Disciplining is indicated by the `DiscOK` parameter in the telemetry. DiscOK = 0 upon startup. DiscOK = 1 when magnitude of phase measurement is less than phase threshold (see **Section 3.3.9 "Set 1PPS Phase Threshold for Discipline Status OK Check (m)"**) for two time constants of duration. DiscOK = 2 when in holdover (disciplining enabled but no 1PPS present).

> **Note:** Automatic Synchronization mode (see **Section 2.8.2 "Automatic Synchronization"**) and Disciplining mode are mutually exclusive. Enabling either in the mode register disables the other.

In CSACdemo, enabling/disabling Disciplining and setting the discipline time constant are both accomplished on the 1PPS panel, accessible from the View menu (See Figure 2-5). To modify the discipline time constant, enter the new value in the field (10–10000) and click **Apply Changes**.

2.9.1 Cable Length Compensation

The zero point of disciplining can be adjusted to accommodate cable and other instrumentation delays (or advances) which impact the arrival time of the 1PPS at the CSAC 1PPS input pin. The compensation value can optionally be stored in the CSAC non-volatile RAM for one-time calibration.

© 2020-2021 Microchip Technology Inc.

The maximum compensation adjustment is ±100 ns, with resolution of 100 ps. The compensation value is entered into the CSAC as a signed integer in units of 100 ps, where positive sign indicates phase advancement of the input 1PPS. For example, if there is 45 ns of delay (approximately 33 feet of RG-58 coaxial cable) between the on-time point and the CSAC 1PPS input then the compensation value would be +450.

Note: Cable length compensation can also be employed to correct for dynamic known errors in the 1PPS reference provided, for example, from an external measurement system. For this reason, upon application the compensation is subsequently applied to the previous 1PPS measurement.

Note: Compensation is implemented in the disciplining algorithm, not in the phase measurement itself. The phase measurement, as reported through telemetry, reports the actual phase measurement, that is, if the CSAC is disciplined with +50 ns of compensation, the phase meter reports –50 ns of phase error.

Compensation is set with the `!DC` command (see **Section 3.3.6 “Set 1PPS Disciplining Cable Length Compensation (DC)”**).

2.10 TIME-OF-DAY

The CSAC maintains time-of-day (TOD) as a 32-bit unsigned integer, which is incremented synchronously with the rising edge of the 1PPS output. Until set otherwise, TOD begins counting from zero when the CSAC is powered on.

TOD is retrieved from the CSAC with the `!T?` command (see **Section 3.3.8 “Time-of-Day (TOD)”**). When the `!T?` command is received, the CSAC waits for the next rising edge of 1PPS before replying with the TOD of the current epoch, that is, if the command is received during epoch N, then the reply N+1 appears immediately following the next 1PPS. This strategy provides the host system with minimum ambiguity in interpreting the response.

TOD can be set with the `!T` command. The `!T` command includes provision both for setting an absolute number or for a differential (±) adjustment of the present TOD. An example is provided in the Time-of-Day section. To avoid ambiguity in setting the TOD, it is recommended that the host system wait for 1PPS and transmit the setting/adjustment immediately thereafter.

The CSACdemo program shows TOD on the Time Of Day panel, accessed from the View menu, as shown in the following screen shot.

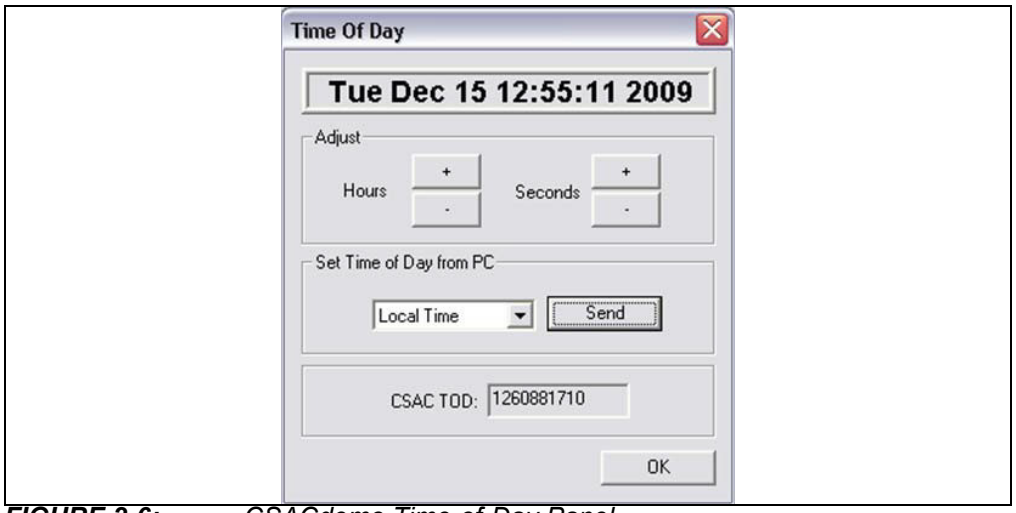


FIGURE 2-6: *CSACdemo Time-of-Day Panel.*

The raw CSAC TOD value is shown in the lower field of the panel (here 1260881710). The upper display of the TOD panel realizes the timekeeping convention of the C programming language (in UNIX and Microsoft Windows), which counts time in seconds from midnight on January 1, 1970. Upon clicking **Send**, it sets the CSAC time according to the host PC's TOD counter (either local time or UTC depending on the setting of the pull-down menu to the left of the **Send**). The + and - buttons for hours and seconds adjustment will increment or decrement the CSAC TOD by ±3600 or ±1 second respectively.

2.11 ANALOG TUNING

To enable analog frequency tuning for implementation in legacy (quartz crystal) applications, the frequency of the CSAC can be tuned with an external voltage applied to pin 1. This functionality can be enabled/disabled through a bit in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**). The applied voltage is digitized by an internal analog-to-digital converter and the correction is applied to the microwave synthesizer at a rate of once per second, that is, the maximum tuning rate is 1 Hz.

When analog tuning is enabled, the voltage applied at pin 1 and the resultant steering are reported in the standard telemetry stream (see **Section 3.3.1 "Telemetry (6 and ^)"**). The tuning voltage input range is 0VDC to 2.5VDC, which corresponds to a full scale tuning range of 4.4×10^{-8}. Nominal zero-correction tuning occurs at a tuning input voltage of 1250 mV. The fractional frequency correction, for a given applied voltage, is given by the following equation.

EQUATION 2-1:

$$\Delta f/f = (V_{TUNE} - 1250\text{mV}) \times 1.77 \times 10^{-11}/(\text{mV})$$

Note: This formula is accurate for the standard CSAC, operating at 10.0 MHz output frequency. Consult the data sheet for tuning curves of CSACs at alternate frequencies. The tuning input pin is nominally biased at ≈1250 mV, that is, approximately zero correction.

© 2020-2021 Microchip Technology Inc.

Note: Bias voltage may vary due to component variations and/or exhibit temperature sensitivity. Therefore, analog tuning should not be enabled unless the functionality is necessary and the analog tuning input pin is connected to a low noise, low impedance voltage source. For non-legacy applications, it is recommended that this feature remain disabled, and that corrections be applied through the digital communications interface (see **Section 2.6 "Frequency Steering"**) to avoid degradation of the CSAC short-term stability due to voltage noise applied to the tuning pin.

Analog tuning can be enabled/disabled and monitored from the CSACdemo application from the **Analog Tuning…** panel (accessible from the View menu), as shown in the following screen shot.



FIGURE 2-7: *CSACdemo Analog Tuning Panel.*

When analog tuning is enabled, the voltage present on pin 1 is displayed in the Analog Tuning field and also reflected in the current reported value of steer on the main panel. To enable or disable analog tuning, select **Enable Analog Tuning** checkbox and click **Apply Changes**.

2.12 ULTRA-LOW POWER OPERATING MODE

The majority of the power in the CSAC is consumed by the physics package and microwave synthesizer. In ultra-low power (ULP) mode, the physics package and synthesizer can be disabled for a user-specified length of time, during which the CSAC operates as a free-running TCXO. Periodically, the atomic clock portion of the CSAC is powered on (again for a user-specified amount of time) and the TCXO is re-calibrated to the atomic frequency. Operating in this mode, the CSAC exhibits the short-term performance of a TCXO with good long-term frequency stability at significantly lower power compared to standard mode. For example, if the atomic clock portion is only powered on for 5 minutes out of every hour (2 minutes for lock acquisition + 3 minutes of run time), then the time-averaged power of the CSAC may be <30 mW.

Between calibration cycles, the CSAC in ULP mode exhibits the performance characteristics of a free-running TCXO and therefore exhibits significantly higher short-term frequency drift and environmental (temperature and vibration) sensitivity than a normally operating CSAC. Furthermore, whenever the CSAC wakes, it essentially re-acquires atomic-lock, which will induce a phase timing error of unknown magnitude on the 1PPS and RF outputs. For this reason, ULP mode is principally recommended only for applications that:

- Require long-term frequency stability during wake periods, rather than short-term frequency or time stability.
- Have a very stable environment (temperature and vibration).

© 2020-2021 Microchip Technology Inc.

Note: Due to the unique behavior and configurability of ULP, the data sheet performance specifications for the CSAC cannot be guaranteed while in ULP mode. The CSAC has short-term drift performance of a low-cost, low-performance TCXO. Contact Microchip for additional assistance in evaluating and optimizing ULP for your specific application.

The following illustration shows an example of a CSAC operating in ULP mode, with wake-time = 300 seconds (5 min.) and sleep-time = 3300 seconds (55 min.).

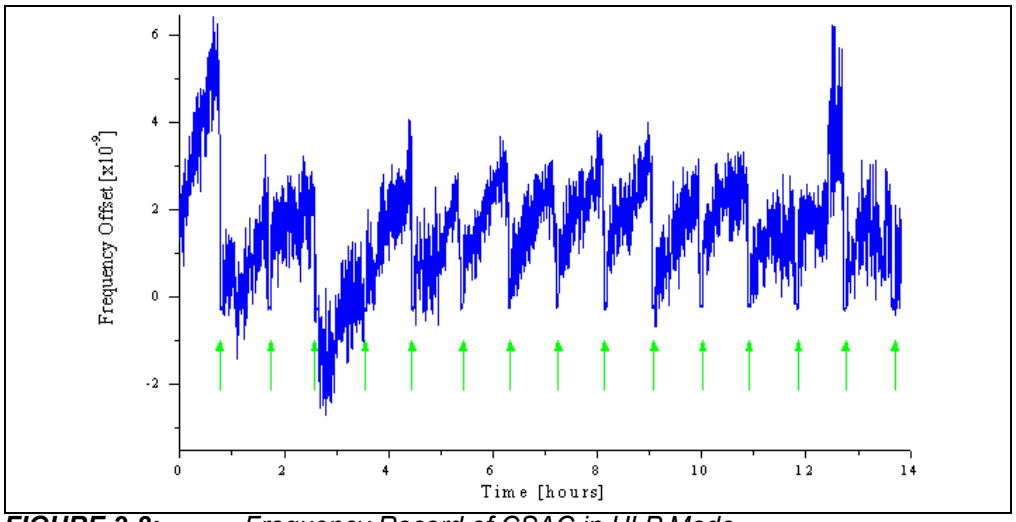


FIGURE 2-8: *Frequency Record of CSAC in ULP Mode.*

The green arrows indicate the on time calibrations. Note the relatively poor TCXO drift and temperature behavior between calibrations.

ULP is an unusual operating mode for an atomic clock and it is important for the user to understand exactly how the clock is behaving to effectively implement this feature in a system. In particular, note the following:

- When operating in ULP mode, the Status register indicates Status = 9 (asleep) when the atomic clock portion of the CSAC is asleep. Each wake cycle is indicated by the usual lock process (Status = 8, 7, 6,…) followed by wake-time seconds of operation at Status = 0 before the cycle repeats. This cycle is also reflected on the BITE pin, which is 1 (high) whenever the CSAC is unlocked (or asleep) and only 0 (low) during the locked periods.
- When using Disciplining (see **Section 2.9 "1PPS Disciplining"**) in conjunction with ULP, disciplining functionality is disabled during sleep and unlocked cycles, though steering information is preserved and updated across wake cycles.
- Frequency Steering commands may be entered when the CSAC is asleep or unlocked but do not affect the output frequency until lock is achieved, typically on the next wake cycle (see **Section 2.6 "Frequency Steering"**). Also, the Latch command is only valid when the CSAC is locked (Status = 0).
- If enabled, Analog Tuning (see **Section 2.11 "Analog Tuning"**) is only active during wake cycles.

ULP is enabled through bit 5 (0x0020) in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**) and the sleep-time and wake-time are set by the `!U` command (see **Section 3.3.7 "Set Ultra-Low Power Mode Parameters (U)"**). These values are non-volatile; they persist across power cycles. Note that the wake-time begins counting after the CSAC achieves lock, so the actual time that

© 2020-2021 Microchip Technology Inc.

the atomic clock portion of the CSAC is powered on is the sum of the time to lock and the user-configured wake-time. The minimum allowed values of wake-time and sleep-time are 10 seconds and 1800 seconds, respectively.

To configure ULP parameters using CSACdemo, select **Ultra-Low Power Mode** from the View menu to access the panel shown in the following screen shot.



FIGURE 2-9: *CSACdemo Ultra-Low Power Mode Configuration Panel.*

Enter the desired settings and click **Apply Changes** to upload new settings to the CSAC.

2.13 1PPS PHASE MEASUREMENT MODE

For firmware versions 1.08 and later, an additional phase meter is implemented with extended range (±500 ms) to measure the time difference between the internal CSAC 1PPS (pin 10) and the externally applied reference 1PPS (pin 9). Measurement resolution is approximately 100 ns.

> **Note:** 1PPS phase measurement mode utilizes both the extended-range phase meter and the high-resolution phase meter (450 ps resolution) used in 1PPS Disciplining (see **Section 2.9 "1PPS Disciplining"**). In this mode, the phase measured by the high-resolution meter is reported if phase is in the range ±1 µs (approximate), otherwise the extended-range meter is reported.

Phase measurement mode may be enabled/disabled through bit 2 (0x0004) in the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**). Phase Measurement mode, Automatic Synchronization, and Disciplining are all mutually exclusive, so enabling a 1PPS-related option in the mode register disables the other 1PPS-related options.

© 2020-2021 Microchip Technology Inc.

NOTES:

© 2020-2021 Microchip Technology Inc.

Chapter 3. Programmer's Reference

Pins 5 and 6 provide a serial interface for communication with the CSAC. The protocol is fundamentally similar to RS-232, with the exception that the voltage levels are CMOS (0V to V_{CC}), rather than ±12V.

The data rate and word structures are as follows:

- 57,600 Baud
- 8 data bits
- No parity
- 1 stop bit (8-N-1)
- No flow control

For interfacing with a standard RS-232 controller interface, which requires ±12V logic levels, an external level shifter must be employed, such as the Maxim MAX202 employed on the evaluation board (see **Section 5.4 "Notes on the Evaluation Board"**).

3.1 OVERVIEW OF TELEMETRY INTERFACE

The CSAC communicates exclusively with printable (non-binary) ASCII characters.

In general, commands are to be preceded by an exclamation point (`!`) and followed by a carriage-return /linefeed `[CRLF]` pair (ASCII 0x0D 0x0A). For convenience and efficiency, most commands also provide a single-character shortcut, which is executed immediately, that is without bracketing by `!` and `[CRLF]`. For example, the single character shortcut `^` is functionally identical to `!^[CRLF]`.

After transmitting `!` but prior to sending `[CRLF]`, a command may be aborted by sending the escape character (ASCII 0x1B).

All commands produce a response from the CSAC, which are human readable, with individual lines ending in `[CRLF]`. If an unsupported or improperly formatted command is received, the CSAC responds with `?[CRLF]`.

3.1.1 Checksum (Error-Checking Option for Telemetry Interface Communications)

For improved communications reliability, an NMEA-style checksum may be enabled through bit 6 (0x0040) of the mode register (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**). When enabled, the checksum is required for all input commands and is present on all replies from the CSAC.

The checksum is a two-byte ASCII representation (in hexadecimal) of the XOR of all characters in the command between—but not including—the `!` and the `[CRLF]` characters. The checksum is preceded by a `*` character and appended to the command immediately prior to the `[CRLF]`. Because commands including checksum are inherently multi-character, single-character shortcuts are not available when checksum is enabled.

Example (enable analog tuning through mode register):

Command: `!MA*0C[CRLF]`

Unit response: `0x0041*4D[CRLF]`

© 2020-2021 Microchip Technology Inc.

Example (disable checksum through mode register)

Command: `!Mc*2E[CRLF]`

Unit response: `0x0000[CRLF]`

If the checksum is not present or if the checksum value is invalid, then the command is not executed and the CSAC responds with `*[CRLF]`.

Example (malformed checksum):

Command: `!Mc*2D[CRLF]`

Unit response: `*[CRLF]`

To experiment with checksum in CSACdemo and observe the calculated checksums in the Trace window, select **Require Cksum** checkbox on the **Options…** panel, as shown in the following screen shot.

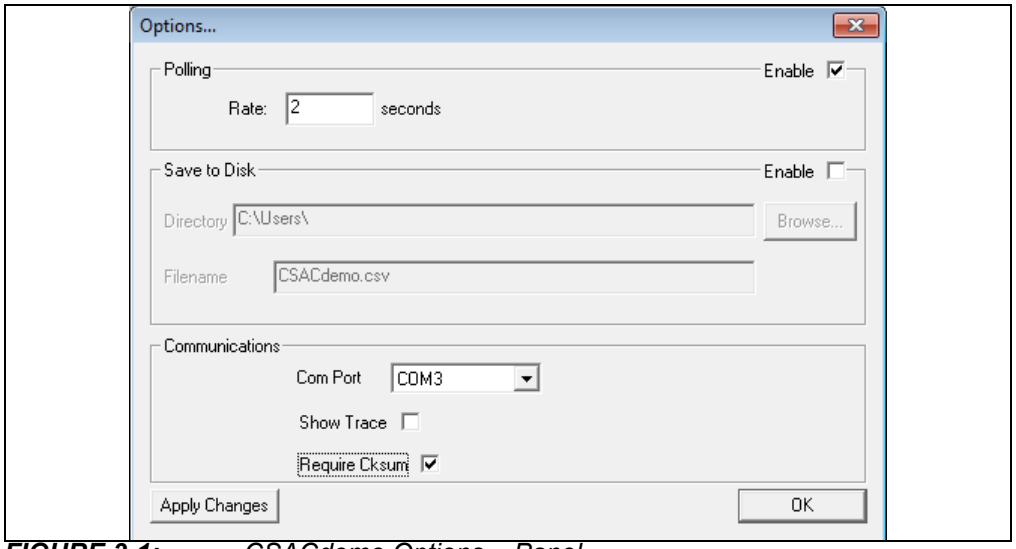


FIGURE 3-1: *CSACdemo Options... Panel.*

3.1.2 How to Calculate the Checksum

Checksum value is a two digit hexadecimal representation of the logical XOR of each character in the command (excluding "`!`" and "`[CRLF]`"). For example, if one wants to implement analog tuning by sending the `!MA[CRLF]` command, then they should send `!MA*0C [CRLF]` in Checksum mode. In the following table, we convert `M` and `A` to their binary equivalents and calculate the XOR in the bottom row. The corresponding hexadecimal value of that XOR is "`C`". Therefore the two-digit Checksum is "`0C`".

TABLE 3-1: CHECKSUM CALCULATION EXAMPLE

Checksum Component	ASCII Character	Binary Value	Hex Value
Input Command Characters	M	1001101	—
	A	1000001	—
Logical XOR	—	0001100	C

3.2 COMMAND SUMMARY

The following table summarizes the CSAC commands.

> **Note:** The `m` and `>` commands are only available for firmware versions 1.08 and later.

© 2020-2021 Microchip Technology Inc.

TABLE 3-2: COMMAND SUMMARY

Shortcut	Description	Command	Reference Section
6	Return telemetry headers as comma-delimited string.	!6[CRLF]	**Section 3.3.1 "Telemetry (6 and ^)"**
^	Return telemetry as comma-delimited string.	!^[CRLF]	**Section 3.3.1 "Telemetry (6 and ^)"**
F	Set/report frequency adjustment.	!F?[CRLF]	**Section 3.3.2 "Frequency Adjustment (F)"**
M	Set/report operating mode register bits.	!M?[CRLF]	**Section 3.3.3 "Set/Clear Operating Modes (M)"**
S	Sync CSAC 1PPS to external 1PPS.	!S[CRLF]	**Section 3.3.4 "1PPS Synchronization (S)"**
D	Set/report 1PPS disciplining time constant.	!D?[CRLF]	**Section 3.3.5 "Set 1PPS Disciplining Time Constant (D)"**
U	Set/report ultra-low power mode parameters.	!U?[CRLF]	**Section 3.3.7 "Set Ultra-Low Power Mode Parameters (U)"**
T	Set/report time-of-day.	!T?[CRLF]	**Section 3.3.8 "Time-of-Day (TOD)"**
m	Set/report 1PPS phase threshold for discipline status OK check.	!m?[CRLF]	**Section 3.3.9 "Set 1PPS Phase Threshold for Discipline Status OK Check (m)"**
>	Set/report 1PPS Out Pulse width as multiple of default width.	!>?[CRLF]	**Section 3.3.10 "Set 1PPS Out Pulse Width as an Integer Multiple of Default Width (>)"**
@	Set/report deferred command.	!@?[CRLF]	**Section 3.3.11 "Deferred Command (@)"**
?	Help.	!?[CRLF]	**Section 3.3.12 "Help (?)"**

3.3 DETAILED COMMAND DESCRIPTIONS

The following are descriptions of the CSAC's commands.

3.3.1 Telemetry (6 and ^)

CSAC supports two commands, `!6` and `!^`, to retrieve the telemetry headers and values, respectively. Both responses are comma-delimited strings, suitable for importing into spreadsheet programs.

Example:

Telemetry headers command: `!6[CRLF]`

Unit response: `Status,Alarm,SN,Mode,Contrast,`
`LaserI,TCXO,HeatP,Sig,Temp,Steer,ATune,Phase,DiscOK,`
`TOD,LTime,Ver[CRLF]`

Example:

Telemetry data command: `!^[CRLF]`

Unit response:
`0,0x0000,1209CS00909,0x0010,4381,0.86,1.573,17.62,0.996,28.26,-24,---,-1,1,1268126502,586969,1.0[CRLF]`

The maximum length of a telemetry string is 135 characters.

Note: The single-characters `6` and `^` are shortcuts for `!6[CRLF]` and `!^[CRLF]`, respectively.

The following table lists the telemetry parameters and their associated header identifiers.

TABLE 3-3: TELEMETRY PARAMETERS (FIRMWARE VERSION 1.09)

Identifier	Description	Notes	String Length
Status	Unit status	See Note 1 and Table 3-4	Up to 2 decimal digits (2 characters)
Alarm	Pending unit alarms	See Note 2 and Table 3-5	"0x" + 4 hexadecimal digits (6 characters max)
SN	Unit serial number	See Note 3	11 characters
Mode	Mode of operation	See Table 3-6	"0x" + 4 hexadecimal digits (6 characters max)
Contrast	Indication of signal level	Typically >2000 when locked, and ≈ 0 when unlocked	32 bits unsigned (10 characters max)
LaserI	Laser current (mA)	Typically 0.6 mA to 1.3 mA	16 bits unsigned + "." + 2 digits precision (8 characters max)
TCXO	Tuning voltage (V)	0VDC to 2.5VDC tuning range ≈ $\pm 10 \times 10^{6}$	16 bits unsigned + "." + 3 digits precision (9 characters max)
HeatP	Physics package heater power (mW)	Typical 6 mW to 20 mW under normal operating conditions and 25°C ambient	16 bits unsigned + "." + 2 digits precision (8 characters max)
Sig	DC signal level (V)	Typical 0.8V to 1.7V under normal operating conditions	16 bits unsigned + "." + 3 digits precision (9 characters max)
Temp	Unit temperature (°C)	Absolute accuracy is ±2°C	16 bits unsigned + "." + 2 digits precision (8 characters max)
Steer	Frequency adjust	In $\times 10^{-12}$ resolution	32 bits signed (11 characters max)
ATune	Analog tuning voltage input	--- when analog tuning is disabled, 0V to 2.5V when enabled	16 bits unsigned + "." + 3 digits precision (9 characters max)
Phase	Difference between CSAC and external 1PPS (ns)	Only present if discipline or phase-measure mode enabled, otherwise --- or NEEDREFPPS	16 bits signed (6 characters max)
DiscOK	Discipline status (0-2)	0 = acquiring, 1 = locked, 2 = holdover when disciplining enabled, otherwise ---	"0", "1", "2" or "---" (3 characters max)
TOD	Time (seconds)	Starts at 0 upon power-up unless set by command	32 bits unsigned (10 characters max)
LTime	Time since lock (seconds)	Starts at 0 upon lock	31 bits unsigned (10 characters max)
FWver	Firmware version	Two digit number M.m where M is major revision and m is minor revision	"1.09" (4 characters, may be longer in future firmware)

Note 1: Status reflects the steps of the clock initialization process. It starts at 8 on boot and decreases to 0 as acquisition proceeds. When Status ≠ 0, BITE = 1. When Status = 0, BITE = 0.

2: Alarms indicate detection of anomalous operating conditions while locked. Alarm is the logical OR of all pending alarms, as shown in the following table. An alarm will not persist if the condition is fixed or if the unit is reset.

3: CSAC serial numbers are of the form YYMMCSXXXXX where YYMM is the year and month of production and XXXXX is the serialized production unit number.

© 2020-2021 Microchip Technology Inc.

TABLE 3-4: STATUS CODES OF CSAC

Status	Acquisition Stage
9	Asleep (ULP mode only).
8	Initial warm-up.
7	Heater equilibration.
6	Microwave power acquisition.
5	Laser current acquisition.
4	Laser power acquisition.
3	Microwave frequency acquisition.
2	Microwave frequency stabilization.
1	Microwave frequency steering.
0	Locked.

Note: If CSAC returns a status code other than shown in Table 3-4, then it is re-acquiring its set points. In this case, warm-up time takes longer than stated on the CSAC SA.45s data sheet. To avoid this, it is recommended to always allow CSAC to remain powered on for >102 seconds after it acquires LOCK. 102 seconds is the minimum amount of time necessary to save CSAC set points to memory, thus avoiding set-point re-acquisition upon its next power up.

TABLE 3-5: ALARM CODES OF CSAC

Alarm	Definition	Alarm Limit
0x0001	Signal contrast low.	Contrast <1000
0x0002	Synthesizer tuning at limit.	Synthesizer detuned from calibration by >30 kHz or <–15 kHz
0x0004	Temperature bridge unbalanced.	Bridge—set-point >±20 mV
0x0010	DC light level low. (Note 1)	Set-point—DCL > 0.1V
0x0020	DC light level high. (Note 1)	DCL—set-point > 0.1V
0x0040	Heater voltage low.	<30 mV
0x0080	Heater voltage high.	>2.48V
0x0100	µW power control low.	<20 mV
0x0200	µW power control high.	>2.48V
0x0400	TCXO control voltage low.	<0.1V
0x0800	TCXO control voltage high.	>2.4V
0x1000	Laser current low.	<0.5 mA
0x2000	Laser current high.	>2.3 mA
0x4000	Stack overflow (firmware error).	—

Note 1: Alarms are intended to indicate the detection of potentially anomalous operating conditions. Alarms codes 0x0010 and 0x0020 may occur momentarily, but do not by themselves indicate a problem and can be ignored by the user. These alarms are intended for factory troubleshooting of failures to acquire lock or loss of lock.

3.3.2 Frequency Adjustment (F)

The output frequency of the CSAC may be adjusted (steered) through the communications port. The internal resolution of the fractional frequency correction is approximately 1×10^{-12}. The correction is entered in integer units of $\times 10^{-15}$. The maximum allowed correction in a single `!FD` command is ±20000000 (2×10^{-8}). The maximum allowed correction in a single `!FA` command is approximately ±2000000000 (2×10^{-6}). Correc-

tions may be applied as either Absolute or Relative, depending on the first character following the !F, that is !FA or !FD for absolute or relative (delta) respectively. In the case of absolute steering, the value of the Steer register is replaced with the new value. In the case of relative (delta) steering, the new value is summed with the existing value in the Steer register, that is, two relative corrections of –10000 result in a total offset of $–2 \times 10^{–11}$. The current steering value is reported in the steer field of the telemetry in units of $\times 10^{–12}$.

The format for the Adjust frequency command is !FYXXXXX[CRLF] where Y is either A or D and XXXXX is the new correction in $\times 10^{–15}$.

Example: Apply absolute tuning correction of $–1.23 \times 10^{–10}$:

Command: !FA-123000[CRLF]

Unit response: Steer = -123[CRLF]

Example: Apply delta tuning correction of $–1.23 \times 10^{–10}$:

Command: !FD-123000[CRLF]

Unit response: Steer = -246[CRLF]

Example: Report current value of steer:

Command: !F?[CRLF]

Unit response: Steer = -246[CRLF]

Note: That the single-character F is a shortcut for !F?[CRLF].

The contents of the Steer register are volatile, that is, the Steer is reset to 0 when power is cycled to the CSAC. In many cases, it is desirable to preserve the steer upon power-down (for example, calibration of the CSAC). This is accomplished by sending a Frequency Latch command to the CSAC, which updates the internal calibration (stored in non-volatile memory) according to the current value of the Steer register and resets Steer to zero. Note that the Latch command is only valid when the CSAC is locked (Status = 0).

Example: Latch the current steer value:

Command: !FL[CRLF]

Unit response: Steer Latched [CRLF] Steer = 0[CRLF]

Once a Latch command is issued, the previously latched value cannot be recovered. There is no command to restore "factory defaults".

Note: The frequency steering command (!F) is recommended for real-time disciplining of CSACs, but the value should not be latched (!FL) on every steer due to the physical limit on the number of times the non-volatile memory may be written before damage (20,000). For example, if an !FL command was applied to the CSAC, accompanying a steer (!F), at a rate of 1/sec, the CSAC may experience operational failure within 8 hours.

3.3.3 Set/Clear Operating Modes (M)

Operating modes of the CSAC are enabled/disabled by individual bits in the mode register. The !M command provides access to set/clear each of the bits independently. The mode register is non-volatile; settings persist across power cycles.

The unit responds by reporting the current value of the mode register in hexadecimal. Each bit in the mode register is associated with enabling/disabling a particular operating mode. The bit assignments are shown in the following table.

© 2020-2021 Microchip Technology Inc.

TABLE 3-6: OPERATING MODES OF CSAC

Enable Bit Assignment	Enable Arguments to !M_	Definition	Disable Argument to !M_
0x0001	A	Analog tuning.	a
0x0002	—	Reserved.	—
0x0004	M	1PPS phase measurement (only available on firmware versions 1.08 and later).	m
0x0008	S	1PPS auto-sync.	s
0x0010	D	Discipline.	d
0x0020	U	Ultra-Low Power mode.	u
0x0040	C	Require checksum on ! command.	c
0x0080	—	Reserved.	—
—	?	Report current settings.	—

Example: Enable and then Disable analog tuning:

Command: `!MA[CRLF]`

Unit response: `0x0001[CRLF]`

Command: `!Ma[CRLF]`

Unit response: `0x0000[CRLF]`

The current value of the mode register is returned in the standard telemetry query (see **Section 3.3.1 "Telemetry (6 and ^)"**) or may be queried independently with the `!M?` command.

Example: Query mode register:

Command: `!M?[CRLF]`

Response: `0x0001[CRLF]`

Note: That the single-character `M` is a shortcut for `!M?[CRLF]`.

Autosync mode, Discipline mode, and Phase Measurement mode (if mode available in the firmware version) are mutually exclusive. Setting a 1PPS-related option automatically disables the other 1PPS-related options.

3.3.4 1PPS Synchronization (S)

To synchronize the 1PPS output (pin 10) to an externally applied 1PPS synchronization input (pin 9), connect the external 1PPS signal to pin 9 and send the `!S` command. The rising edge of the 1PPS output will synchronize to within ±100 ns (approximately) of the next rising edge of the 1PPS input. If a valid 1PPS input does not appear at the 1PPS input within 3 seconds, the operation is aborted and an error is returned.

Example: Synchronize 1PPS:

Command: `!S[CRLF]`

Unit response: `S[CRLF]`

or: `E[CRLF]`

The unit response (S or E) occurs after either successful synchronization or 3-second timeout. This permits the host system to verify successful synchronization.

Note: The single-character `S` is a shortcut for `!S[CRLF]`.

3.3.5 Set 1PPS Disciplining Time Constant (D)

The time constant for disciplining to an externally supplied 1PPS reference source may be selected to provide optimal performance in a given application (see **Section 5.1 "The Art of Disciplining"**).

The time constant can range between 10 to 10000 seconds. The 1PPS disciplining time constant is set with the `!D` command. The format for setting the time constant is `!DX[CRLF]` where X is the new time constant in seconds.

Example: Set disciplining time constant to 80 seconds:

Command: `!D80[CRLF]`

Response: `80[CRLF]`

To query the current time constant setting, without modifying the value, use the command `!D?`

Example: Query current disciplining time constant:

Command: `!D?[CRLF]`

Response: `80[CRLF]`

Note: The single-character `D` is a shortcut for `!D?[CRLF]`.

3.3.6 Set 1PPS Disciplining Cable Length Compensation (DC)

Cable length compensation can be applied to allow for known delay (or advance) in the arrival time of the reference 1PPS at the CSAC (see **Section 2.9.1 "Cable Length Compensation"**). Cable length compensation is represented as a signed integer in units of 100 ps, with a maximum value of ±1000 (100 ns).

The sign of the compensation is such that a positive value reflects known delay in the arrival time of the 1PPS. For instance, 33 feet of RG-58 cable requires compensation of +45 ns.

The format for setting the cable length compensation value is `!DCX[CRLF]` where X is the new compensation value.

Example: Set cable length compensation to +15 nanoseconds:

Command: `!DC150[CRLF]`

Response: `150[CRLF]`

To query the current compensation setting, without modifying the value, use the command `!DC?`

Example: Query current compensation setting:

Command: `!DC?[CRLF]`

Response: `150[CRLF]`

To store the current compensation setting in non-volatile RAM, use the command `!DCL`

Example: Latch current value of compensation to power-up default:

Command: `!DCL[CRLF]`

Response: `Phase comp latched[CRLF]`

© 2020-2021 Microchip Technology Inc.

3.3.7 Set Ultra-Low Power Mode Parameters (U)

> **Note:** Placing the CSAC in ULP mode results in short-term drift performance of its internal TCXO.

The ultra-low power operating mode is defined by two parameters, Sleep-Time and Wake-Time, which may be set with the `!U` command in this format: `!USSS,WWW[CRLF]` where SSS is the sleep time in seconds and WWW is the wake time in seconds.

Example: Set sleep time = 55 minutes, wake time = 5 minutes:

Command: `!U3300,300[CRLF]`

Response: `3300,300[CRLF]`

The allowed ranges of Sleep-Time and Wake-Time are 1800 seconds to 65535 seconds and 10 seconds to –65535 seconds, respectively.

To query the ULP settings without modifying their values, use the command `!U?`.

Example: Query current ULP settings:

Command: `!U?[CRLF]`

Response: `3300,300[CRLF]`

> **Note:** The single-character `U` is a shortcut for `!U?[CRLF]`.

3.3.8 Time-of-Day (TOD)

TOD is maintained internally within the CSAC, represented by a single unsigned long integer value, which begins counting up from 0 when the CSAC is powered on. The TOD is synchronized with the 1PPS output. TOD is routinely transmitted in the telemetry string (see **Section 3.3.1 "Telemetry (6 and ^)"**).

TOD may be set externally with the `!T` command in this format: `!TYXXXX[CRLF]` where Y is either A for absolute setting or D for a delta adjustment of TOD and XXXX is either the unsigned integer TOD (typically either UNIX/Windows time or GPS time) or a signed integer adjustment to the TOD.

Example: Absolute setting TOD to 1221578499:

Command: `!TA1221578499[CRLF]`

Unit response: `TimeOfDay = 1221578499[CRLF]`

Example: Retard TOD by 3600 seconds = 1 hour:

Command: `!TD-3600[CRLF]`

Unit response: `TimeOfDay = 1221574902[CRLF]`

The TOD may be reported synchronous with the 1PPS output:

Example: Retrieve TOD command:

Command: `!T?[CRLF]`

Unit Response: `XXXX[CRLF]` where XXXX is the current TOD.

> **Note:** This response does not occur until the next 1PPS output pulse.

When queried with the `!T?` command, the first character of TOD appears on the communications port within 20 ms of the rising edge of the next 1PPS output pulse. Because this necessarily creates a delay of up to a second between sending the `!T?` command and receiving a response from the CSAC, the host system must allow for an

RS-232 receive timeout of at least 1000 ms when anticipating a response to the `!T?` command. For less critical timing applications, the TOD can be somewhat ambiguously parsed from the standard telemetry string (see **Section 3.3.1 "Telemetry (6 and ^)"**).

> **Note:** The single-character `T` is a shortcut for `!T?[CRLF]`.

3.3.9 Set 1PPS Phase Threshold for Discipline Status OK Check (m)

The 1PPS phase threshold (for discipline status OK check) when disciplining to an externally supplied 1PPS reference source may be configured to provide optimal performance in a given application.

For applications with a long disciplining time constant and a noisier 1PPS reference (such as GPS), there could be large variations in the reported 1PPS phase of a CSAC disciplined ok (checked through ADEV measurement) but the phase threshold being set to a larger value ensures the DiscOK = 1 indication is set correctly (see **Section 2.9 "1PPS Disciplining"**).

For applications with a short disciplining time constant, the phase threshold can be set to a smaller value. The range of 1PPS Phase Threshold for Discipline Status OK Check is 1 nanosecond to 10^9 nanoseconds (absolute values), with a default of 20 nanoseconds.

To set the phase threshold (for Discipline Status OK Check), the command has this format: `!mX[CRLF]` where X is the new phase threshold's magnitude/absolute value in nanoseconds.

Example: Set 1PPS phase threshold for discipline status OK Check to ±20 nanoseconds:

Command: `!m20[CRLF]`

Response: `20[CRLF]`

To query the 1PPS phase threshold setting, without modifying the values, use the command `!m?`.

Example: Query current 1PPS Phase Threshold setting:

Command: `!m?[CRLF]`

Response: `20[CRLF]`

> **Note:** The single-character `m` is a shortcut for `!m?[CRLF]`.

3.3.10 Set 1PPS Out Pulse Width as an Integer Multiple of Default Width (>)

CSAC's 1PPS output (pin 10) has a default pulse width that may not be sufficiently long for certain applications. In such cases, the pulse width can be set to an integer times the default pulse width by using the `!>` command with this format: `!>X[CRLF]` where X is the unsigned integer used as a multiple of the default 1PPS Out Pulse Width to set the desired 1PPS Out's Pulse Width.

The allowed range of 1PPS Out Pulse Width integer multiple of default Pulse Width is from 1 to 4.

Example: Set 1PPS Out Pulse Width as a 2x multiple of default Pulse Width:

Command: `!>2[CRLF]`

Response: `PPS Pulse Width = 2 times ~100 usec [CRLF]`

© 2020-2021 Microchip Technology Inc.

Note: The default pulse width is dependent on the selected frequency option for RF output (pin 12).

When RF output frequency of 10 MHz (option 001) is selected, then the 1PPS out pulse width default is ~100 microseconds, while for other RF output frequency option's the 1PPS out pulse width is as specified in the data sheet.

To query the 1PPS Out Pulse Width setting, without modifying the values, use the command `!>?`.

Example: Query current 1PPS Out Pulse Width setting:

Command: `!>?[CRLF]`

Response: `PPS Pulse Width = 4 times ~100 usec[CRLF]`

Note: The single-character `>` is a shortcut for `!>?[CRLF]`.

3.3.11 Deferred Command (@)

Any command can be sent at a deferred time by using the `!@` command with this format:

`!T@XXXX,YYYY[CRLF]` where XXXX is the deferred time in seconds and YYYY is the command that is sent after the deferred time.

Example: Defer sending the 6 command by 10 seconds:

Command: `!@10,6[CRLF]`

Unit response: `Deferred = 10,6`

Unit response (after 10 seconds): `Status,Alarm,SN,Mode,Contrast, LaserI,TCXO,HeatP,Sig,Temp,Steer,ATune,Phase,DiscOK, TOD,LTime,Ver`

3.3.12 Help (?)

The following table lists all available commands in response to the `?` command.

TABLE 3-7: UNIT RESPONSE TO HELP COMMAND (?)

Command	Description
F-	Adjust frequency.
^-	Telemetry.
6-	Telemetry headers.
D-	Set 1PPS discipline tau.
m-	Set 1PPS discipline threshold for phase in ns.
>-	Set 1PPS out pulse width as 1–4 times default.
S-	Sync 1PPS.
U-	Set parameters for ultra-low power mode.
M-	Change mode register.
T-	Change/report time of day.
?-	Show this list.
@-	Delayed command execution.

For firmware versions 1.08 and later, the response also contains the above lines on `m` and `>` commands.

Note: The single character `?` is a shortcut for `!?[CRLF]`.

NOTES:

© 2020-2021 Microchip Technology Inc.

Chapter 4. Developer's Kit

The CSAC Developer's Kit includes all of the necessary hardware, and cabling to facilitate validation of performance, brass-board demonstrations, and software interface development.

4.1 PACKAGE CONTENTS

The following table lists the contents of the developer's kit (Part # 990-00123-000).

TABLE 4-1: CONTENTS OF CSAC DEVELOPER'S KIT

Item	Part Number	Notes
Evaluation board	054-00279-000	"Notes on the Evaluation Board" (see page 29)
Power adapter	140-00041-000	5VDC 5 mm center positive.
RS-232 cable	060-00322-000	—

4.2 EVALUATION BOARD OVERVIEW

Detailed schematics of the evaluation board are provided at the end of this document under **Section 5.4 "Notes on the Evaluation Board"**. The following illustration shows the connections to the evaluation board.

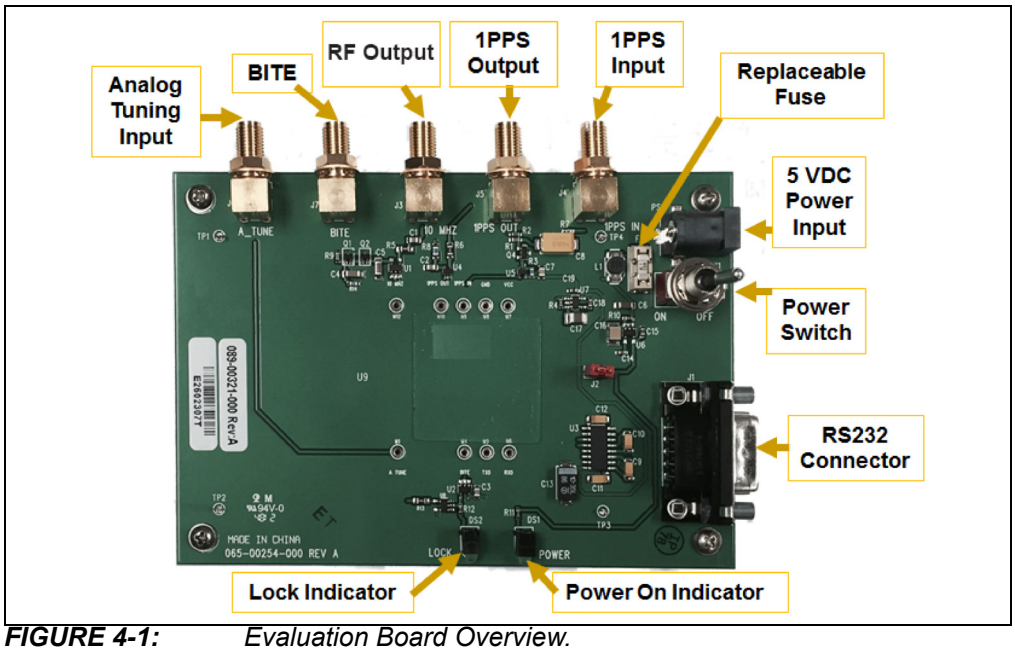


FIGURE 4-1: *Evaluation Board Overview.*

The following items are included in the developer's kit PCB and power supply.

- **RF Output (SMA):** The CSAC output is an RF, CMOS 0VDC to 3.3VDC waveform. A high-speed buffer (U1) on the evaluation board converts the CMOS output to an AC-coupled output capable of delivering 10 dBm to a 50Ω load.
- **3.3VDC Jumper:** The evaluation board provides regulated 3.3VDC to the CSAC.

© 2020-2021 Microchip Technology Inc.

In order to allow convenient measurement of the CSAC power consumption, a jumper is provided in the V_{CC} connection to the CSAC. To measure the CSAC current draw, turn off the evaluation board and install a low-impedance current meter in place of the jumper. Observe proper ESD protocols in making this measurement.

- **Replaceable Fuse:** Littel fuse part number 0453 01.5.
- **5VDC Input:** Input power to the evaluation board is provided on a 5 mm (center positive) coaxial connector (PS1). To avoid damage to the test fixture, it is highly recommended to use only the power adapter provided by Microchip with the Developer's Kit.
- **RS-232 Connection (DB9M):** The evaluation board provides a level shifter (U3), which converts the CSAC 0VDC to 3.3VDC serial interface to the RS-232 standard ±12V for direct interface with a PC COM port. Connect the test fixture (J1) to a PC with a standard (non-Null) DB9F-DB9F RS-232 cable. To avoid complication, use the proper cable provided by Microchip with the developer's kit.
- **Lock Indicator LED:** Indicates normal operation following initial acquisition of the clock signal. This is the logical complement of the BITE output (CSAC pin 4).
- **BITE (SMA):** This is a buffered output from pin 4 of the CSAC.
- **Power Switch:** Controls power to the evaluation board and to the CSAC.
- **Power LED:** Indicates the state of the power switch.
- **Analog Tuning Input (SMA):** This input is directly connected to pin 1 of the CSAC.
- **1PPS Input (SMA):** The 1PPS input connection to the evaluation board accepts a 1PPS reference of arbitrary amplitude (logic high: 2V < V_{IN} < 20V) and generates a 0V to 3.3V CMOS pulse to the CSAC. This input is capacitively coupled to the level-shifting circuit on the evaluation board (see Figure 5-3) and therefore the applied pulse width must be <10 ms in duration.
- **1PPS Output (SMA):** The 1PPS output is buffered by a CMOS 0V to 3.3V logic gate on the evaluation board.

4.3 INSTALLING THE CSAC ON THE TEST FIXTURE

CAUTION

To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC.

Remove the CSAC and evaluation board from their ESD protective bags only in an ESD-safe environment.

Note: The CSAC pinout is keyed (see Table 1-2) so the CSAC can only be inserted in the proper orientation. Gently insert the CSAC into the socket on the evaluation board.

4.4 CABLING

Connect the provided RS-232 cable between the evaluation board and the COM port on the PC. On laptops without an available COM port, a USB-to-RS-232 adapter, such as National Instruments USB-232, can be used.

Make sure the power switch is OFF on the evaluation board, as shown in Figure 4-1. Connect the 5V power adapter between the 5V power input and a wall outlet. (Check labeling on included power supply to ensure compliance with local utility ratings.)

© 2020-2021 Microchip Technology Inc.

CSAC signal outputs are available from the evaluation board on connectors J3 (RF) and J5 (1PPS). Connect either (or both) of these to your test equipment (frequency counter, spectrum analyzer, and so on).

4.5 CSACDEMO SOFTWARE INSTALLATION

The Microchip CSACdemo software (part number 084-00365-000) provides a convenient graphical user interface for monitoring and controlling the CSAC. CSACdemo also is used for collecting and archiving monitor data from the CSAC. It can be installed and run on any PC that runs Microsoft Windows XP, Windows 7, or Windows 10 and has at least one available RS-232 (COM) port.

> **Note:** Multiple CSACs can be monitored from a single PC, provided additional COM ports are available.

The software installation is available for download from the Microchip website.

Upon accepting all of the default installation options (recommended), the CSACdemo software is installed in *C:\Program Files\Microsemi\CSAC*, a startup icon is added to the **Start > All > Programs > Microchip > CSAC** menu, and a CSACdemo icon is placed on the desktop.

4.6 CSACDEMO OPERATION

The following sections outline how to operate the CSACdemo software.

4.6.1 Initial Power-On

Connect power and RS- 232 to the evaluation board as described in **Section 4.4 "Cabling"**. Turn on the power switch on the evaluation board. Double-click the CSACdemo icon on the connected PC.

4.6.2 Establishing Communications

When communications are successfully established, the CSACdemo main window appears as shown in the following screen shot.

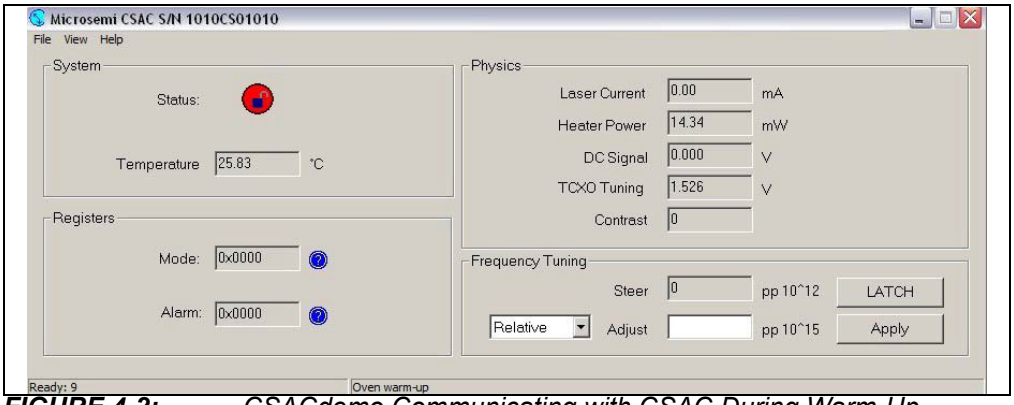


FIGURE 4-2: *CSACdemo Communicating with CSAC During Warm-Up.*

The title bar of the window indicates the unit serial number (here 1010CS01010). The main body of the window shows most of telemetry values from the unit (see **Section 3.3.1 "Telemetry (6 and ^)"**).

Initially, upon power-up, the status indicator reflects CSAC's unlocked condition (BITE = 1). The left field of the bottom status bar indicates the number of seconds until the next poll (here 9) and the right field indicates the unit status (here Oven Warm-up).

© 2020-2021 Microchip Technology Inc.

In the event of communication failure, the status indicator appears as a question mark in a yellow circle. In this case, check the cabling and power supply. The bottom left status bar may also indicate the source of the communication failure. If the COM port is in use by another application, the status bar reports RS-232 open failed, otherwise, it will likely indicate Instrument not responding. If you are using a PC serial port other than COM1, select **Options…** from the **File…** menu and select a different COM Port as shown in Figure 12 (see page 19). Select the correct COM port from the pull-down menu and click **Apply Changes** to re-attempt communications.

4.6.3 Monitoring Communications

For development of application-specific embedded firmware for CSAC, it is helpful to observe the communications between the CSACdemo program and the CSAC. Enable the **Show Trace** checkbox in the **Communications** section of the **Options…** panel and click **Apply Changes** to view the bidirectional protocol.

With the trace visible, the CSACdemo main panel appears as shown in the following screen shot.

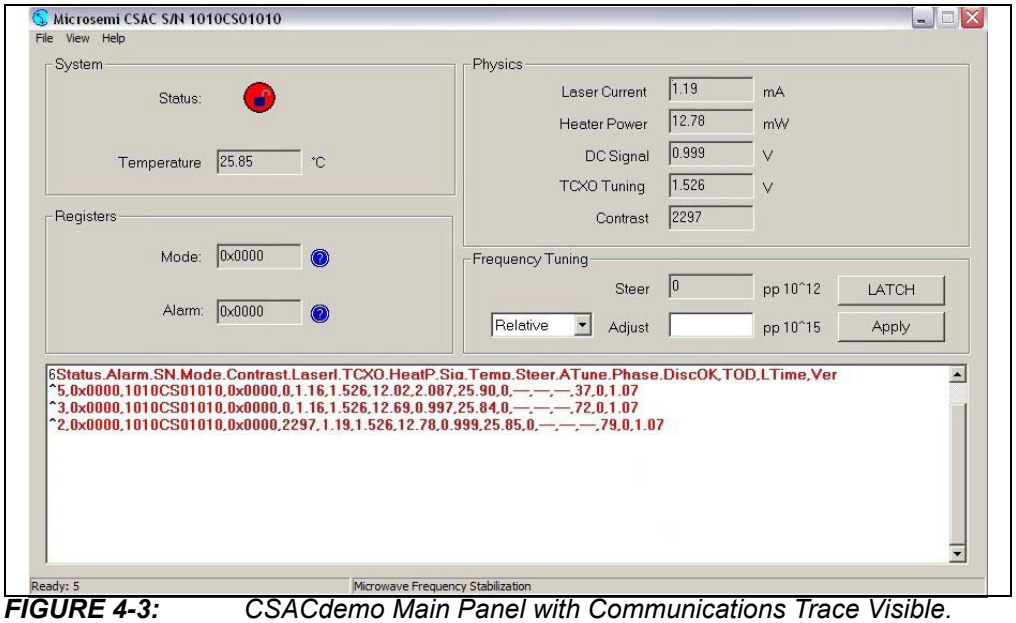


FIGURE 4-3: *CSACdemo Main Panel with Communications Trace Visible.*

Note:	Communications from the host PC to the CSAC are shown in blue and communications from the CSAC to the host are shown in red.

4.6.4 Observing Acquisition

Initially, when the CSAC is powered up, the LOCK LED on the evaluation board momentarily turns on then off once again. During acquisition, the Unit Status field in the lower right corner of CSACdemo will proceed through the stages corresponding to the values of the Status register (see Table 3-4).

Acquisition takes <3 minutes in a 25°C ambient (up to a maximum of 5 minutes at –10°C). When acquisition is complete, the LOCK LED on the evaluation board illuminates, the CSACdemo right hand status bar indicates Locked, and the status indicator changes from changes from an unlocked icon in a red circle to locked icon in a green circle. After locked, the main panel of CSACdemo appears as shown in the following screen shot.

© 2020-2021 Microchip Technology Inc.

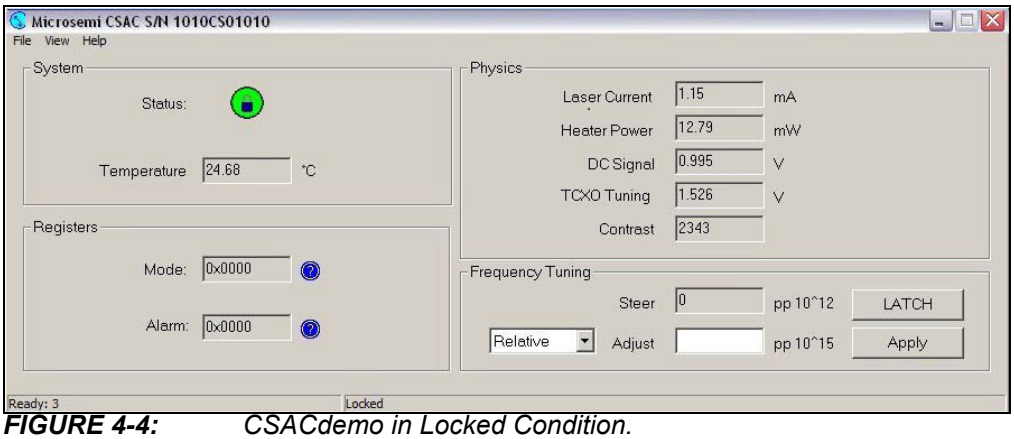


FIGURE 4-4: *CSACdemo in Locked Condition.*

The previous screen shot shows typical values for a normally operating CSAC. In this case, the internal case temperature of the CSAC is 24.86°C, the operating mode is 0x0000 (see **Section 3.3.3 "Set/Clear Operating Modes (M)"**) and there are no alarms. The physics package parameters in Figure 4-4 are fairly typical as well: the laser current is about 1.15 mA, the physics package heaters are drawing less than 25 mW, and the DC signal level is about 1V. The TCXO tuning is mid-range on 0V to 2.5V and the contrast is comfortably above 1000.

4.7 DATA ACQUISITION WITH CSACDEMO

For long-term monitoring of the CSAC, select the **Options…** panel from the **File** menu (see Figure 3-1).

Choose a polling rate in seconds. For short-term (1 to 2 days) measurements, a polling rate of 10 seconds is optimal, and accumulates data onto disk at a rate of about 1 MB/day. For longer term measurements (30 days to 100 days), a longer polling rate, such as 60 seconds, reduces the growth of the data file to 150 kB/day.

Enable **Save to Disk** with the checkbox in the top right of the panel.

Use the **Browse…** button to select an existing Directory to archive the CSAC data.

> **Note:** You must have write permission to the selected directory. Type in a **File-name** for the data.

When you are finished, the panel will look like the following screen shot.

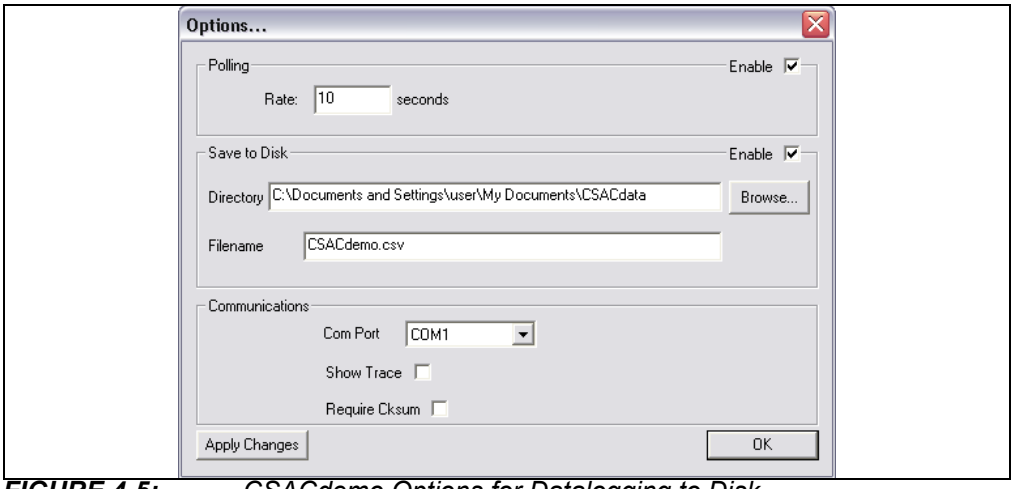


FIGURE 4-5: *CSACdemo Options for Datalogging to Disk.*

Click **Apply Changes** to implement the new options or **OK** to discard changes and exit the panel.

The data is stored in ASCII comma-separated values (CSV) format, which allows for convenient import into most popular spreadsheet and analysis software. The first line in the file contains the column headers (see **Section 3.3.1 "Telemetry (6 and ^)"**). Subsequent lines contain the corresponding periodically polled data. The first column in the file contains time stamps, derived from the host computer's clock, in Modified Julian Date (MJD) format, referenced to universal coordinated time (UTC).

© 2020-2021 Microchip Technology Inc.

Chapter 5. Design Guide

The following sections are the design guide for the CSAC.

5.1 THE ART OF DISCIPLINING

Implemented correctly, disciplining can be utilized to calibrate the CSAC frequency in the field, even if a reference source is only occasionally or sporadically available, thereby improving the long-term performance (phase and frequency drift) of the CSAC. At the same time, the disciplined CSAC may be used to clean-up the short-term stability of an accurate, but noisy, reference source, such as GPS.

Implemented incorrectly, disciplining may degrade the performance of the CSAC. For example, the CSAC disciplined with a short time constant to a source that is noisier than CSAC, such as GPS.

Implementing a successful disciplining strategy involves understanding the noise properties of the CSAC, the reference source, and the phase meter, and selecting the appropriate time constant that makes the best use of the available timing information.

The following graph shows typical instability (Allan Deviation) of the CSAC (in red), along with the noise floor of the phase meter (in green). Also shown are the instabilities of typical reference sources, GPS (in blue) and a high-performance cesium beam frequency standard (in purple).

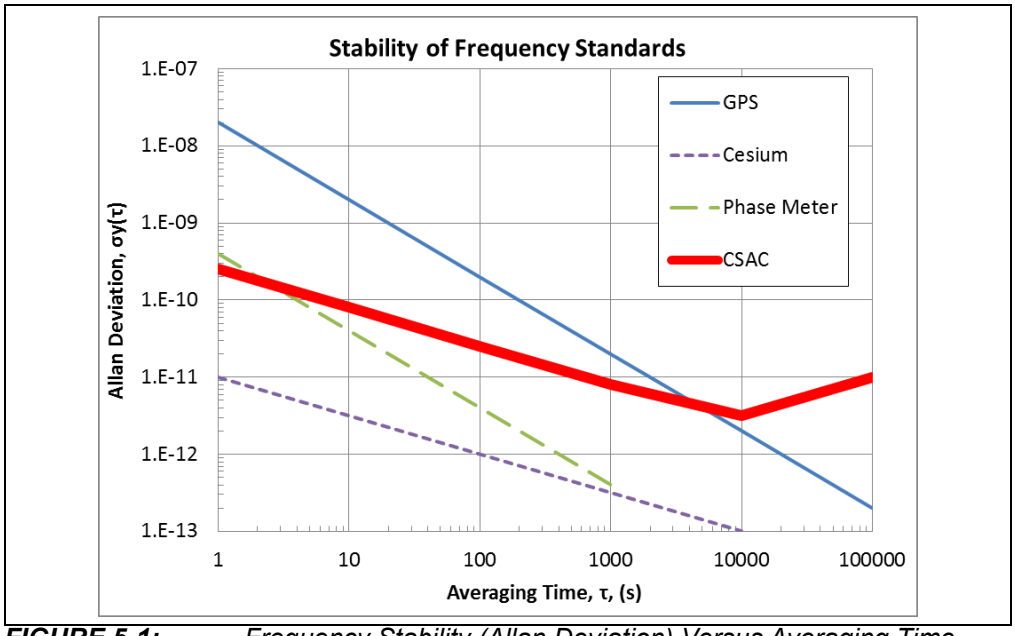


FIGURE 5-1: *Frequency Stability (Allan Deviation) Versus Averaging Time.*

When disciplining, the stability of the output of the CSAC (combined clock) at any averaging time reflects the noise properties of the dominant (most noisy) source. For example, if disciplining the CSAC to a GPS source, which is noisier than the CSAC for averaging times $\tau < 5000$ seconds, the disciplining time constant should be set to $\tau > 5000$ seconds so that the (superior) CSAC stability dominates for $\tau < 5000$ seconds and the (superior) GPS stability dominates for $\tau > 5000$ seconds. On the other hand,

© 2020-2021 Microchip Technology Inc.

consider the case where the CSAC is disciplined to a high-performance cesium clock, which is more stable than the CSAC on all time scales. The noise is dominated by the phase meter for $\tau < 2$ seconds and by the CSAC for $\tau > 2$ seconds. In this case, the disciplining time constant could be set to $\tau = 2$ seconds for optimal performance.

The following graph shows an example of a CSAC, which is disciplined to a superior reference (in this case a hydrogen maser) with a time constant of 20 seconds. For this measurement, the CSAC was deliberately mis-tuned in both frequency (y) and phase (φ) prior to the measurement, by $y = 10 \times 10^{-10}$ and $\varphi = 50$ ns.

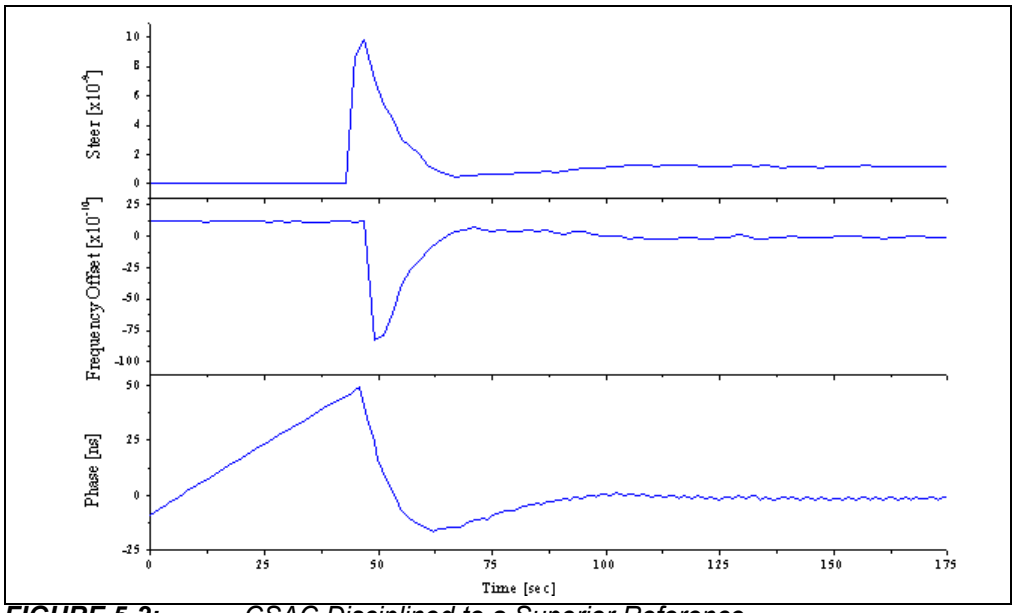


FIGURE 5-2: *CSAC Disciplined to a Superior Reference.*

In the previous graph, when disciplining was enabled, at t = 45 seconds, the steering algorithm immediately inserted a frequency offset of -9×10^{-9}, to steer out the 50 ns phase error with 20 second time constant. The steering gradually reduces as the phase approaches zero such that both frequency and phase are corrected to within 1/e of their initial values at one time constant (20 seconds) and $1/e^2$ within two time constants (40 seconds). After five to six time constants (≈ 100 seconds), frequency and phase are corrected to within $\pm 5 \times 10^{-13}$ and ±5 ns, respectively.

5.2 HEAT SINK

The CSAC does not require a heat sink because it consumes low power and therefore produces little heat. Furthermore, the external parts of CSAC are mu-metal (80% nickel), which is a poor thermal conductor (1/5 that of aluminum). There is no useful thermal path from the inside components to the baseplate or the cover.

5.3 NOTES ON SOLDERING

For initial testing and evaluation, it is recommended that the pins must not be modified or soldered to a PCB. The recommended socket for PCB attachment is Tyco P/N 4-5332070-4.

After evaluation, the pins can be hand soldered to a PCB using 63/37 tin/lead solder with a maximum soldering tip temperature of 329°C (625°F).

Hand soldering is a necessary requirement for CSAC, and solder re-flow is not recommended because the CSAC cannot go above storage temperature (it is likely to damage it).

© 2020-2021 Microchip Technology Inc.

The lead material is 52 Alloy with a plating of 50 µin gold minimum (ASTM 8488-01) over 100 µin nickel (QQ-N-290).

5.4 NOTES ON THE EVALUATION BOARD

The following illustration shows the reference schematic for the evaluation board.

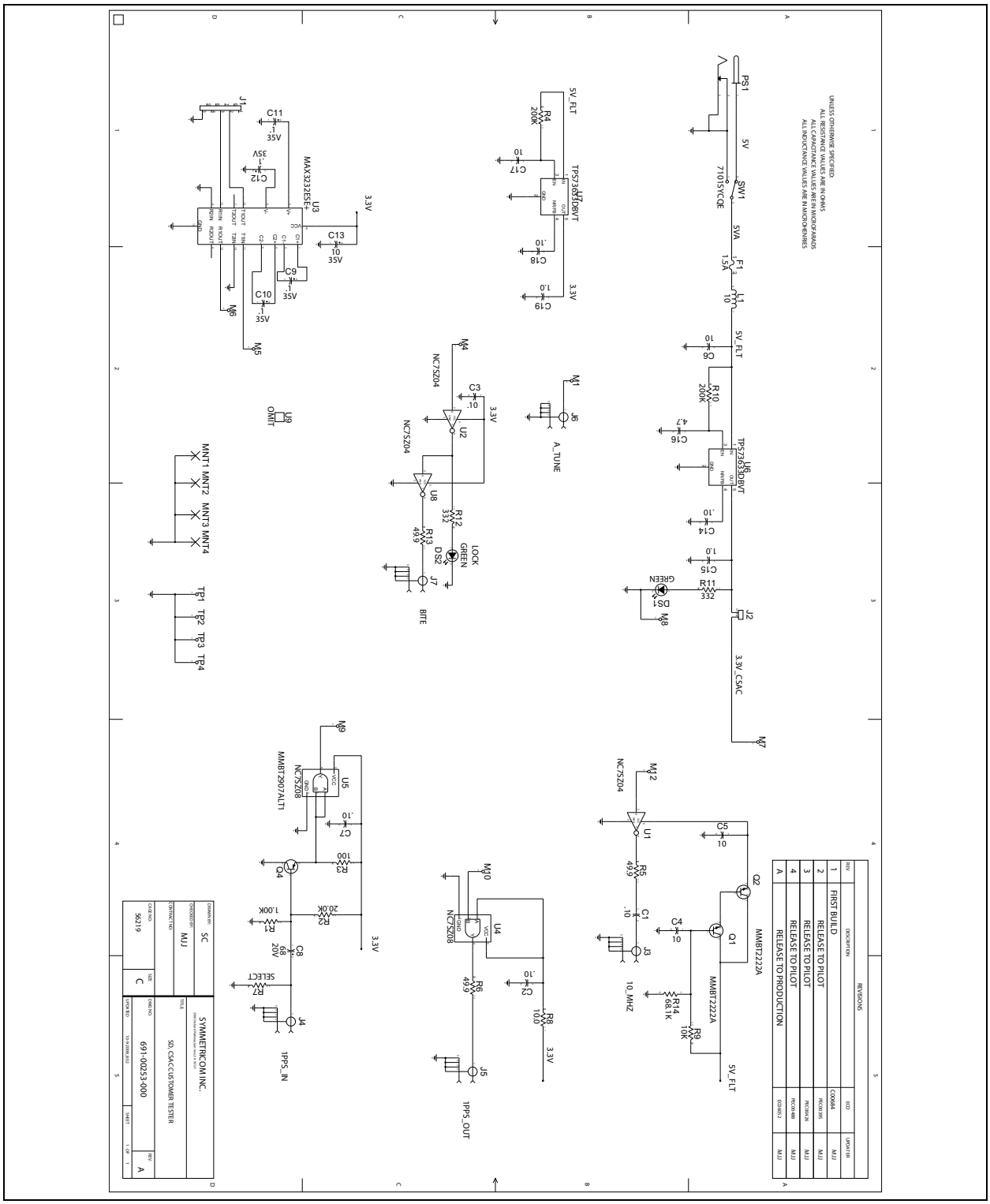


FIGURE 5-3: *Reference Schematic for Evaluation Board.*

The 1PPS input on the evaluation board is capacitively coupled to the CSAC through a common collector transistor stage and a UHS inverter. This is to protect the CSAC in the evaluation environment, from 1PPS signals >5V.

The 10 MHz output from the CSAC is buffered and capacitively coupled on the evaluation board. It also offers flexibility to condition the signal as needed by the user.

V_{CC} for the UHS inverter is supplied with a resistor divider and Darlington pair to provide a good filter for removing 50 Hz to 60 Hz AC line noise. However, caution must be taken if designed into a circuit elsewhere as the output voltage may vary under higher current loads.

5.5 TIME ERROR OF A CSAC

Time error of any clock is dependent on its operating conditions (temperature and vibration) and the clocks inherent stability (Aging, ADEV). Time error is given by:

EQUATION 5-1:

$$E(t) = E_0 + \int_0^{\tau} y(t)dt + \varepsilon(t)$$

$$E(t) = E_0 + \left(y_0 t + \frac{1}{2}at^2\right) + \int_0^{\tau} y_e(t)dt + \tau\sigma(\tau)$$

Where:
E(t) = Time error accumulation at a time "t" after initial synchronization.
E_0 = Initial time error at t = 0.
y(t) = Fractional frequency of the clock at time "t", approximated as
$y(t) = y_0 + at + y_e(t)$.
y_0 = Fractional frequency offset at t = 0.
a = Clock aging rate.
$y_e(t)$ = Fractional frequency offset due to environmental effects (that is, temperature).
$\varepsilon(t)$ = Random fractional frequency fluctuations.
$\varepsilon(t) = \tau\sigma(\tau)$
$\sigma(t)$ = Allan deviation at sampling rate (τ)

5.6 WRITES TO NVRAM

CSAC has a physical limit to the number of writes to NVRAM <20,000. To maximize the lifetime of the CSAC, restrict the number of NVRAM writes accordingly.

The following are the scenarios of a write to NVRAM:

- Issuing a Frequency Latch command (format `!FL`) causes an NVRAM write.
- Issuing a PPS cable length compensation latch command (format `!DCL`) causes an NVRAM write.
- Issuing a PPS disciplining tau set command that changes discipline tau (format `!Dn` where n is a decimal number) causes an NVRAM write.
- Issuing a mode command that changes mode register (format `!Mx` where x is an alphabetical character) in list below causes an NVRAM write:
  - Communications Checksum on/off (`!MC` vs `!Mc`)
  - External oscillator on/off (`!MZ` vs `!Mz`)
  - PPS auto-sync on/off (`!MS` vs `!Ms`)
  - PPS disciplining on/off (`!MD` vs `!Md`)

© 2020-2021 Microchip Technology Inc.

  - PPS measure on/off (`!MM` vs `!Mm`)
  - Analog tuning on/off (`!MA` vs `!Ma`)
  - ULP on/off (`!MU` vs `!Mu`)
- Issuing a ULP configuration command (format `!Un,p` where n and p are decimal numbers) causes an NVRAM write.
- Every ULP cycle, firmware does an automatic NVRAM write.
- Every auto-reset (status 0->8) due to alarm where status reverts from lock state, firmware does an automatic NVRAM write.
- Periodically every 30 days in clock-lock state, firmware does an automatic NVRAM write.
- Issuing a PPS pulse width set command that changes pulse width (format `!>N` where N is a decimal number) will cause an NVRAM write. (FW1.08 and later.)
- Issuing a PPS disciplining status threshold phase command that changes phase threshold (format `!mN` where N is a decimal number) will cause an NVRAM write. (FW1.08 and later.)
- Lock set points are saved after each acquisition of a lock state. This write occurs ~102 seconds after Lock is achieved.

© 2020-2021 Microchip Technology Inc.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

© 2020-2021 Microchip Technology Inc.

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP