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MM-6295 Data Sheet

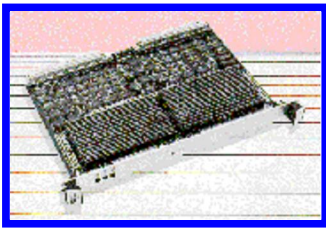
512Mbyte, 64 Data Bits, 55 Mbyte/sec VME/VME64 DRAM Memory Module

This page contains [features](#), a [description](#), [specifications](#), and [ordering information](#) for the MM-6295 memory module.

FEATURES:

- **Capacity:** 32M, 64M, 128M, 256M, 512M bytes
 - **Cycle/Access Time:**
 - Random Read: 250/150 nsec
 - Random Write: 200/60 nsec
 - Block Transfer Read: 140/40 nsec
 - Block Transfer Write: 130/40 nsec
 - **VMEbus-compatible:** per Rev. D: A32/A24, D64/D32/D16/D8 (UAT)
 - **Block transfer (BLT):** within 256 byte boundaries in the D32 mode, and 2 Kbyte boundaries in the D64 mode
 - **Parity:** Parity generation and checking on each byte
 - **Module selection:** on 1 Mbyte boundaries, with switch-selectable lower and upper limits
 - **Lifetime Warranty** on parts and labor
-

DESCRIPTION:



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Extensive use of surface mount technology and 4 Mbit DRAMs allows the MM-6295D memory module to occupy a single 6U card slot with up to 512 Mbytes capacity. Its data transfer rate is 55 Mbytes/sec. and it operates with a 64-bit word per VMEbus specification Rev. D.

The MM-6295D supports A32/A24, D64/D32/D16/D8. Besides the D64 block mode read and write accesses, the MM-6295D responds to A32 and A24 address modifiers for long word, word and byte transfers. Address modifier codes are programmed into a socketed PAL, which allows A32 or A24 masters to access memory when residing on the same bus. Module selection is on 1 Mbyte boundaries, with switch-selectable upper and lower limits.

Each 8-bit byte has an associated bit for parity error detection. Parity errors are indicated via BERR*.

Ensuring module reliability, complete inspection and testing is performed while running memory diagnostics. In addition, all units undergo 48 hours of burn-in while running diagnostics. Furthermore, Micro Memory backs up board reliability with a **Lifetime Warranty**.

SPECIFICATIONS:

Capacity

32M, 64M, 128M, 256M, 512M bytes

Cycle/Access Time (nsec)

Random Read: 250/150 nsec

Random Write: 200/60

Block Transfer Read: 140/40

Block Transfer Write: 130/40

Address

A32/A24 address bits

Data In/Data Out

D64/D32/D16/D8 (UAT)

Sequential Access

Block transfer (BLT) within 256 byte boundaries in the D32 mode; 2 Kbyte boundaries in the D64 mode

Address Modifiers

6-bit, decoded by socketed PAL with the following codes:

A24: 39, 3A, 3D and 3E

A32: 09, 0A, 0D and 0E

A24 with BLT: 38, 3F

A32 with BLT: 0B, 0F

A24/D64 with BLT: 38, 3C

A32/D64 with BLT: 08, 0C

Parity

Byte-wide parity generation and checking; parity output stored and transmitted via BERR*

Interface

VMEbus compatible per Rev D

Modes of Operation

Read, write, read-modify-write, long word, word, unaligned, block transfer

Refresh

Hidden refresh

Memory Selection

1 Mbyte boundaries, switch-selectable for the upper and lower limits

Operating Temperature

0 to 60 degrees (Celsius)

Storage Temperature

-40 to +85 degrees (Celsius)

Relative Humidity

Up to 95% without condensation

Power Requirements:

+5V (Fully Populated)

Operate 4.6A (max.)



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