

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

SYNCHRONOUS DRAM MODULE

MT8LSDT1664A - 128MB
MT16LSDT3264A - 256MB

For the latest data sheet, please refer to the Micron Web site: www.micron.com/datasheets

FEATURES

- PC100- and PC133-compliant
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 125 MHz and 133 MHz SDRAM components
- Unbuffered
- 128MB (16 Meg x 64)(x8 SDRAMS)
- 256MB (32 Meg x 64)(x8 SDRAMS)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

OPTIONS — MARKING

- Package
  - Unbuffered — A
  - 168-pin DIMM (gold) — G
- Frequency/CAS Latency
  - 133 MHz/CL = 2 — -13E
  - 133 MHz/CL = 3 — -133
  - 100 MHz/CL = 2 — -10E

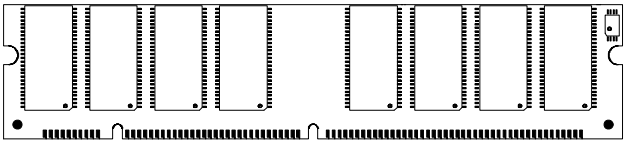
DEVICE TIMING

Module Markings	PC100 CL - ^{t}RCD - ^{t}RP	PC133 CL - ^{t}RCD - ^{t}RP
-13E	2 - 2 - 2	2 - 2 - 2
-133	2 - 2 - 2	3 - 3 - 3
-10E	2 - 2 - 2	**NA**

ADDRESS TABLE

	256MB Module	512MB Module
Refresh Count	4K	4K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)
Row Addressing	4K (A0–A11)	4K (A0–A11)
Column Addressing	1K (A0–A9)	1K (A0–A9)
Module Banks	1 (S0,S2)	2 (S0,S2; S1,S3)

PIN ASSIGNMENT (Front View)
168-Pin DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	NC	90	VDD	132	NC
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	VSS	106	NC	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	NC	73	VDD	115	RAS#	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	NC	168	VDD

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT8LSDT1664AG-13E_	16 Meg x 64	133 MHz
MT8LSDT1664AG-133_	16 Meg x 64	133 MHz
MT8LSDT1664AG-10E_	16 Meg x 64	100 MHz
MT16LSDT3264AG-13E_	32 Meg x 64	133 MHz
MT16LSDT3264AG-133_	32 Meg x 64	133 MHz
MT16LSDT3264AG-10E_	32 Meg x 64	100 MHz

NOTE: The designators for component and PCB revision are the last two characters of each part number Consult factory for current revision codes. Example: MT16LSDT3264AG-133B1.

GENERAL DESCRIPTION

The MT8LSDT1664A and MT16LSDT3264A are high-speed CMOS, dynamic random-access, 128MB and 256MB memory modules organized in a x64 configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0-A11 select the device row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing one of the other three device banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

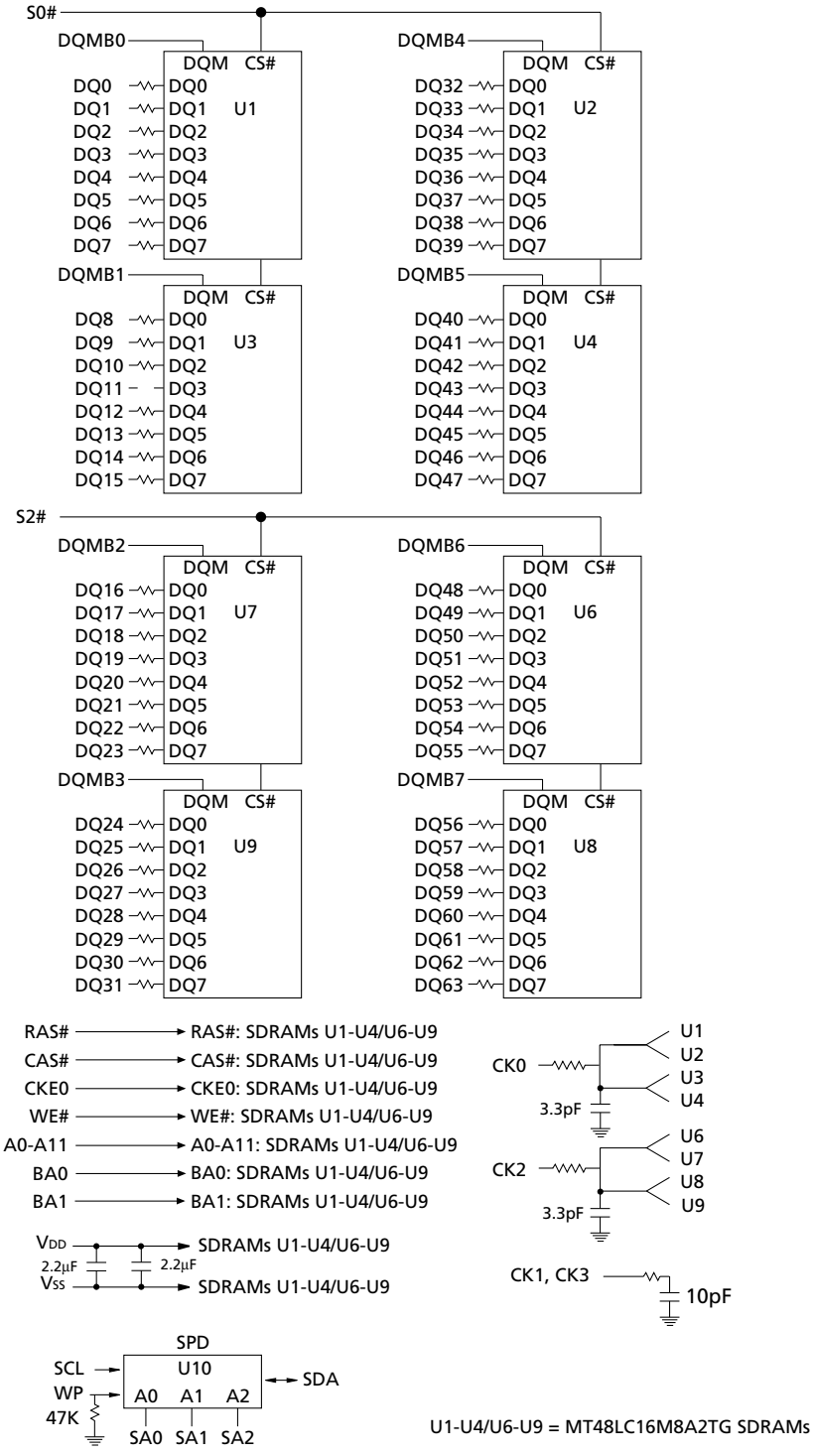
SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

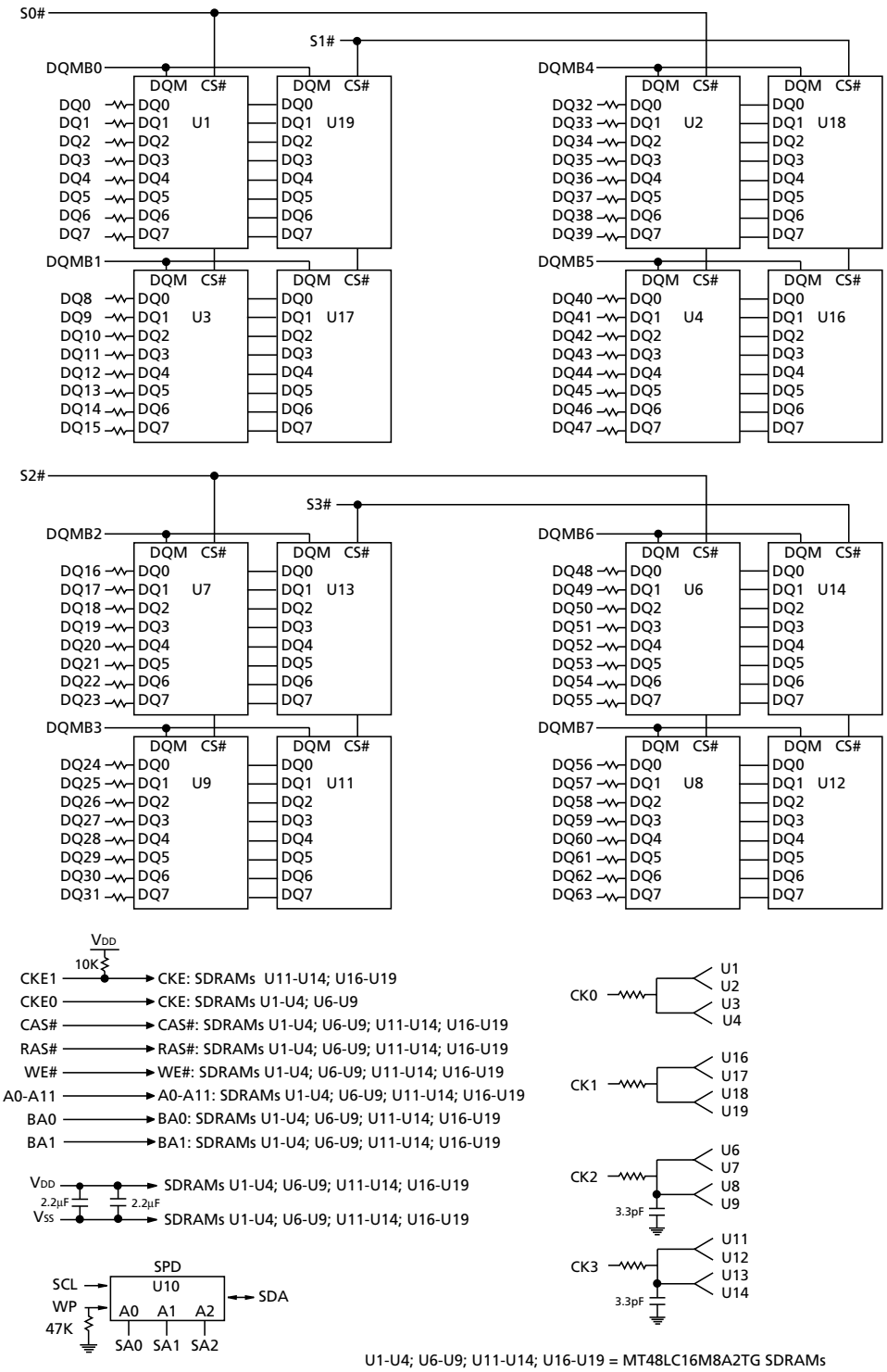
FUNCTIONAL BLOCK DIAGRAM
MT8LSDT1664A (128MB)



NOTE: 1. All resistor values are 10 ohms unless otherwise specified.
2. Reference designators in this diagram do not necessarily match the actual module.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

FUNCTIONAL BLOCK DIAGRAM
MT16LSDT3264A (256MB)



NOTE: 1. All resistor values are 10 ohms unless otherwise specified.
2. Reference designators in this diagram do not necessarily match the actual module.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
27, 115, 111	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S0#-S3#) define the command being entered.
42, 79, 125, 163	CK0-CK3	Input	Clock: CK0-CK3 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
63, 128	CKE0, CKE1	Input	Clock Enable: CKE0-CKE1 activate (HIGH) and deactivate (LOW) the CK0-CK3 signals. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all device banks idle), ACTIVE POWER-DOWN (row ACTIVE in any device bank) or CLOCK SUSPEND operation (burst access in progress). CKE0-CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0-CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0-CK3, are disabled during power-down and self refresh modes, providing low standby power.
30, 45, 114, 129	S0#-S3#	Input	Chip Select: S0#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#-S3# are registered HIGH. S0#-S3# are considered part of the command code.
28-29, 46-47, 112-113, 130-131	DQMB0-DQMB7	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
33, 34, 35, 36, 37, 38, 117, 118, 119, 120, 121, 123	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A9, with A10 defining auto precharge) to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine if all device banks are to be precharged (A10 HIGH) or device bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
81	WP	Input	Write Protect: Serial presence-detect hardware write protect.
83	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
165-167	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/O: Data bus.
82	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground.
21, 22, 24, 25, 31, 44, 48, 50-53, 61, 62, 80, 105, 106, 108, 109, 126, 132, 134-137, 145-147, 164	NC	–	Not Connected: These pins are not connected on this module.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

SDRAM COMPONENT DESCRIPTION

In general, the 128Mb SDRAMs are quad-bank DRAMs that operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). The four banks of the x8 configured devices used for these modules are configured as 4,096 bit-rows by 1,024 bit-columns, by 8 input/output bits.

MODULE FUNCTIONAL DESCRIPTION

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed; BA0 and BA1 select the device bank, A0–A11 select the device row. The address bits A0–A9 registered coincident with the READ or WRITE command are used to select the starting device column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Register Definition

MODE REGISTER

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in the Mode Register Definition Diagram. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

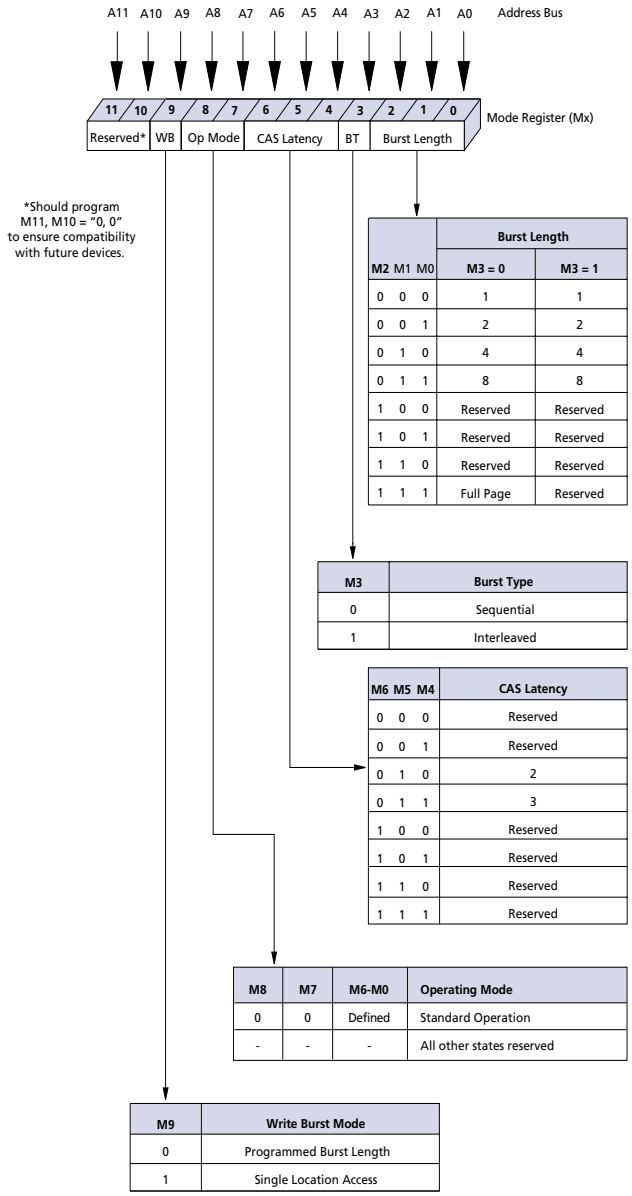
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in the Burst Definition Table. The block is uniquely selected by A1–A9 when the burst length is set to two; by A2–A9 when the burst length is set to four; and by A3–A9 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in the Burst Definition Table.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in the Burst Definition Table.



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Mode Register Definition Diagram

Burst Definition Table

Burst Length	Starting Column Address:	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A9 (location 0-y)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not supported

NOTE:
1. For full-page accesses: y = 1,024 .
2. For a burst length of two, A1-A9 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A9 select the block-of-four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A9 select the block-of-eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0-A9 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A9 select the unique column to be accessed, and mode register bit M3 is ignored.

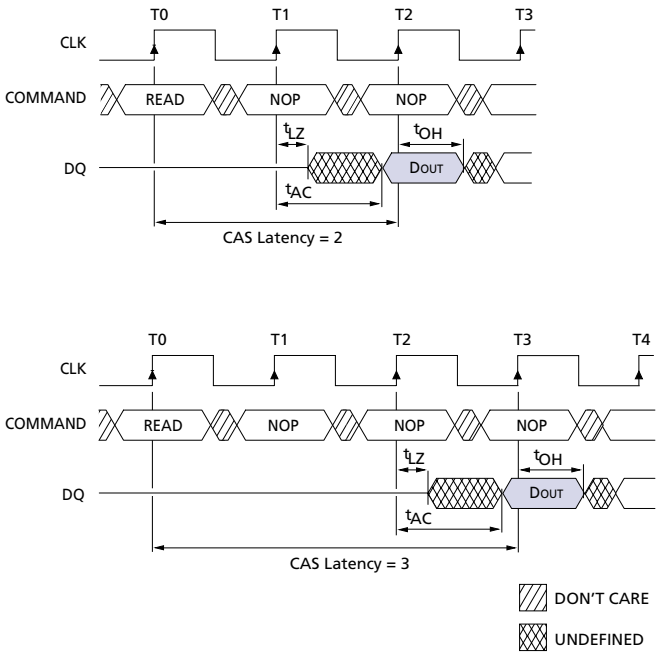
Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in the CAS Latency Diagram. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.



CAS Latency Diagram

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

CAS Latency Table

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
-13E	≤ 133	≤ 143
-133	≤ 100	≤ 133
-10E	≤ 100	≤ 125

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

COMMANDS

The Truth Table provides a quick reference of available commands. This is followed by written description of each command. For a more detailed description of commands and operations, refer to the 128Mb SDRAM component data sheet.

TRUTH TABLE – SDRAM Commands and DQMB Operation

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A11 define the op-code written to the mode register.
3. A0-A11provide device row address, and BA0, BA1 determine which device bank is made active.
4. A0-A9 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine which device bank is being precharged. A10 HIGH: all device banks are precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD}, $V_{DD}Q$ Supply
Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature,
T_A ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation, 128MB 8W
Power Dissipation, 256MB 16W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS - 128MB Module

(Notes: 1, 5, 6; notes appear following parameter tables); (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}, $V_{DD}Q$	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-40	40	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS - 256MB Module

(Notes: 1, 5, 6; notes appear following parameter tables); (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}, $V_{DD}Q$	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	-10	10	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

IDD SPECIFICATIONS AND CONDITIONS*: 128MB Module

(Notes: 1, 5, 6, 11, 13; notes appear following the parameter tables);
(VDD, VDDQ = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MAX -13E	MAX -133	MAX -10E	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; tRC = tRC (MIN)		IDD1[a]	1280	1200	1120	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; All device device banks idle; CKE = LOW		IDD2[b]	16	16	16	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after tRCD met; No accesses in progress		IDD3[a]	400	400	320	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active		IDD4[a]	1320	1280	1200	mA	3, 18, 19, 30
AUTO REFRESH CURRENT	tRFC = tRFC (MIN)	IDD5[b]	2640	2480	2160	mA	3, 12, 18, 19, 30, 31
CKE = HIGH; CS# = HIGH	tRFC = 15.625µs	IDD6[b]	24	24	24	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7[b]	16	16	16	mA	4

IDD SPECIFICATIONS AND CONDITIONS*: 256MB Module

(Notes: 1, 6, 11, 13; notes appear following parameter tables)
(VDD, VDDQ = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MAX -13E	MAX -133	MAX -10E	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; tRC = tRC (MIN)		IDD1[a]	1296	1216	1136	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; All device banks idle; CKE = LOW		IDD2[b]	32	32	32	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after tRCD met; No accesses in progress		IDD3[a]	416	416	336	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active		IDD4[a]	1336	1216	1136	mA	3, 18, 19, 30
AUTO REFRESH CURRENT	tRFC = tRFC (MIN)	IDD5[b]	5280	4960	4320	mA	3, 12, 18, 19, 30, 31
CS# = HIGH; CKE = HIGH	tRFC = 15.625 µs	IDD6[b]	48	48	48	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7[b]	32	32	32	mA	4

*DRAM components only.
a - Value calculated as one module bank in this operating condition, and all other module banks in Power-Down Mode.
b - Value calculated reflects all module banks in this operating condition.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

CAPACITANCE* (128MB)

		128MB		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**
Input Capacitance: A0-A12, BA0, BA1, RAS#, CAS#, WE#	C_{I1}	20	30.4	pF
Input Capacitance: CK0-CK3	C_{I2}	13.3	17.3	pF
Input Capacitance: S0#-S3#	C_{I3}	10	15.2	pF
Input Capacitance: CKE0, CKE1	C_{I4}	20	30.4	pF
Input Capacitance: DQMB0-DQMB7	C_{I5}	2.5	3.8	pF
Input/Output Capacitance: SCL, SA0-SA2, SDA	C_{I6}	–	10	pF
Input/Output Capacitance: DQ0-DQ63	C_{IO}	4	6	pF

CAPACITANCE* (256MB)

		256MB		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**
Input Capacitance: A0-A12, BA0, BA1, RAS#, CAS#, WE#	C_{I1}	40	60.8	pF
Input Capacitance: CK0-CK3	C_{I2}	13.3	17.3	pF
Input Capacitance: S0#-S3#	C_{I3}	10	15.2	pF
Input Capacitance: CKE0, CKE1	C_{I4}	20	30.4	pF
Input Capacitance: DQMB0-DQMB7	C_{I5}	5	7.6	pF
Input/Output Capacitance: SCL, SA0-SA2, SDA	C_{I6}	–	10	pF
Input/Output Capacitance: DQ0-DQ63	C_{IO}	8	12	pF

*This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 8, 9, 11; notes appear following parameter tables)

AC CHARACTERISTICS			-13E		-133		-10E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from	CL = 3	$^tAC(3)$		5.4		5.4		6	ns	27
CLK (pos. edge)	CL = 2	$^tAC(2)$		5.4		6		6	ns	
Address hold time		^tAH	0.8		0.8		1		ns	
Address setup time		^tAS	1.5		1.5		2		ns	
CLK high-level width		^tCH	2.5		2.5		3		ns	
CLK low-level width		^tCL	2.5		2.5		3		ns	
Clock cycle time	CL = 3	$^tCK(3)$	7		7.5		8		ns	23
	CL = 2	$^tCK(2)$	7.5		10		10		ns	23
CKE hold time		^tCKH	0.8		0.8		1		ns	
CKE setup time		^tCKS	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		2		ns	
Data-in hold time		^tDH	0.8		0.8		1		ns	
Data-in setup time		^tDS	1.5		1.5		2		ns	
Data-out high-impedance	CL = 3	$^tHZ(3)$		5.4		5.4		6	ns	10
time	CL = 2	$^tHZ(2)$		5.4		6		7	ns	10
Data-out low-impedance time		^tLZ	1		1		1		ns	
Data-out hold time (load)		^tOH	3		3		3		ns	
Data-out hold time (no load)		^tOH_N	1.8		1.8		1.8		ns	28
ACTIVE to PRECHARGE command		^tRAS	37	120,000	44	120,000	50	120,000	ns	29
ACTIVE to ACTIVE command period		^tRC	60		66		70		ns	
ACTIVE to READ or WRITE delay		^tRCD	15		20		20		ns	
Refresh period (8,192 rows)		^tREF		64		64		64	ms	
AUTO REFRESH period		^tRFC	66		66		70		ns	
PRECHARGE command period		^tRP	15		20		20		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	14		15		20		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^tWR	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7ns		ns	24
			14		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		^tXSR	67		75		80		ns	20

*Module AC timing parameters comply with PC100 and PC133 Design Specs, based on component parameters.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

AC FUNCTIONAL CHARACTERISTICS

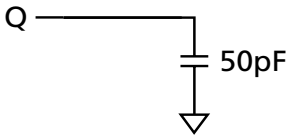
(Notes: 5, 6, 7, 8, 9, 11; notes appear following parameter tables)

PARAMETER		SYMBOL	-13E	-133	-10E	UNITS	NOTES
READ/WRITE command to READ/WRITE command		tCCD	1	1	1	tCK	17
CKE to clock disable or power-down entry mode		tCKED	1	1	1	tCK	14
CKE to clock enable or power-down exit setup mode		tPED	1	1	1	tCK	14
DQM to input data delay		tDQD	0	0	0	tCK	17
DQM to data mask during WRITEs		tDQM	0	0	0	tCK	17
DQM to data high-impedance during READs		tDQZ	2	2	2	tCK	17
WRITE command to input data delay		tDWD	0	0	0	tCK	17
Data-in to ACTIVE command		tDAL	4	5	4	tCK	15, 21
Data-in to PRECHARGE command		tDPL	2	2	2	tCK	16, 21
Last data-in to burst STOP command		tBDL	1	1	1	tCK	17
Last data-in to new READ/WRITE command		tCDL	1	1	1	tCK	17
Last data-in to PRECHARGE command		tRDL	2	2	2	tCK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	2	tCK	26
Data-out to high-impedance from PRECHARGE command	CL = 3	tROH(3)	3	3	3	tCK	17
	CL = 2	tROH(2)	2	2	2	tCK	17

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ T_A ≤ +70°C).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1 ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 10ns for -10E, and ^{t}CK = 7.5ns for -133 and -13E.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7ns for -13E; 7.5ns for -133 and 7ns for -10E after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. ^{t}AC for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. The value of ^{t}RAS. use in -13E speed grade module SPDs is calculated from ^{t}RC - ^{t}RP = 45ns.
30. For -10E, CL= 2 and ^{t}CK = 10ns; for -133, CL = 3 and ^{t}CK = 7.5ns; for -13E, CL = 2 and ^{t}CK = 7.5ns.
31. CKE is HIGH during refresh command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD}6 limit is actually a nominal value and does not result in a fail value.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

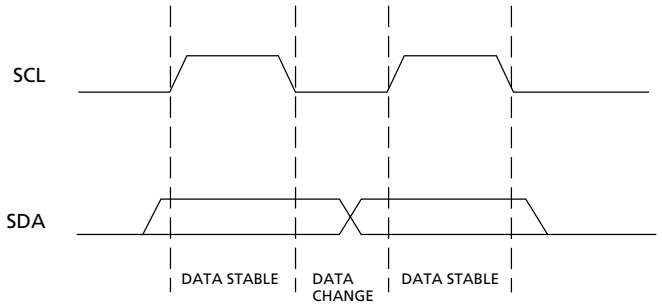


Figure 1
Data Validity

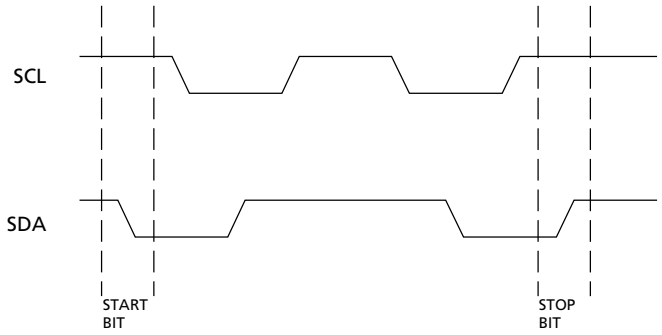


Figure 2
Definition of Start and Stop

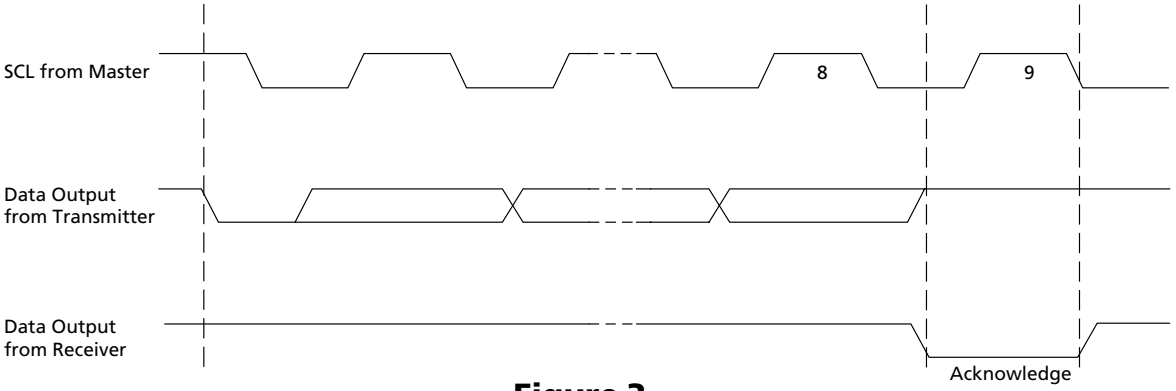


Figure 3
Acknowledge Response From Receiver

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

EEPROM DEVICE SELECT CODE

(The most significant bit (b7) is sent first)

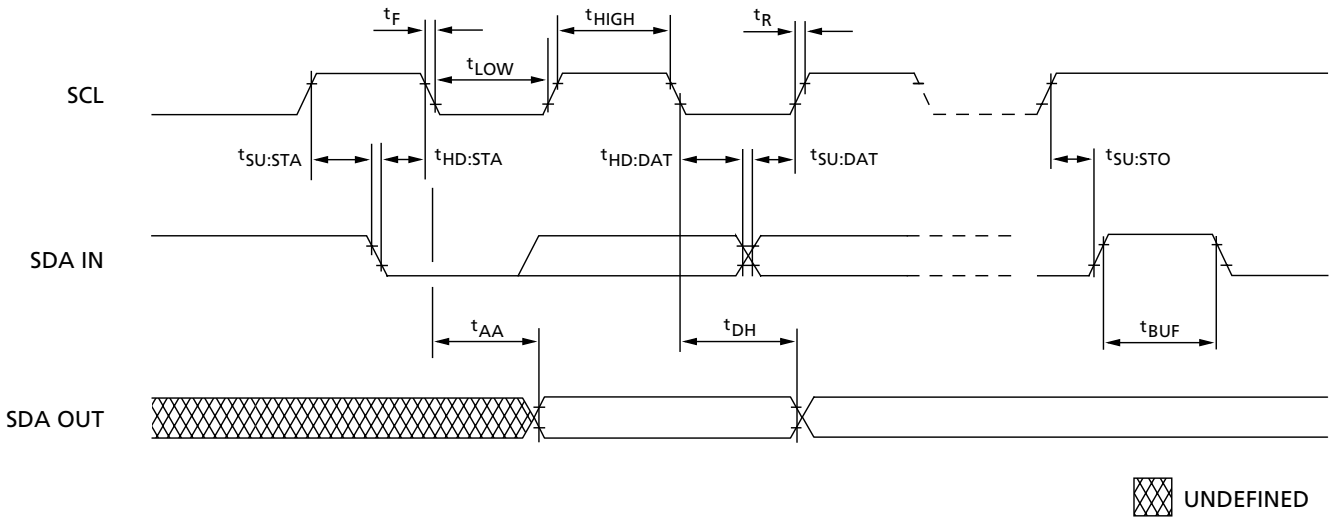
	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	RW
Protection Register Select Code	0	1	1	0	E2	E1	E0	RW

EEPROM OPERATING MODES

($X = V_{IH}$ or V_{IL})

MODE	RW Bit	WC[1]	BYTES	Initial Sequence
Current Address Read	1	X	1	Start, Device Select, RW = 1
Random Address Read	0	X	1	Start, Device Select, RW = 0, Address
	1	X		reSTART, Device Select, RW = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, RW = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, RW = 0

SPD EEPROM TIMING DIAGRAM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs

SYMBOL	MIN	MAX	UNITS
tHIGH	4		µs
tLOW	4.7		µs
tR		1	µs
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWRC		10	ms	2

NOTE: 1. All voltages referenced to V_{SS}.
2. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

SERIAL PRESENCE-DETECT MATRIX

(Note: 1) (V_{DD} = +3.3V ±0.3V)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8LSDT1664AG	MT16LSDT3264AG
0	NUMBER OF BYTES USED BY MICRON	128	80	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08	08
2	MEMORY TYPE	SDRAM	04	04
3	NUMBER OF ROW ADDRESSES	12	0C	0C
4	NUMBER OF COLUMN ADDRESSES	10	0A	0A
5	NUMBER OF MODULE BANKS	1 or 2	01	02
6	MODULE DATA WIDTH	64	40	40
7	MODULE DATA WIDTH (continued)	0	00	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL	01	01
9	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 3)	7 (-13E) 7.5 (-133) 8 (-10E)	70 75 80	70 75 80
10	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 3)	5.4 (-13E/-133) 6 (-10E)	54 60	54 60
11	MODULE CONFIGURATION TYPE	NONPARITY	00	00
12	REFRESH RATE/TYPE	15.625µs/SELF	80	80
13	SDRAM WIDTH (PRIMARY SDRAM)	8	08	08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE	00	00
15	MINIMUM CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES, ^{t}CCD	1	01	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE	8F	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04	04
18	CAS LATENCIES SUPPORTED	2, 3	06	06
19	CS LATENCY	0	01	01
20	WE LATENCY	0	01	01
21	SDRAM MODULE ATTRIBUTES	UNBUFFERED	00	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E	0E	0E
23	SDRAM CYCLE TIME , ^{t}CK (CAS LATENCY = 2)	7.5 (13E) 10 (-133/-10E)	75 A0	75 A0
24	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 2)	54 (-13E) 6 (-133/-10E)	54 60	54 60
25	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 1)		00	00
26	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 1)		00	00
27	MINIMUM ROW PRECHARGE TIME, ^{t}RP	15 (-13E) 20 (-133/-10E)	0F 14	0F 14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	14 (-13E) 15 (-133) 20 (-10E)	0E 0F 14	0E 0F 14
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD	15 (-13E) 20 (-133/-10E)	0F 14	0F 14

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

SERIAL PRESENCE-DETECT MATRIX (continued)

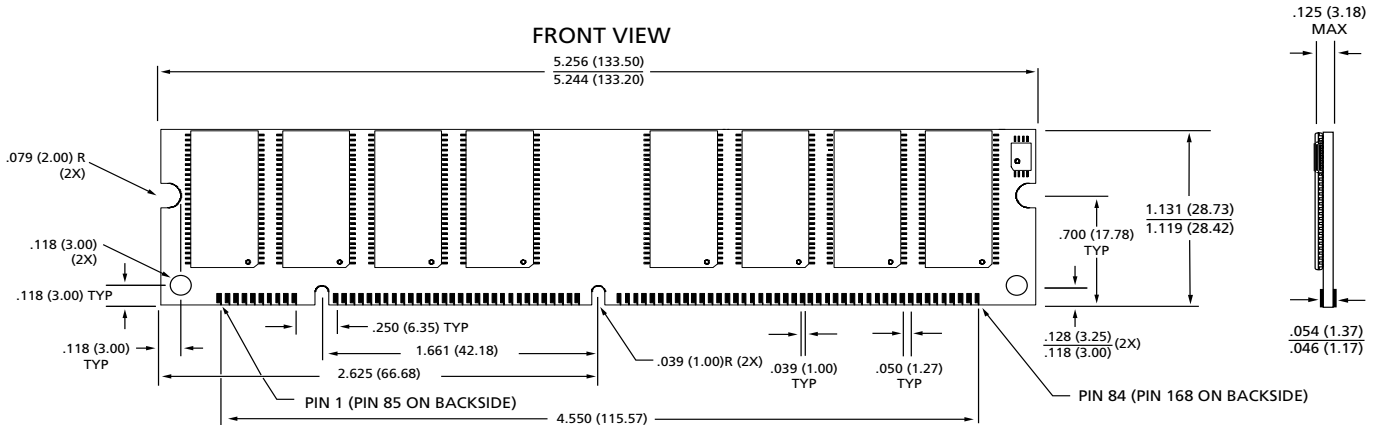
(Notes: 1, 2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8LSDT1664AG	MT16LSDT3264AG
30	MINIMUM RAS# PULSE WIDTH, ^{t}RAS (Note: 3)	45 (-13E) 44 (133) 50 (-10E)	2D 2C 32	2D 2C 32
31	MODULE BANK DENSITY	128MB	20	20
32	COMMAND AND ADDRESS SETUP TIME, ^{t}AS, ^{t}CMS	1.5 (-13E/-133) 2 (-10E)	15 20	15 20
33	COMMAND AND ADDRESS HOLD TIME, ^{t}AH, ^{t}CMH	0.8 (-13E/-133) 1 (-10E)	08 10	08 10
34	DATA SIGNAL INPUT SETUP TIME, ^{t}DS	1.5 (-13E/-133) 2 (-10E)	15 20	15 20
35	DATA SIGNAL INPUT HOLD TIME, ^{t}DH	0.8 (-13E/-133) 1 (-10E)	08 10	08 10
36-61	RESERVED		00	00
62	SPD REVISION	REV. 1.2	12	12
63	CHECKSUM FOR BYTES 0-62	(-13E) (-133) (-10E)	68 AE F6	69 AF F7
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C	2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)		FF	FF
72	MANUFACTURING LOCATION		01 02 03 04 05 06	01 02 03 04 05 06
73-90	MODULE PART NUMBER (ASCII)		xx	xx
91	PCB IDENTIFICATION CODE		01 02 03 04	01 02 03 04
92	IDENTIFICATION CODE (CONT.)	0	00	00
93	YEAR OF MANUFACTURE IN BCD		xx	xx
94	WEEK OF MANUFACTURE IN BCD		xx	xx
95-98	MODULE SERIAL NUMBER		xx	xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)			
126	SYSTEM FREQUENCY	100 MHz (-13E/-133/-10E)	64	64
127	SDRAM COMPONENT & CLOCK DETAIL		AF	FF

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.
3. The value of ^{t}RAS used for -13E modules is calculated from ^{t}RC - ^{t}RP. Actual device spec. value is 37ns.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

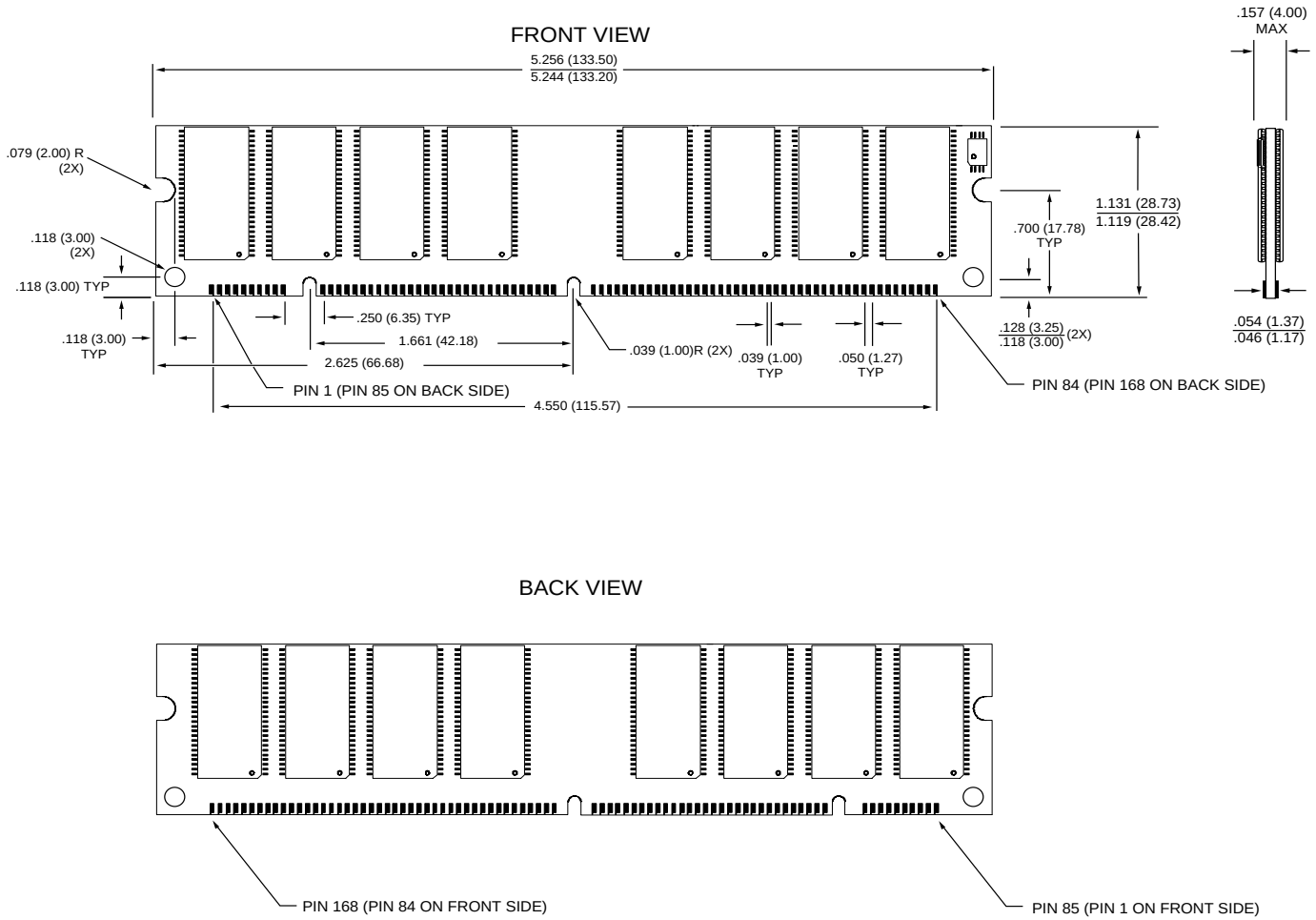
128MB MODULE



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

256MB MODULE



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

DATA SHEET DESIGNATION

Preliminary: This data sheet contains initial characterization limits that are subject to chage upon full characterization of production devices.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992

Micron is a registered trademark and the Micron logo and M logo are trademarks of Micron Technology, Inc.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2001, Micron Technology, Inc.

Micron Memory DRAM Module Reference Guide

Density	Description		Pins	Components on Module			Part Number	Speed	Height	Availability	
										Samples	Prod.
4MB	SS	1 Meg x 32 Gold SIMM/Tin SIMM	72	(2)	1 Meg x 16		MT2D132G/M (X)	50,60	.800"	Now	Now
4MB	SS	1 Meg x 32 3.3V Gold SODIMM	72	(2)	1 Meg x 16	3.3V TSOP	MT2LDT132HG (X)	60	1.000"	Now	Now
4MB	SS	1 Meg x 32 3.3V Gold DIMM	100	(2)	1 Meg x 16	3.3V TSOP	MT2LD132UG (X)	60	1.000"	Now	Now
8MB	DS	2 Meg x 32 Gold SIMM/Tin SIMM	72	(4)	1 Meg x 16		MT4D232DG/M (X)	50,60	.800"	Now	Now
8MB	SS	2 Meg x 32 3.3V Gold SODIMM	72	(4)	1 Meg x 16	3.3V TSOP	MT4LDT232HG (X)	60	1.000"	Now	Now
8MB	SS	2 Meg x 32 3.3V Gold DIMM	100	(4)	1 Meg x 16	3.3V	MT4LD232UG (X)	60	1.000"	Now	Now
8MB	SS	1 Meg x 64 3.3V Gold SODIMM	144	(4)	1 Meg x 16	3.3V TSOP	MT4LDT164HG (X)	60	1.000"	Now	Now
8MB	DS	1 Meg x 64 3.3V Gold DIMM	168	(4)	1 Meg x 16	3.3V TSOP	MT4LDT164AG (X)	60	1.000"	Now	Now
16MB	SS	4 Meg x 32 Gold SIMM/Tin SIMM	72	(8)	4 Meg x 4		MT8D432G/M (X)	50, 60	1.000"	Now	Now
16MB	SS	4 Meg x 36 ECC Gold SIMM/Tin SIMM	72	(9)	4 Meg x 4		MT9D436G/M (X)	50, 60	1.000"	Now	Now
16MB	DS	4 Meg x 32 3.3V Gold SODIMM	72	(8)	4 Meg x 4	3.3V TSOP	MT8LDT432HG (X)	60	1.000"	Now	Now
16MB	SS	4 Meg x 32 3.3V Gold SODIMM	72	(2)	4 Meg x 16	3.3V TSOP	MT2LDT432HG (X)	60	1.000"	Now	Now
16MB	SS	4 Meg x 32 3.3V Gold DIMM	100	(2)	4 Meg x 16	3.3V TSOP	MT2LDT432UG (X)	60	1.000"	Now	Now
32MB	DS	8 Meg x 32 Gold SIMM/Tin SIMM	72	(16)	4 Meg x 4		MT16D832G/M (X)	50, 60	1.000"	Now	Now
32MB	DS	8 Meg x 36 ECC Gold SIMM/Tin SIMM	72	(18)	4 Meg x 4		MT18D836G/M (X)	50, 60	1.000"	Now	Now
32MB	DS	8 Meg x 32 3.3V Gold SODIMM	72	(4)	4 Meg x 16	3.3V TSOP	MT4LDT832HG (X)	60	1.000"	Now	Now
32MB	DS	8 Meg x 32 3.3V Gold DIMM	100	(4)	4 Meg x 16	3.3V TSOP	MT4LDT832UG (X)	60	1.000"	Now	Now
32MB	DS	4 Meg x 64 3.3V Gold SODIMM	144	(4)	4 Meg x 16	3.3V TSOP	MT4LDT464HG (X)(S)	50,60	1.000"	Now	Now
32MB	SS	4 Meg x 64 3.3V Gold DIMM	168	(4)	4 Meg x 16	3.3V TSOP	MT4LDT464AG (X)	50,60	1.000"	Now	Now
32MB	DS	4 Meg x 64 3.3V Gold DIMM	168	(16)	4 Meg x 4	3.3V	MT16LD464AG (X)	60	1.000"	Now	Now
32MB	DS	4 Meg x 72 3.3V ECC Gold DIMM	168	(18)	4 Meg x 4	3.3V	MT18LD472(A)G (X)	60	Unbuff = 1.000", Buff = 1.000"	Now	Now
32MB	SS	4 Meg x 72 3.3V ECC Gold DIMM	168	(5)	4 Meg x 16	3.3V TSOP	MT5LDT472(A)G (X)	60	Unbuff = 1.000", Buff = 1.050"	Now	Now
64MB	DS	8 Meg x 64 3.3V Gold SODIMM	144	(8)	8 Meg x 8	3.3V TSOP	MT8LDT864HG (X)(S)	60	1.050"	Now	Now
64MB	DS	8 Meg x 64 3.3V Gold DIMM	168	(32)	4 Meg x 4	3.3V	MT32LD864AG (X)	60	1.500"	Now	Now
64MB	SS	8 Meg x 64 3.3V Gold DIMM	168	(8)	8 Meg x 8	3.3V	MT8LD864AG (X)	50, 60	1.100"	Now	Now
64MB	DS	8 Meg x 72 3.3V ECC Gold DIMM	168	(36)	4 Meg x 4	3.3V	MT36LD872(A)G (X)	60	Unbuff = 1.500", Buff = 1.500"	Now	Now
64MB	SS	8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V	MT9LD872(A)G (X)	50, 60	Unbuff = 1.100", Buff = 1.250"	Now	Now
64MB	SS	8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V TSOP	MT9LDT872G (X)	50, 60	1.350"	Now	Now
128MB	DS	16 Meg x 64 3.3V Gold DIMM	168	(16)	16 Meg x 4	3.3V	MT16LD1664AG (X)	50,60	1.250"	Now	Now
128MB	DS	16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 4	3.3V	MT18LD1672(A)G (X)	50,60	Unbuff = 1.250", Buff = 1.100"	Now	Now
128MB	DS	16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 4	3.3V TSOP	MT18LDT1672G (X)	50,60	2.000"	Now	Now
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(36)	16 Meg x 4	3.3V	MT36LD3272G (X)	50, 60	2.000"	Now	Now
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(36)	16 Meg x 4	3.3V TSOP	MT36LDT3272G (X)	50, 60	2.000"	Now	Now

Rev. 3/26/01

SS - Single Sided **DS** - Double Sided **G** - Gold Plated **M** - Tin Plated **U** - 100-pin DIMM **(H)** - Small-Outline DIMM (SODIMM)
(X) - EDO; no "X" denotes FPM version **(A)** - 8-CAS; SPD version; unbuffered (no "A" denotes buffered version for x72 DIMMs) **(S)** - Self Refresh

Micron Technology, Inc. reserves the right to change products or specifications without notice.

Micron Memory SDRAM Module Reference Guide

Density	Description	Pins	Components on Module			Base Part Number	Speed	Die Rev.	PCB (height)	MHz*	Availability		Notes
											Samples	Production	
4MB	SS 1 Meg x 32 3.3V Gold DIMM	100	(2)	1 Meg x 16	3.3V TSOP	MT2LSDT132UG	-10E1	E = Y72G	1 = 6649 (1.000")	100	Now	Now	
							-8E1			125	Now	Now	
	SS 1 Meg x 32 AIMM		(2)	1 Meg x 16	3.3V TSOP	MT2LSDT132AGP	-6E2	E = Y72G	2 = 0164B (1.4")	133	Now	Now	AIMM
	SS 1 Meg x 32 AIMM		(1)	2 Meg x 32	3.3V TSOP	MT1LSDT132AGP	-6E1	E = Y84W	1 = 0178 (1.4")	133	Now	Now	AIMM
8MB	DS 2 Meg x 32 3.3V Gold DIMM	100	(4)	1 Meg x 16	3.3V TSOP	MT4LSDT232UDG	-10E1	E = Y72G	1 = 6649 (1.000")	100	Now	Now	
							-8E1			125	Now	Now	
16MB	SS 4 Meg x 32 3.3V Gold DIMM	100	(2)	4 Meg x 16	3.3V TSOP	MT2LSDT432UG	-10C1	C = Y84	1 = 6660 (1.000")	100	Now	Now	
							-8C1			125	Now	Now	
32MB	DS 8 Meg x 32 3.3V Gold DIMM	100	(4)	4 Meg x 16	3.3V TSOP	MT4LSDT832UDG	-10C1	C = Y84	1 = 6660 (1.000")	100	Now	Now	
							-8C1			125	Now	Now	
32MB	DS 4 Meg x 64 3.3V Gold SODIMM	144*	(4)	4 Meg x 16	3.3V TSOP	MT4LSDT464HG	-662C1	C = Y84	1 = 6645 (1.150")	66	Now	Now	
							-662C2		2 = 6669 (1.000")	66	Now	Now	
							-10EC3		3 = 0118B (1.000")	100	Now	Now	PC100
							-10EC4		4 = 0180 (1.000")	100	Now	Now	PC100
							-133C4			133	Now	Now	PC133 rev 1.0
							-13EC4			133	Now	Now	PC133 rev 1.0
32MB	SS 4 Meg x 64 3.3V Gold DIMM	168	(4)	4 Meg x 16	3.3V TSOP	MT4LSDT464AG	-662C6	C = Y84	6 = 0134B (1.000")	66	Now	Now	
							-10CC6			100	Now	Now	
							-10EC6			100	Now	Now	
							-133C6			133	Now	Now	CL3
							-13EC6			133	Now	Now	CL2
32MB	SS 4 Meg x 72 3.3V ECC Gold DIMM	168*	(5)	4 Meg x 16	3.3V TSOP	MT5LSDT472AG	-662C6	C = Y84	6 = 0134B (1.000")	66	Now	Now	
							-10CC6			100	Now	Now	
							-10EC6			100	Now	Now	
							-133C6			133	Now	Now	CL3
							-13EC6			133	Now	Now	CL2
64MB	DS 16 Meg x 32 3.3V Gold DIMM	100	(4)	16 Meg x 8	3.3V TSOP	MT4LSDT1632UG	-10B1	B = Y85B	1 = 6692(1.15")	100	Now	Now	
							-8B1	E = Y95C		125	Now	Now	
							-10E1			100	Now	Now	
							-8E1			125	Now	Now	
			(4)	8 Meg x 16	3.3V TSOP	MT4LSDT1632UDG	-10B1	B = Y85B	1 = 6660(1.00")	100	Now	Now	
							-8B1	F = Y95W		125	Now	Now	
							-10F1			100	2Q01	3Q01	
							-8F1			125	2Q01	3Q01	
64MB	DS 8 Meg x 64 3.3V Gold SODIMM	144*	(8)	8 Meg x 8	3.3V TSOP	MT8LSDT864HG	-662C3	C = Y84	3 = 6678 (1.050")	66	Now	Now	
			(8)	4 Meg x 16	3.3V TSOP		-10EC5		5 = 0115C (1.250")	100	Now	Now	PC100
64MB	DS 8 Meg x 64 3.3V Gold SODIMM	144*	(4)	8 Meg x 16	3.3V TSOP	MT4LSDT864HG	-662B1	B = Y85B	1 = 0118B (1.000")	66	Now	Now	
							-10EB1	F = Y95W	2 = 0180 (1.000")	100	Now	Now	PC100
							-10EB2			100	Now	Now	PC100
							-133B2			133	Now	Now	PC133 rev 1.0
							-13EB2			133	Now	Now	PC133 rev 1.0
							-10EF2			100	2Q01	3Q01	
							-133F2			133	2Q01	3Q01	
							-13EF2			133	2Q01	3Q01	
64MB	SS 8 Meg x 64 3.3V Gold DIMM	168	(8)	8 Meg x 8	3.3V TSOP	MT8LSDT864AG	-662C7	C = Y84	7 = 0104B (1.375")	66	Now	Now	
							-10CC7			100	Now	Now	
							-10EC7			100	Now	Now	
							-133C7			133	Now	Now	CL3
							-13EC7			133	Now	Now	CL2
64MB	SS 8 Meg x 64 3.3V Gold DIMM	168	(4)	8 Meg x 16	3.3V TSOP	MT4LSDT864AG	-662B1	B = Y85B	1 = 0134B (1.00")	66	Now	Now	
							-10CB1	F = Y95W		100	Now	Now	
							-10EB1			100	Now	Now	
							-133B1			133	Now	Now	CL3
							-13EB1			133	Now	Now	CL2
							-10EF1			100	2Q01	3Q01	
							-133F1			133	2Q01	3Q01	
							-13EF1			133	2Q01	3Q01	
	DS 8 Meg x 64 3.3V Gold DIMM	144	(4)	8 Meg x 16	3.3V TSOP	MT4LSDT864WG	-133F1	F = Y95W	1 = 0182 (1.18")	133	2Q01	3Q01	Micro DIMM
64MB	SS 8 Meg x 72 3.3V Gold DIMM	168	(5)	8 Meg x 16	3.3V TSOP	MT5LSDT872AG	-10EB1	B = Y85B	1 = 0134B (1.00")	100	Now	Now	
							-133B1	F = Y95W		133	Now	Now	CL3
							-13EB1			133	Now	Now	CL2
							-10EF1			100	2Q01	3Q01	
							-133F1			133	2Q01	3Q01	
							-13EF1			133	2Q01	3Q01	
64MB	SS 8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V TSOP	MT9LSDT872AG	-662C7	C = Y84	7 = 0104B (1.375")	66	Now	Now	
							-10CC7			100	Now	Now	
							-10EC7			100	Now	Now	
							-133C7			133	Now	Now	CL3
							-13EC7			133	Now	Now	CL2
64MB	SS 8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V TSOP	MT9LSDT872G	-10CC3	C = Y84	3 = 0144 (1.500")	100	Now	Now	
							-10EC3			100	Now	Now	
							-133C3			133	Now	Now	CL3
							-13EC3			133	Now	Now	CL2
128MB	DS 32 Meg x 32 3.3V Gold DIMM	100	(8)	16 Meg x 8	3.3V TSOP	MT8LSDT3232UG	-10B1	B = Y85B	1 = 6692 (1.15")	100	Now	Now	
							-8B1	E = Y95C		125	Now	Now	
							-10E1			100	Now	Now	
							-8E1			125	Now	Now	
			(8)	8 Meg x 16	3.3V TSOP	MT8LSDT3232UDG	-10B1	B = Y85B	1 = TBD (1.15")	100	TBD	TBD	
							-8B1	F = Y95W		125	TBD	TBD	
							-10F1			100	TBD	TBD	
							-8F1			125	TBD	TBD	
128MB	DS 16 Meg x 64 3.3V Gold SODIMM	144	(8)	8 Meg x 16	3.3V TSOP	MT8LSDT1664HG	-10CB1	B = Y85B	1 = 0115C (1.25")	100	Now	Now	PC100
							-10EB1	F = Y95W	2 = 6678 (1.050")	100	Now	Now	PC100
				16 Meg x 8	3.3V TSOP		-662B2		3 = 0179 (1.25")	66	Now	Now	
				8 Meg x 16	3.3V TSOP		-10EB3			100	Now	Now	PC100
							-133B3			133	Now	Now	PC133 rev 1.0
							-13EB3			133	Now	Now	PC133 rev 1.0
							-10EF3			100	2Q01	3Q01	
							-133F3			133	2Q01	3Q01	
							-13EF3			133	2Q01	3Q01	
128MB	DS 16 Meg x 64 3.3V Gold DIMM	168	(16)	8 Meg x 8	3.3V TSOP	MT16LSDT1664AG	-662C7	C = Y84	7 = 0104B(1.375")	66	Now	Now	
							-10CC7			100	Now	Now	
							-10EC7			100	Now	Now	
							-133C7			133	Now	Now	CL3
							-13EC7			133	Now	Now	CL2
128MB	DS 16 Meg x 64 3.3V Gold DIMM	168	(8)	16 Meg x 8	3.3V TSOP	MT8LSDT1664AG	-10CB1	B = Y85B	1 = 0104B(1.375")	100	Now	Now	
							-10EB1	E = Y95C		100	Now	Now	
							-133B1			133	Now	Now	CL3
							-13EB1			133	Now	Now	CL2
							-10EE1			100	Now	Now	
							-133E1			133	Now	Now	CL3
							-13EE1			133	Now	Now	CL2
	SS 16 Meg x 64 3.3V Gold DIMM	168	(4)	16 Meg x 16	3.3V TSOP	MT4LSDT1664AG	-10EB1	B = Y96	1 = TBD (1.00")	100	2Q01	3Q01	
							-133B1			133	2Q01	3Q01	
							-13EB1			133	TBD	TBD	
	DS 16 Meg x 64 3.3V Gold DIMM	144	(4)	16 Meg x 16	3.3V TSOP	MT4LSDT1664WG	-133B1	B = Y96	1 = 0182 (1.18")	133	2Q01	3Q01	Micro DIMM
	DS 16 Meg x 64 3.3V Gold DIMM	144	(4)	16 Meg x 16	3.3V TSOP	MT4LSDT1664HG	-10EB1	B = Y96	1 = 0180 (1.00")	100	2Q01	3Q01	
							-133B1			133	2Q01	3Q01	
							-13EB1			133	TBD	TBD	
128MB	DS 16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	8 Meg x 8	3.3V TSOP	MT18LSDT1672AG	-662C7	C = Y84	7 = 0104B(1.375")	66	Now	Now	
							-10CC7			100	Now	Now	
							-10EC7			100	Now	Now	
							-133C7			133	Now	Now	CL3
							-13EC7			133	Now	Now	CL2
128MB	SS 16 Meg x 72 3.3V ECC Gold DIMM	168	(9)	16 Meg x 8	3.3V TSOP	MT9LSDT1672AG	-10CB1	B = Y85B	1 = 0104B(1.375")	100	Now	Now	
							-10EB1	E = Y95C		100	Now	Now	
							-133B1			133	Now	Now	CL3
							-13EB1			133	Now	Now	CL2
							-10EE1			100	Now	Now	
							-133E1			133	Now	Now	CL3
							-13EE1			133	Now	Now	CL2
	SS 16 Meg x 72 3.3V ECC Gold DIMM	168	(5)	32 Meg x 8	3.3V TSOP	MT5LSDT1672AG	-10EB1	B = Y96	1 = TBD (1.00")	100	2Q01	3Q01	
							-133B1			133	2Q01	3Q01	
							-13EB1			133	TBD	TBD	
		168	(9)	16 Meg x 8	3.3V TSOP	MT9LSDT1672G	-10CB1	B = Y85B	1 = 0144(1.500")	100	Now	Now	
							-10EB1	E = Y95C		100	Now	Now	
							-133B1		2 = 0198(1.125")	133	Now	Now	CL3

									-13EB1			133	Now	Now	CL2
									-10EE1			100	Now	Now	
									-133E1			133	Now	Now	CL3
									-13EE1			133	Now	Now	CL2
	DS								-10EE2			100	2Q01	3Q01	1U
									-133E2			133	2Q01	3Q01	1U
									-13EE2			133	2Q01	3Q01	1U
128MB	DS	16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 4	3.3V TSOP	MT18LSDT1672G	-10CC2	C = Y84	2 = 0129 (1.700")	100	Now	Now	
								-10EC2			100	Now	Now	
								-133C2			133	Now	Now	CL3
								-13EC2			133	Now	Now	CL2
256MB	DS	32 Meg x 64 3.3V Gold DIMM	168	(16)	16 Meg x 8	3.3V TSOP	MT16LSDT3264AG	-10CB1	B = Y85B	1 = 0104B (1.375")	100	Now	Now	
								-10EB1	E = Y95C		100	Now	Now	
								-133B1			133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	DS	32 Meg x 64 3.3V Gold SODIMM	144	(8)	16 Meg x 16	3.3V TSOP	MT8LSDT3264HG	-10EB1	B = Y96	1 = 0179 (1.25")	100	Now	Now	PC100
								-133B1			133	Now	Now	PC133 rev 1.0
	SS	32 Meg x 64 3.3V Gold DIMM	168	(8)	32 Meg x 8	3.3V TSOP	MT8LSDT3264AG	-10EB1	B = Y96	1 = TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
	DS	32 Meg x 64 3.3V Gold SODIMM	144	(8)	32 Meg x 8	3.3V fBGA	MT8LSDF3264WG	-133B1	B = Y96	1 = 0189 (1.25")	133	3Q01	4Q01	Micro DIMM
	DS	32 Meg x 64 3.3V Gold SODIMM	144	(16)	16 Meg x 8	3.3V fBGA	MT16LSDF3264HG	-10EB2	B = Y85B	2 = 0155 (1.25")	100	Now	Now	
								-133B2	E = Y95C	3 = 0185 (1.25")	133	Now	Now	
								-10EE3			100	2Q01	3Q01	
								-133E3			133	2Q01	3Q01	
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 8	3.3V TSOP	MT18LSDT3272AG	-10CB1	B = Y85B	1 = 0104B (1.375")	100	Now	Now	
								-10EB1	E = Y95C		100	Now	Now	
								-133B1			133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(18)	32 Meg x 4	3.3V TSOP	MT18LSDT3272G	-10EB1	B = Y85B	1 = 0129 (1.700")	100	Now	Now	
								-133B1	E = Y95C		133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 8	3.3V TSOP	MT18LSDT3272DG	-10EB1	B = Y85B	1 = 0156 (1.7")	100	Now	Now	
								-133B1	E = Y95C		133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	SS	32 Meg x 72 3.3V ECC Gold DIMM	168	(9)	32 Meg x 8	3.3V TSOP	MT9LSDT3272AG	-10EB1	B = Y96	1 = TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
	SS	32 Meg x 72 3.3V ECC Gold DIMM	168	(9)	32 Meg x 8	3.3V TSOP	MT9LSDT3272G	-10EB1	B = Y96	1 = TBD (1.70")	100	2Q01	3Q01	
								-133B1		2 = 0198(1.125")	133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
	DS							-10EB2			100	2Q01	3Q01	1U
								-133B2			133	2Q01	3Q01	1U
								-13EB2			133	TBD	TBD	1U
512MB	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(36)	32 Meg x 4	3.3V FBGA	MT36LSDF6472G	-10EB1	B = Y85B	1 = 0123(1.70")	100	Now	Now	11x13pkg
								-133B2		2 = 0142(1.70")	133	Now	Now	CL3
	DS	64 Meg x 64 3.3V Gold DIMM	168	(16)	32 Meg x 8	3.3V TSOP	MT16LSDT6464AG	-10EB1	B = Y96	1 = TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2
	DS	64 Meg x 64 3.3V Gold DIMM	144	(16)	32 Meg x 8	3.3V FBGA	MT16LSDF6464HG	-10EB1	B = Y96	1 = 0185 (1.25")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	32 Meg x 8	3.3V TSOP	MT18LSDT6472AG	-10EB1	B = Y96	1 =TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	64 Meg x 4	3.3V TSOP	MT18LSDT6472G	-10EB1	B = Y96	1 = 0129 (1.700")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	32 Meg x 8	3.3V TSOP	MT18LSDT6472DG	-10EB1	B = Y96	1 =0156 (1.70")	100	2Q01	3Q01	
								-133B1		2 =0198 (1.125")	133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
								-10EB2			100	2Q01	3Q01	1U
								-133B2			133	2Q01	3Q01	1U
								-13EB2			133	TBD	TBD	1U
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	64 Meg x 4	3.3V FBGA	MT18LSDF6472G	-10EB1	B = Y96	1 = 0187 (1.05")	100	2Q01	3Q01	1U
								-133B1			133	2Q01	3Q01	1U
								-13EB1			133	TBD	TBD	1U
1GB	DS	128 Meg x 72 3.3V ECC Gold DIMM	168	(36)	64 Meg x 4	3.3V fBGA	MT36LSDF12872G	-10EB1	B = Y96	1 = TBD (1.700")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2

a	b
Part Number = a + b	
Example: MT36LSDF12872G-13EB1	

Rev. 3/26/01

*For 168-pin DIMMs (66 MHz/100 MHz), adheres to Intel's 4-Clock SDRAM module specs (66 MHz will use -10 components; 100 MHz will use -8 components). For 100-pin DIMMs, 100 MHz uses -10 components; adheres to JEDEC standard.

SS - Single Sided **DS** - Double Sided **G** - Gold Plated **U** - 100-pin DIMM **UDG** - Double-sided, dual-bank 100-pin DIMM
(H) - Small-Outline DIMM (SODIMM) **LP** - Low Power **(A)** - 8-CAS; SPD version; unbuffered (no "A" denotes registered version for x72 DIMMs)
(W) - Micro DIMM

Intel is a registered trademark of Intel Corporation. Micron Technology, Inc. reserves the right to change products or specifications without notice.

Micron Memory DDR SDRAM Module Reference Guide

Density	Description		Pins	Components on Module			Base Part Number	Speed	Die Rev.	PCB (height)	MHz	Availability	
												Samples	Production
64MB	SS	8 Meg x 64 2.5V Gold SODIMM	200	(4)	8 Meg x 16	TSOP	MT4VDDT864HG	-202B1	B = T95	1 = 0175 (1.25")	200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	SS	8 Meg x 64 2.5V Gold DIMM	184	(4)	8 Meg x 16	TSOP	MT4VDDT864AG	-202B1	B = T95	1 = 0151 (1.0")	200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	8 Meg x 64 2.5V Gold DIMM	172	(4)	8 Meg x 16	TSOP	MT4VDDT864WG	-202B1	B = T95	1 = 0207 (1.25")	200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
128MB	SS	16 Meg x64 2.5V Gold DIMM	184	(8)	16 Meg x 8	TSOP	MT8VDDT1664AG	-202A1	A = T85	1 = 0161 (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	16 Meg x64 2.5V Gold SODIMM	200	(8)	16 Meg x 8	TSOP	MT8VDDT1664HG	-202A1	A = T85	1 = 0168(1.25")	200	Contact Mktg	Contact Mktg
								-265A1			266	Contact Mktg	Contact Mktg
	DS	16 Meg x64 2.5V Gold SODIMM	200	(8)	8 Meg x 16	TSOP	MT8VDDT1664HG	-202B2	B = T95	2 = 0174 (1.25")	200	2Q01	3Q01
								-265B2			266	2Q01	3Q01
								-262B2			266	TBD	TBD
	SS	16 Meg x 64 2.5V Gold SODIMM	200	(4)	16 Meg x 16	TSOP	MT4VDDT1664HG	-202A1	A = T96	1 = 0175 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	SS	16 Meg x 64 2.5V Gold SODIMM	184	(4)	16 Meg x 16	TSOP	MT4VDDT1664AG	-202A1	A = T96	1 = 0151 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS	16 Meg x 64 2.5V Gold SODIMM	172	(4)	16 Meg x 16	TSOP	MT4VDDT1664WG	-202A1	A = T96	1 = 0207 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
	SS	16 Meg x72 ECC 2.5V Gold DIMM	184	(9)	16 Meg x 8	TSOP	MT9VDDT1672AG	-202A1	A = T85	1 = 0161 (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	SS	16 Meg x72 ECC 2.5V Gold DIMM	184	(5)	16 Meg x 16	TSOP	MT5VDDT1672AG	-202A1	A = T96	1 = 0151 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	SS	16 Meg x72 ECC 2.5V Gold DIMM	184	(9)	16 Meg x 8	TSOP	MT9VDDT1672G	-202A1	A = T85	1 = 0162 (1.70")	200	Now	Now
								-265A1	B = T95	2 = TBD (1.2")	266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS							-202A2			200	2Q01	3Q01
								-265A2			266	2Q01	3Q01
								-202B2			200	2Q01	3Q01
								-265B2			266	2Q01	3Q01
256MB	DS	32 Meg x64 2.5V Gold DIMM	184	(16)	16 Meg x 8	TSOP	MT16VDDT3264AG	-202A1	A = T85	1 = 0116B (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	32 Meg x64 2.5V Gold SODIMM	200	(8)	16 Meg x 16	TSOP	MT8VDDT3264HG	-202A1	A = T96	1 = 0174 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	SS	32 Meg x64 2.5V Gold SODIMM	184	(8)	32 Meg x 8	TSOP	MT8VDDT3264AG	-202A1	A = T96	1 = 0161 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
256MB	DS	32 Meg 72 ECC 2.5V Gold DIMM	184	(18)	16 Meg x 8	TSOP	MT18VDDT3272AG	-202A1	A = T85	1 = 0116B (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	32 Meg 72 ECC 2.5V Gold DIMM	184	(18)	32 Meg x 4	TSOP	MT18VDDT3272G	-202A1	A = T85	1 = 0163 (1.70")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	32 Meg 72 ECC 2.5V Gold DIMM	184	(18)	16 Meg x 8	TSOP	MT18VDDT3272DG	-202A1	A = T85	1 = 0162 (1.70")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	SS		184	(9)	32 Meg x 8	TSOP	MT9VDDT3272AG	-202A1	A = T96	1 = 0161 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			200	TBD	TBD
	DS		184	(9)	32 Meg x 8	TSOP	MT9VDDT3272G	-202A1	A = T96	1 = TBD (1.2")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			200	TBD	TBD
512MB	DS	64 Meg 64 2.5V Gold DIMM	184	(16)	32 Meg x 8	TSOP	MT16VDDT6464AG	-202A1	A = T96	1 = 0116B (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS	64 Meg 72 ECC 2.5V Gold DIMM	184	(18)	32 Meg x 8	TSOP	MT18VDDT6472AG	-202A1	A = T96	1 = 0116B (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS	64 Meg 72 ECC 2.5V Gold DIMM	184	(18)	32 Meg x 8	TSOP	MT18VDDT6472DG	-202A1	A = T96	1 = 0162 (1.70")	200	2Q01	3Q01
								-265A1		2 = TBD (1.2")	266	2Q01	3Q01
								-262A1			266	TBD	TBD
								-202A2			200	2Q01	3Q01
								-265A2			266	2Q01	3Q01
	DS	64 Meg 72 ECC 2.5V Gold DIMM	184	(18)	64 Meg x 4	TSOP	MT18VDDT6472G	-202A1	A = T96	1 = 0163 (1.70")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS		184	(18)	64 Meg x 4	FBGA	MT18VDDF6472G	-202A1	A = T96	1 = TBD (1.125")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
1GB	DS	128 Meg 72 ECC 2.5V Gold DIMM	184	(36)	64 Meg x 4	FBGA	MT36VDDF12872G	-202A1	A = T96	1 = 0173 (1.70")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD

a	b
Part Number = a + b	
Example MT36VDDT6472G-262B1	

SS - Single Sided **DS** - Double Sided **G** - Gold Plated
(H) - Small-Outline DIMM (SODIMM) **(A)** - 8-CAS; SPD version; unbuffered (no "A" denotes registered version for x72 DIMMs)

Micron Memory Rambus® RIMM™ Module Reference Guide

Density	Description		Pins	Components on Module		Base Part Number	Speed	Die Rev.	PCB (height)	MHz	Availability	
											Samples	Production
128MB	SS	64 Meg x 16 non-ECC	184	(4)	16 Meg x 16	MT4VR6416AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
128MB	SS	32 Meg x 18 ECC	184	(4)	16 Meg x 18	MT4VR6418AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
256MB	SS	64 Meg x 16 non-ECC	184	(8)	16 Meg x 16	MT8VR12816AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
256MB	SS	64 Meg x 18 ECC	184	(8)	16 Meg x 18	MT8VR12818AG	-653A1	A = R96A	1 =TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
512MB	DS	128 Meg x 16 non-ECC	184	(16)	16 Meg x 16	MT16VR25616AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
512MB	DS	128 Meg x 18 ECC	184	(16)	16 Meg x 18	MT16VR25618AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD

a	b
Part Number = a + b	
Example MT16VR25618AG-840A1	

Rev. 3/26/01

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP