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bc635VME/bc350VXI
TIME AND FREQUENCY PROCESSOR

Operation and Technical Manual

October 1994

datum inc
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bc635VME/bc350VXI
TIME AND FREQUENCY PROCESSOR

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CHAPTER 1
INTRODUCTION

1.0 GENERAL

This bc635VME / bc350VXI *T*ime and *F*requency *P*rocessor (TFP) Operation and Technical Manual provides the following information:

Introduction and key feature description

Installation and setup

Detailed operation and programming interfaces

Input and output signals

Programming examples

Drawing set

1.1 KEY FEATURES

The TFP has been designed with the following key features:

Time on demand (days through 0.1 microseconds) with zero latency. This feature is implemented with hardware registers which latch the current time upon host request

Event logging (days through 0.1 microseconds). This feature is implemented with a second set of hardware registers. Time is captured on a positive or negative input edge.

Six operational modes are supported. Modes are distinguished by the reference source.

MODE	SOURCE OF SYNCHRONIZATION
0	Timecode - IRIGA IRIGB XR3 2137 NASA36 (modulated or DC)
1	Free running - on board VCXO used as reference
2	1 PPS - accepts input one pulse per second
3	RTC - uses battery backed on board real time clock IC
5	GPS (optional) - double wide configuration including GPS receiver
6	GPS (optional) - uses GPS receiver / antenna (receiver in antenna)

Provides an output clock synchronized to the selected reference; programmable 1,5, or 10 MHz TTL.

All modes of operation are supplemented by flywheel operation i.e. If synchronization source is lost the TFP will continue to function at the last known reference rate.

Generates synchronized IRIGB timecode; modulated and DC level shift formats are produced simultaneously.

Programmable frequency output (periodics) is provided. The output frequency is 10,000,000 / (n1 * n2). 1<n1<65536 & 1<n2<65536

A time coincidence strobe output is provided. Programmable from days through milliseconds. This strobe also has an each second mode programmable to milliseconds.

Five maskable interrupt sources are supported. IRQ levels 1 through 7 are programmable.

INT#	SOURCE OF INTERRUPT
0	External event input has occurred
1	A periodic output has occurred
2	The time coincidence strobe has occurred
3	A one second epoch (1 PPS output) has occurred
4	An output data packet is available

Time of day, hours, minutes, and seconds, are displayed on front panel LED's.

Most inputs and outputs are accessible via the P2 connector.

1.2 PHYSICAL AND FUNCTIONAL OVERVIEW

The TFP is a B size module (6U X 160 mm) . Operation is controlled by a block of 32 D16 registers written and read by the host via the VMEbus (A16 : D16). The TFP is available in two versions. The bc635VME is intended for use in a VMEbus system with most I/O signals available on rows A and C of the P2 connector. The bc350VXI is intended for use in a VXIbus system, and is shipped without a P2 connector. A dip switch is used to select VME or VXI compatibility. In VMEbus systems the register block can be located on any 64 byte boundary. In VXIbus systems the register block can be located at any of the 256 Logical Addresses (A15 and A14 must be high). The Logical Address is returned during an interrupt acknowledge cycle.

1.3 PERFORMANCE SPECIFICATIONS

1.3.1 TIMECODE READER

FORMAT	IRIGA IRIGB XR3 2137 NASA36
CARRIER RANGE	+/- 50 PPM
FLYWHEEL ACCURACY	drift < 2 millisecond per hour (applies to all operational modes)
MODULATION RATIO	3:1 to 6:1
INPUT AMPLITUDE	0.5 to 5 volts peak to peak
INPUT IMPEDANCE	10K ohms AC coupled

1.3.2 TIMECODE GENERATOR

FORMAT	IRIGB
MODULATION RATIO	3:1
OUTPUT AMPLITUDE	0 to10 volts peak to peak
DC LEVEL SHIFT	TTL / CMOS compatible

1.3.3 BUS CHARACTERISTICS

ADDRESS SPACE	A16, AM codes $29 and $2D, 64 bytes
DATA TRANSFER	D16
INTERRUPTER	D08(0), I(1-7), ROAK
POWER	+5 @ 1.5amps +12 @ 50 milliamp -12 @ 30 milliamp

1.3.4 DIGITAL INPUTS

EVENT CAPTURE	TTL / CMOS positive or negative edge triggered
	20 nanoseconds min.width 250 nanoseconds min. period
EXTERNAL 1PPS	TTL / CMOS positive edge on time
	20 nanoseconds minimum width

1.3.5 DIGITAL OUTPUTS

1 PPS	TTL / CMOS positive edge on time
PERIODICS	TTL / CMOS positive edge on time
STROBE	TTL / CMOS positive edge on time
1, 5, 10 MHz clock	TTL / CMOS positive edge on time

1.3.6 EXTERNAL 10 MHz INPUT

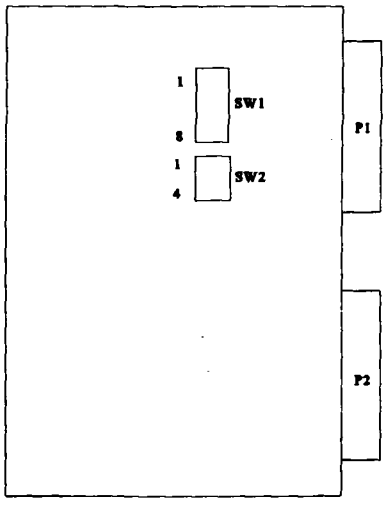
DIGITAL INPUT (or)	TTL / CMOS 45% to 55% duty cycle
SINEWAVE INPUT	1.2 to 4 volts peak to peak

1.3.7 ENVIRONMENTAL SPECIFICATIONS

TEMPERATURE	OPERATING	0 to 70 degrees centigrade
	NON-OPERATING	-50 to 125 degrees centigrade
RELATIVE HUMIDITY	OPERATING	5% to 95% non-condensing
ALTITUDE	OPERATING	-400 to 18,000 meters MSL

CHAPTER 2
INSTALLATION AND SETUP

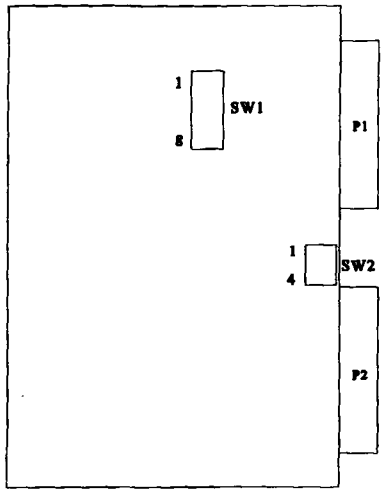
2.0 VME / VXI COMPATIBILITY SWITCHES



SW1 and SW2 LOCATION REVA thru REVD

The TFP is designed for both VMEbus and VXIbus compatibility. Switches SW2-3 and SW2-4 are used to select the bus protocol. To select VXIbus compatibility set SW2-3 and SW2-4 to the *OPEN* or *OFF* position. To select VMEbus compatibility set SW2-3 and SW2-4 to the *CLOSED* or *ON* position.

Switch SW2-3 controls the register block addressing within the A16 address space. With this switch in the VXI position, address bits A14 and A15 must be 1 for A16 selection. Switch SW1 is then used to select the Logical Address for the module. With SW2-3 in the VME position, the module can be mapped to any 64 byte block in the A16 address space. SW2-1 and SW2-2 set the A14 and A15 address bits, and SW1 is used to set the A13 through A6 address bits.



SW1 and SW2 LOCATION REVE

Switch SW2-4 controls the status / ID byte returned during interrupt acknowledge cycles. With SW2-4 in the VXI position, the Status / ID byte returned during interrupt acknowledge cycles is the Logical Address set with SW1. When SW2-4 is in the VME position, the Status / ID byte returned during interrupt acknowledge cycles is the user programmable vector loaded into the VECTOR register (discussed in *CHAPTER 3).*

2.1 VMEbus BASE ADDRESS SELECTION

Base address selection for the VMEbus requires the setting of switch SW1 (A6 thru A13) and SW2 (A14 and A15). The bc635VME occupies 64 bytes in the A16 address space and can be freely located on any 64 byte boundary. The correspondence of the switch positions to the address bits is illustrated below.

	SW2		SW1								A16 address range used. (The *BASE* address is on the left.)
Address Bit	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	
Switch Number	2	1	8	7	6	5	4	3	2	1	
Example switch settings for SW1 and SW2.	0	0	0	0	0	0	0	0	0	0	0x0000 - 0x003F
	0	0	0	0	0	0	0	0	0	1	0x0040 - 0x007F
1 = OPEN or OFF	0	0	0	0	0	0	0	0	1	0	0x0080 - 0x00BF
0 = CLOSED or ON	0	0	0	0	0	0	0	0	1	1	0x00C0 - 0x00FF
	0	0	0	0	0	0	0	1	0	0	0x0100 - 0x013F
	...	...	...	...	...	...	...	...	...	...	...
	...	...	...	...	...	...	...	...	...	...	...
	1	1	1	1	1	1	1	0	1	1	0xFEC0 - 0xFEFF
	1	1	1	1	1	1	1	1	0	0	0xFF00 - 0xFF3F
	1	1	1	1	1	1	1	1	0	1	0xFF40 - 0xFF7F
	1	1	1	1	1	1	1	1	1	0	0xFF80 - 0xFFBF
	1	1	1	1	1	1	1	1	1	1	0xFFC0 - 0xFFFF

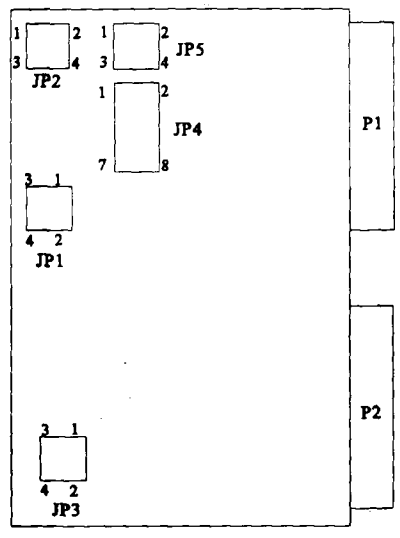
To select a base address set each of the switches to the logical zero (*CLOSED* or *ON*) or the logical one (*OPEN* or *OFF*) state.

2.2 bc350VXI LOGICAL ADDRESS SELECTION

Logical Address selection for the VXIbus requires the setting of switch SW1 (A6 thru A13). The bc350VXI occupies 64 bytes in the A16 address space and can be located at any of the 256 Logical Addresses within the VXIbus. The correspondence between the switch positions and the address bits, and the logical state corresponding to a switch setting follows the description provided in *SECTION 2.1.*

2.3 JUMPERS (default setting in bold type)

The jumper locations for the REV A thru REV C TFP versions are shown in the adjacent illustration. The jumper blocks are not drawn to scale in order to make the numbers more visible. It might be helpful to refer to the schematic diagrams to obtain a clearer idea of the function of each jumper option.



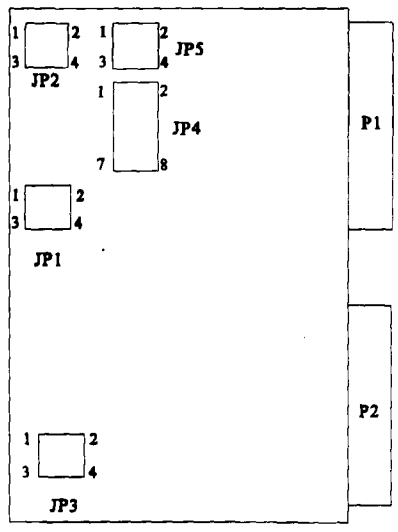
JUMPER LOCATION REV A thru REV C

JP1
With the jumper in the 1-2 position the TFP is configured to use DC level shift input timecode. In the **3-4** or open position the TFP is configured to use modulated timecode.

JP2 (GPS OPTION)
In the **1-2** position the TFP is configured to use a single ended 1PPS GPS input. In the 3-4 position the TFP is configured to use a differential 1PPS GPS input.

JP3 (GPS OPTION)
In the **1-2** position the TFP is configured to use the ACUTIME Smart Antenna or SV-6 as the GPS sensor. In the 3-4 position the TFP is configured to use the TANS as the GPS sensor.
The ACUTIME, SV-6, and TANS are GPS sensors manufactured by Trimble Navigation Inc.

JP4
The jumpers in the JP4 group are designed to be moved as a pair. That is positions **3-4 and 5-6** define one configuration, and positions 1-2 and 7-8 define a second configuration. In the default configuration the TFP is configured with an auxiliary RS-422 output. In the second configuration the TFP as configured in a daisy-chain mode (the RS-422 input is jumpered to the RS-422 output. This jumper set is intended to be used in a digital synchronization mode. At the present time this mode has not been implemented.



JUMPER LOCATION REV D & UP

JP5
In the **1-2** position this jumper places a 100 ohm load between the RS-422 input lines. In the 3-4 position the 100 ohm load is by-passed. When the TFP is the terminal device on an RS-422 daisy chain the load should be used. When the TFP is

not at the end of the chain the load should be omitted.

2.4 INSTALLATION

To install the TFP into a computer chassis follow the steps below.

Remove the IACKIN*/IACKOUT* back plane jumper for the TFP slot. This step should be performed even if TFP interrupts are not used.

bc635VME users must verify that signals on rows A and C of the P2 connector are not used for VSB or other purposes. The TFP provides signal I/O on row A and C that may produce a conflict. If a conflict does exist, a solution is to obtain a bc635VME with the P2 connector removed.

Verify that power is off and insert the TFP into the chassis, securing it in the slot by tightening the two front panel screws.

CHAPTER 3
INTERFACES

3.0 GENERAL

The TFP occupies 64 bytes in the VMEbus / VXIbus A16 address space. Refer to *SECTION 2.1* for details on VMEbus base address selection, and to *SECTION 2.2* for VXIbus Logical Address selection. TFP data transfers are D16 with the exception of packet I/O which allows D08(0) transfers. A glossary of key terms commonly used in the discussion of timing operation is provided below.

EPOCH
A reference time or event. Epoch often refers to a one pulse per second event.

FLYWHEEL
To maintain time or frequency accuracy as well as local resources allow when a time or frequency reference has been lost or removed.

PERIODIC
A programmable frequency which is obtained by dividing the TFP reference frequency. Periodics are sometimes referred to as 'heartbeats'. Periodics may optionally be synchronous with the 1PPS epoch if the period is expressible as a ratio of integers.

MAJOR TIME
Units of time larger than or equal to seconds. A *day hr:min:sec* format is usually implied.

MINOR TIME
Subsecond time to whatever resolution is supported.

PACKET
A group of bytes conforming to a defined structure. Packets are usually used in bit serial or byte serial data transmission to allow framing of the transmitted data.

3.1 DATA INPUT AND OUTPUT

Communication with the TFP is performed using a set of memory mapped registers. These registers may be *read only (R), write only (W), or read/write (R/W)*. In some cases a *read/write* register is structured to support dissimilar data in the *read* and *write* directions. The table below summarizes the type of register located at each hexadecimal offset, and provides a brief description of the register function. The data format and detailed descriptions of each register are provided in the next section.

TFP REGISTER MAP SUMMARY			
HEX OFFSET	*TYPE*	*LABEL*	*FUNCTION READ / WRITE*
0	R	ID Reg.	VXIbus ID Register
2	R	Device	VXIbus Device Type Register
4	R/W	Status / Control	VXIbus Status / Control Registers
6-08	reserved		
0A	R	TIMEREQ	Time Request (Time Latching Strobe)
0C	R	TIME0	Requested Time (includes status byte)
0E	R	TIME1	Requested Time
10	R	TIME2	Requested Time
12	R	TIME3	Requested Time
14	R	TIME4	Requested Time
16	R	EVENT0	Event Time
18	R/W	EVENT1 / STROBE1	Event Time / Strobe Time
1A	R/W	EVENT2 / STROBE2	Event Time / Strobe Time
1C	R/W	EVENT3 / STROBE3	Event Time / Strobe Time
1E	R	EVENT4	Event Time
20	R/W	UNLOCK	Release Lockout / Capture Time
22	R/W	ACK	Acknowledge Register
24	R/W	CMD	Command Register
26	R/W	FIFO	FIFO Input / Output (D16 or D08(O))
28	R/W	MASK	Interrupt Mask
2A	R/W	INTSTAT	Interrupt Status
2C	R/W	VECTOR	Interrupt Vector
2E	R/W	LEVEL	Interrupt Level
30-3E	reserved		

OFFSET 0x00 *ID Reg.* *RESET VALUE 0xFEF4*

This register was implemented to satisfy the VXIbus Specification. Bit assignments are as follows.

bit #	15-14	13-12	11-0
use of field	device class	addressing modes	manufacturer's ID
TFP meaning	Register Based	A16 only	0xEF4

OFFSET 0x02 *DEVICE* *RESET VALUE 0xF350*

This register simply contains (in the case of an A16 only device) a manufacturer's card ID.

OFFSET 0x04 *STATUS* *RESET VALUE 0xFFFF*

The TFP does not support VXIbus initialization and diagnostic features. The reset value is always returned.

OFFSET 0x04 *CONTROL* *RESET VALUE 0xFFFE*

Writing to this register with bit 0 set will deassert any pending interrupts and will clear all used bits in offsets 0x20 through 0x2E (except FIFO at offset 0x28). Writing to this register with bit 0 cleared has no effect. All other bits are ignored during a write.

OFFSET 0x0A *TIMEREQ* *RESET VALUE NA*

Reading this register latches the current time and status into offsets 0x0C through 0x14. The value read is indeterminant.

****** WARNING ******

Many compilers will optimize out of existence an assignment made to a local variable if that variable is not used. For example, the following code snippet may not read offset 0x0A.

```
timeptr = (short *)(BASE + 0x0A) ;      /* initialize pointer */
local_dummy = *timeptr++ ;              /* latch the time ?? */
read_time(timeptr) ;                    /* read the time */
```

The following form is recommended. Use of the global prevents optimizing out.

```
timeptr = (short *) (BASE + 0x0A) ;     /* initialize pointer */
global_dummy = *timeptr++ ;             /* latch the time */
read_time(timeptr) ;                    /* read the time */
```

OFFSET 0x0C	*TIME0*	*RESET VALUE NA*
OFFSET 0x0E	*TIME1*	*RESET VALUE NA*
OFFSET 0x10	*TIME2*	*RESET VALUE NA*
OFFSET 0x12	*TIME3*	*RESET VALUE NA*
OFFSET 0x14	*TIME4*	*RESET VALUE NA*

For clarity the above offsets have been grouped.

bit #	15-12	11-8	7-4	3-0
TIME0 field	not defined	not defined	status (note 1)	days hundreds
TIME1 field	days tens	days units	hours tens	hours units
TIME2 field	minutes tens	minutes units	seconds tens	seconds units
TIME3 field	10E-1 seconds	10E-2 seconds	10E-3 seconds	10E-4 seconds
TIME4 field	10E-5 seconds	10E-6 seconds	10E-7 seconds	not defined

OFFSET 0x16	*EVENT0*	*RESET VALUE NA*
OFFSET 0x18	*EVENT1*	*RESET VALUE NA*
OFFSET 0x1A	*EVENT2*	*RESET VALUE NA*
OFFSET 0x1C	*EVENT3*	*RESET VALUE NA*
OFFSET 0x1E	*EVENT4*	*RESET VALUE NA*

For clarity the above offsets have been grouped.

bit #	15-12	11-8	7-4	3-0
EVENT0 field	not defined	not defined	status (note 1)	days hundreds
EVENT1 field	days tens	days units	hours tens	hours units
EVENT2 field	minutes tens	minutes units	seconds tens	seconds units
EVENT3 field	10E-1 seconds	10E-2 seconds	10E-3 seconds	10E-4 seconds
EVENT4 field	10E-5 seconds	10E-6 seconds	10E-7 seconds	not defined

note 1 bit 6 1 = frequency offset > 5E8 0 = frequency offset < 5E8
bit 5 1 = time offset > X microsec 0 = time offset < X microsec
(X = 5 for mode 0 X = 2 more all other modes)
bit 4 1 = flywheeling (not locked) 0 = locked to selected reference

OFFSET 0x18 *STROBE1* *RESET VALUE 0xXX00*
OFFSET 0x1A *STROBE2* *RESET VALUE 0x0000*
OFFSET 0x1C *STROBE3* *RESET VALUE 0x0000*

For clarity the above offsets have been grouped.

bit #	15-12	11-8	7-4	3-0
STROBE1 field	not defined	not defined	hours tens	hours units
STROBE2 field	minutes tens	minutes units	seconds tens	seconds units
STROBE3 field	10E-1 seconds	10E-2 seconds	10E-3 seconds	not defined

OFFSET 0x20 *UNLOCK* *RESET VALUE NA*

A read of this register releases the time capture lockout function if it has been enabled. See *CMD OFFSET 0x24*for additional details. The data read from this offset is meaningless. A write to the UNLOCK register acts as a secondary time latching strobe. Time is latched in *EVENT0 - EVENT4*. This feature allows the host to capture two times independently.

OFFSET 0x22 *ACK* *RESET VALUE 0xXX00*

bit#	CONTROL	FUNCTION (*SET = '1' = high voltage* *CLEAR = '0' = low voltage)*
0	TFP **HOST**	SETS bit to acknowledge the receipt of a valid input packet from host **CLEARS bit by writing to this register with bit 0 SET**
1	reserved	
2	TFP **HOST**	SETS bit when output FIFO contains a data packet. **CLEARS bit by writing to this register with bit 2 SET.** **This bit can generate an interrupt. (see OFFSET 0x2A INTSTAT)**
3	reserved	
4	TFP **HOST**	SETS bit if output FIFO contains data. CLEARS bit if output FIFO empty. **CLEARS output FIFO by writing to this register with bit 4 SET.**
5	reserved	
6	reserved	
7	**HOST**	**Must write to this register with bit 7 SET to cause TFP to take action on the data packet previously written to the input FIFO.**
8-15	reserved	

OFFSET 0x24 *CMD* *RESET VALUE 0xXX00*

This register is used to command the TFP to perform specific functions.

bit#	NAME	FUNCTION
0	LOCKEN	Event capture lockout (0 = disable lockout 1 = enable lockout). Prevents a new event from overwriting a previous event until an *UNLOCK* is performed (see *OFFSET 0x20 UNLOCK).*
1	HBEN	Enable periodic time capture (0 = disable 1 = enable). When enabled the periodic output is logically OR'ED with the event input, and the time of the periodic may be read in *EVENT0 - EVENT4.*
2	EVSENSE	Event capture sense select (0 = rising edge 1= falling edge)
3	EVENTEN	Event capture enable (0 = disable 1 = enable)
4	STREN	Time coincidence output strobe enable (0 = disable 1 = enable)
5	STRMODE	Strobe mode (0 = use major and minor time 1 = use minor time only) In mode (1) an output strobe is produced each second.
6	FREQSEL0	0 10 MHz 1 5 MHz 0 1 MHz 1 1 MHz
7	FREQSEL1	0 0 1 1
8-15	reserved	

OFFSET 0x26 *FIFO* *RESET VALUE NA*

Reads take data from the output *FIFO.* Writes place data into the input *FIFO.* Both the input *FIFO* and the output *FIFO* may also be accessed via D08(O) at offset 0x27. Each *FIFO* has a depth of 512 bytes.

Data must be written to and read from the *FIFO* in the following data packet format.

byte 1	0x01	header byte (ASCII SOH)
byte 2	'A' thru 'Z'	idbyte (defined in *CHAPTER 4)*
byte 3	data	always ASCII i.e. 0 = 0x30
byte 4	data	
.	.	the number of data bytes varies
byte N	data	
byte N+1	0x17	tail byte (ASCII ETB)

OFFSET 0x28 *MASK* *RESET VALUE 0xXX00*

bit #	INT #	SOURCE OF INTERRUPT
0	0	External event input has occurred
1	1	Periodic pulse output has occurred
2	2	Time coincidence strobe has occurred
3	3	The one pulse per second (1PPS) output has occurred
4	4	A data packet is available in the output *FIFO*
5-15	reserved	

An interrupt source is enabled by writing a '1' to the mask bit corresponding to that source. An interrupt source is disabled by writing a '0' to the mask bit corresponding to that source.

OFFSET 0x2A *INTSTAT* *RESET VALUE 0xXX00*

The *INTSTAT* register has the same basic structure as the *MASK* register. The TFP sets bits 0 through 4 of this register depending upon which of the interrupt source generated the interrupt. The *INTSTAT* register bits are set regardless of the state of the mask bits. This feature allows the host to poll for the occurrence of the interrupt sources. *INTSTAT* bits are cleared by writing to the *INTSTAT* register with the correspond bit(s) set.

*** WARNING ***

It is the transition of an *INTSTAT* bit from a zero to a one that causes an interrupt to be generated (assuming, of course, that the corresponding *MASK* bit was set). If the bit in the *INTSTAT* register is not cleared by the host it is not possible to generate a second interrupt. It is good programming practice to clear the *INTSTAT* register immediately after interrupts have been enabled.

OFFSET 0x2C *VECTOR* *RESET VALUE 0xXX00*

The *VECTOR* register holds the 8 bit Status / ID byte that the TFP will return during interrupt acknowledge cycles for VMEbus applications.

The *LEVEL* register selects the level at which an interrupt will be generated. Only bits 0 through 2 are used. These bits are encoded as follows:

bit 2	1	0	IRQ LEVEL
0	0	0	disabled
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

CHAPTER 4
FIFO DATA PACKETS

4.0 GENERAL

Communication with the TFP is performed using a byte serial data packet protocol. The packet bytes are read from and written to the TFP using D08(O) transfers at offset 0x27 or D16 transfers at offset 0x26. If the case of a D16 transfer only the low order byte is used. The packet structure is defined in *CHAPTER 3 Section 3.1 OFFSET 0x26.*

4.1 WRITING DATA PACKETS

The following steps should be followed when loading data packets to the TFP. Failure to perform one or more of these steps correctly is a common reason for customer support calls.

Write the packet to the input *FIFO.*

Clear bit 0 of the *ACK* register by writing 0x01 to the *ACK* register.

Inform the TFP that an input packet is available by writing 0x80 to the *ACK* register.

The TFP will set bit 0 of the *ACK* register when the packet is processed.

When the host sets bits 7 of the *ACK* register an interrupt to the TFP CPU is generated. The TFP service routine performs minimalist packet integrity checking. The TFP checks that the first packet byte is 0x01 (ASCII SOH). If the SOH is found the TFP loads *FIFO* data into an input buffer until a byte value of 0x17 (ASCII ETB) is found. The packet is then processed in accordance with the idbyte value. When processing is complete the TFP sets bit 1 of the *ACK* register, clears the input *FIFO*, and resumes its previous task. If an SOH is not the first packet byte or if more than 40 bytes are read before encountering an ETB or if the idbyte value is invalid, then TFP clears the *FIFO*, sets bits 1 of the *ACK* register, and resumes its previous task.

4.1.1 PACKET 'A' - SELECT TFP OPERATIONAL MODE

This packet contains a single data byte ('0' through '7') which defines the TFP operational mode. The modes are enumerated below.

MODE 0 TIMECODE DECODING MODE

The TFP uses an input timecode as the timing reference. The following codes are supported (see packet 'H'): IRIGA, IRIGB, 2137, XR3, and NASA36. Both modulated carrier and DC level shift formats are supported (DC level shift is not supported for 2137 or XR3 codes). The TFP locks its crystal oscillator to the input code rate. The oscillator has a control range of +/- 30 PPM for the standard DIP version, and +/- 2 PPM for the optional oven version. If the input code is outside these limits the TFP will exhibit periodic slips (if the TFP reference deviates from the input source by more than +/- 1 millisecond a forced jamsync is performed). If the input code is lost or removed theTFP will continue to 'flywheel' at the last known code rate. Typical accuracy is 5 parts in 10E7

(2 milliseconds of drift per hour).

MODE 1 FREE RUNNING MODE

This mode is virtually the same as mode 2. Without a 1PPS input the TFP runs at the last known oscillator frequency. Major time can be set with the 'B' packet. The TFP timebase can be adjusted with packet 'D'.

MODE 2 EXTERNAL 1 PPS MODE

The TFP synchronizes to the signal on the 1PPS input. Major time can be loaded with the 'B' packet. The acquisition range is the same as described in mode 0.

MODE 3 REAL TIME CLOCK MODE

The TFP synchronizes to the onboard real time clock (RTC) IC, and the major time is also derived from the clock IC. The RTC is battery backed. This mode is not recommended when using the oven oscillator because the accuracy of the RTC is not high enough to ensure that the oven will be able to track it with slippages. See Mode 0 description.

MODE 4 DIGITAL SYNC MODE

This mode is not implemented.

MODE 5 GPS MODE WITH GPS RECEIVER ONBOARD

The TFP only supports this mode in the bc735VME / bc357VXI configuration. It currently available in only a double wide 6U form factor.

MODE 6 GPS MODE WITH GPS RECEIVER LOCATED IN THE ANTENNA

This is an optional mode available with the bc637VME / bc357VXI configuration. It is described in a separate manual.

MODE 7 DIAGNOSTIC AND DEFAULT SETTING MODE

Initially this mode was provided to allow the TFP to be photographed. The LED display is loaded with static time *12:34:56*. As more battery backed parameters were added it became useful to use this mode as a means of setting all battery backed data to standard defaults. This data and the default values established by mode 7 are as follows.

VARIABLE	DEFAULT	DESCRIPTION
mode	0	TFP operational mode
timecode	IRIGB	reference timecode expected
format	modulated	modulated timecode expected
gencode	IRIGB	TFP generates IRIGB
path	1	path selection variable (see 'P' packet)
local	0	local time offset (GPS modes only)
accum	32000	VCXO DAC value (nominally centered)
leapsec	0	GPS to UTC leap second correction (only used in GPS modes)

The diagnostic utility of this mode resides in the fact that the operator can immediately determine if the host program is communicating properly with the TFP by simply observing the display. To borrow from the classic K&R. To make *12:34:56* appear "you have to be able to create the program text, compile it, run it, and find out where your output went. With these mechanical details mastered, everything else is comparatively easy."

4.1.2 PACKET 'B' SET MAJOR TIME

In mode 1 and mode 2 the only way to set major time is using this packet. It is not likely that this packet would be used in any other mode since all other modes derive major time from the timing reference signal. The packet format is as follows:

byte	1	SOH
byte	2	'B'
byte	3	days hundreds
byte	4	days tens
byte	5	days units (Jan 1 is defined as day 001)
byte	6	hours tens
byte	7	hours units
byte	8	minutes tens
byte	9	minutes units
byte	10	seconds tens
byte	11	seconds units
byte	12	ETB

Note: All data fields must be ASCII.

The time loaded by packet 'B' will not be used until the 1 second epoch following the load. The TFP increments the time before loading it to output buffer registers. The time is incremented at approximately 900 milliseconds into the current frame, and the buffer registers are loaded 950 milliseconds into the current frame. The buffer registers are transferred to a set of holding registers synchronously with the 1PPS output. The time loaded by packet 'B' should be input well in advance of the 918 millisecond point in the frame, and should reference the current frame.

4.1.3 PACKET 'C' COMMAND INPUT

This packet has a single data byte and is used to direct the TPF to take the specific actions below.

'1'	not used	(warmstart on early software versions)
'2'	software reset	vectors TFP CPU to power on reset point
'3'	jamsynch	force TFP minor time to zero on the next 1PPS input
'4'	not used	(jamsynch lockout on early software versions)
'5'	buf to RTC	load current time to the Real Time Clock IC
'6'	variables	dumps battery backed RAM to *FIFO (factory use only)*

4.1.4 PACKET 'D' LOAD D/A CONVERTER

The TFP reference crystal oscillator is voltage controlled using the buffered output of a 16 bit D/A converter as the controlling voltage. Packet 'D' allows the user to directly load a 16 bit value to the D/A converter. This feature would allow a user to fine tune the TFP timebase in the free running mode. We are not aware of any other use for this packet in normal operation. Since this voltage is routed out of the TFP via pin 9 on the J1 connector to allow external oscillators to be disciplined, it would provide a means to devise a frequency control algorithm independent of the TFP. The format is shown below. (See also bit 3 of the path byte loaded by the 'P' packet.)

byte	1	SOH
byte	2	'D'
byte	3	'0' - 'F' bits 12-15
byte	4	'0' - 'F' bits 08-11
byte	5	'0' - 'F' bits 04-07
byte	6	'0' - 'F' bits 01-03
byte	7	ETB

Note: As always, data is in ASCII.

4.1.5 PACKET 'F' HEARTBEAT (PERIODIC) CONTROL

This packet establishes the frequency of the TFP output periodics. The number of output pulses is defined by the following equation.

$$N = 10{,}000{,}000 / (n1 * n2)$$

where N = output pulses per second
n1 = a programmable number in the range of 2 to 65535
n2 = a programmable number in the range of 2 to 65535

The 'F' packet establishes the value of n1 and n2. There is a one byte qualifier associated with the 'F' packet. This qualifier allows the periodics to be asynchronous or synchronous with respect to the 1 PPS epoch. If the synchronous format is chosen n1 and n2 must be selected such that N is an integer.

The duty cycle of the output waveform is dependent on the particular values of n1 and n2 selected; divider n2 physically follows divider n1. The following example serves as an illustration. If n1 * n2 = 20, the output frequency is 500kHz. If n1 is selected as 10 and n2 is selected as 2 a square wave is output since the last divider is a divide by 2. If n1 is selected as 2 and n2 is selected as 10 the output waveform is a pulse train with a one tenth duty cycle.

The packet 'F' format is as follows:

byte	1	SOH
byte	2	'F'
byte	3	'2' for asynchronous '5' for synchronous
byte	4	'0' - 'F" m1 bits 12-15
byte	5	'0' - 'F' m1 bits 08-11
byte	6	'0' - 'F' m1 bits 04-07
byte	7	'0' - 'F' m1 bits 00-03
byte	8	'0' - 'F' m2 bits 12-15
byte	9	'0' - 'F' m2 bits 08-11
byte	10	'0' - 'F' m2 bits 04-07
byte	11	'0' - 'F' m2 bits 00-03
byte	12	ETB

If a '2' (asynchronous) qualifier is used then the values of n1 and n2 are the same as the packet values m and m2. If the '5' (synchronous) qualifier is used, then the values of n1 and n2 are equal of packet values m+1 and m2+1 respectively. For example, if a synchronous 500KHz square wave is desired then the qualifier byte is '5', m = 9, and m2 = 1. Additional insight into the operation of the counter can be gained by reading the INTEL documentation for the 82C54 integrated circuit. The '2' and '5' qualifiers correspond to the INTEL defined modes 2 and 5.

4.1.6 PACKET 'G' OFFSET CONTROL

It is frequently desired to program an offset into the basic TFP timekeeping functions relative to the reference input. For example, if the reference input is an IRIGB timecode, there may be significant cable delay between the IRIGB generator and the TFP location. Packet 'G' allows this time difference to be removed by inserting the known amount of offset between the IRIGB reference and TFP locations. The offset is programmable in units of 100 nanoseconds, and may be positive or negative. The format is shown below.

byte	1	SOH
byte	2	'G'
byte	3	'+' or '-' advance or retard
byte	4	'0' - '9' BCD millisecond hundreds
byte	5	'0' - '9' BCD millisecond tens
byte	6	'0' - '9' BCD millisecond units
byte	7	'0' - '9' BCD microsecond hundreds
byte	8	'0' - '9' BCD microsecond tens
byte	9	'0' - '9' BCD microsecond units
byte	10	'0' - '9' BCD nanosecond hundreds
byte	11	ETB

For the IRIGB scenario described above a positive offset should be used.

*** *WARNING* ***

If offsets larger than +/- 990 microseconds are used, then the TFP jamsynch feature must be turned off using packet 'P'. The reason for this requirement is that under normal operation if a difference between the reference time and the TFP time is detected to be greater than +/- 1 millisecond the TFP timebase is "jammed" to the reference time so that a lengthy steering process is avoided.

4.1.7 PACKET 'H' SET TIMECODE FORMAT FOR MODE 0

Packet 'H' allows the host to select the timecode format and modulation type. The packet format is as follows. The timecode format and modulation values are maintained in battery backed RAM.

byte	1	SOH
byte	2	'H'
byte	3	format
byte	4	modulation
byte	4	ETB

format choices

'A'	IRIGA
'B'	IRIGB
'C'	2137 (XR3 with 100Hz symbol rate)
'N'	NASA36
'X'	XR3 (25Hz symbol rate)

modulation choices

'M'	amplitude modulated sinewave
'D'	pulse code modulation (DC level shift) DC level shift not is supported for 2137 and XR3 codes.

4.1.8 PACKET 'I' CLOCK SOURCE SELECT

Packet 'I' is used to select the clock source for the TFP. The TFP uses a frequency of 10MHz for all timing functions. The 10 MHZ be may derived from the TFP VCXO or it may be supplied from an external oscillator via J1 pin#1 or P2 pin#C22. The packet format is as follows.

byte	1	SOH
byte	2	'I'
byte	3	'E' or 'I' External or Internal
byte	4	ETB

On power on the TFP always defaults to the internal oscillator selection.

4.1.9 PACKET 'J' SEND DATA TO GPS RECEIVER

The format and content variations are discussed in a separate manual.

4.1.10 PACKET 'K' SELECT GENERATOR CODE

The timecode generated by the TFP is selected by packet 'K'. Only two options are available as described below. The generator code type is maintained in battery backed RAM.

byte	1	SOH
byte	2	'K'
byte	3	code
byte	4	ETB

code options

'B'	generate IRIGB amplitude modulated and DC level shift
'H'	generate IRIGH DC level shift only

4.1.11 PACKET 'L' SET REAL TIME CLOCK

This packet loads the battery backed real time clock IC which is used as the source of major time and 1PPS epoch when mode 3 is selected. The format is shown below.

byte	1	SOH
byte	2	'L'
byte	3	years tens
byte	4	years units
byte	5	months tens
byte	6	months units (January = month 1)
byte	7	day of month tens
byte	8	day of month units
byte	9	hours tens
byte	10	hours units
byte	11	minutes tens
byte	12	minutes units
byte	13	seconds tens
byte	14	seconds units
byte	15	ETB

As usual all data is in the ASCII format. The TFP need not be in mode 3 when packet 'L' is downloaded.

4.1.12 PACKET 'M' LOCAL TIME OFFSET SELECT

This packet allows time to be displayed with an hour offset. This situation usually arises when the source of time is in a UTC (Universal Time Coordinated) format and the local time is desired to be displayed. The offset only applies to the hours digits. The format is as follows.

byte	1	SOH
byte	2	'M'
byte	3	sign '+' or '-'
byte	4	hours tens
byte	5	hours units
ETB		

The hours are in range from -12 to +12. A positive sign is from the prime meridian heading East, and a negative sign is used from the prime meridian heading West. For example, Eastern Standard Time would be -05 relative to UTC.

4.1.13 PACKET 'O' REQUEST DATA FROM THE TFP

This packet is used to request data from the TFP which is not available via the register interfaces. It was added a 'catch all' packet for universal data transfer. This packet has been created with a very extensible format, and additional data will be made available as customer needs and suggestions are addressed. Currently three different data packets may be requested using the 'O' packet. The formats are as follows:

REQUEST FORMAT

byte	1	SOH
byte	2	'O'
byte	3	'0' or '1' or '2' ...
byte	4	ETB

RESPONSE FORMAT '0' REQUEST RTC TIME (SEE PACKET 'L')

byte	1	SOH
byte	2	'o' (lower case letter)
byte	3	'0'
byte	4	years tens
byte	5	years units
byte	6	months tens
byte	7	months units
byte	8	day of month tens
byte	9	day of month units
byte	10	hours tens
byte	11	hours units
byte	12	minutes tens
byte	13	minutes units
byte	14	seconds tens

byte 15 seconds units
byte 16 ETB

RESPONSE FORMAT '1' REQUEST CURRENT D to A VALUE

byte 1 SOH
byte 2 'o' (lower case letter)
byte 3 '1'
byte 4 '0' - 'F' bits 12-15
byte 5 '0' - 'F' bits 08-11
byte 6 '0' - 'F' bits 04-07
byte 7 '0' - 'F' bits 00-03
byte 8 ETB

RESPONSE FORMAT '2' REQUEST LEAP SECONDS (currently GPS specific)

byte 1 SOH
byte 2 'o' (lower case letter)
byte 3 '2'
byte 4 leap second tens
byte 5 leap second units
byte 6 ETB

RESPONSE FORMAT '3' REQUEST RTC YEAR

byte 1 SOH
byte 2 'o' (lower case letter)
byte 3 '3'
byte 4 RTC year tens
byte 5 RTC year units
byte 6 ETB

RESPONSE FORMAT '4' REQUEST YEAR

byte 1 SOH
byte 2 'o' (lower case letter)
byte 3 '4'
byte 4 year tens
byte 5 year units
byte 6 ETB

The TFP signals a packet ready condition by setting bit2 in the *ACK* register. It is the responsibility of the host to clear this bit by writing to the *ACK* register with bit2 set.

4.1.14 PACKET 'P' PATH SELECTION

The term path selection is not the best descriptor for the action of this packet. It might better be called a switch or branch selector. The purpose of this packet is to allow the user to exercise control over certain TFP processes. The path packet is used to download a single byte. Each bit in the byte has a toggling action relative to a TFP function. The format is described below.

byte	1	SOH
byte	2	'P'
byte	3	'0' - 'F' path upper nibble
byte	4	'0' - 'F' path lower nibble
byte	4	ETB

upper nibble bit definitions:

bit	3	0 = normal time format	1 = long second format <1>
bit	2	0 = no broadcast of RTC	1 = broadcast packet 'o' '3' each second
bit	1	0 = use GPS leap seconds	1 = ignore GPS leap seconds
bit	0	0 = *FIFO* echo off	1 = *FIFO* echo on

lower nibble definitions:

bit	3	0 = enable TFP disciplining	1 = disable TFP discipline
bit	2	0 = enable jamsynch	1 = disable jamsynch
bit	1	0 = leap year off	1 = leap year on
bit	0	not used (previously enabled diagnostics which are now always off)	

<1> *TIME0 thru TIME4* contain atomic seconds since January 6th 1980. Use only in GPS modes.

4.1.15 PACKET 'Q' SET DISCIPLINING GAIN

This packet allows the gain and sense of the disciplining process to be set via the host bus. Originally this feature was used for Bancomm developmental purposes, bit it would also be indispensable to anyone attempting to discipline an external oscillator using the TFP. The format is as follows.

byte	1	SOH
byte	2	'Q'
byte	3	'0' - 'F' least significant nibble
byte	4	'0' - 'F' most significant nibble
byte	5	sense '1' = positive '0' = negative
byte	6	ETB

4.1.16 PACKET 'S' SET YEAR

This packet allows user to set year in modes 0, 1 and 2.

byte	1	SOH
byte	2	'R'
byte	3	year tens
byte	4	year units
byte	5	ETB

CHAPTER 5

PROGRAMMING EXAMPLES

5.0 GENERAL

The example code fragments in this chapter are written in the C programming language. The examples have been tested at Bancomm, and should be transportable to most programming environments. A system dependent base address is defined below where 'YYYY' indicates a 64 kbyte page of memory used for A16 data and 'SSSS' indicates the SW1 and SW2 switch settings.

```
#define BASE            0xYYYYSSSS
```

The following definitions pertain to FIFO data transfer.

```
#define SOH             0x01
#define ETB             0x17
#define FIFO            (short*)(BASE+0x27)
```

The following global variables are also declared and used throughout this chapter.

```
short   dummy, *readptr, time[5] ;
long    i ;
```

5.1 READING TIME ON DEMAND

The following example reads the time from the TFP registers *TIME0 thru TIME4* and loads this data into the array time[]. Note that the time is latched by reading the *TIMEREQ* register, and that the register is assigned to a global variable. In most cases assignment to a global avoids the possibility that the dummy read operation will be removed by an optimizing compiler (beware).

```
readptr = (short*)(BASE + 0x0A) ;                /* initialize pointer */
dummy = *readptr++ ;                             /* latch time increment pointer */
for(i=0 ; i<5 ; i++)  time[i] = *readptr++ ;     /* read the time registers */
```

5.2 EXTERNAL EVENT TIME CAPTURE

This example sets up the TFP event capture to occur on a rising edge and generate an interrupt. The time capture lockout mechanism is also used.

```
#define EVENT0      (short*)(BASE+0x16)
#define CMD         (short*)(BASE+0x24)
#define VECTOR      (short*)(BASE+0x2C)
#define MASK        (short*)(BASE+0x28)
#define INTSTAT     (short*)(BASE+0x2A)
#define LEVEL       (short*)(BASE+0X2E)
#define UNLOCK      (short*)(BASE+0x20)
```

```
/* INITIALIZE TFP EVENT HARDWARE */

*CMD = 0x09 ;              /* enable event and lockout */
*VECTOR = 0x40 ;           /* interrupt vector */
*LEVEL = 0x03 ;            /* interrupt level set */
*INSTAT = 0x01 ;           /* clear INSTAT bit */
*MASK = 0x01 ;             /* enable the interrupt */


/* INTERRUPT SERVICE ROUTINE FRAGMENT */

readptr = EVENT0 ;
for(i=0 ; i<5 ; i++)  time[i] = *readptr++;
dummy = *UNLOCK ;                    /* release capture lockout */
*INTSTAT = 0x01 ;                    /* clear INSTAT bit */
```

5.3 PROGRAM PERIODIC FREQUENCY OF 1000 HZ

This example uses a generalized send_packet() function to program a 1000 Hz output periodic synchronized to the TFP 1 PPS epoch.

```
#define ACK          (short*)(BASE+0x22)

void send_packet(char *charptr)
{
        *FIFO = SOH ;
        while(*charptr) *FIFO = *charptr++ ;     /* load body of packet */
        *FIFO = ETB ;
        *ACK = 0x81 ;                            /* command TFP & clear ACK */
        while(!(*ACK & 0x01)) ;                  /* wait for TFP acknowledge */
}

/* CODE FRAGMENT WHICH SETS PERIODIC */

        send_packet("F500630063") ;              /* 0x0063 = 99 = (100-1) */
```

5.4 SET MODE 1 AND THE MAJOR TIME

This example selects the free runnning mode and sets the TFP major time. Using the 'B' packet.

```
        send_packet("A1") ;              /* select mode 1 */
        *INSTAT = 0x08 ;                 /* clear INSTAT 1PPS bit */
        while(!(*INSTAT & 0x08) ;        /* wait for 1PPS */
        send_packet("B123112233") ;      /* set the days thru seconds */
```

5.5 SELECT MODE 0 (IRIGB) AND ADVANCE TFP 2.5 MILLISECONDS

The following code fragment selects the mode, timecode, and offset. The last 'P' packet is used to disable jamsynchs since the required offset is larger than 990 microseconds. See the 'G' packet description for additional details on the jamsynch function.

```
send_packet("A0") ;          /* select mode 0 */
send_packet("HB") ;          /* select IRIGB timecode */
send_packet("G+0025000") ;   /* advance 2.5 milliseconds */
send_packet("P04") ;         /* disable jamsynchs */
```

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CHAPTER 6

INPUTS AND OUTPUTS

6.0 INPUTS AND OUTPUTS

Front panel I/O consists of an LED time and status display, a BNC timecode input, a BNC timecode output, a 15 pin 'D' plug, and a 15 pin 'D' socket..

The current TFP time *hr:min:sec* is displayed using seven segment LED digits. If the TFP is flywheeling the digit decimal points are also illuminated. The time display is incremented at 990 milliseconds into the current frame. (One customer measured the LED radix point with a photo diode and reported that it was indeed early!)

Timecode is input using BNC connector J3. Input amplitudes from 0.5 to 5 volts peak to peak are accomodated. Timecode is output on BNC connector J2. The output amplitude is adjustable using 10 turn potentiometer VR1 located just below J2 and accessible with the TFP in place. The signals on socket J1 and plug J4 are summarized in the table below.

SIGNALS ON J1 15 PIN 'DS'		SIGNALS ON J4 15 PIN 'DP'	
PIN	SIGNAL	PIN	SIGNAL
1	external 10 MHz input	1	RS-422 Rx(+)
2	ground	2	RS-422 Rx(-)
3	strobe output	3	RS-422 Tx(+)
4	1 PPS output	4	RS-422 Tx(-)
5	timecode output (AM)	5	ground
6	external event input	6	not used
7	timecode input	7	GPS 1PPS
8	timecode return	8	GPS RS-422 Rx(+)
9	oscillator control output	9	GPS RS-422 Rx(-)
10	not used	10	ground
11	timecode output (DCLS)	11	GPS RS-422 Tx(-)
12	ground	12	GPS RS-422 Tx(+)
13	1,5,10 MHz output	13	not used
14	external 1PPS input	14	ground
15	periodics output	15	GPS +12 VDC

The following TFP specific signals are available on the P2 connector.

TFP SIGNALS ON VMEbus P2	
PIN	SIGNAL
C1	timecode input
C2	timecode return
C3	timecode output (DCLS)
C4	timecode output (AM)
C6	external event input
C8	strobe output
C9	periodic output
C10	external 1PPS input
C11	1PPS output
C12	1,5,10 MHz output
C22	10MHz input
C24	oscillator control output
C18 C20	RS-422 Tx(+) Rx(+)
A18 A20	RS-422 Tx(-) Rx(-)
A26	RS-422 Rx(-) GPS (Note 1)
C26	RS-422 Rx(+) GPS (Note 1)
A28	GPS 1PPS (Note 1)

Note 1 : Hardware Rev. E and later

CHAPTER 7
REVISION HISTORY

7.0 GENERAL

This chapter summarizes the TFP hardware revisions and compatibility issues.

REV. A

The original hardware release. This version had a wiring error between the TFP CPU data bus and the Maxim 7218C LED display driver IC. Basically the data lines were inverted in a high order to low order bit sense. The problem was fixed by rearranging the bits in the firmware before downloading to the Maxim IC.

REV. B

Fixed wiring error in REV. A

REV. C

The 15 pin 'D' plug connector was added to allow the ACUTIME GPS antenna to be used. RJ11 connectors J4 and J5 were removed. The reference designators on the silk screen were reordered at this time.

REV. D

Two filter capacitors were added. These capacitors were parallel with other components on previous revisions.

REV. E

An oven oscillator option was added and the transformer coupling option was removed. Additional signals were routed to the P2 connector. A pull down resistor was added to the INTACK line to prevent indeterminant state before LCA's are loaded. A board stiffener was added.

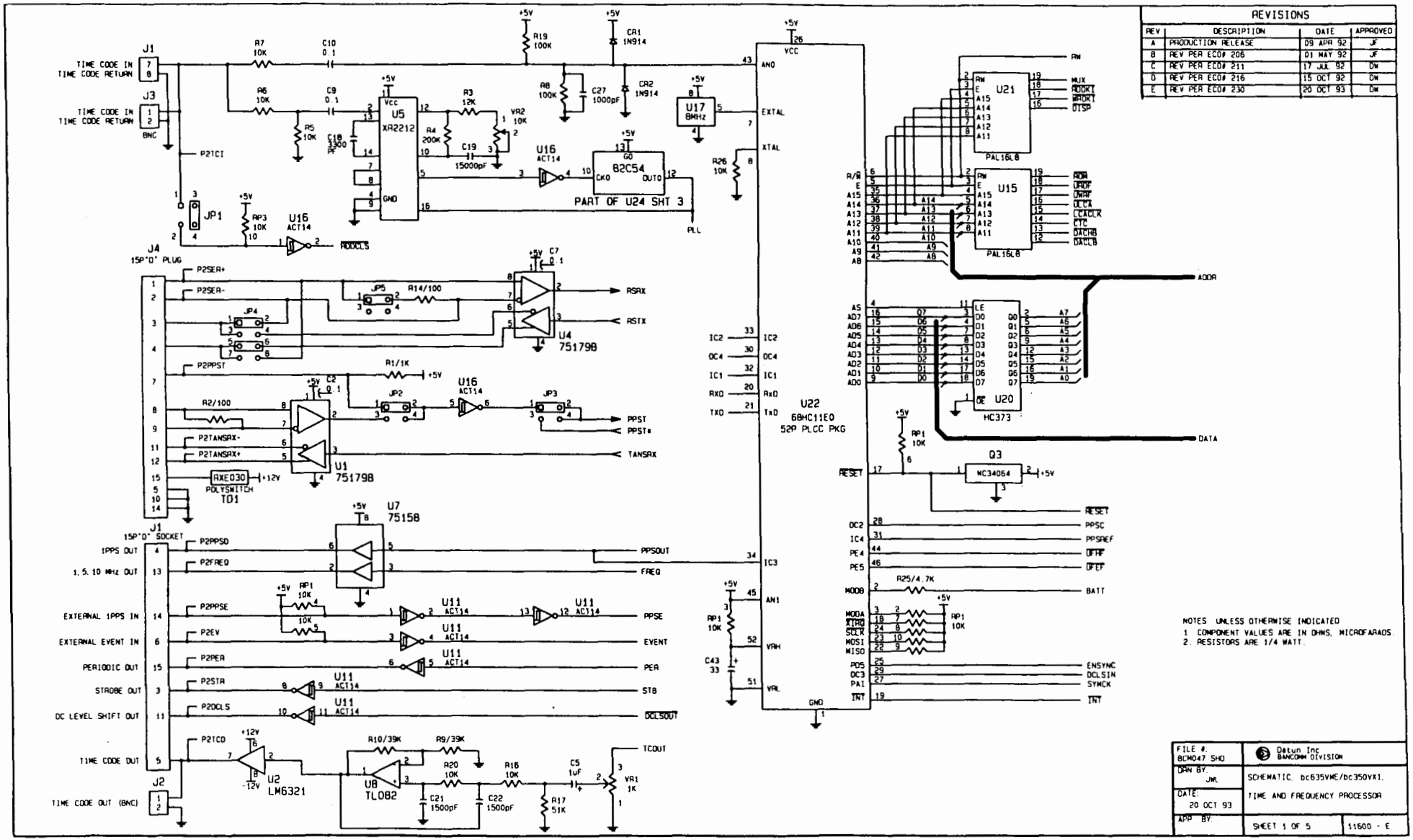
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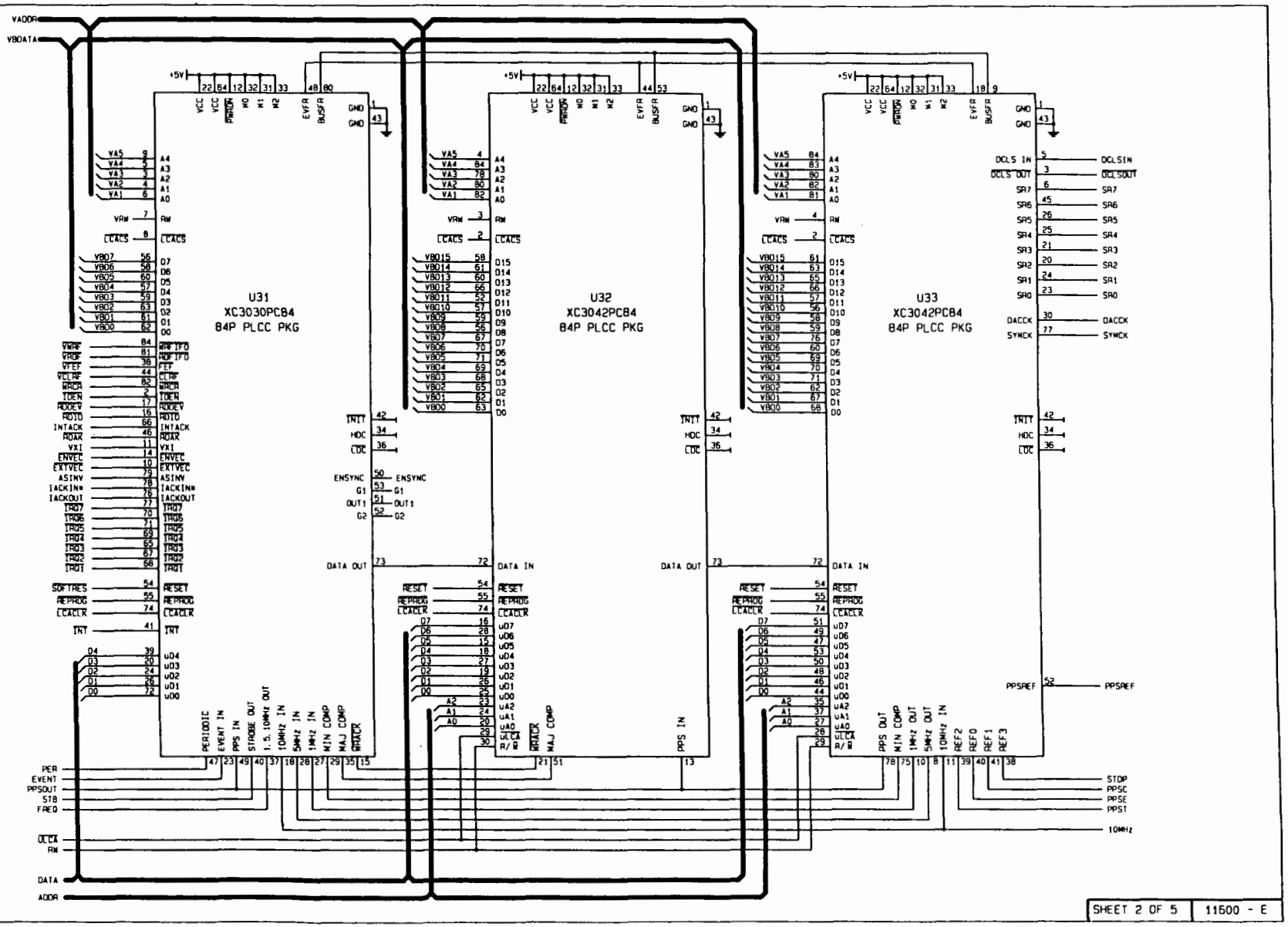
CHAPTER 8
DRAWING SET

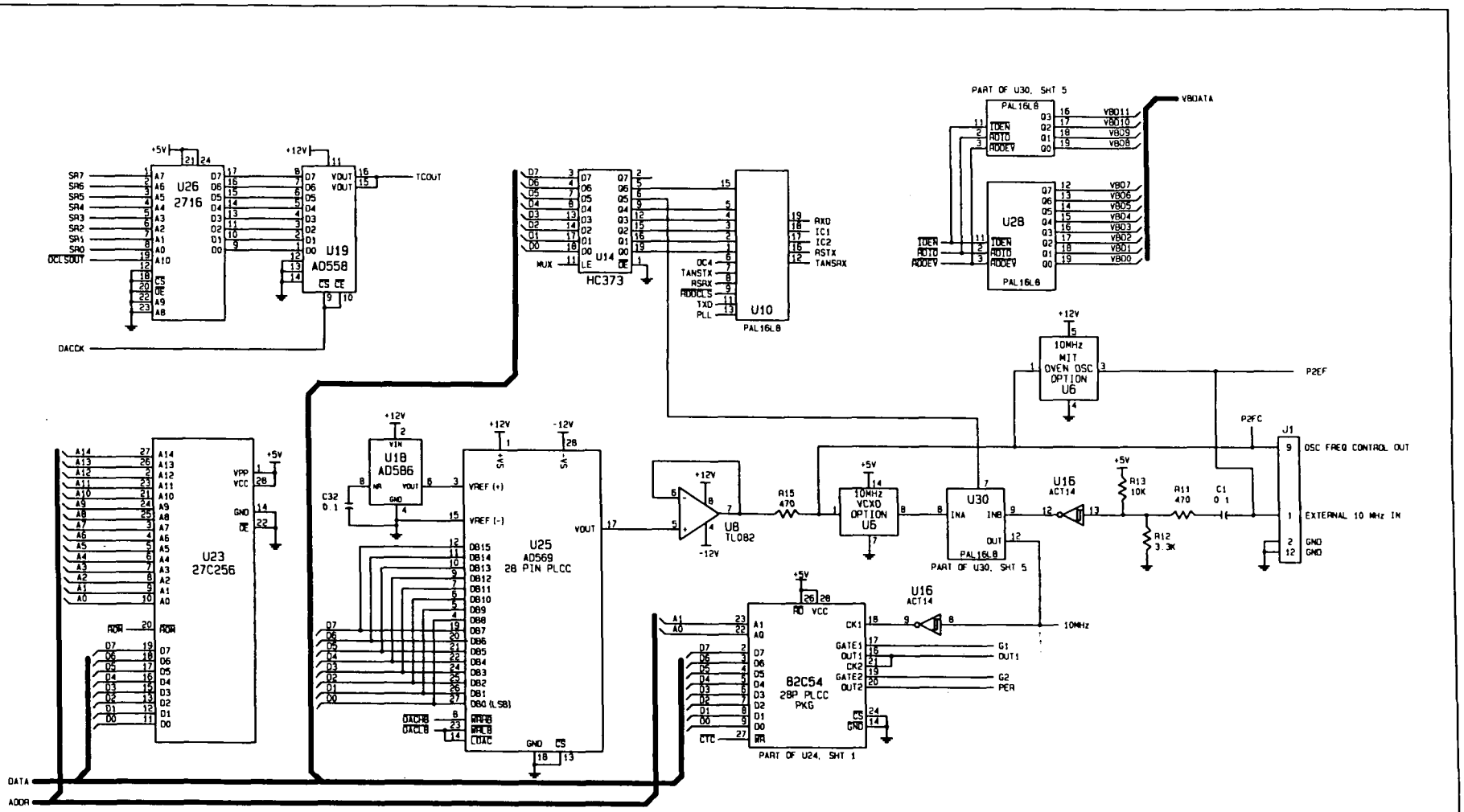
8.0 GENERAL

This chapter contains the schematic diagram, assembly drawing, and parts list for the bc635VME/bc350VXI *T*ime and *F*requency *P*rocessor.

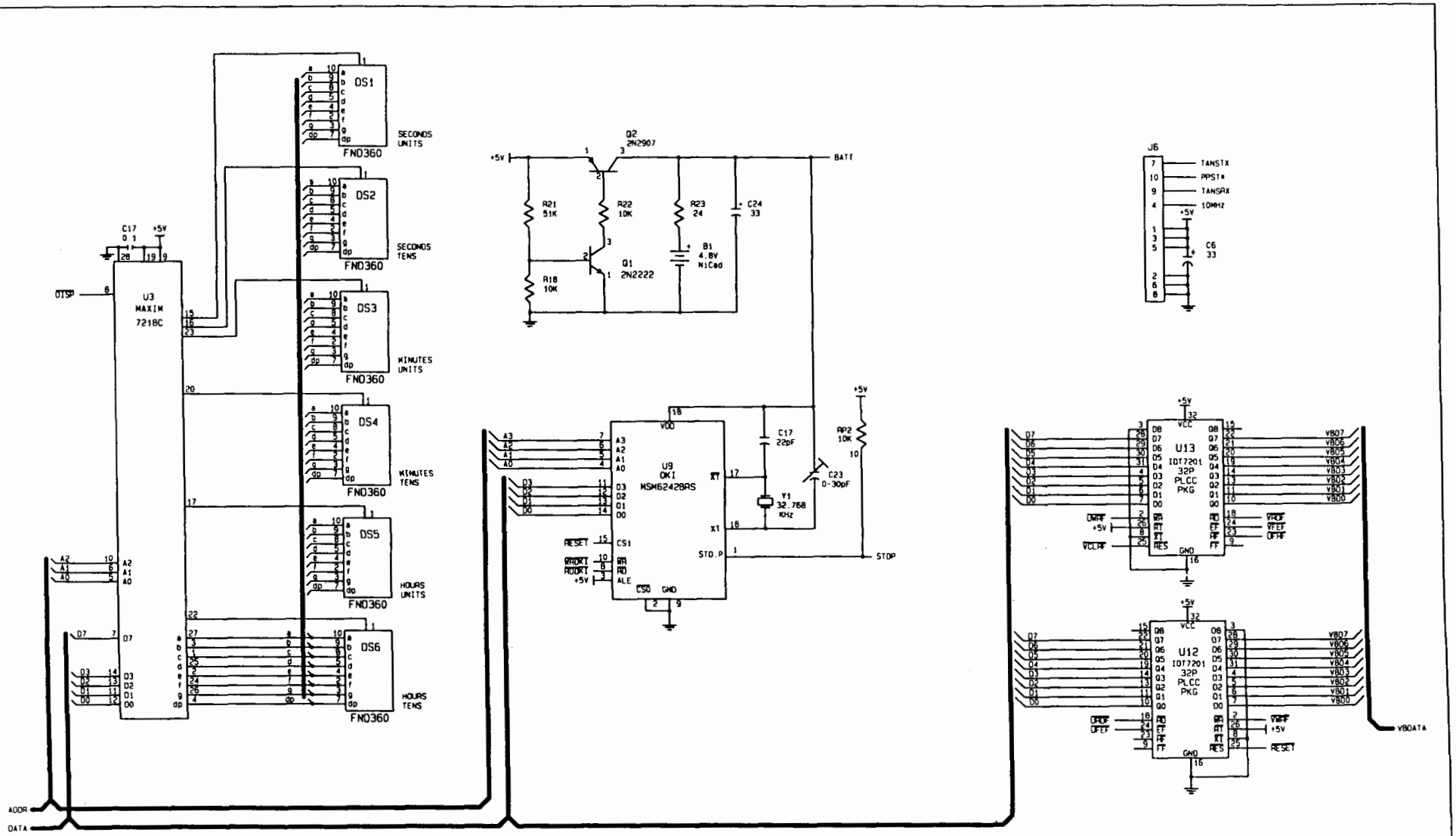
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REVISIONS
REV | DESCRIPTION | DATE | APPROVED
A | PRODUCTION RELEASE | 09 APR 92 | JF
B | REV PER ECO# 206 | 01 MAY 92 | JF
C | REV PER ECO# 211 | 17 JUL 92 | DW
D | REV PER ECO# 216 | 15 OCT 92 | DW
E | REV PER ECO# 230 | 20 OCT 93 | DW
NOTES UNLESS OTHERWISE INDICATED
1. COMPONENT VALUES ARE IN OHMS, MICROFARADS.
2. RESISTORS ARE 1/4 WATT.
FILE #: BCM047.SHO
DAN BY: JML
DATE: 20 OCT 93
APP BY:
Datum Inc BANCOMM DIVISION
SCHEMATIC bc635VME/bc350YX1.
TIME AND FREQUENCY PROCESSOR
SHEET 1 OF 5
11600 - E
U22 68HC11E0 52P PLCC PKG
U5 XR2212
U16 82C54
PART OF U24 SHT 3
U4 75179B
U1 75179B
U7 75158
U2 LM6321
U8 TL082
U21 PAL16L8
U15 PAL16L8
U20 HC373
Q3 MC34064
TIME CODE IN
TIME CODE RETURN
TIME CODE OUT (BNC)
1PPS OUT
1, 5, 10 MHz OUT
EXTERNAL 1PPS IN
EXTERNAL EVENT IN
PERIODIC OUT
STROBE OUT
DC LEVEL SHIFT OUT
ADDR
DATA
RESET
BATT
ENSYNC
DCLSIN
SYNCK
INT

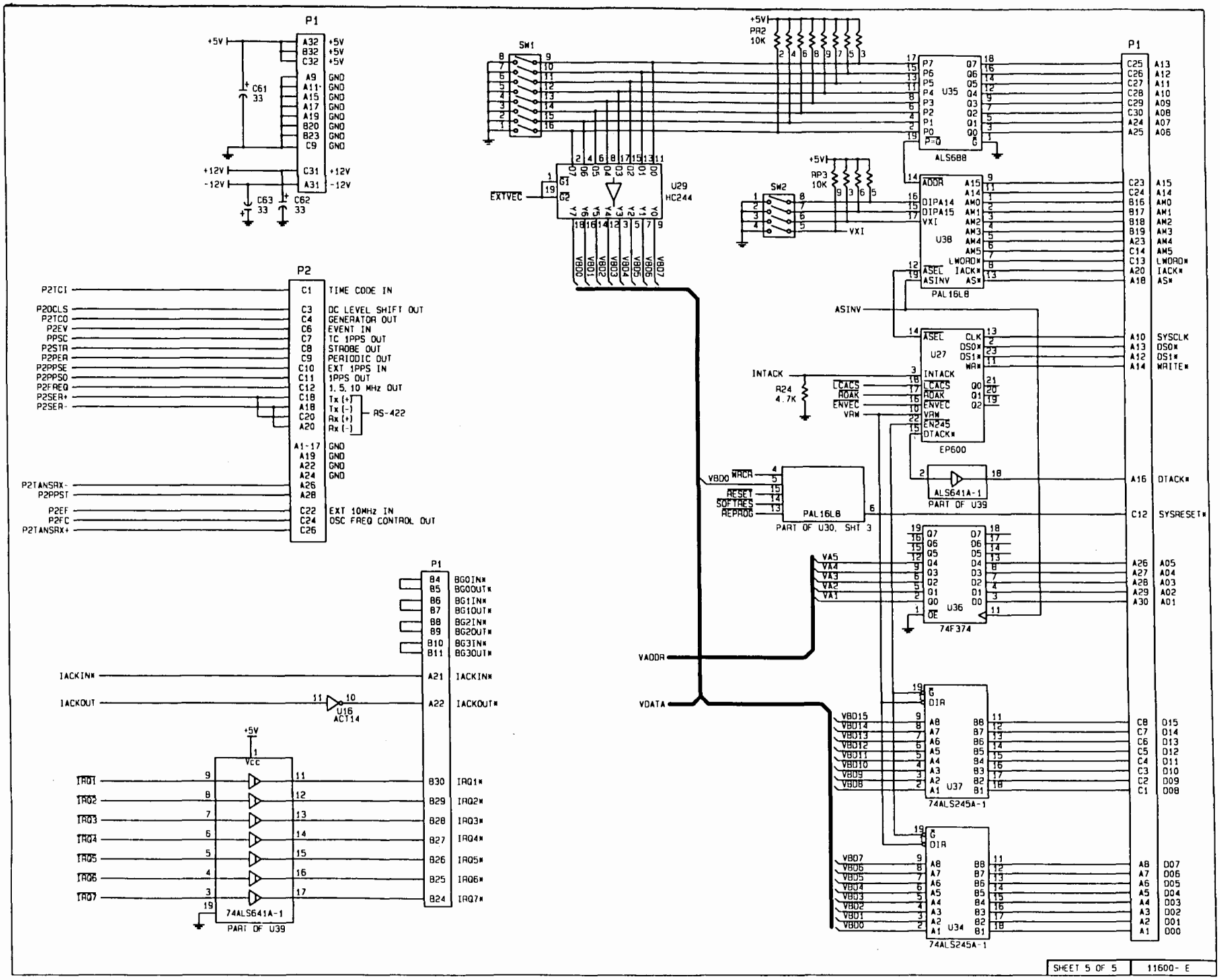

U31
XC3030PC84
84P PLCC PKG
U32
XC3042PC84
84P PLCC PKG
U33
XC3042PC84
84P PLCC PKG
VADDR
VBDATA
+5V
GND
VCC
PRGRM
M0
M1
M2
EVFR
BUSFR
A4
A3
A2
A1
A0
RW
CCACS
D7
D6
D5
D4
D3
D2
D1
D0
INTT
HDC
CDC
ENSYNC
G1
OUT1
G2
DATA OUT
DATA IN
RESET
REPROG
CCACLR
INT
uD7
uD6
uD5
uD4
uD3
uD2
uD1
uD0
uA2
uA1
uA0
ULCA
R/W
PERIODIC
EVENT IN
PPS IN
STROBE OUT
1.5.10MHz OUT
10MHz IN
5MHz IN
1MHz IN
MIN COMP
MAJ COMP
MRACR
PPS OUT
1MHz OUT
5MHz OUT
REF2
REF0
REF1
REF3
DCLS IN
DCLS OUT
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
DACCK
SYNCK
PPSREF
PER
EVENT
PPSOUT
STB
FREQ
ULCA
RW
DATA
ADDR
STOP
PPSC
PPSE
PPST
10MHz

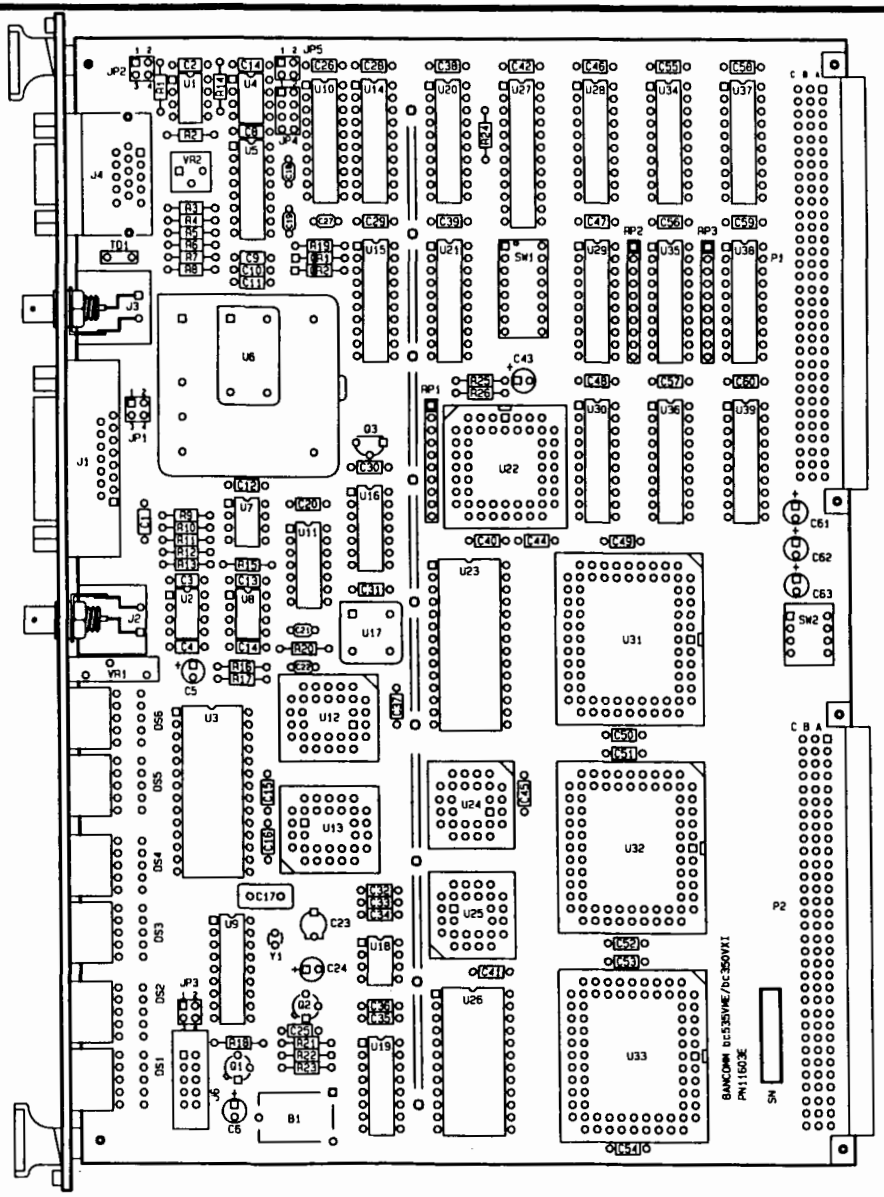


SHEET 3 OF 5	11600 - E



SHEET 4 OF 5	11600 - E


P1
+5V
A32 +5V
B32 +5V
C32 +5V
A9 GND
A11 GND
A15 GND
A17 GND
A19 GND
B20 GND
B23 GND
C9 GND
+12V
-12V
C31 +12V
A31 -12V
C61 33
C63 33
C62 33
P2
P2TCI C1 TIME CODE IN
P20CLS C3 DC LEVEL SHIFT OUT
P2TCO C4 GENERATOR OUT
P2EV C6 EVENT IN
PPSC C7 TC 1PPS OUT
P2STR C8 STROBE OUT
P2PER C9 PERIODIC OUT
P2PPSE C10 EXT 1PPS IN
P2PPSO C11 1PPS OUT
P2FREQ C12 1, 5, 10 MHz OUT
P2SER+ C18 Tx (+)
P2SER- A18 Tx (-)
C20 Rx (+)
A20 Rx (-)
RS-422
A1-17 GND
A19 GND
A22 GND
A24 GND
P2TANSRX- A26
P2PPST A28
P2EF C22 EXT 10MHz IN
P2FC C24 OSC FREQ CONTROL OUT
P2TANSRX+ C26
P1
B4 BG0IN*
B5 BG0OUT*
B6 BG1IN*
B7 BG1OUT*
B8 BG2IN*
B9 BG2OUT*
B10 BG3IN*
B11 BG3OUT*
IACKIN* A21 IACKIN*
IACKOUT A22 IACKOUT*
U16 ACT14
+5V
Vcc
IRQ1 B30 IRQ1*
IRQ2 B29 IRQ2*
IRQ3 B28 IRQ3*
IRQ4 B27 IRQ4*
IRQ5 B26 IRQ5*
IRQ6 B25 IRQ6*
IRQ7 B24 IRQ7*
74ALS641A-1
PART OF U39
SW1
+5V
PR2 10K
U35
P7 P6 P5 P4 P3 P2 P1 P0 P=Q
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 G
ALS688
P1
C25 A13
C26 A12
C27 A11
C28 A10
C29 A09
C30 A08
A24 A07
A25 A06
EXTVEC
U29
HC244
SW2
RP3 10K
VXI
U38
DIPA14
DIPA15
VXI
ADDR
ASEL
ASINV
A15 A14 A0 A1 A2 A3 A4 A5 LWORD* IACK* AS*
C23 A15
C24 A14
B16 A0
B17 A1
B18 A2
B19 A3
A23 A4
C14 A5
C13 LWORD*
A20 IACK*
A18 AS*
PAL16L8
ASINV
ASEL
U27
CLK DS0* DS1* WR*
A10 SYSCLK
A13 DS0*
A12 DS1*
A14 WRITE*
INTACK
R24 4.7K
LCACS
ADAK
ENVEC
VAM
EN245
DTACK*
EP600
VBD0
WACK
RESET
SOFTRES
REPROG
PAL16L8
PART OF U30, SHT 3
ALS641A-1
PART OF U39
A16 DTACK*
C12 SYSRESET*
VA5
VA4
VA3
VA2
VA1
U36
74F374
A26 A05
A27 A04
A28 A03
A29 A02
A30 A01
VADDR
VDATA
G
DIR
VBD15
VBD14
VBD13
VBD12
VBD11
VBD10
VBD9
VBD8
U37
74ALS245A-1
C8 D15
C7 D14
C6 D13
C5 D12
C4 D11
C3 D10
C2 D09
C1 D08
VBD7
VBD6
VBD5
VBD4
VBD3
VBD2
VBD1
VBD0
U34
74ALS245A-1
A8 D07
A7 D06
A6 D05
A5 D04
A4 D03
A3 D02
A2 D01
A1 D00
SHEET 5 OF 5
11600- E



REVISIONS			
LTR	DESCRIPTION	DATE	APVD
A	FIRST PRODUCTION RELEASE	09 APR 92	J.F.
B	REV PER ECO# 206	01 MAY 92	J.F.
C	REV PER ECO# 211	17 JUL 92	D.W.
D	REV PER ECO# 216	15 OCT 92	D.W.
E	REV PER ECO# 230	25 OCT 93	D.W.

GPS RECEIVER
CHIP GOES INTO
POSITION U23
PER BANCOMM TECH SUPPORT
1-800-348-0648
2-MAR-93 @ 10:45AM

UC200 FILE: A635_E1.SCH	Datum Inc BANCOMM DIVISION	
DRWN BY: JWL	ASSY, bc635VME/bc350VXI	
DATE: 24 OCT 93	TIME & FREQUENCY PROCESOR	
APP. BY:	SHEET: 1 OF 2	11603 - E

BANCOMM DIV: BILL OF MATERIALS FOR THE bc635VME/bc350VXI T&F PROCESSOR

03-17-1994

S UC	AS	OPT	BC P/N	DATUM P/N	MANF P/N	MANUFACTURER	VALUE	DESCRIPTION	QTY	REF DESIG.
200			1420007		8500-0-1.0	CCI		PC BOARD STIFFENER	1	NONE
200			1501220	0227-0220	SC0R5CC220J	ARCO	22 PF, 300V	DIPPED MICA CAPACITOR	1	C17
200			1503336	0219-0336	336RM025M	IC	33 MF, 35V	ALUMINUM ELECTROLYTIC CAP.	6	C6,24,43,61,62,63
200			1504105	1998105I9035	196B105I9035HA1	SPRAGUE	1.0 MF, 35V	TANTALUM CAP, RADIAL LEADS	1	C5
200			1506152		SR211C152KAA	AVI	1500 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	2	C21,22
200			1506153		SR211C153KAA	AVI	15000 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	1	C19
200			1506332		SR211C332KAA	AVI	3300 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	1	C18
200			1509102		SR211A102JAA	AVI	1000 PF, 100V	MONO CERAMIC CAPACITOR .2R/L	1	C27
200			1512103		TZ03R300ER	MURATA	0-30 PF	CERAMIC TRIMMING CAP, ADJ.	1	C23
200			1515104	CZ80C104MM	MD015E104MAA	AVI/67349	0.1 MF, 50V	DIP GUARD CAPACITOR	49	C1-4,7-16,20,25,26,28-42,44-60
200			1701200		11602E	BANCOMM DIV, DATUM	bc635VME/350VXI	PRINTED CIRCUIT BOARD	1	PCB1
200			2101003	1704-1094-1	31-221	AMPHENOL	50 OHM	FRONT MNT BNC BULKHEAD RECEP.	2	J2,3
200			2104001		913346	ERNI	96 POS	DIN CONNECTOR, MALE	1	P1
200			2111010	1702-6002-10	3591-6002	3M (CONNECTORS)	10 POS	CONTACT HEADER	1	J6
200			2117061		TSW-130-07-G-D	SAMTEC	2X30 POS	STRAIGHT TERMINAL STRIP	1	JP1-3,5=2x2,JP4=2X4
200			2124115		745393-1	AMP	15 POS	'D' SOCKET, .318 RTANG PCBMNT	1	J1
200			2148010		10-2822-90C	ARIES	10 POS	RTANG PCB MOUNT, LED SOCKET	6	DS1-6
200			2149024	1708-3518	824-AG310	AUGAT	24 POS	SLIM DIP SOCKET	1	REF U27
200			2150020	1708-0320	10620-01-445	ANDON/SPECTRA	20 POS	DIP SOCKET	6	REF U10,15,21,28,30,38
200			2150024	1708-3100-24	10624-01-445	ANDON/SPECTRA	24 POS	DIP SOCKET	1	REF U26
200			2150028	1708-3100-28	10628-01-445	ANDON/SPECTRA	28 POS	DIP SOCKET	1	REF U23
200			2152028		641746-2	AMP	28 POS	PLCC REC CHIP CARRIER	2	REF U24,25
200			2152032		821665-1	AMP	32 POS	PLCC REC CHIP CARRIER	2	REF U12,13
200			2152052		641748-2	AMP	52 POS	PLCC REC CHIP CARRIER	1	REF U22
200			2152084	643066-2	PLCC-84-AGW	ADAM TECH	84 POS	PLCC REC CHIP CARRIER	3	REF U31,32,33
200			2192015		HDL15-PL-B	ADAM TECH\SPECTRA	15 POS	HD D-SUB,.350 RTANG PCMT MALE	1	J4
200			2302007		DS-VT-300	SEIKO	32.768 Khz	CRYSTAL	1	Y1
200			2306008	ECS2100-8.00	I209	BIGI-KEY	8MHz	HALF SIZE TTL/CMOS CLOCK OSC	1	U17
200			2401611		11605B	BANCOMM DIV, DATUM	bc635V	FRONT PANEL	1	BKT1
200			2404600		VME-6U-1450	PHILLIPS COMPONENTS		VME EJTRACTOR HANDLES KIT	1	BKT1
200			2802002		3341-1S	3M		JACK SCREW KIT	2	J1,4
200			3703002		LTB360HR	LITEON	HI-BRIGHT	7 SEGMENT DISPLRY, 0.36 INCH	6	REF: DS1-6
200			3902001		PRB4.8-15-H3	PLAINVIEW INC.	4.8V	NICAD PCMNT BATTERY	1	B1
200			4305030		RIE030	RAYCHEM		POLYSWITCH	1	TD1
200			4701101	0102-0101	RC07GF101J	ALLEN BRADLEY	100 OHM, 1/4W	FIXED RESISTOR	2	R2,14
200			4701102	0102-0102	RC07GF102J	ALLEN BRADLEY	1 K OHM, 1/4W	FIXED RESISTOR	1	R1
200			4701103	0102-0103	RC07GF103J	ALLEN BRADLEY	10 K OHM, 1/4W	FIXED RESISTOR	9	R5,6,7,13,16,18,20,22,26
200			4701104	0102-0104	RC07GF104J	ALLEN BRADLEY	100 K OHM, 1/4W	FIXED RESISTOR	2	R8,19
200			4701123	0102-0123	RC07GF123J	ALLEN BRADLEY	12 K OHM, 1/4W	FIXED RESISTOR	1	R3
200			4701204	0102-0204	RC07GF204J	ALLEN BRADLEY	200 K OHM, 1/4W	FIXED RESISTOR	1	R4
200			4701240		RC07GF240J	ALLEN BRADLEY	24 OHM, 1/4W	FIXED RESISTOR	1	R23
200			4701332	0102-0332	RC07GF332J	ALLEN BRADLEY	3.3 K OHM, 1/4W	FIXED RESISTOR	1	R12
200			4701393	0102-0393	RC07GF3933	ALLEN BRADLEY	39 K OHM, 1/4W	FIXED RESISTOR	2	R9,10
200			4701471	0102-0471	RC07GF471J	ALLEN BRADLEY	470 OHM, 1/4W	FIXED RESISTOR	2	R11,15
200			4701472	0102-0472	RC07GF472J	ALLEN BRADLEY	4.7 K OHM, 1/4W	FIXED RESISTOR	2	R24,25
200			4701513	0102-0513	RC07GF513J	ALLEN BRADLEY	51 K OHM, 1/4W	FIXED RESISTOR	2	R17,21
200			4703103		72P103	BECKMAN	10 K OHM, 1/2W	SINGLE TURN POTENTIOMETER	1	VR2
200			4704102		89PR1K	BECKMAN	1 K OHM, 1/2W	POTENTIOMETER	1	VR1
200			4705103		710A103	ALLEN BRADLEY	10 K OHM, 1/8W	C-SIP RESISTORS, 10 PIN 'I'	3	RP1,2,3
200			4801002		2N2222			NPN SWITCHING/AMPLIFIER (TO18)	1	Q1
200			4802002		2N2907A	MOTOROLA	3P 8 PKG	PNP SWITCHING/AMPLIFIER (TO18)	1	Q2
200			4803001	0500-0306	IN914			SILICON DIODE	2	CR1,2
200			5108001		76SB04	GRAYHILL		4PST DIP SWITCH	1	SW2
200			5108002		76SB08	GRAYHILL		8PST DIP SWITCH	1	SW1
200			9002510		74ACT14	RCA	14P DIP PKG	HEI SCHMITT INVERTER	2	U11,16
200			9004858		MM74FJ74N	NATIONAL	20P DIP PKG	OCTAL D FLIP FLOP	1	U36
200			9008657	0301-HC37-3	74HC373	VARIOUS	20P DIP PKG	OCTAL D TRANSPARENT LATCH, T/S	2	U14,20
200			9015940		SN74ALS688N	TI	20P DIP PKG	8 BIT MAGNITUDE COMPARATOR	1	U35
200			9102003		MC68HC11E0FN	MOTOROLA	52P PLCC PKG	MICROCOMPUTER	1	U22 (SKT)
200			9103036		MSM6242BRS/GS-VK	OKI	18P DIP PKG	REAL TIME CLOCK/CALENDAR	1	U9
200			9103040		82C54-2	INTEL	28P PLCC PKG	PROGRAMMABLE COUNTER TIMER	1	U24 (SKT)
200			9201030		MC34064P-5	MOTOROLA	3P CASE29-04 PKG	UNDERVOLTAGE SENSING DEVICE	1	U3
200			9203005		AD558JN	ANALOG	16P DIP PKG	8 BIT DACPORT	1	U19
200			9203030		AD569JP	ANALOG DEVICES	28P PLCC PKG	16-BIT MONITONIC V/O DAC	1	U25 (SKT)
200			9204020	0301-7218-1	ICM7218CIPI	MAXIM	28P DIP PKG .6W	8 DIGIT LED DISPLAY DRIVER	1	U3
200			9207070		SN75158P	TI	08P DIP PKG	DUAL 50 OHM TTL LINE DRIVER	1	U7
200			9207079		SN75179B	TI	08P DIP PKG	DIFF DRIVER/RECIVER PAIR	2	U1,4
200			9207615	0301-HC24-6	74HC244	NATIONAL	20P DIP PKG	OCTAL BUFFER/LINE DRIVER	1	U29
200			9207920		SN74ALS245A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	2	U34,37
200			9207925		SN74ALS641A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	1	U39
200			9306007		LM6321N	NATIONAL	08P DIP PKG	HIGH SPEED BUFFER	1	U2
200			9306035	0301-0002	TL082	TI	08P DIP PKG	DUAL BIPOLAR JFET OP AMP	1	U8
200			9307030		XR2212CP	EXAR	16P DIP PKG	PHASE LOCKED LOOP	1	U5
200			9313005		AD586JQ	ANALOG DEVICES	08P DIP PKG	HIGH-PRECISION 5V REF.	1	U18
200			9404010		IDT7201SA120J	IDT	32P PLCC PKG	FIFO 9 X 512	2	U12,13 (SKT)
200			9405001		EP600DC-3	ALTERA	24P DIP PKG .3W	EPLD	1	U27 (SKT)
200			9405013		PAL16L8B	NMI	20P DIP PKG .3W	PAL	6	U10,15,21,28,30,38 (SKT)
200			9405058		IC3030-50PC84C	XILINI	84P PLCC PKG	PLD	1	U31 (SKT)
200			9405060		IC3042-50PC84C	XILINI	84P PLCC PKG	PLD	2	U32,33 (SKT)
200			9406005	0301-27C1-6	2716	VARIOUS	24P DIP PKG .6W	2 K X 8 UV ERASABLE PROM	1	U26 (SKT)
200			9406040	0301-27C2-56	27C256	VARIOUS	28P DIP PKG .6W	32 K BYTE, CMOS EPROM	1	U23 (SKT)
200	00							STANDARD ASSEMBLY		
200	00		2305002		C0-401V-AI	VECTRON	10 MHz	VCXO	1	U6
200		AMT					bc637V GPS ONLY	ANTENNA OPTION		
200		AMT	2193015		HDT15-SB	ADAM TECH/SPECTRA	15 POS	HD D-SUB,SOLDER CUP FEMALE	1	AMT
200		AMT	9700007		18636/19360-50	TRIMBLE NAV.	ANTENNA	TRIMBLE ACUTIME W/TSI & RS422	1	
200		BNC						EXT. CABLE PARTS		
200		BNC	2106001		31-317	AMPHENOL	50 OHM	BNC JACK, STRIGHT	4	
200		BNC	2123015		DAE15P	CANNON	15 POS	'D' PLUG	1	
200		OVN						OVEN OSCILLATOR OPTION		
200		OVN	2307001		240-0330 AT	MILLIREN TECH. INC.	10 MHz	OVEN OSCILLATOR	1	U6
200		VME					bc635VME	OPTION (WITH P2 CONNECTOR)		
200		VME	2104001		913346	ERNI	96 POS	DIN CONNECTOR, MALE	1	P2

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