

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Microsemi / Symmetricom / TrueTime GPS-VME* at our website: *Click HERE*

TABLE OF CONTENTS

SECTION	PARAGRAPH	TITLE
ONE		**GENERAL INFORMATION**
	1.1	Scope of Manual
	1.2	Purpose of Equipment
	1.3	Physical Description
	1.4	Environmental Specifications
	1.5	Power Requirements
	1.6	Signal Specifications
	1.6.1	General To All Modes
		A. VME Bus
		B. Interrupts
		C. Time Compare Outputs
		D. External Freeze Event Input
		E. Rate Generator Output
		F. Auto Leap Year
		G. Internal Oscillator
		H. External Start Input
		I. Pulse Rate
		J. IRIG B DC (TTL) Time Code Output
		K. IRIG B Amplitude Modulated Time Code Output
		L. IRIG B DC (TTL) Time Code Output
	1.6.2	Generator Specifications
		A. General
		B. External Time Base
	1.6.3	Sync-Generator Specification
		A. General
		B. GPS Reference
		C. Reference Code Input, Carrier
		D. Reference Code Input, DC (RS-422)
	1.6.4	I/O Connector Specifications
		A. VME P2/J2 Connector
		B. Front Panel BNC Connector
		1. External Event Input
		2. Reference Code Input
		3. Generator Code Output
		4. 1 PPS Output
TWO		**INSTALLATION AND OPERATION**
	2.1	Introduction
	2.2	Installation
	2.3	Operation, General Information
	2.4	Operation, Detailed Information

TABLE OF CONTENTS
(Continued)

SECTION	PARAGRAPH	TITLE
TWO		**INSTALLATION AND OPERATION**
	2.4.1	Generator
	2.4.2	GPS Synchronized Generator
	2.4.3	Code Synchronized Generator
	2.4.4	Front Panel Indicators And Display
	2.4.5	Oscillator Discipline
	2.4.6	Reading Time
	2.4.7	Reading Position
	2.4.8	Loading Position
	2.4.9	Operational Configuration And Status Registers
	2.4.10	VME Interrupt Control
	2.4.11	VME-SG-GPS Memory Map
	2.5	Programming Examples
THREE		**MANUFACTURERS SPECIFICATIONS**
FOUR		**DRAWINGS**

Drawing Number	Title
560-1146	VME-SG Front Panel Assembly/BOM
560-5608	VME-SG2 Assembly/BOM
560-5603	VME Processor Board Assembly/BOM

GENERAL INFORMATION

1.1 SCOPE OF MANUAL

This manual contains the information necessary to operate and maintain the TrueTime VME Timing Cards. Multiple configurations are described. This VME product line consists of the VME Timing board which by itself is referred to as the VME-SG. When a GPS Engine is added to the basic VME Timing board assembly the product becomes known as the GPS-VME. All functions described in this manual are available in the GPS-VME version. The VME-SG does not provide GPS related functions. Both the GPS-VME and the VME-SG may be configured with the optional alphanumeric display front panel assembly. In this manual these two board configurations are referred to as the Model VME-SG-GPS.

1.2 PURPOSE OF EQUIPMENT

The VME-SG-GPS is a precision time source that conforms with the IEEE 1014.C-1 VMEbus Specification. The VME-SG-GPS operates in one of the following three modes: Generator, GPS Synchronized Generator (GPS-VME only) or Code Synchronized Generator. In all modes the VME-SG-GPS is designed to supply precise time to a VME based computer. The time consists of microseconds through thousands of years. In the Generator mode the time can be started, stopped and preset via the VME bus. The Generator counters can also be started using an external reference 1 PPS pulse. In the GPS Synchronized Generator mode the card operates with the GPS Engine. Time and position are derived from the NAVSTAR Global Positioning System (GPS). In the Code Synchronized Generator mode the generator will phase lock to an external IRIG B time code. The code format can be either amplitude modulated or DC shift at RS-422 logic levels. In all synchronized modes the internal oscillator is disciplined to remove any frequency offset with respect to the external reference. This is necessary to maintain precise phase lock and to minimize drift error if the input reference is lost.

Time information and status are available to the VME computer bus in five, 16 bit words. Each word contains up to 4 packed BCD time values. Since no time ready flags must be set before time information can be read, the data is immediately available (zero latency). On board DIP switches select the memory address space where the VME-SG board resides.

Two independent time capture register sets are provided. Time is latched or "frozen" in one set of registers by a user read operation via the VME bus. This will provide time on request. The second set of capture registers has the time latched into it when an External Event pulse occurs. This allows time tagging of an External Event. An event normally is programmed to generate an interrupt to flag its occurance.

A Rate Generator is provided that is configured by the user to output one of 5 different pulse rates to the P2 connector. The Rate Pulse can also be configured to produce an interrupt to the VME processor.

Two Time Compare register sets are available that are preset with time values from hundreds of days through microseconds via the VME bus. When either compare time is equal to the generator time an output pulse is generated.

Four independently programmable interrupts are available each with software selectable priority. The interrupt sources are the External Event, Rate Pulse, Time Compare 1 and Time Compare 2.

The VME-SG-GPS is configured as an A16/D16 slave board responding to the Address Modifier codes hex 29 (short non-priviledged) and hex 2D (short supervisory). The VME-SG-GPS is memory mapped on any 256 byte boundary of the VME bus short address space using the eight position DIP switch located on the board.

1.3 PHYSICAL DESCRIPTION

The VME-SG configuration is a single slot board meeting the VME standard 6U height specification. When the optional display is added two slots are required. The GPS-VME configuration requires two slots with a 6U height.

1.4 ENVIRONMENTAL SPECIFICATIONS

The Model VME-SG-GPS is designed to operate over a wide ambient temperature range.

The environmental specifications are:

a. Operating	-	0 to +50 degrees C (+32 to +122 F)
b. Storage	-	-17 to +100 degrees C (0 to +212 F)
c. Humidity	-	To 95% relative, non-condensing

1.5 POWER REQUIREMENTS

The maximum input power specifications are:

a.Voltage	-	+5VDC @ 700 ma ± 12 VDC @ 50 ma each, (from VME bus connector)

1.6 SIGNAL SPECIFICATIONS

1.6.1 GENERAL TO ALL MODES

A.	VME Bus	-	Falling edge of /DSA to falling Access Time edge of /DTAK is less than 400 nanoseconds.
B.	Interrupts		
	Number	-	Four independent
	Priority	-	Configurable to any of seven levels.
	Sources	-	External Event

- Programmed Rate Generator
- Programmed Compare Time #1
- Programmed Compare Time #2

C. Time Compare Outputs

Outputs a pulse at the programmed compare time #1.
Outputs a pulse at the programmed compare time #2.
Asserts the Interval level during the interval between compare time #1 and compare time #2.

Resolution	-	1 microsecond
Pulse Width	-	2 milliseconds
Compare Mask	-	milliseconds through hundreds of days
Signal Level	-	Positive going, +5v @ +/- 6ma

See section 1.6.4 for P2/J2 pin assignment

D. External Freeze Event Input

Edge	-	Rising or falling
Input	-	Logic 0: 0 +.5 VDC
Voltage		Logic 1: +2.5 to 5 VDC
Input	-	4.7 K ohms to +5 VDC

The External Freeze Event signal may be input at the front panel BNC or on the P2/J2 connector. See section 1.6.4 for P2/J2 pin assignment.

E. Rate Generator Output

Outputs a programmed pulse rate. Rising edge on-time.

Rates	-	10K, 1K, 100, 10 and 1 Pulse Per Second (PPS)
Signal Level	-	Positive going, +5v @ +/- 6ma

See section 1.6.4 for P2/J2 pin assignment.

F. Auto Leap Year - calculated using year

G. Internal Oscillator (TCVCXO)

Frequency	-	10MHz
Stability	-	1 PPM, 0 to +50 Degrees C
Aging	-	< 1PPM/Year

H. External Start Input

Start Timing	-	Selectable positive or negative edge.
Input Voltage	-	Logic Zero: 0vdc, +/- .5vdc
		Logic One: >+2.5vdc, <+5vdc
		Input Impedance: 4.7K Ohms to +5v

The External Start signal is input on the P2/J2 connector.
See section 1.6.4 for P2/J2 pin assignment.

I. Pulse Rate

Frequencies	-	1PPS
Duty Cyle	-	50%
Amplitude	-	0vdc to +5vdc @ +/- 6ma
Timing	-	Positive going edge on time

See section 1.6.4 for P2/J2 pin assignment.

J. IRIG B DC Time Code Output (TTL)

Amplitude	-	0vdc to +5vdc @ +/- 6ma

See section 1.6.4 for P2/J2 pin assignment.

K. IRIG B Amplitude Modulated Time Code Output

Amplitude	-	Adjustable from 0vpp to 10vpp into 600 Ohms to ground
Ratio	-	Adjustable from 2:1 to 5:1

See section 1.6.4 for P2/J2 pin assignment.

L. IRIG B DC Time Code Output (RS-422)

Signal Output	-	RS-422 Logic Levels

See section 1.6.4 for P2/J2 pin assignment.

1.6.2 GENERATOR SPECIFICATIONS

A. General Specifications

Indicators LEDs	-	Power, 1PPS

B. External Time Base Input (generator only)

Frequency	-	10MPPS
Input Voltage	-	Logic Zero: 0vdc, +/- .5vdc Logic One: >+2.5vdc, <+5vdc

The External Time Base signal is input on the P2/J2 connector.
See section 1.6.4 for P2/J2 pin assignment.

1.6.3 SYNCHRONIZED GENERATOR SPECIFICATIONS

A. General Specifications

Indicator LEDs	-	Power
	-	1 PPS
	-	Phase Locked
	-	Input Code Error

B. GPS Reference

Phase Accuracy	-	Less than 1 microsecond to UTC, typically less than 500 nanoseconds
Osc. Freq. Discipline	-	Better than 1 E -7, typically 5 E -8
Phase Correction Step Size	-	100 nanosecond after PHASE LOCK
Position	-	Latitude, Longitude and Elevation 100 meters 2DRMS
Time To First Lock	-	<20 minutes when at least 4 satellites available
User Time Bias	-	$\pm$ 99999 nanoseconds
Local Offset	-	$\pm$ 12 hours

C. Reference Code Input, Carrier

Format	-	IRIG B122
Amplitude	-	1vpp to 10vpp
Impedance	-	10K ohms to ground
Ratio	-	2:1 to 5:1
Error Bypass	-	Fixed at 3 frames
Osc. Freq. Discipline	-	Better than 1 E -7, typically 5 E -8
Phase Accuracy	-	Less than 2 microsecond, typically less than 1 microsecond

Phase Step Size	-	100 nanosecond after PHASE LOCK Correction
Phase Compensation	-	± 1 millisecond in 1 microsecond steps

The Time Code signal may be input at the front panel BNC or on the P2/J2 connector.
See section 1.6.4 for P2/J2 the pin assignment.

D. Reference Code Input, DC Shift (RS-422)

Format	-	IRIG B122
Signal	-	RS-422 logic level
Impedance	-	120 ohms selectable using JP1
Error Bypass	-	Fixed at 3 frames
Phase Accuracy	-	Less than 1 microsecond, typically less than 500 nanoseconds
Osc. Freq. Discipline	-	Better than 1 E -7, typically 5 E -8
Phase Correction Step Size	-	100 nanosecond after PHASE LOCK

The Time Code signal is input at the P2/J2 connector.
See section 1.6.4 for P2/J2 the pin assignment.

1.6.4 I/O CONNECTOR SPECIFICATIONS

1. VME P2/J2 Connector

PIN #	ASSIGNMENT	PIN #	ASSIGNMENT
C1	1PPS OUT	A1	GND
C2	RATE PULSE OUT	A2	GND
C3	CODE INPUT (AM)	A3	GND
C4	TIME COMP #1 OUT	A4	GND
C5	TIME COMP #2 OUT	A5	GND
C6	INTERVAL OUT	A6	GND
C7	EXT EVENT INPUT	A7	GND
C8	EXTERNAL OSC INPUT	A8	GND
C9	GEN CODE OUT DC (TTL)	A9	GND
C10	GEN CODE OUT AM	A10	GND
C11	GEN CODE OUT (RS-422)+	A11	GEN CODE OUT (RS-422)-
C12	REF CODE IN (RS-422)+	A12	REF CODE IN (RS-422)-
C13	REF CODE OUT (RS-422)+	A13	REF CODE OUT (RS-422)-

Table 1-1

Note:

Gen Codes and Ref Codes are IRIG B format.
Ref Code Out (RS-422) is the Ref Code Input signal re-driven through an RS-422 driver for daisy chained systems.

2. Front Panel BNC Connectors

a. External Event Input

The External Event input is available on the front panel BNC labeled EXT EVENT. This input is in parallel with the same input on the P2/J2 connector.

b. Reference Code Input

The amplitude modulated time code input is available on the front panel BNC labeled CODE IN. This input is in parallel with the same input on the P2/J2 connector.

c. Generator Code Output

The amplitude modulated time code output is available on the front panel BNC labeled GEN CODE. This output is in parallel with the same output on the P2/J2 connector.

d. 1PPS Output

The 1 pulse per second (PPS) output is available on the front panel BNC labeled 1PPS. This output is in parallel with the same output on the P2/J2 connector.

1.6.5 JUMPER SPECIFICATIONS

RS-422 Term Res (120 ohms)	-	Install jumper between JP1-2 and JP1-3 to enable termination (ON). Install jumper between JP1-1 and JP1-2 to disable (OFF).
GPS battery backup	-	Install jumper between JP2-2 and JP2-3 to connect battery (ON). Install jumper between JP2-1 and JP2-2 to disable (OFF).

1.6.6 OPTIONAL FRONT PANEL ALPHANUMERIC DISPLAY

Type	-	4 character by 4 line LED
Display Info	-	Time (days, hrs, min & sec) Date (month, day-of-month, year) Oper Mode (gen, code sync-gen, GPS sync-gen*) Sync Status (oper errors, phase) Latitude*(degrees, minutes& seconds) Longitude* (degrees, minutes & seconds) Elevation* (meters) Tracking Status* (number of satellites) Self Test (error code)

*available in GPS-VME only

SECTION TWO

INSTALLATION AND OPERATION

2.1 INTRODUCTION

This section contains installation instructions and operating procedures for the VME-SG-GPS. As stated in section one there are two configurations of this product. The timing processor board alone is referred to as the VME-SG 2. When the GPS Engine is installed the board is referred to as the GPS-VME. The GPS-VME is capable of providing GPS related functions only.

2.2 INSTALLATION

Unpack the unit and carefully inspect it for shipping damage. Any damage must be reported to the carrier immediately.

Prior to insertion of the card into the users subrack the following setup/configuration operations must be performed.

A. Base Address Selection:
The VME-SG-GPS will operate in the short address space selected by the DIP switch located in U2. The DIP switch has 8 sections identified as 1 - 8. Each section may be set ON or OFF to place the address space of the VME-SG-GPS on any 256-byte boundary. The switch sections correspond to VME address bits A8 - A15. Section 1 selects the least significant address. When the switch is in the ON position the zero address condition is asserted. Therefore, to select the lowest address in VME memory all 8 switch sections should be set "ON".

VME ADDRESS STRUCTURE

(24 bits represented)

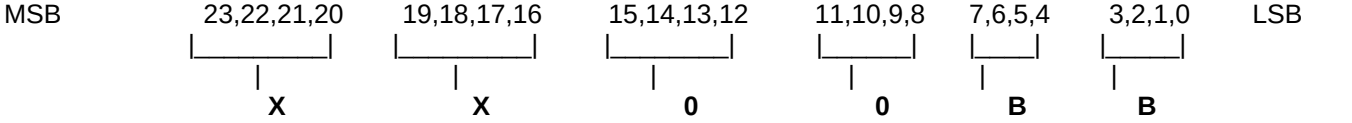


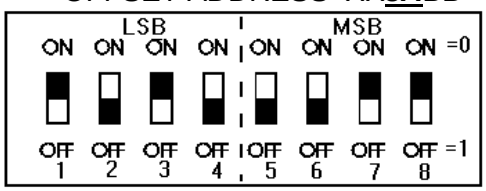
Figure 1 represents an OFFSET address of **00** Hex **XX00BB** where **XX** is the user defined MSB's, **00** is the user selectable VME-SG-GPS OFFSET and **BB** is the Board address space which is allocated for the VME-SG-GPS's I/O.

Switch Positions 1 through 8 control the OFFSET address of the VME-SG card.

To set the OFFSET ADDRESS:

Select the offset address **HEX** value you want to use, such as	3A
Convert the hex value to **BINARY**,	00111010
REVERSE the order of the Binary number,	01011100
Set switches 1-8 using this **REVERSE BINARY NUMBER**.	ON=0, OFF=1

(Example 1) OFFSET ADDRESS XX***3A***BB

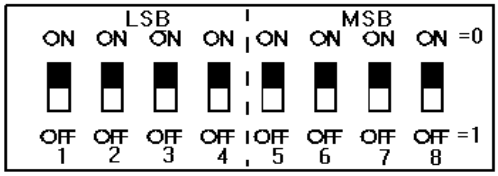


0=ON, 1=OFF
Black= Switch Position

Hex	**3A**
Binary	**00111010**
Reversed Order	**01011100**

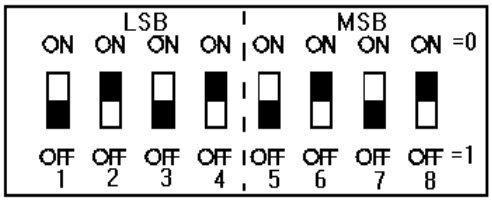
(Example 2)

FACTORY DEFAULT OFFSET ADDRESS XX***OO***BB



Hex	**00**
Binary	**00000000**
Reversed Order	**00000000**

(Example 3) OFFSET ADDRESS XX***55***BB



Hex	**55**
Binary	**01010101**
Reversed Order	**10101010**

B. Backplane Jumpers:
The VME-SG-GPS has interrupt capability and the /IACKIN and the /IACKOUT signal lines are passed in and out of the board. Be sure that any backplane jumpers on these pins in the slot allocated to the VME-SG-GPS are removed even if the VME-SG-GPS interrupts are not enabled.

C. P2 Connector Conflicts:
Some systems use the P2/J2 connector for their local bus or other control signals. Several VME-SG-GPS input and output signals are located on the P2/J2 connector in rows A and C. Verify that there is no conflict. Table 1-1 in section 1.6.4 describes the pins used on the P2/J2 connector.

Mount the unit in the desired location and secure the front panel mounting screws. Mount the antenna in the desired location (see drawing 142-800). Connect the antenna lead-in to the front panel of the VME-SG-GPS.

2.3 OPERATION, GENERAL INFORMATION

This section describes operating procedures for the standard VME-SG-GPS. This manual describes some options that may not be present in the users particular card configuration.

Section 2.5 provides programming examples to further illustrate the operational capabilities of the VME-SG-GPS.

The VME-SG-GPS is configured as an A16/D16 slave board responding to the Address Modifier codes hex 29 (short non-privileged) and 2D (short supervisory). The interface consists of address decode logic, the VME-2000 interface controller chip and various bus interface handshake logic.

There are three operating modes that may be selected by the user. They are Generator, GPS Synchronized Generator and Code Synchronized Generator mode. At power up, the unit will initialize itself in the GPS Synchronized Generator mode.

Time and status information that is read from the card and configuration and control information that is written to the card is achieved with a 16 bit Dual Port RAM and specific hardware registers. The Dual Port RAM is the storage location for time, status and control information. The VME-SG-GPS writes the time and status words to the RAM at locations controlled by RAM addressing logic. Other areas of the RAM are written to directly via the VME interface to load configuration and control words. All operating modes and control of the VME-SG-GPS is performed using these location. Section 2.4.9 provides a detailed description of the control registers.

The VME-SG-GPS is capable of generating interrupts from up to four independent sources. The sources are the External Event input, the Pulse Rate logic and the 2 Time Compare Outputs. Each interrupt source separately configured with priority level as well as the interrupt vector returned over the VME bus during an interrupt acknowledge sequence. The Bus Interrupt Module (BIM) handles the VME interrupt operations. This device is programmed directly over the VME interface. Section 2.4.10 describes the Interrupt Control logic.

The VME-SG-GPS Rate Generation logic provides 5 different pulse rate outputs. The pulses can also trigger the VME bus interrupt (INT1). All pulse rate outputs are synchronous with the board timing. The pulse rate output is also available on the P2/J2 bus. Section 2.4.9 describes programming the Rate Generation Logic. Section 2.5 lists example routines.

The VME-SG-GPS contains 2 Time Coincidence Compare registers that each output a strobe at their programmed compare times. There is also an Interval logic level that is triggered high with compare strobe #1 and set low with compare strobe #2. The strobes are rising edge on-time and are set microsecond resolution. The compare strobes are also used to generate interrupts (INT2 and INT3) to the VME interface.

Time is captured using the External Event detection logic. The external event pulse active edge (rising or falling) selection is defined by Configuration Register #2, bit #2 (see section 2.4.6). When the external event pulse occurs, Time Capture register #2 contains the time. The External Event input pulse is programmed to generate the VME bus interrupt (INT0) to flag the user that the event input occurred.

A battery is provided on the board to supply power to the GPS Engine when the main power is off. The battery power drives RAM memory and a real time clock located on the GPS Engine card. The RAM is used to store position and almanac information. If this information is not available at power up the GPS Engine will perform a cold start and enter a Search The Sky mode to locate satellites. When a satellite is tracked, new almanac data is downloaded. This process can take anywhere from 12 to 25 minutes. This process is necessary to compute position and determine accurate time. See Position Mode in section 2.4 for more information.

After the VME-SG-GPS has attained phase lock and computed position, these parameters are maintained in the battery backed GPS Engine even if power is lost. When power is restored these parameters will be transferred into the time and position registers in the main processor board. This occurs a few seconds after the card has initialized itself. If UTC time is selected for output (config register #2, bit 7) the time information will indicate a difference of several seconds after power up since GPS time rather than UTC time is maintained in the GPS Engine during the power down time.

A jumper is installed on JP2 between pins 2 and 3 to connect the battery at the factory prior to shipment. If the card is to be stored for extended periods (months) the jumper should be installed between pins 1 and 2 which disconnects the battery. When power is ON there is no battery current drain.

2.4 OPERATION, DETAILED INFORMATION

2.4.1 GENERATOR

The Generator accumulates time using an internal or external time base and provides time information to the VME bus consisting of microseconds through thousands of years. The VME-SG-GPS contains two time capture register sets. Each capture register consists of five 16 bit word locations where the current time is "frozen". Time is captured in register number 1 when a time requests via the VME bus occurs. Time is captured in register number 2 by an External Event input. This allows the user to request time on demand as needed and also record when an external event has occurred even if both occur simultaneously.

The generator is started and stopped using Configuration Register #1. The user may preset the time from milliseconds through years while the Generator is stopped or running. The generator can be synchronously started using an externally generated 1 PPS signal. The start strobe, when enabled, is input via the External Event input connector. Either the rising or falling transition of the pulse is selected.

2.4.2 GPS SYCHRONIZED GENERATOR

The GPS Synchronized Generator mode operates as a Generator that is synchronized to the GPS Engine. The GPS Engine receives transmissions from the Global Positioning Satellite system and derives time that is traceable to the National Institute of Standards and Technology (NIST). If the GPS Engine indicates that good time is available, the card will phase lock the generator time registers. The VME-SG-GPS card contains a Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO). The VCTCXO is disciplined to remove any frequency errors. The phase errors are removed by the Phase Correction logic which advances or retards the generator time using 100 nanoseconds steps.

When time from the GPS Engine is valid the front panel LOCK LED will blink slowly (2 second rate) until the phase errors are less than 10 microseconds. At that time the LOCK LED will blink faster (twice per second) until the generator is phase locked to < 1 microsecond and the oscillator frequency has stabilized. At that time the LOCK LED will be ON continuously. When time from the GPS Engine is not valid the LOCK LED will be OFF. If the GPS Engine is not operating properly the red LED indicator on the front panel identified as ERR illuminates. This LED may illuminate momentarily when power is applied to the card or when the operational mode is changed. See Table 2-1 .

2.4.3 CODE SYCHRONIZED GENERATOR

The Code Synchronized Generator mode operates as a Generator that is synchronized to an external IRIG B input code. The VME-SG-GPS card will operate with either IRIG B amplitude modulated or IRIG B DC shift at RS-422 logic levels. The code input format selection is made via Configuration register 2, bit 3. The Sync-Gen will phase lock to the input code and discipline the VCTCXO. The phase correction logic advances or retards the time to keep it phase locked to the IRIG reference. The Generator time is phase shifted by 100 nanoseconds steps. The front panel LOCK LED indicator operates in the same manner as in the GPS Synchronized Generator mode indicating relative phase accuracy. See table 2-1. An ERR LED indicator on the front panel illuminates when the input code is not present, is of the wrong format or fails to pass numerous error detection criteria.

2.4.4 FRONT PANEL INDICATORS AND DISPLAY

LED INDICATORS - The VME-SG-GPS front panel has four indicator LEDs. They are labeled POWER, 1PPS, LOCK and ERR. The POWER indicator is on when power is applied to the card. The 1PPS indicator will blink once per second when the generator is running. The LOCK and ERR indicators are only used in the synchronized generator modes. The table below and sections 2.4.3 and 2.4.2 describe their operation.

LED NAME	CONDITION	DEFINITION
LOCK	Blinking Slowly	Phase Error> 10 microseconds
	Blinks Twice/sec	Phase Error < 10 microseconds
	ON Constantly	Phase Error within spec
	OFF Constantly	Reference not valid
ERR	ON Constantly	Reference failure
	OFF Constantly	Reference is OK

Table 2-1, Front Panel LEDs

ALPHANUMERIC DISPLAY - An optional alphanumeric LED display is available that consists of 4 lines by 4 characters. The display allows the user to observe time, date, operational mode, sync status, position, satellite tracking status and self test results. A switch on the front panel is used to select the different displays. The time display will flash after power up in the GPS Sync-generator mode until LOCK has occurred. This indicates that the time is not accurate.

2.4.5 OSCILLATOR DISCIPLINE

The VME-SG-GPS will discipline the VCTCXO by driving a control voltage to the oscillator so that its frequency relative to the time reference is as small as possible. The accumulative phase error generated due to the frequency error of the oscillator is used to drive the voltage control circuitry. If the time reference is lost oscillator discipline will cease. The time will drift at a rate that is dependent on how well the oscillator was disciplined and future changes in ambient temperature. The oscillator will discipline to the reference to better than 1 part in ten to the seventh (typically 5 parts in ten to the eighth). The oscillator has a temperature stability of 1 part in ten to the sixth from 0 to 50 degrees C. The major contributor to time drift when no reference is present is temperature.

2.4.6 READING TIME

There are two capture register sets available in the VME-SG-GPS for the storing and reading of the Generator time. There are time read examples in the Programming Examples description Section 2.5.

Time Capture Registers #1
A computer read command via the VME interface is used to "freeze" the time in Capture Register Set #1. The address that is read to assert the freeze is at the board base address plus offset hex 40. The time is read in five 16 bit words at offsets hex 42 (word 1), 80 (word 2), 82 (word 3), 84 (word 4) and 86 (word5). Reading the location at offset hex 44 releases the freeze registers.

Time Capture Register #2
Time Capture Register 2 is "frozen" by the External Event input pulse. The time is read in five 16 bit words at offsets hex 46 (word 1), 88 (word 2), 8A (word 3), 8C (word 4) and 8E (word 5). Reading the location at offset hex 48 releases the freeze condition. The External Event interrupt is used to determine that an external pulse occurred.

The data is in a packed BCD format as described below in table 2-2.

	Data Bits 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Word 1	Unit Msec	Hund Mic-sec	Tens Mic-sec	Unit Mic-sec
Word 2	Tens Seconds	Unit Seconds	Hund Msec	Tens Msec
Word 3	Tens Hours	Unit Hours	Tens Minutes	Unit Minutes
Word 4	Status *	Hund Days	Tens Days	Unit Days
Word 5	Thous Years	Hund Years	Tens Years	Unit Years

* Status Definition
Bit 12 - Input Reference Error (Sync-Gen Modes)
Bit 13 - Phase Locked (Sync-Gen Modes)
Bit 14 - Reserved
Bit 15 - Reserved

Table 2-2, Time Words

2.4.7 READING POSITION

When in the GPS synchronized generator mode position information is generated by the GPS Engine. Position consists of latitude and longitude in degrees, minutes, seconds with North/South/East/West indicators and elevation in meters above or below sea level. The position information actually defines the location of the antenna.

Position data is read at address offsets hex 90 - 9E. All values are packed BCD except for the North/South and East/West indications which are ASCII byte values. Table 2-3 below describes each position register with its address offset and data organization.

0090		Latitude (0, Hund, Tens, Units degrees)
0092		Latitude (Tmin, Umin, Tsec, Usec)
0094		Latitude (N/S, Tenths seconds)
0096		Longitude (0, Hund, Tens, Units degrees)
0098		Longitude (Tmin, Umin, Tsec, Usec)
009A		Longitude (E/W, Tenths Seconds)
009C		Elevation (Sign, Ten Thous & Thous Meters)
009E		Elevation (hund, Tens, Unit and Tenths Meters)
	**	The right most value is in the least significant nibble of the 16 bit word.

Table 2-3, Position

2.4.8 LOADING POSITION

When in the GPS synchronized generator mode the position of the antenna is loaded using the position registers described above. It is sometimes advantageous to load the position of the antenna since accurate antenna position will reduce timing errors. Accurate time is computed if only one satellite is tracked when the position information is known. Due to buildings or other physical obstruction 4 or more satellites may not be in view with great enough regularity to allow the VME-SG-GPS card to compute position conveniently.

The Position Computation Mode must first be set to KNOWN so the GPS Engine will stop computing new position data. In all modes the position is output to the registers described above except when the Position Update Inhibit bit is set. This bit is contained in configuration register #2, bit #4. This bit allows the registers to be used for loading new position from the VME bus.

The position data is written to the position registers in the same format described above. When this is completed the Position Load Request bit in configuration register #2, bit 5 is set. This causes the position data and current time to be formatted and transferred to the GPS Engine. If the GPS Engine is not tracking satellites the current time information residing in the VME-SG-GPS card must be roughly accurate (within several minutes).

Both the Load Position Request bit and the Position Update Inhibit bits will clear when the load sequence has completed.

2.4.9 OPERATIONAL CONFIGURATION AND STATUS REGISTERS

The user has access to several registers which are used to control and read status from the VME-SG-GPS. All of these registers are written to and read via the VME bus. The Configuration registers are used to control all generator and synchronized generator operations. Several registers contain position (Longitude, Latitude and Elevation) and GPS receiver operational status. The user determines the physical address of the registers by adding the hexadecimal offset for each register to the VME-SG-GPS base address. Section 2.2 part A describes the VME-SG-GPS base address. The following describes each of the configuration and status registers:

CONFIGURATION REGISTER 1 (base address + hex 00A0)
This register is used to set the Operational mode, Start/Stop the Generator, enable the Generator preset, select internal or external oscillator, and enable the interrupts.

bits:	0	-	Operation Mode Select (bit 1)
	1	-	Operation Mode Select (bit 2)
	2	-	Generator Stop
	3	-	Generator Preset Enable
	4	-	External Start Enable
	5	-	External Oscillator Select
	6	-	NU (not used)
	7	-	Interrupt Enable
	8	-	NU
	9	-	NU
	10	-	NU
	11	-	NU
	12	-	NU
	13	-	NU
	14	-	NU
	15	-	NU

a) Mode - Bits 0 and 1 determine the operation mode as follows:

bit 2	bit 1		
0	0	-	Generator
0	1	-	GPS Synchronized Generator
1	0	-	IRIG B Synchronized Generator

Generator Mode - In this mode the VME-SG-GPS card operates as a simple generator that increments time using the internal or external time base. Some generator controls available are start and stop, external start via an external pulse and time preset.

GPS SYNC-GEN - In this mode the VME-SG-GPS card will use the GPS Engine to determine time and position. Most generator controls as described above are disabled in the Sync-gen modes.
IRIG B SYNC-GEN - In this mode the VME-SG-GPS card will use an external time code input as a time reference. The input code format is IRIG B (amplitude modulated) or IRIG B (DC shift at RS-422 logic levels). The format is selected using Configuration Register 2, bit 3. When IRIG B at RS-422 levels is used the signal input is terminated with a 120 ohm resister when a jumper is installed on JP1 pins 2 and 3.

b) Generator Start/Stop - The Generator accumulates time when bit 2 is zero. The Generator stops when this bit is a 1.

c) Generator Preset - Bit 3 controls the presetting of the Generator time. When this bit is set the VME-SG-GPS will clear the Generator time counters (unit microseconds through hundreds of microseconds) and transfer the time found in the Time Preset registers (milliseconds through thousands of years). This bit will self clear after the preset has completed.

d) External Start Enable - Bit 4 enables the Generator External Start function. This feature allows the user to synchronize the card in the generator mode to an external reference 1PPS pulse.

After the generator mode is selected, connect the external start 1 PPS at either the External Event BNC on the front panel or on pin C7 of the P2/J2 connector.

First, determine if the rising or falling edge of the reference 1 PPS marks the beginning of the second and select the appropriate edge as described under CONFIGURATION REGISTER 2, External Event Falling Edge Select in this section.

Second, stop the Generator using bit 2 as described above under Generator Start/Stop.

Next, load the start time into the Preset Time Registers as described later in this section.

Finally, set bit 4 of Configuration Register 1. The next 1 PPS edge will Start the generator. Set bit 4 in the second prior to the start time.

e) External Oscillator Select - Set bit 5 to select the external 10 MHz input as the Generator time base. Clear bit 5 to select the internal time base. The external oscillator input is on pin C8 of the P2/J2 connector. An external oscillator should only be selected in the generator mode. The 10 MHz input must be at TTL logic levels. The signal duty cycle should be greater than 10%.

f) Interrupt Enable - Each interrupt has an associated latch that is set when its interrupt source occurs but only if the Interrupt Enable (bit 7) is set. Since spurious interrupt sources could occur during initialization and setup this bit initializes in the cleared (disabled) state. This will guarantee that only interrupts sources that occur after the bit has been set will drive the VME interrupt logic. The BIM chip must still be programmed to enabled each interrupt and set priority levels. For details see VME Interrupt Control in section 2.4.10.

CONFIGURATION REGISTER2 (base address + hex 00A2)

This register controls the External Event active edge selection, Sync-Gen reference code format and synchronization and the Interval output negation.

bits:	0	-	Not Used (NU)
	1	-	NU
	2	-	Ext Event Active Edge Select
	3	-	IRIG B Format (AM or DC)
	4	-	Position Update Inhibit
	5	-	Position Load Request
	6	-	Negate Interval
	7	-	GPS Time Output
	8	-	NU
	9	-	NU
	10	-	NU
	11	-	NU
	12	-	NU
	13	-	NU
	14	-	NU
	15	-	NU

a) External Event Active Edge Select - Bit 2 selects the active edge (rising or falling) of the signal that drives the External Event input. When this bit is a zero the rising edge is active. A one selects the falling edge.

b) IRIG B Format Select - Bit 3 is used when in the Code Sync-Generator mode. The VME-SG-GPS card is capable of using either IRIG B amplitude modulated code or IRIG B DC shift at RS-422 logic levels. When bit 3 is zero the amplitude modulated format is used and when set DC shift is used. IRIG B amplitude modulated is input to the VME-SG-GPS card at the front panel Code Input BNC or at P2/J2 pin C3. The DC format is input P2/J2 pins C9 (+) and A9 (-). See section one for the P2/J2 pin description.

c) Position Update Inhibit - Normally bit 4 is not set and position information (latitude, longitude and elevation) are available from the GPS Engine. Position information is read from the position registers at offset hex 90 - 9E. It may be necessary to enter the position when multiple satellite visibility is limited due to physical obstructions such as buildings. The card must first be placed in the "Known" Position Mode. The updating of the position registers is inhibited by setting bit 4. After the known position has been entered, bit 5, the Position Load bit (described below) is set. This will enable the VME-SG-GPS card to transfer the new position to the GPS Engine. The Position Output Disable bit and the Position Load bit will both be cleared when the load operation has completed. See the Loading Position description in this section 2.4.8.

d) Position Load - this bit (5) is used in conjunction with the Position Output Disable bit described above. It generates a request to the VME-SG-GPS to transfer the position information loaded by the user into the GPS Engine.

e) Negate Interval - Set bit 6 to clear the Interval output signal. This bit may be set at any time the user wishes to guarantee that the Interval output is negated or to abort a time coincidence operation when already in the interval period. Bit 6 is automatically cleared when the Interval is cleared. This process will generate a Stop pulse.

f) GPS Time Output Flag When the VME-SG-GPS card is in the GPS Sync-gen mode, setting bit 7 will cause time outputs to reflect GPS time. When bit 7 is a zero the card outputs UTC time. UTC time is affected by leap seconds. GPS time will normally be several seconds ahead of UTC time and is not affected by leap seconds.

POSITION MODE (base address + hex 00A4)

This register is used to select the GPS Position Mode. The GPS Receiver will compute position information if 4 or more satellites are available with a Vertical and Horizontal Dilution of Precision (VDOP and HDOP) of 6 or less. If the position is known, time may be determined with only one satellite. The Position Mode allows the user to determine the manner in which the position of the antenna (latitude, longitude and elevation) is determined. There are 4 modes available. Each mode with the value representing it in the Position Mode registers is shown below:

Character		MODE
0	-	Known
1	-	Survey
2	-	Automatic
3	-	Dynamic

a. KNOWN - In the Known mode the current position will be held fixed. If the user knows the position of the antenna it is entered via the Position registers when in this Position Mode. Position data can be entered only while the Position Mode is in the Known mode. If the unit is stationary this mode will provide the best timing accuracy assuming the position is correct. When the position is known only one satellite is necessary to determine accurate time.

b. SURVEY - In the Survey mode the GPS Receiver is directed to compute position. There must be 4 satellites in view to calculate Latitude, Longitude and Elevation. When only 3 satellites are available the Elevation will be held fixed at the last computed value. The GPS Engine will compute position only when HDOP and VDOP values are less than 6.

c. AUTO - The Automatic mode is a combination of the Survey and Known Position modes. When the Auto Position mode is asserted the GPS Receiver is placed in the Survey mode until accurate position with DOPs of 6 or less has been computed. At that time the unit will automatically switch to the Known mode, holding the current accurate position fixed. This mode makes it unnecessary for the user to watch the unit to determine when good position has been computed and then place the unit in the Known mode.

d. DYNAMIC - The Dynamic mode is used when the unit is moving at velocities up to 1000 knots. The GPS Receiver can determine 3 dimensional position (Latitude, Longitude and Elevation) when 4 or more satellites are in view. When only 3 satellites are available the last elevation value computed will be held fixed and the unit will compute 2 dimensional position. Time lock is not possible if less than 3 satellites are available.

LOCAL OFFSET (base address + hex 00A6)
This register allows for the output of local time from the VME-SG-GPS. This parameter is used in the GPS synchronized generator mode only to convert the time received from the GPS Engine time reference to local time. The Local Offset is any value between + 12 and - 12 hours. The following describes the Local Offset word:

Data Bits		
15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
+/- Sign (ASCII)	Tens Hours	Unit Hours

RATE OUTPUT SELECTION (hex 00A8)
This parameter controls the Pulse Rate generation logic. The Pulse Rate output is available at the P2/J2 connector pin C2. Five different Pulse Rates are available as described in the table below. The rising edge of the pulse rate output is active and "on time". The duty cycles for the different rate outputs are specified in section one.

The Pulse Rate output can also generate VME interrupts. For more information about the Rate Generation INT1 interrupt see section 2.4.10.

Character		RATE
0	-	Pulse Rate Disabled
1	-	10,000 Pulses Per Second (PPS)
2	-	1000 PPS
3	-	100 PPS
4	-	10 PPS
5	-	1 PPS

OSCILLATOR CONTROL VOLTAGE SETTING (hex 00AA)
The Oscillator Control Voltage Setting is a 16 bit hexadecimal value that indicates the current output from the frequency control digital to analog (DAC) converter. The DAC output controls the frequency of the crystal oscillator that is the time base for all generator/sync-generator operations. This output will range between 0 and hex FFFF. In the GPS sync-gen mode after the card has attained phase lock, a midrange DAC value of about hex 7FFF $\pm$ 1000 is normal. With aging the oscillator DAC setting will change to maintain good oscillator discipline. If DAC settings near 0 or hex FFFF are observed this indicates that either a failure has occurred or the oscillator needs to be recalibrated.

In the Code Sync-gen modes this value may vary from its midrange value significantly depending on the frequency accuracy and stability of the generator that is providing the IRIG B reference code.

GENERATOR PRESET TIME REGISTERS (hex 00AC - 00B8)
The 9 byte locations shown in the table below are used to preset the Generator. Only the least significant byte in each word location is used. The preset registers contain milliseconds through thousands of years. The registers are shown with their base address offset.

Label	Description	Hex Address Offset
PUMS	Unit Milliseconds	00AC
PMS	Hundreds & Tens Msec	00AE
PSEC	Tens & Unit Seconds	00B0
PMIN	Tens & Unit Minutes	00B2
PHRS	Tens & Unit Hours	00B4
PDYS1	Tens & Unit Days	00B6
PDYS2	Hundreds Days	00B8
PYRS1	Tens & Units Years	00BA
PYRS2	Thous & Hund Years	00BC

Once loaded the contents of the preset registers are transferred to the Generator time registers when the Generator Preset Enable flag (Configuration Word 1, bit 3) is set. This bit is automatically cleared after the load takes place. The data as shown in the table above is formatted in packed BCD. The least significant digit is in the lower 4 bits of the byte.

POSITION UPDATE FLAG (hex 00BE)
The position information (latitude, longitude and elevation) is updated once per second. The data is written during the 998 millisecond of the second. Prior to the update at approximately 995 milliseconds the Position Update flag is set. The flag will clear at zero milliseconds. The user should not read the position information while the Position Update flag is set. Since the flag will go high before the data is written the user may read the position data any time the flag is not set and know that there are at least 3 milliseconds before the data will possibly change.

CODE SYNC-GEN PHASE COMPENSATION (hex 00D0)
When the VME-SG-GPS card is using IRIG B AM code as the time reference there are inherent propagation delays present. The delays are normally due to signal distribution amplifiers, or other transmission media that is present. In addition input code is input to the cards Automatic Gain Control (AGC) circuit and then a Zero Crossing detector. Both of these circuits can contribute small delays. The Code Sync-gen Phase Compensation word is used to correct any fixed phase errors either positive or negative. The word written to hex offset D0 must be a 16 bit signed binary number representing microseconds of compensation. The range of compensation is between - 1000 and + 1000 microseconds. A magnitude of 1000 microseconds is all that will result even if larger values are entered.

GPS USER TIME BIAS (hex 00D2 - 00D4)
The GPS User Time Bias is only used in the GPS Sync-gen mode to compensate for cable or preamplifier time delays. The available values range from -99999 to +99999 ns. There are two 16 bit words allocated for this parameter. The table below shows how the data is organized. The first word containing sign and ten thousands of nanoseconds is at offset hex D2. Thousands through units nanoseconds are packed in the word at offset hex D4.

Data Bits			
15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
+/- Sign (ASCII)		0	10,000 nsec
Thous nsec	Hund nsec	Tens nsec	Unit nsec

NUMBER OF SATELLITES TRACKED (hex 00D6)
This word provides the number of satellites that the GPS Engine is currently tracking.

SELF TEST (hex 00DE)
The Self Test word indicates the results of diagnostic testing that is done at power up and during normal operation. The Self Test results are found in the least significant byte at offset hex DE. The byte will contain a BCD number value representing any operational errors that may have occurred. The table below describes all the possible error conditions and their number representation.

Code		Error Condition
0	-	No errors detected
1	-	RAM memory failure
2	-	Processor clock failure
3	-	GPS engine communication failure
4	-	GPS engine operational failure
5	-	DAC setting near maximum or minimum

COINCIDENCE TIME COMPARE REGISTERS (hex 00E0 - 00FE)
The VME-SG-GPS has two sets of coincidence time compare registers identified as #1 and #2. When the generator time is equal to the values in either compare registers a pulse output will be asserted on the P2/J2 connector. The Interval level output sets at the occurrence of coincidence compare time #1 and resets at the occurrence of coincidence compare time #2. The compare pulses are 2 milliseconds wide.

Each Coincidence Compare register set is made up of eight locations one byte wide. The compare values entered are from microseconds through hundreds of days. The registers are shown in the table below with their contents and base address offsets. Each Coincidence Compare register set also has a MASK value. The MASK value is a hexadecimal (4 bit) number between 0 - hex A. The MASK limits the range of time that will be used in the compare operation. For example if the MASK value is zero, all compare time values (hundreds days - microseconds) are used. If the MASK value is a 1, then the hundreds of days value is ignored. The table below indicates the time values that are used with each associated MASK value. Using a MASK value allows compare pulses to occur at regular time intervals. For example a MASK value of hex B would only allow compares from microseconds through milliseconds to occur. This would cause a pulse to occur every ten milliseconds at the precise microsecond programmed.

Label	Description	Hex Address Offset
COMP1-1	Tens & Units Microseconds	00E0
COMP1-2	Unit Msec & Hundreds Microsec	00E2
COMP1-3	Hundreds & Tens Milliseconds	00E4
COMP1-4	Tens & Unit Seconds	00E6
COMP1-5	Tens & Unit Minutes	00E8
COMP1-6	Tens & Unit Hours	00EA
COMP1-7	Tens & Unit Days	00EC
COMP1-8	MASK1, Hundreds Days	00EE
COMP2-1	Tens & Units Microseconds	00F0
COMP2-2	Unit Msec & Hundreds Microsec	00F2
COMP2-3	Hundreds & Tens Milliseconds	00F4
COMP2-4	Tens & Unit Seconds	00F6
COMP2-5	Tens & Unit Minutes	00F8
COMP2-6	Tens & Unit Hours	00FA
COMP2-7	Tens & Unit Days	00FC
COMP2-8	MASK2, Hundreds Days	00FE

MASK		TIME COMAPE		
hex	0	Hundreds Days	-	Microseconds
	1	Tens Days	-	Microseconds
	2	Unit Days	-	Microseconds
	3	Tens Hours	-	Microseconds
	4	Unit Hours	-	Microseconds
	5	Tens Minutes	-	Microseconds
	6	Unit Minutes	-	Microseconds
	7	Tens Seconds	-	Microseconds
	8	Unit Seconds -	Microseconds	
	9	Hund Millisec	-	Microseconds
	A	Tens Millisec	-	Microseconds
	B	Unit Millisec	-	Microseconds

Each Coincidence Compare output is designed to generate its own independent interrupt. The Coincidence Compare #1 output pulse will generate the INT2 interrupt. The Coincidence Compare #2 pulse will generate the INT3 interrupt. For more information see section 2.4.10.

2.4.10 VME INTERRUPT CONTROL

The heart of the Interrupt Control logic is the Bus Interrupter Module (BIM). It handles up to 4 independent sources of interrupt requests and is fully programmable directly over the VME bus. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the BIM chip can respond supplying an interrupt vector. Control and setup is facilitated by a separate control register for each interrupt source. This manual includes programming examples in section 2.5 that show how to setup the BIM for various interrupting sources with priority and vector setup.

The following table lists the offset from the VME-SG-GPS base address where the Control and Vector registers for each interrupt source is located.

Register	Source	Offset
INT0	Control External Event	0000
INT1	Control Rate Generator	0002
INT2	Control Coincidence Compare #1 Pulse	0004
INT3	Control Coincidence Compare #2 Pulse	0006
INT0	Vector External Event	0008
INT1	Vector Rate Generator	000A
INT2	Vector Coincidence Compare #1 Pulse	000C
INT3	Vector Coincidence Compare #2 Pulse	000E

BIM CONTROL REGISTERS

There is one control register for each interrupt source. Each 8-bit control registers is divided into several fields. The following is a description of each bits functions:

bits: 0 - L0 (IRQ Interrupt Level bit 0)
1 - L1 (" " " bit 1)
2 - L2 (" " " bit 2)
3 - IRAC (Interrupt Auto Clear)
4 - IRE (Interrupt Enable)
5 - X/IN (External/Internal)
6 - FAC (Flag Auto Clear)
7 - Flag

L0, L1, L2 - Bits 0, 1 and 2 determine the interrupt response level. The following table illustrates the possible settings:

L2	L1	L0	IRQ LEVEL
0	0	0	Disabled
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

IRAC (Interrupt Auto-Clear) - Set bit 3 to clear the Interrupt Enable bit (below) during an interrupt acknowledge cycle responding to this request. To enable the interrupt for further interrupts the IRE bit must be set again by writing to the control register.

IRE (Interrupt Enable) - Set bit 4 to enable the interrupt associated with the control register.

X/IN (External/Internal) - Bit 5 determines the response of the BIM during an interrupt acknowledge cycle. If the X/IN bit is clear the BIM will respond with vector data and a /DTACK signal. When set, no vector is supplied and no /DTACK is given. The VME-SG-GPS should always be configured with this bit cleared as no other device will supply the necessary interrupt vector.

FAC (Flag Auto-Clear) - Set bit 6 to cause the FLAG bit (below) to automatically clear during an interrupt acknowledge cycle.

FLAG - Bit 7 is a flag bit that is provided for the user if desired. It has no effect on the operation of the BIM chip.

BIM VECTOR REGISTERS

There is one vector register for each interrupt source. Each vector register may be programmed to supply a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/IN) control register bit is clear. The byte is used to compute the location in the vector table where the address of the interrupt service routine is located. The location in the vector table is computed by multiplying the vector byte by 4 since each vector table jump address occupies 4 bytes.

2.4.11 VME-SG-GPS MEMORY MAP

The following table describes the VME-SG-GPS memory map. Each locations address is computed by adding the offset to the data or register of interest to the cards base address. As described in section 2.2 part A the base address is defined by the 8 section dip switch located on the board.

Base Address Offset (hex)	Location Description
0000	BIM Control Register INT0
0002	BIM Control Register INT1
0004	BIM Control Register INT2
0006	BIM Control Register INT3
0008	BIM Vector Register INT0
000A	BIM Vector Register INT1
000C	BIM Vector Register INT2
000E	BIM Vector Register INT3
0040	Generator Time Request
0042	Gen Freeze Reg 1, Word 1, (Umsec, Husec, Tusec, Uusec)
0044	Gen Freeze Reg 1 Release
0046	Gen Freeze Reg 2, Word 1, (Umsec, Husec, Tusec, Uusec)
0048	Gen Freeze Reg 2 Release
0080	Gen Freeze Reg 1, Word 2 (Tsec, Usec, Hmsec, Tmsec)
0082	Gen Freeze Reg 1, Word 3 (Thours, Uhours, Tmin, Umin)
0084	Gen Freeze Reg 1, Word 4 (Status*, Hdays, Tdays, Umin) Status Bits: 1 - Reference Error 2 - SyncGen Phase Locked 3 - Reserved 4 - Reserved
0086	Gen Freeze Reg 1, Word 5 (Thyears, Hyears, Tyears, Uyears)

Base Address Offset (hex)	Location Description
0088	Gen Freeze Reg 2, Word 2 (Tsec, Usec, Hmsec, Tmsec)
008A	Gen Freeze Reg 2, Word 3 (Thours, Uhours, Tmin, Umin)
008C	Gen Freeze Reg 2, Word 4 (Status*, Hdays, Tdays, Udays) Status bits: 1 - Reference Error 2 - SyncGen Phase Locked 3 - Reserved 4 - Reserved
008E	Gen Freeze Reg 2, Word 5 (Thyears, Hyears, Tyears, Uyears)
0090	Latitude (0, Hund, Tens, Units degrees)
0092	Latitude (Tmin, Umin, Tsec, Usec)
0094	Latitude (North/South, Tenths seconds)
0096	Longitude (0, Hund, Tens, Units degrees)
0098	Longitude (Tmin, Umin, Tsec, Usec)
009A	Longitude (East/West, Tenths Seconds)
009C	Elevation (Sign, Ten Thous & Thous Meters)
009E	Elevation (hund, Tens, Unit & Tenths Meters)

Base Address Offset (hex)	Location Description
00A0	Configuration Reg 1 bits: 0 - Mode Bit 1 1 - Mode Bit 2 2 - Gen Stop 3 - Gen Preset Enable 4 - External Start Enable 5 - External Osc Select 6 - NU 7 - Interrupt Enable 8 - NU 9 - NU 10 - NU 11 - NU 12 - NU 13 - NU 14 - NU 15 - NU
00A2	Configuration Reg 2 bits: 0 - NU 1 - NU 2 - Ext Event Fall Edge Active 3 - Sync Gen IRIG B (AM or DC) 4 - Position Update Inhibit 5 - Position Load Request 6 - Negate Interval Output 7 - GPS Time Select (optional) 8 - NU 9 - NU 10 - NU 11 - NU 12 - NU 13 - NU 14 - NU 15 - NU
00A4	Position Computation Mode
00A6	Local Time Offset (sign, hours)
00A8	Pulse Rate Output Select
00AA	DAC Setting (hexadecimal)

Base Address Offset (hex)	Location Description	
00AC	Gen Preset	(0, Msec)
00AE	“ “	(Hmsec, Tmsec)
00B0	“ “	(Tsec, Usec)
00B2	“ “	(Tmin, Umin)
00B4	“ “	(Thours, Uhours)
00B6	“ “	(Tdays, Udays)
00B8	“ “	(0, Hdays)
00BA	“ “	(Tyears, Uyears)
00BC	“ “	(Thyears, Hyears)
00BE		Position Update Flag
00D0		Code Sync-gen Phase Compensation
00D2		GPS User Time Bias (word1)
00D4		GPS User Time Bias (word2)
00D6		Number Satellites Tracked
00D8		Reserved Registers
00DA		“ “
00DC		“ “
00DE		Self Test
00E0		Coin Compare #1 (Tusec, Uusec)
00E2		“ “ “ (Umsec, Husec)
00E4		“ “ “ (Hmsec, Tmsec)
00E6		“ “ “ (Tsec, Usec)
00E8		“ “ “ (Tmin, Umin)
00EA		“ “ “ (Thours, Uhours)
00EC		“ “ “ (Tdays, Udays)
00EE		“ “ “ (Mask, Hdays)
00F0		Coin Compare #2 (Tusec, Uusec)
00F2		“ “ “ (Umsec, Husec)
00F4		“ “ “ (Hmsec, Tmsec)
00F6		“ “ “ (Tsec, Usec)
00F8		“ “ “ (Tmin, Umin)
00FA		“ “ “ (Thours, Uhours)
00FC		“ “ “ (Tdays, Udays)
00FE		“ “ “ (Mask, Hdays)

```
 0000                    CPU     "68000.TBL"     ; CPU TABLE
   000000                HOF     "MOT16"         ; HEX OUTPUT FO
RMAT

 0000000D      =         CR:     EQU     0DH
 0000000A      =         LF:     EQU     0AH
 000C0082      =         UARTD:  EQU     0C0082H         ;UART DATA ADDR
ESS
 000C0080      =         UARTS:  EQU     0C0080H         ;UART STATUS AD
DRESS
 00008000      =         PFLAG:  EQU     008000H         ;PROMPT FLAG RE
GISTER
 00008002      =         IOFLAG: EQU     008002H         ;INTERVAL OVER
FLAG REGISTER

 00FF0040      =         FRZ1:   EQU     0FF0040H        ;FREEZE CMD ADD
RESS GEN REG 1
 00FF0042      =         GREG1A: EQU     0FF0042H        ;GEN REG 1, WOR
D A (UNIT MICROSEC - .001 SEC)
 00FF0044      =         FRZ1_:  EQU     0FF0044H        ;UNFREEZE CMD A
DDRESS GEN REG 1
 00FF0080      =         GREG1B: EQU     0FF0080H        ;GEN REG 1, WOR
D B (.01 SEC - TENS SEC)
 00FF0082      =         GREG1C: EQU     0FF0082H        ;GEN REG 1, WOR
D C (MINS & HOURS)
 00FF0084      =         GREG1D: EQU     0FF0084H        ;GEN REG 1, WOR
D D (DAYS & STATUS)
 00FF0086      =         GREG1E: EQU     0FF0086H        ;GEN REG 1, WOR
D E (CONTROL FUNCTIONS OR YEARS)

 00FF0046      =         GREG2A: EQU     0FF0046H        ;GEN REG 2, WOR
D A (UNIT MICROSEC - .001 SEC)
 00FF0048      =         FRZ2_:  EQU     0FF0048H        ;UNFREEZE CMD A
DDRESS GEN REG 2
 00FF0088      =         GREG2B: EQU     0FF0088H        ;GEN REG 2, WOR
D B (.01 SEC - TENS SEC)
 00FF008A      =         GREG2C: EQU     0FF008AH        ;GEN REG 2, WOR
D C (MINS & HOURS)
 00FF008C      =         GREG2D: EQU     0FF008CH        ;GEN REG 2, WOR
D D (DAYS & STATUS)
 00FF008E      =         GREG2E: EQU     0FF008EH        ;GEN REG 2, WOR
D E (CONTROL FUNCTIONS OR YEARS)

 00FF0000      =         BIMC1:  EQU     0FF0000H        ;BIM CONTROL RE
G 1
 00FF0002      =         BIMC2:  EQU     0FF0002H        ;BIM CONTROL RE
G 2
 00FF0004      =         BIMC3:  EQU     0FF0004H        ;BIM CONTROL RE
G 3
 00FF0006      =         BIMC4:  EQU     0FF0006H        ;BIM CONTROL RE
```

```
G 4
 00FF0008      =          BIMV1:  EQU     0FF0008H        ;BIM VECTOR REG
 1
 00FF000A      =          BIMV2:  EQU     0FF000AH        ;BIM VECTOR REG
 2
 00FF000C      =          BIMV3:  EQU     0FF000CH        ;BIM VECTOR REG
 3
 00FF000E      =          BIMV4:  EQU     0FF000EH        ;BIM VECTOR REG
 4

 00FF00A0      =          CFREG1: EQU     0FF00A0H        ;CONFIG/CONTROL
 REG 1
 00FF00A2      =          CFREG2: EQU     0FF00A2H        ;   "       "
  "  2
 00FF00A6      =          LOCAL:  EQU     0FF00A6H        ;LOCAL OFFSET
 00FF00A8      =          RATE:   EQU     0FF00A8H        ;VME RATE
 00FF00AA      =          DAC:    EQU     0FF00AAH        ;VME DAC OUTPUT
 00FF00AC      =          GPRST1: EQU     0FF00ACH        ;GENERATOR PRES
ET REGISTER (  0 , Umsec)
 00FF00AE      =          GPRST2: EQU     0FF00AEH        ;      "        "
       "    (Hmsec, Tmsec)
 00FF00B0      =          GPRST3: EQU     0FF00B0H        ;      "        "
       "    (Tsec, Usec)
 00FF00B2      =          GPRST4: EQU     0FF00B2H        ;      "        "
       "    (Tmin, Umin)
 00FF00B4      =          GPRST5: EQU     0FF00B4H        ;      "        "
       "    (Thrs, Uhrs)
 00FF00B6      =          GPRST6: EQU     0FF00B6H        ;      "        "
       "    (Tday, Uday)
 00FF00B8      =          GPRST7: EQU     0FF00B8H        ;      "        "
       "    (  0 , Hday)
 00FF00BA      =          GPRST8: EQU     0FF00BAH        ;      "        "
       "    (Tyrs, Uyrs)
 00FF00BC      =          GPRST9: EQU     0FF00BCH        ;      "        "
       "    (THyrs, Hyrs)
 00FF00BE      =          WARN:   EQU     0FF00BEH        ;POSITION UPDAT
E WARNING FLAG
 00FF00D0      =          SGCOMP: EQU     0FF00D0H        ;CODE SYNC-GEN
COMPENSATION
 00FF00D8      =          SPARE1: EQU     0FF00D8H        ;SPARE LOCATION
S
 00FF00DA      =          SPARE2: EQU     0FF00DAH        ;   "       "

 00FF00DC      =          SPARE3: EQU     0FF00DCH        ;   "       "

 00FF00DE      =          STEST:  EQU     0FF00DEH        ;SELF TEST

                          ;       COMPARE TIME #1

 00FF00E0      =          CMP1_1: EQU     0FF00E0H        ;COMP TIME (Tus
ec, Uusec)
 00FF00E2      =          CMP1_2: EQU     0FF00E2H        ;   "      "  (Um
```

```
sec, Husec)
 00FF00E4      =          CMP1_3: EQU      0FF00E4H          ;  "      "  (Hm
sec, Tmsec)
 00FF00E6      =          CMP1_4: EQU      0FF00E6H          ;  "      "  (Ts
ec, Usec)
 00FF00E8      =          CMP1_5: EQU      0FF00E8H          ;  "      "  (Tm
in, Umin)
 00FF00EA      =          CMP1_6: EQU      0FF00EAH          ;  "      "  (Th
rs, Uhrs)
 00FF00EC      =          CMP1_7: EQU      0FF00ECH          ;  "      "  (Td
ay, Uday)
 00FF00EE      =          CMP1_8: EQU      0FF00EEH          ;  "      "  (
0 , Hday).

                         ;        COMPARE TIME #2

 00FF00F0      =          CMP2_1: EQU      0FF00F0H          ;COMP TIME (Tus
ec, Uusec)
 00FF00F2      =          CMP2_2: EQU      0FF00F2H          ;  "      "  (Ums
ec, Husec)
 00FF00F4      =          CMP2_3: EQU      0FF00F4H          ;  "      "  (Hms
ec, Tmsec)
 00FF00F6      =          CMP2_4: EQU      0FF00F6H          ;  "      "  (Tse
c, Usec)
 00FF00F8      =          CMP2_5: EQU      0FF00F8H          ;  "      "  (Tmi
n, Umin)
 00FF00FA      =          CMP2_6: EQU      0FF00FAH          ;  "      "  (Thr
s, Uhrs)
 00FF00FC      =          CMP2_7: EQU      0FF00FCH          ;  "      "  (Tda
y, Uday)
 00FF00FE      =          CMP2_8: EQU      0FF00FEH          ;  "      "  (  0
 , Hday)

 0000                     HOF      "MOT8"             ; HEX OUTPUT FORMAT


 0000                     ORG      0000H              ;LOAD IN USER DRAM AREA
                        ;*****************************************************
**********
                         ;        THIS ROUTINE WILL DISPLAY ALL OPERATIONAL PARAM
ETERS    *
                         ;        TIME, OPERATIONAL MODE AND STATUS
         *
                        ;*****************************************************
**********
 0000 207C00FF00BAMALL: MOVEA.L #CFREG1,A0         ;LOAD CONFIG 1 ADDRESS
 0006 30FC0002          MOVE.W  #02H,(A0)+         ;SET TO CODE SYNC-GENER
ATOR
 000A 30BC0000          MOVE.W  #00H,(A0)          ;SET FOR AM CODE REFERE
NCE
 000E 60000010          BRA     DALL
```

```
 0012 207C00FF00BDCALL: MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 0018 30FC0002          MOVE.W  #02H,(A0)+       ;SET TO CODE SYNC-GENER
ATOR
 001C 30BC0008          MOVE.W  #08H,(A0)        ;SET FOR DC CODE REFERE
NCE

 0020 61000858  DALL:   BSR     HOME             ;HOME DISPLAY
 0024 610007AE  DALL1:  BSR     READY
 0028 207C000C00        MOVEA.L #UARTD,A0        ;LOAD UART DATA ADDRESS
 002E 10BC0017          MOVE.B  #17H,(A0)        ;CURSOR OFF

 0032 303900FF00TMCHK1: MOVE.W  WARN.L,D0        ;LOAD POSITION UPDATE F
LAG
 0038 6700FFF8          BEQ     TMCHK1           ;IF ZERO BRANCH
 003C 303900FF00TMCHK2: MOVE.W  WARN.L,D0        ;LOAD POSITION UPDATE F
LAG
 0042 6600FFF8          BNE     TMCHK2           ;IF SET BRANCH

 0046 303900FF00        MOVE.W  FRZ1.L,D0        ;FREEZE TIME
 004C 4E71              NOP
 004E 4E71              NOP
 0050 303900FF00        MOVE.W  GREG1A.L,D0      ;LOAD WORD 1
 0056 323900FF00        MOVE.W  GREG1B.L,D1      ;LOAD WORD 2
 005C 343900FF00        MOVE.W  GREG1C.L,D2      ;LOAD WORD 3
 0062 363900FF00        MOVE.W  GREG1D.L,D3      ;LOAD WORD 4
 0068 383900FF00        MOVE.W  GREG1E.L,D4      ;LOAD WORD 5
 006E 3A3900FF00        MOVE.W  FRZ1_.L,D5       ;RELEASE FREEZE REG

 0074 6100058E          BSR     OTIME            ;CALL TIME OUTPUT SUBRO
UTINE
 0078 6100063E          BSR     OSTAT            ;CALL STATUS OUTPUT
 007C 61000686          BSR     OMODE            ;OUTPUT OPERATIONAL MOD
E
 0080 610006B2          BSR     DACOUT           ;CALL DAC READING
 0084 610006E0          BSR     SELTST           ;OUTPUT SELF TEST
 0088 1C3C0009          MOVE.B  #09,D6           ;MOVE CURSOR UP 9 LINES
 008C 610007C8          BSR     CUP              ;CURSOR UP
 0090 6000FFA0          BRA     TMCHK1

                ;*****************************************************
**********
                ;       THIS ROUTINE WILL SETUP INTERRUPT #1 (EXT EVENT
) TO USE *
                ;       USE INTERRUPT SERVICE ROUTINE 1 (IRSRV1).
        *
                ;*****************************************************
**********
 0094 207C00FF00RTN2:   MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 009A 30BC0002          MOVE.W  #02H,(A0)        ;START SYNC-GENERATOR
 009E 207C00FF00        MOVEA.L #BIMC1,A0        ;LOAD BIM CONTROL REG1
ADDRESS
 00A4 30BC0011          MOVE.W  #11H,(A0)        ;SET INTERRUPT PRIORITY
```

```
 ETC
 00A8 207C00FF00          MOVEA.L #BIMV1,A0        ;LOAD BIM VECTOR REG1 A
DDRESS
 00AE 30BC0040            MOVE.W  #40H,(A0)        ;WRITE VECTOR NUMBER
 00B2 41FA03B6            LEA.L   ISRV1(PC),A0     ;LOAD ADDRESS OF INTERR
UPT SERVICE ROUTINE
 00B6 227C000001          MOVEA.L #0100H,A1        ;LOAD VECTOR ADDRESS
 00BC 2288                MOVE.L  A0,(A1)          ;WRITE VECTOR
 00BE 43FA0836            LEA.L   MSG3(PC),A1
 00C2 610007CA            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE
 00C6 43FA07D2            LEA.L   MSG1(PC),A1
 00CA 610007C2            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE
 00CE 207C00FF00          MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 00D4 30BC0082            MOVE.W  #82H,(A0)        ;START SYNC-GENERATOR &
 ENABLE INTERRUPTS
 00D8 6000FFFE  WAIT2:    BRA     WAIT2            ;WAIT


                ;*****************************************************
**********
                ;       THIS TEST WILL SETUP INTERRUPT #1 (EXT EVENT) T
O USE   *
                ;       USE INTERRUPT SERVICE ROUTINE 2 (IRSRV2).
        *
                ;*****************************************************
**********
 00DC 207C00FF00TEST1:    MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 00E2 30BC0002            MOVE.W  #02H,(A0)        ;START SYNC-GENERATOR
 00E6 207C00FF00          MOVEA.L #BIMC1,A0        ;LOAD BIM CONTROL REG1
ADDRESS
 00EC 30BC0011            MOVE.W  #11H,(A0)        ;SET INTERRUPT PRIORITY
 ETC
 00F0 207C00FF00          MOVEA.L #BIMV1,A0        ;LOAD BIM VECTOR REG1 A
DDRESS
 00F6 30BC0040            MOVE.W  #40H,(A0)        ;WRITE VECTOR NUMBER
 00FA 41FA03CE            LEA.L   ISRV2(PC),A0     ;LOAD ADDRESS OF INTERR
UPT SERVICE ROUTINE
 00FE 227C000001          MOVEA.L #0100H,A1        ;LOAD VECTOR ADDRESS
 0104 2288                MOVE.L  A0,(A1)          ;WRITE VECTOR
 0106 43FA07EE            LEA.L   MSG3(PC),A1
 010A 61000782            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE
 010E 43FA07B8            LEA.L   MSG2(PC),A1
 0112 6100077A            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE
 0116 207C00FF00          MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 011C 30BC0082            MOVE.W  #82H,(A0)        ;START SYNC-GENERATOR &
 ENABLE INTERRUPTS
 0120 6000FFFE  WAIT3:    BRA     WAIT3            ;WAIT
```

```
                    ;*******************************************************
**********
                    ;       THIS TEST WILL SETUP COMPARE TIME REGISTERS AND
 THE     *
                    ;       GENERATOR PRESET REGISTERS.
          *
                    ;       THIS ROUTINE WILL SETUP UNIT FOR A .1 MSEC INTE
RVAL AT *
                    ;       10 SECONDS.
          *
                    ;*******************************************************
**********
 0124 207C000080TEST2:  MOVEA.L #PFLAG,A0        ;LOAD PROMPT FLAG ADDRE
SS
 012A 30BC00FF          MOVE.W  #0FFH,(A0)       ;SET FLAG
 012E 207C000080TST2:   MOVEA.L #IOFLAG,A0       ;LOAD INT OVER FLAG ADD
RESS
 0134 30BC0000          MOVE.W  #00,(A0)         ;CLEAR FLAG
 0138 207C00FF00        MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 013E 30BC0004          MOVE.W  #04H,(A0)        ;DISABLE INTERRUPTS
 0142 207C00FF00        MOVEA.L #BIMC3,A0        ;LOAD BIM CONTROL REG3
ADDRESS
 0148 30BC0000          MOVE.W  #00H,(A0)        ;SET INTERRUPT PRIORITY
 ETC (DISABLE INT3)
 014C 207C00FF00        MOVEA.L #BIMC4,A0        ;LOAD BIM CONTROL REG4
ADDRESS
 0152 30BC0011          MOVE.W  #11H,(A0)        ;SET INTERRUPT PRIORITY
 ETC
 0156 207C00FF00        MOVEA.L #BIMV4,A0        ;LOAD BIM VECTOR REG4 A
DDRESS
 015C 30BC0041          MOVE.W  #41H,(A0)        ;WRITE VECTOR NUMBER
 0160 41FA041C          LEA.L   COMP2(PC),A0     ;LOAD ADDRESS OF INTERR
UPT SERVICE ROUTINE
 0164 227C000001        MOVEA.L #0104H,A1        ;LOAD VECTOR ADDRESS
 016A 2288              MOVE.L  A0,(A1)          ;WRITE VECTOR

                    ;       PRESET GENERATOR
 016C 207C00FF00        MOVEA.L #GPRST1,A0       ;LOAD ADDRESS OF GEN PR
ESET REG #1
 0172 30FC0000          MOVE.W  #00H,(A0)+       ;WRITE TO PRESET REGIST
ER 1
 0176 30FC0000          MOVE.W  #00H,(A0)+       ;REGISTER 2
 017A 30FC0000          MOVE.W  #00H,(A0)+       ;REGISTER 3
 017E 30FC0045          MOVE.W  #45H,(A0)+       ;REGISTER 4
 0182 30FC0017          MOVE.W  #17H,(A0)+       ;REGISTER 5
 0186 30FC0029          MOVE.W  #29H,(A0)+       ;REGISTER 6
 018A 30FC0003          MOVE.W  #03H,(A0)+       ;REGISTER 7
 018E 30FC0092          MOVE.W  #92H,(A0)+       ;REGISTER 8
 0192 30FC0019          MOVE.W  #19H,(A0)+       ;REGISTER 9
```

```
                        ;       PRESET COMP1 TIME

 0196 207C00FF00                MOVEA.L #CMP1_1,A0      ;LOAD ADDRESS OF COMP T
IME REG #1
 019C 30FC0000                  MOVE.W  #00H,(A0)+      ;WRITE TO COMPARE REG 1
 01A0 30FC0000                  MOVE.W  #00H,(A0)+      ;REGISTER 2
 01A4 30FC0000                  MOVE.W  #00H,(A0)+      ;REGISTER 3
 01A8 30FC0010                  MOVE.W  #10H,(A0)+      ;REGISTER 4 (SEC)
 01AC 30FC0045                  MOVE.W  #45H,(A0)+      ;REGISTER 5
 01B0 30FC0017                  MOVE.W  #17H,(A0)+      ;REGISTER 6
 01B4 30FC0029                  MOVE.W  #29H,(A0)+      ;REGISTER 7
 01B8 30FC0003                  MOVE.W  #03H,(A0)+      ;REGISTER 8

                        ;       PRESET COMP2 TIME

 01BC 30FC0000                  MOVE.W  #00H,(A0)+      ;WRITE TO COMP2
 01C0 30FC0001                  MOVE.W  #01H,(A0)+      ;REGISTER 2 (.1 MSEC)
 01C4 30FC0000                  MOVE.W  #00H,(A0)+      ;REGISTER 3
 01C8 30FC0010                  MOVE.W  #10H,(A0)+      ;REGISTER 4 (SEC)
 01CC 30FC0045                  MOVE.W  #45H,(A0)+      ;REGISTER 5
 01D0 30FC0017                  MOVE.W  #17H,(A0)+      ;REGISTER 6
 01D4 30FC0029                  MOVE.W  #29H,(A0)+      ;REGISTER 7
 01D8 30FC0003                  MOVE.W  #03H,(A0)+      ;REGISTER 8

 01DC 207C00FF00                MOVEA.L #CFREG1,A0      ;LOAD CONFIG 1 ADDRESS
 01E2 30BC0088                  MOVE.W  #88H,(A0)       ;START/PRESET GEN AND E
NABLE INTERRUPTS
 01E6 207C000080                MOVEA.L #PFLAG,A0       ;LOAD PROMPT FLAG
 01EC 3010                      MOVE.W  (A0),D0
 01EE 6700000E                  BEQ     CTCK1           ;IF NOT SET BRANCH
 01F2 30BC0000                  MOVE.W  #00H,(A0)       ;CLEAR PROMPT FLAG
 01F6 43FA072A                  LEA.L   MSG4(PC),A1
 01FA 61000692                  BSR     OSTRNG          ;CALL STRING OUTPUT ROU
TINE
 01FE 61000012  CTCK1:          BSR     TMCHK           ;CALL TIME CHECK SUBROU
TINE
 0202 207C000080                MOVEA.L #IOFLAG,A0      ;LOAD INTVL OVER FLAG A
DDRESS
 0208 3010                      MOVE.W  (A0),D0         ;LOAD FLAG
 020A 6600FF22                  BNE     TST2            ;IF SET BRANCH
 020E 6000FFEE                  BRA     CTCK1

 0212 303900FF00TMCHK:          MOVE.W  WARN.L,D0       ;LOAD POSITION UPDATE F
LAG
 0218 6700FFF8                  BEQ     TMCHK           ;IF ZERO BRANCH
 021C 303900FF00TMCK:           MOVE.W  WARN.L,D0       ;LOAD POSITION UPDATE F
LAG
 0222 6600FFF8                  BNE     TMCK            ;IF SET BRANCH

 0226 303900FF00                MOVE.W  FRZ1.L,D0       ;FREEZE TIME
 022C 4E71                      NOP
 022E 4E71                      NOP
```

```
 0230 303900FF00          MOVE.W  GREG1A.L,D0      ;LOAD WORD 1
 0236 323900FF00          MOVE.W  GREG1B.L,D1      ;LOAD WORD 2
 023C 343900FF00          MOVE.W  GREG1C.L,D2      ;LOAD WORD 3
 0242 363900FF00          MOVE.W  GREG1D.L,D3      ;LOAD WORD 4
 0248 383900FF00          MOVE.W  GREG1E.L,D4      ;LOAD WORD 5
 024E 3A3900FF00          MOVE.W  FRZ1_.L,D5       ;RELEASE FREEZE REG

 0254 610003AE            BSR     OTIME            ;CALL TIME OUTPUT SUBRO
UTINE
 0258 6100045E            BSR     OSTAT            ;CALL STATUS OUTPUT

 025C 4E75                RTS

                 ;*******************************************************
**********
                 ;        THIS TEST WILL SETUP INTERRUPT #3 AND #4 (COMP1
/COMP2)          *
                 ;        IT ALSO SETS THE GENERATOR PRESET REGISTERS AND
 THE     *
                 ;        COMP1 AND COMP2 TIMES AT 10 AND 12 SECONDS RESP
ECTIVELY         *
                 ;*******************************************************
**********
 025E 207C000080TEST3:   MOVEA.L #PFLAG,A0        ;LOAD FLAG ADDRESS
 0264 30BC00FF           MOVE.W  #0FFH,(A0)       ;SET PROMPT FLAG
 0268 207C000080TST3:    MOVEA.L #IOFLAG,A0       ;LOAD INT OVER FLAG ADD
RESS
 026E 30BC0000           MOVE.W  #00,(A0)         ;CLEAR FLAG
 0272 207C00FF00         MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 0278 30FC0004           MOVE.W  #04H,(A0)+       ;DISABLE INTERRUPTS
 027C 30BC0000           MOVE.W  #00H,(A0)        ;SETUP CONF REG 2 (STRO
BE SELECTS)
 0280 207C00FF00         MOVEA.L #BIMC3,A0        ;LOAD BIM CONTROL REG3
ADDRESS
 0286 30BC0011           MOVE.W  #11H,(A0)        ;SET INTERRUPT PRIORITY
 ETC
 028A 207C00FF00         MOVEA.L #BIMV3,A0        ;LOAD BIM VECTOR REG3 A
DDRESS
 0290 30BC0040           MOVE.W  #40H,(A0)        ;WRITE VECTOR NUMBER
 0294 41FA028A           LEA.L   COMP1(PC),A0     ;LOAD ADDRESS OF INTERR
UPT SERVICE ROUTINE
 0298 227C000001         MOVEA.L #0100H,A1        ;LOAD VECTOR ADDRESS
 029E 2288               MOVE.L  A0,(A1)          ;WRITE VECTOR
 02A0 207C00FF00         MOVEA.L #BIMC4,A0        ;LOAD BIM CONTROL REG4
ADDRESS
 02A6 30BC0011           MOVE.W  #11H,(A0)        ;SET INTERRUPT PRIORITY
 ETC
 02AA 207C00FF00         MOVEA.L #BIMV4,A0        ;LOAD BIM VECTOR REG4 A
DDRESS
 02B0 30BC0041           MOVE.W  #41H,(A0)        ;WRITE VECTOR NUMBER
 02B4 41FA02C8           LEA.L   COMP2(PC),A0     ;LOAD ADDRESS OF INTERR
UPT SERVICE ROUTINE
```

```
 02B8 227C000001          MOVEA.L #0104H,A1       ;LOAD VECTOR ADDRESS
 02BE 2288                MOVE.L  A0,(A1)         ;WRITE VECTOR

                  ;       PRESET GENERATOR
 02C0 207C00FF00          MOVEA.L #GPRST1,A0      ;LOAD ADDRESS OF GEN PR
ESET REG #1
 02C6 30FC0000            MOVE.W  #00,(A0)+       ;WRITE TO PRESET REGIST
ER 1
 02CA 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 2
 02CE 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 3
 02D2 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 4
 02D6 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 5
 02DA 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 6
 02DE 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 7

                  ;       PRESET COMP1 TIME

 02E2 207C00FF00          MOVEA.L #CMP1_1,A0      ;LOAD ADDRESS OF COMPAR
E TIME REG #1
 02E8 30FC0000            MOVE.W  #00,(A0)+       ;WRITE TO START REGISTE
R 1
 02EC 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 2
 02F0 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 3
 02F4 30FC0010            MOVE.W  #10H,(A0)+      ;REGISTER 4 (SEC)
 02F8 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 5
 02FC 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 6
 0300 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 7
 0304 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 8

                  ;       PRESET COMP2 TIME

 0308 30FC0000            MOVE.W  #00,(A0)+       ;WRITE TO COMP2
 030C 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 2
 0310 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 3
 0314 30FC0012            MOVE.W  #12H,(A0)+      ;REGISTER 4 (SEC)
 0318 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 5
 031C 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 6
 0320 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 7
 0324 30FC0000            MOVE.W  #00,(A0)+       ;REGISTER 8

 0328 207C00FF00          MOVEA.L #CFREG1,A0      ;LOAD CONFIG 1 ADDRESS
 032E 30BC0088            MOVE.W  #88H,(A0)       ;START/PRESET GEN AND E
NABLE INTERRUPTS
 0332 207C000080          MOVEA.L #PFLAG,A0       ;LOAD PROMPT FLAG ADDRE
SS
 0338 3010                MOVE.W  (A0),D0         ;LOAD FLAG
 033A 6700000E            BEQ     CTCK2           ;IF NOT SET BRANCH
 033E 30BC0000            MOVE.W  #00H,(A0)       ;CLEAR PROMPT FLAG
 0342 43FA0609            LEA.L   MSG5(PC),A1
 0346 61000546            BSR     OSTRNG          ;CALL STRING OUTPUT ROU
TINE
 034A 6100FEC6  CTCK2:    BSR     TMCHK           ;CALL TIME CHECK SUBROU
```

```
TINE
 034E 207C000080          MOVEA.L #IOFLAG,A0       ;LOAD FLAG ADDRESS
 0354 3010                MOVE.W  (A0),D0          ;LOAD INTVL OVER FLAG
 0356 6600FF10            BNE     TST3             ;IF SET BRANCH
 035A 6000FFEE            BRA     CTCK2

                 ;*************************************************************
**********
                 ;        THIS TEST WILL SETUP THE RATE GENERATOR
         *
                 ;        (AUTOMATICALLY CHANGES RATE OUTPUT)
         *
                 ;*************************************************************
**********
 035E            TEST4:
 035E 43FA0645            LEA.L   MSG7(PC),A1
 0362 6100052A            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE
 0366 207C00FF00          MOVEA.L #RATE,A0         ;LOAD RATE COUNT REGIST
ER
 036C 30BC0000            MOVE.W  #00H,(A0)        ;WRITE NONE RATE SELECT
ION
 0370 207C00FF00          MOVEA.L #CFREG1,A0       ;LOAD CONFIG 1 ADDRESS
 0376 30BC0000            MOVE.W  #00H,(A0)        ;START GENERATOR
 037A 203C000000          MOVE.L  #4,D0            ;SET COUNTER
 0380 60000008            BRA     TMCH4L
 0384 203C000000TST4:     MOVE.L  #0,D0            ;CLEAR COUNTER
 038A 323900FF00TMCH4L:   MOVE.W  WARN.L,D1        ;LOAD POSITION UPDATE F
LAG
 0390 6700FFF8            BEQ     TMCH4L           ;IF ZERO BRANCH
 0394 323900FF00TMCH4H:   MOVE.W  WARN.L,D1        ;LOAD POSITION UPDATE F
LAG
 039A 6600FFF8            BNE     TMCH4H           ;IF SET BRANCH
 039E D0BC000000          ADD.L   #01,D0           ;ADD ONE TO COUNTER
 03A4 B0BC000000          CMP.L   #05,D0           ;CHECK VALUE
 03AA 6D00FFDE            BLT     TMCH4L           ;IF < 5 BRANCH

 03AE 207C00FF00          MOVEA.L #RATE,A0         ;LOAD RATE COUNT REGIST
ER
 03B4 3010                MOVE.W  (A0),D0          ;LOAD CURRENT RATE
 03B6 B07C0005            CMP.W   #05,D0           ;CHECK RATE
 03BA 6D00000A            BLT     IRATE            ;IF OK BRANCH
 03BE 303C0000            MOVE.W  #0,D0            ;SET RATE TO NONE
 03C2 60000006            BRA     WRATE
 03C6 D07C0001  IRATE:    ADD.W   #01,D0           ;INCREMENT RATE
 03CA 3080      WRATE:    MOVE.W  D0,(A0)          ;WRITE NEW RATE
 03CC 43FA05F8            LEA.L   MSG8(PC),A1
 03D0 610004BC            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE

 03D4 43FA0603            LEA.L   RTE0(PC),A1
 03D8 B07C0000            CMP.W   #0,D0            ;CHECK RATE
```

```
 03DC 67000036          BEQ     ORATE
 03E0 43FA05FF          LEA.L   RTE1(PC),A1
 03E4 B07C0001          CMP.W   #1,D0
 03E8 6700002A          BEQ     ORATE
 03EC 43FA05FB          LEA.L   RTE2(PC),A1
 03F0 B07C0002          CMP.W   #2,D0
 03F4 6700001E          BEQ     ORATE
 03F8 43FA05F7          LEA.L   RTE3(PC),A1
 03FC B07C0003          CMP.W   #3,D0
 0400 67000012          BEQ     ORATE
 0404 43FA05F3          LEA.L   RTE4(PC),A1
 0408 B07C0004          CMP.W   #4,D0
 040C 67000006          BEQ     ORATE
 0410 43FA05EF          LEA.L   RTE5(PC),A1
 0414 61000478  ORATE:  BSR     OSTRNG
 0418 6000FF6A          BRA     TST4
                ;*******************************************************
**********
                ;       THIS TEST WILL SETUP THE RATE GENERATOR INTERRU
PT      *
                ;*******************************************************
**********
 041C           TEST5:
 041C 207C00FF00        MOVEA.L #BIMC2,A0       ;LOAD BIM CONTROL REG2
ADDRESS
 0422 30BC0011          MOVE.W  #11H,(A0)       ;SET INTERRUPT PRIORITY
 ETC
 0426 207C00FF00        MOVEA.L #BIMV2,A0       ;LOAD BIM VECTOR REG2 A
DDRESS
 042C 30BC0040          MOVE.W  #40H,(A0)       ;WRITE VECTOR NUMBER
 0430 41FA0038          LEA.L   ISRV1(PC),A0    ;LOAD ADDRESS OF INTERR
UPT SERVICE ROUTINE
 0434 227C000001        MOVEA.L #0100H,A1       ;LOAD VECTOR ADDRESS
 043A 2288              MOVE.L  A0,(A1)         ;WRITE VECTOR
 043C 43FA053B          LEA.L   MSG6(PC),A1
 0440 6100044C          BSR     OSTRNG          ;CALL STRING OUTPUT ROU
TINE
 0444 207C00FF00        MOVEA.L #RATE,A0        ;LOAD RATE COUNT REGIST
ER
 044A 30BC0004          MOVE.W  #04H,(A0)       ;WRITE 10 PPS RATE SELE
CTION
 044E 207C00FF00        MOVEA.L #CFREG1,A0      ;LOAD CONFIG 1 ADDRESS
 0454 30BC0000          MOVE.W  #00H,(A0)       ;START GENERATOR
 0458 207C00FF00        MOVEA.L #CFREG1,A0      ;LOAD CONFIG 1 ADDRESS
 045E 3010              MOVE.W  (A0),D0         ;LOAD CFREG1
 0460 807C0080          OR.W    #80H,D0         ;ENABLE INTERRUPTS
 0464 3080              MOVE.W  D0,(A0)         ;RETURN NEW VALUE TO CA
RD
 0466 6000FFFE  WAIT5:  BRA     WAIT5           ;WAIT

                ;.......................................................
.........
```

```
                ;       THIS INTERRUPT SERVICE ROUTINE WILL READ AND DI
SPLAY   :
                ;       THE TIME FROM GENERATOR FREEZE REGISTER #1
        :
                ;.....................................................
.........:
 046A           ISRV1:
 046A 2F00              MOVE.L  D0,-(A7)
 046C 2F01              MOVE.L  D1,-(A7)
 046E 2F02              MOVE.L  D2,-(A7)
 0470 2F03              MOVE.L  D3,-(A7)
 0472 2F04              MOVE.L  D4,-(A7)
 0474 2F05              MOVE.L  D5,-(A7)
 0476 2F06              MOVE.L  D6,-(A7)
 0478 2F08              MOVE.L  A0,-(A7)
 047A 2F09              MOVE.L  A1,-(A7)
 047C 2F0A              MOVE.L  A2,-(A7)
 047E 2F0B              MOVE.L  A3,-(A7)
 0480 2F0C              MOVE.L  A4,-(A7)
 0482 2F0D              MOVE.L  A5,-(A7)
 0484 2F0E              MOVE.L  A6,-(A7)
 0486 61000006          BSR     START2          ;CALL STRING OUTPUT ROU
TINE
 048A 6000015A          BRA     RESREG          ;RESTORE REGISTERS FROM
 STACK

 048E 303900FF00START2: MOVE.W  FRZ1.L,D0       ;FREEZE TIME
 0494 4E71              NOP
 0496 4E71              NOP
 0498 303900FF00        MOVE.W  GREG1A.L,D0     ;LOAD WORD 1
 049E 323900FF00        MOVE.W  GREG1B.L,D1     ;LOAD WORD 2
 04A4 343900FF00        MOVE.W  GREG1C.L,D2     ;LOAD WORD 3
 04AA 363900FF00        MOVE.W  GREG1D.L,D3     ;LOAD WORD 4
 04B0 383900FF00        MOVE.W  GREG1E.L,D4     ;LOAD WORD 5
 04B6 3A3900FF00        MOVE.W  FRZ1_.L,D5      ;RELEASE FREEZE REG
 04BC 4E71              NOP
 04BE 4E71              NOP
 04C0 61000142          BSR     OTIME           ;CALL TIME OUTPUT SUBRO
UTINE
 04C4 610001F2          BSR     OSTAT           ;CALL STATUS OUTPUT
 04C8 4E75              RTS
                ;.....................................................
.........
                ;       THIS INTERRUPT SERVICE ROUTINE WILL READ AND DI
SPLAY   :
                ;       THE TIME FROM GENERATOR FREEZE REGISTER #2
        :
                ;.....................................................
.........:
 04CA           ISRV2:
 04CA 2F00              MOVE.L  D0,-(A7)
 04CC 2F01              MOVE.L  D1,-(A7)
```

```
 04CE 2F02                MOVE.L  D2,-(A7)
 04D0 2F03                MOVE.L  D3,-(A7)
 04D2 2F04                MOVE.L  D4,-(A7)
 04D4 2F05                MOVE.L  D5,-(A7)
 04D6 2F06                MOVE.L  D6,-(A7)
 04D8 2F08                MOVE.L  A0,-(A7)
 04DA 2F09                MOVE.L  A1,-(A7)
 04DC 2F0A                MOVE.L  A2,-(A7)
 04DE 2F0B                MOVE.L  A3,-(A7)
 04E0 2F0C                MOVE.L  A4,-(A7)
 04E2 2F0D                MOVE.L  A5,-(A7)
 04E4 2F0E                MOVE.L  A6,-(A7)
 04E6 61000006            BSR     START3          ;CALL STRING OUTPUT ROU
TINE
 04EA 600000FA            BRA     RESREG          ;RESTORE REGISTERS FROM
 STACK

 04EE 303900FF00START3:   MOVE.W  GREG2A.L,D0     ;LOAD WORD 1
 04F4 323900FF00          MOVE.W  GREG2B.L,D1     ;LOAD WORD 2
 04FA 343900FF00          MOVE.W  GREG2C.L,D2     ;LOAD WORD 3
 0500 363900FF00          MOVE.W  GREG2D.L,D3     ;LOAD WORD 4
 0506 383900FF00          MOVE.W  GREG2E.L,D4     ;LOAD WORD 5
 050C 3A3900FF00          MOVE.W  FRZ2_.L,D5      ;RELEASE FREEZE REG
 0512 4E71                NOP
 0514 4E71                NOP
 0516 610000EC            BSR     OTIME           ;CALL TIME OUTPUT SUBRO
UTINE
 051A 6100019C            BSR     OSTAT           ;CALL STATUS OUTPUT
 051E 4E75                RTS

                  ;.......................................
                  ;       COMPARE TIME INTERRUPT SERVICE  :
                  ;.......................................:
 0520             COMP1:
 0520 2F00                MOVE.L  D0,-(A7)
 0522 2F01                MOVE.L  D1,-(A7)
 0524 2F02                MOVE.L  D2,-(A7)
 0526 2F03                MOVE.L  D3,-(A7)
 0528 2F04                MOVE.L  D4,-(A7)
 052A 2F05                MOVE.L  D5,-(A7)
 052C 2F06                MOVE.L  D6,-(A7)
 052E 2F08                MOVE.L  A0,-(A7)
 0530 2F09                MOVE.L  A1,-(A7)
 0532 2F0A                MOVE.L  A2,-(A7)
 0534 2F0B                MOVE.L  A3,-(A7)
 0536 2F0C                MOVE.L  A4,-(A7)
 0538 2F0D                MOVE.L  A5,-(A7)
 053A 2F0E                MOVE.L  A6,-(A7)
 053C 303900FF00          MOVE.W  FRZ1.L,D0       ;FREEZE TIME
 0542 4E71                NOP
 0544 4E71                NOP
 0546 303900FF00          MOVE.W  GREG1A.L,D0     ;LOAD WORD 1
```

```
 054C 323900FF00          MOVE.W  GREG1B.L,D1      ;LOAD WORD 2
 0552 343900FF00          MOVE.W  GREG1C.L,D2      ;LOAD WORD 3
 0558 363900FF00          MOVE.W  GREG1D.L,D3      ;LOAD WORD 4
 055E 383900FF00          MOVE.W  GREG1E.L,D4      ;LOAD WORD 5
 0564 3A3900FF00          MOVE.W  FRZ1_.L,D5       ;RELEASE FREEZE REG
 056A 4E71                NOP
 056C 4E71                NOP
 056E 61000094            BSR     OTIME            ;CALL TIME OUTPUT SUBRO
UTINE
 0572 43FA04DC            LEA.L   STFND(PC),A1
 0576 61000316            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE
 057A 6000006A            BRA     RESREG           ;RESTORE REGISTERS FROM
 STACK

                  ;.......................................
                  ;       COMP2 TIME INTERRUPT SERVICE    :
                  ;.......................................:
 057E             COMP2:
 057E 2F00                MOVE.L  D0,-(A7)
 0580 2F01                MOVE.L  D1,-(A7)
 0582 2F02                MOVE.L  D2,-(A7)
 0584 2F03                MOVE.L  D3,-(A7)
 0586 2F04                MOVE.L  D4,-(A7)
 0588 2F05                MOVE.L  D5,-(A7)
 058A 2F06                MOVE.L  D6,-(A7)
 058C 2F08                MOVE.L  A0,-(A7)
 058E 2F09                MOVE.L  A1,-(A7)
 0590 2F0A                MOVE.L  A2,-(A7)
 0592 2F0B                MOVE.L  A3,-(A7)
 0594 2F0C                MOVE.L  A4,-(A7)
 0596 2F0D                MOVE.L  A5,-(A7)
 0598 2F0E                MOVE.L  A6,-(A7)
 059A 303900FF00          MOVE.W  FRZ1.L,D0        ;FREEZE TIME
 05A0 4E71                NOP
 05A2 4E71                NOP
 05A4 303900FF00          MOVE.W  GREG1A.L,D0      ;LOAD WORD 1
 05AA 323900FF00          MOVE.W  GREG1B.L,D1      ;LOAD WORD 2
 05B0 343900FF00          MOVE.W  GREG1C.L,D2      ;LOAD WORD 3
 05B6 363900FF00          MOVE.W  GREG1D.L,D3      ;LOAD WORD 4
 05BC 383900FF00          MOVE.W  GREG1E.L,D4      ;LOAD WORD 5
 05C2 3A3900FF00          MOVE.W  FRZ1_.L,D5       ;RELEASE FREEZE REG
 05C8 4E71                NOP
 05CA 4E71                NOP
 05CC 61000036            BSR     OTIME            ;CALL TIME OUTPUT SUBRO
UTINE
 05D0 43FA0495            LEA.L   SPFND(PC),A1
 05D4 610002B8            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE
 05D8 207C000080          MOVEA.L #IOFLAG,A0       ;LOAD FLAG ADDRESS
 05DE 30BC00FF            MOVE.W  #0FFH,(A0)       ;SET INTVL OVER FLAG
 05E2 60000002            BRA     RESREG           ;RESTORE REGISTERS FROM
```

```
STACK


05E6 2C5F      RESREG: MOVEA.L (A7)+,A6
05E8 2A5F              MOVEA.L (A7)+,A5
05EA 285F              MOVEA.L (A7)+,A4
05EC 265F              MOVEA.L (A7)+,A3
05EE 245F              MOVEA.L (A7)+,A2
05F0 225F              MOVEA.L (A7)+,A1
05F2 205F              MOVEA.L (A7)+,A0
05F4 2C1F              MOVE.L  (A7)+,D6
05F6 2A1F              MOVE.L  (A7)+,D5
05F8 281F              MOVE.L  (A7)+,D4
05FA 261F              MOVE.L  (A7)+,D3
05FC 241F              MOVE.L  (A7)+,D2
05FE 221F              MOVE.L  (A7)+,D1
0600 201F              MOVE.L  (A7)+,D0
0602 4E73              RTE
                ;.................................
                ;       OUTPUT TIME SUBROUTINE  :
                ;.................................:
0604 61000202  OTIME:  BSR     CRTN             ;OUTPUT CARRIAGE RETURN
0608 610001A4         BSR     DSPACE           ;WRITE A SPACE
060C 3C04             MOVE.W  D4,D6            ;WRITE THOUS YEARS
060E E04E             LSR.W   #0,D6            ;SHIFT RIGHT 8 PLACES
0610 E84E             LSR.W   #4,D6            ;SHIFT RIGHT 4 PLACES
0612 610001AA         BSR     MKASC            ;CALL OUTPUT
0616 3C04             MOVE.W  D4,D6            ;WRITE HUND YEARS
0618 E04E             LSR.W   #0,D6            ;SHIFT RIGHT 8 PLACES
061A 610001A2         BSR     MKASC            ;CALL OUTPUT
061E 3C04             MOVE.W  D4,D6            ;WRITE TENS YEARS
0620 E84E             LSR.W   #4,D6
0622 6100019A         BSR     MKASC
0626 3C04             MOVE.W  D4,D6            ;WRITE UNIT YEARS
0628 61000194         BSR     MKASC
062C 61000208         BSR     COL              ;WRITE A COLLON

0630 3C03             MOVE.W  D3,D6            ;WRITE HUND DAYS
0632 E04E             LSR.W   #0,D6            ;SHIFT RIGHT 8 PLACES
0634 61000188         BSR     MKASC            ;CALL OUTPUT
0638 3C03             MOVE.W  D3,D6            ;WRITE TENS DAYS
063A E84E             LSR.W   #4,D6
063C 61000180         BSR     MKASC
0640 3C03             MOVE.W  D3,D6            ;WRITE UNIT DAYS
0642 6100017A         BSR     MKASC
0646 610001EE         BSR     COL              ;WRITE A COLLON
064A 3C02             MOVE.W  D2,D6            ;WRITE TENS HOURS
064C E04E             LSR.W   #0,D6            ;SHIFT RIGHT 8 PLACES
064E E84E             LSR.W   #4,D6            ;SHIFT ANOTHER 4
0650 6100016C         BSR     MKASC            ;CALL OUTPUT
0654 3C02             MOVE.W  D2,D6            ;WRITE UNIT HOURS
0656 E04E             LSR.W   #0,D6
```

```
 0658 61000164          BSR     MKASC
 065C 610001D8          BSR     COL             ;WRITE A COLLON
 0660 3C02              MOVE.W  D2,D6           ;WRITE TENS MINUTES
 0662 E84E              LSR.W   #4,D6
 0664 61000158          BSR     MKASC
 0668 3C02              MOVE.W  D2,D6           ;WRITE UNIT MINUTES
 066A 61000152          BSR     MKASC
 066E 610001C6          BSR     COL             ;WRITE A COLLON
 0672 3C01              MOVE.W  D1,D6           ;WRITE TENS SECONDS
 0674 E04E              LSR.W   #0,D6           ;SHIFT RIGHT 8 PLACES
 0676 E84E              LSR.W   #4,D6           ;SHIFT ANOTHER 4
 0678 61000144          BSR     MKASC           ;CALL OUTPUT
 067C 3C01              MOVE.W  D1,D6           ;WRITE UNIT SECONDS
 067E E04E              LSR.W   #0,D6           ;SHIFT RIGHT 8 PLACES
 0680 6100013C          BSR     MKASC           ;CALL OUTPUT
 0684 610001C0          BSR     PER             ;WRITE A PERIOD
 0688 3C01              MOVE.W  D1,D6           ;WRITE .1 SEC
 068A E84E              LSR.W   #4,D6           ;SHIFT RIGHT 4 PLACES
 068C 61000130          BSR     MKASC           ;CALL OUTPUT
 0690 3C01              MOVE.W  D1,D6           ;WRITE .01 SEC
 0692 6100012A          BSR     MKASC           ;CALL OUTPUT
 0696 3C00              MOVE.W  D0,D6           ;WRITE .001 SECONDS
 0698 E04E              LSR.W   #0,D6           ;SHIFT RIGHT 8 PLACES
 069A E84E              LSR.W   #4,D6           ;SHIFT ANOTHER 4
 069C 61000120          BSR     MKASC
 06A0 3C00              MOVE.W  D0,D6           ;WRITE .0001 SECONDS
 06A2 E04E              LSR.W   #0,D6           ;SHIFT RIGHT 8 PLACES
 06A4 61000118          BSR     MKASC
 06A8 3C00              MOVE.W  D0,D6           ;WRITE .00001 SEC
 06AA E84E              LSR.W   #4,D6           ;SHIFT 4 PLACES
 06AC 61000110          BSR     MKASC           ;CALL OUTPUT
 06B0 3C00              MOVE.W  D0,D6           ;WRITE .000001 SEC
 06B2 6100010A          BSR     MKASC           ;CALL OUTPUT
 06B6 4E75              RTS

 06B8           OSTAT:
 06B8 303900FF00        MOVE.W  CFREG1.L,D0     ;LOAD CONFIG REG 1
 06BE 02000003          ANDI.B  #03H,D0         ;MASK OFF UPPER 6 BITS
 06C2 6700003E          BEQ     EXIT            ;IF GENERATOR MODE EXIT
 06C6 3C03              MOVE.W  D3,D6           ;CHECK STATUS
 06C8 0806000C          BTST.L  #12,D6          ;CHECK CODE ERROR BIT
 06CC 6600000E          BNE     CERR            ;IF SET BRANCH
 06D0 43FA034E          LEA.L   FAIL_(PC),A1
 06D4 610001B8          BSR     OSTRNG          ;CALL STRING OUTPUT ROU
TINE
 06D8 6000000A          BRA     CKLOCK
 06DC 43FA032E  CERR:   LEA.L   FAIL(PC),A1
 06E0 610001AC          BSR     OSTRNG          ;CALL STRING OUTPUT ROU
TINE
 06E4 3C03      CKLOCK: MOVE.W  D3,D6           ;CHECK STATUS
 06E6 0806000D          BTST.L  #13,D6          ;CHECK PHASE LOCK BIT
 06EA 6600000E          BNE     PHLOCK          ;IF SET BRANCH
```

```
 06EE 43FA034F          LEA.L   LOCK_(PC),A1
 06F2 6100019A          BSR     OSTRNG          ;CALL STRING OUTPUT ROU
TINE
 06F6 6000000A          BRA     EXIT
 06FA 43FA0332  PHLOCK: LEA.L   LOCK(PC),A1
 06FE 6100018E          BSR     OSTRNG          ;CALL STRING OUTPUT ROU
TINE
 0702 4E75      EXIT:   RTS

 0704 61000112  OMODE:  BSR     CRLF
 0708 43FA0374          LEA.L   OPMODE(PC),A1   ;WRITE OPERATIONAL MODE
 PROMPT
 070C 61000180          BSR     OSTRNG
 0710 3C3900FF00        MOVE.W  CFREG1.L,D6
 0716 CC7C0003          AND.W   #03H,D6
 071A 43FA036F          LEA.L   GENMD(PC),A1
 071E BC3C0000          CMP.B   #0,D6           ;CHECK VALUE
 0722 67000006          BEQ     OPMD1           ;IF ZERO BRANCH
 0726 43FA0373          LEA.L   CODMD(PC),A1
 072A 61000162  OPMD1:  BSR     OSTRNG
 072E 610000E8          BSR     CRLF
 0732 4E75              RTS

 0734 43FA0375  DACOUT: LEA.L   DDAC(PC),A1     ;WRITE DAC PROMPT
 0738 61000154          BSR     OSTRNG
 073C 3C3900FF00        MOVE.W  DAC.L,D6
 0742 E95E              ROL.W   #4,D6
 0744 6100009E          BSR     HEXOUT
 0748 3C3900FF00        MOVE.W  DAC.L,D6
 074E E15E              ROL.W   #0,D6
 0750 61000092          BSR     HEXOUT
 0754 E95E              ROL.W   #4,D6
 0756 6100008C          BSR     HEXOUT
 075A E95E              ROL.W   #4,D6
 075C 61000086          BSR     HEXOUT
 0760 610000B6          BSR     CRLF
 0764 4E75              RTS

 0766 43FA0357  SELTST: LEA.L   STST(PC),A1     ;WRITE SELF TEST PROMPT
 076A 61000122          BSR     OSTRNG
 076E 3C3900FF00        MOVE.W  STEST.L,D6
 0774 61000048          BSR     MKASC
 0778 6100009E          BSR     CRLF
 077C 4E75              RTS

 077E E95E      OPACK:  ROL.W   #4,D6
 0780 6100001A          BSR     OPACK1
 0784 E95E              ROL.W   #4,D6
 0786 61000014          BSR     OPACK1
 078A 610000AA          BSR     COL
 078E E95E              ROL.W   #4,D6
 0790 6100000A          BSR     OPACK1
```

```
 0794 E95E              ROL.W   #4,D6
 0796 61000004          BSR     OPACK1
 079A 4E75              RTS

 079C 2F06      OPACK1: MOVE.L  D6,-(A7)        ;SAVE D6 ON STACK
 079E 0206000F          ANDI.B  #0FH,D6
 07A2 8C3C0030          OR.B    #30H,D6
 07A6 6100001E          BSR     OUTPUT
 07AA 2C1F              MOVE.L  (A7)+,D6        ;RESTORE D6 FROM STACK
 07AC 4E75              RTS

 07AE 61000024  DSPACE: BSR     READY
 07B2 207C000C00        MOVEA.L #UARTD,A0       ;LOAD UART DATA ADDRESS
 07B8 10BC0020          MOVE.B  #20H,(A0)       ;OUTPUT A SPACE
 07BC 4E75              RTS


 07BE 0206000F  MKASC:  ANDI.B  #0FH,D6
 07C2 8C3C0030          OR.B    #30H,D6

 07C6 6100000C  OUTPUT: BSR     READY           ;WAIT TILL TRANSMIT REG
 EMPTY
 07CA 207C000C00        MOVEA.L #UARTD,A0       ;LOAD UART DATA ADDRESS
 07D0 1086              MOVE.B  D6,(A0)         ;OUTPUT CHARACTER
 07D2 4E75              RTS

 07D4 247C000C00READY:  MOVEA.L #UARTS,A2       ;LOAD UART STATUS ADDRE
SS
 07DA 08120001          BTST.B  #01,(A2)        ;CHECK IF TRANSMIT REG
EMPTY
 07DE 6700FFF4          BEQ     READY           ;IF NOT BRANCH
 07E2 4E75              RTS

 07E4 0206000F  HEXOUT: ANDI.B  #0FH,D6
 07E8 BC3C0009          CMP.B   #09,D6
 07EC 63000010          BLS     HXOUT1          ;IF =< 9 BRANCH
 07F0 9C3C000A          SUB.B   #10,D6          ;SUBTRACT 10
 07F4 DC3C0041          ADD.B   #41H,D6         ;MAKE ASCII
 07F8 6100FFCC          BSR     OUTPUT
 07FC 4E75              RTS
 07FE 8C3C0030  HXOUT1: OR.B    #30H,D6
 0802 6100FFC2          BSR     OUTPUT
 0806 4E75              RTS


 0808 6100FFCA  CRTN:   BSR     READY
 080C 207C000C00        MOVEA.L #UARTD,A0       ;LOAD UART DATA ADDRESS
 0812 10BC000D          MOVE.B  #CR,(A0)        ;OUTPUT A CARRIAGE RETU
RN
 0816 4E75              RTS

 0818 6100FFBA  CRLF:   BSR     READY
```

```
 081C 207C000C00          MOVEA.L #UARTD,A0        ;LOAD UART DATA ADDRESS
 0822 10BC000D            MOVE.B  #CR,(A0)         ;OUTPUT A CARRIAGE RETU
RN

 0826 6100FFAC  LNFD:     BSR     READY
 082A 207C000C00          MOVEA.L #UARTD,A0        ;LOAD UART DATA ADDRESS
 0830 10BC000A            MOVE.B  #LF,(A0)         ;OUTPUT A LINE FEED
 0834 4E75                RTS

 0836 6100FF9C  COL:      BSR     READY
 083A 207C000C00          MOVEA.L #UARTD,A0        ;LOAD UART DATA ADDRESS
 0840 10BC003A            MOVE.B  #3AH,(A0)        ;OUTPUT A COLLON
 0844 4E75                RTS

 0846 6100FF8C  PER:      BSR     READY
 084A 207C000C00          MOVEA.L #UARTD,A0        ;LOAD UART DATA ADDRESS
 0850 10BC002E            MOVE.B  #2EH,(A0)        ;OUTPUT A PERIOD
 0854 4E75                RTS

 0856 BC3C0000  CUP:      CMP.B   #0,D6            ;CHECK COUNT
 085A 67000018            BEQ     CUPEX            ;IF ZERO BRANCH
 085E 9C3C0001            SUB.B   #1,D6
 0862 6100FF70            BSR     READY
 0866 207C000C00          MOVEA.L #UARTD,A0        ;LOAD UART DATA ADDRESS
 086C 10BC001A            MOVE.B  #1AH,(A0)        ;OUTPUT CURSOR UP
 0870 6000FFE4            BRA     CUP
 0874 6100FF92  CUPEX:    BSR     CRTN
 0878 4E75                RTS

 087A 43FA018D  HOME:     LEA.L   HOM(PC),A1
 087E 6100000E            BSR     OSTRNG           ;CALL STRING OUTPUT ROU
TINE

 0882 3C3C0FFF  DELAY:    MOVE.W  #0FFFH,D6        ;PRESET COUNTER
 0886 9C7C0001  HAGAIN:   SUB.W   #01,D6           ;DECREMENT
 088A 66FA                BNE.S   HAGAIN
 088C 4E75                RTS

 088E 1C19      OSTRNG:   MOVE.B  (A1)+,D6
 0890 6706                BEQ.S   STEX
 0892 6100FF32            BSR     OUTPUT
 0896 60F6                BRA.S   OSTRNG

 0898 4E75      STEX:     RTS

 089A 3536302D35MSG1:     DFB     "560-56xx Series, VME/VME-SG, Capture R
eg #1",0DH,0AH,00
 08C8 3536302D35MSG2:     DFB     "560-56xx Series, VME/VME-SG, Capture R
eg #2",0DH,0AH,00
 08F6 0D0A455854MSG3:     DFB     0DH,0AH,"EXTERNAL EVENT INTERRUPT TEST
INSTALLED",0DH,0AH,00
 0922 0D0A2E3120MSG4:     DFB     0DH,0AH,".1 MSEC INTERVAL OUTPUT TEST I
```

```
NSTALLED",0DH,0AH,00
 094D 0D0A434F4DMSG5:    DFB     0DH,0AH,"COMP#1/COMP#2, INTERRUPT TEST
INSTALLED",0DH,0AH,00
 0979 0D0A524154MSG6:    DFB     0DH,0AH,"RATE GENERATOR INTERRUPT TEST
INSTALLED",0DH,0AH,00
 09A5 0D0A524154MSG7:    DFB     0DH,0AH,"RATE GENERATOR TEST INSTALLED"
,0DH,0AH
 09C6 0D43555252MSG8:    DFB     0DH,"CURRENT RATE IS  ",00
 09D9 4F46462020RTE0:    DFB     "OFF    ",00
 09E1 31304B2050RTE1:    DFB     "10K PPS",00
 09E9 314B205050RTE2:    DFB     "1K PPS ",00
 09F1 3130302050RTE3:    DFB     "100 PPS",00
 09F9 3130205050RTE4:    DFB     "10 PPS ",00
 0A01 3120534543RTE5:    DFB     "1 SEC  ",00
 0A09 0C0100    HOM:     DFB     0CH,01H,00
 0A0C 2052454645FAIL:    DFB     " REFERENCE FAILURE ",00
 0A20 2052454645FAIL_:   DFB     " REFERENCE OK",00
 0A2E 2C20504841LOCK:    DFB     ", PHASE LOCKED  ",00
 0A3F 2020202020LOCK_:   DFB     "                ",00
 0A50 2C20434F4DSTFND:   DFB     ", COMP#1 TIME FOUND ",0DH,0AH,00
 0A67 2C20434F4DSPFND:   DFB     ", COMP#2 TIME FOUND ",0DH,0AH,00
 0A7E 204F504552OPMODE:  DFB     " OPER MODE  ",00
 0A8B 2047454E45GENMD:   DFB     " GENERATOR     ",00
 0A9B 20434F4445CODMD:   DFB     " CODE SYNC-GEN ",00
 0AAB 2044414320DDAC:    DFB     " DAC SETTING (hex) ",00
 0ABF 2053454C46STST:    DFB     " SELF TEST   ",00
 0ACD 2020202020BLNK:    DFB     "       ",00

 0000                    END

0000  BAMALL              0012  BDCALL              0000  BIMC1

0002  BIMC2               0004  BIMC3               0006  BIMC4

0008  BIMV1               000A  BIMV2               000C  BIMV3

000E  BIMV4               0ACD  BLNK                06DC  CERR

00A0  CFREG1              00A2  CFREG2              06E4  CKLOCK

00E0  CMP1_1              00E2  CMP1_2              00E4  CMP1_3

00E6  CMP1_4              00E8  CMP1_5              00EA  CMP1_6

00EC  CMP1_7              00EE  CMP1_8              00F0  CMP2_1

00F2  CMP2_2              00F4  CMP2_3              00F6  CMP2_4

00F8  CMP2_5              00FA  CMP2_6              00FC  CMP2_7

00FE  CMP2_8              0A9B  CODMD               0836  COL
```

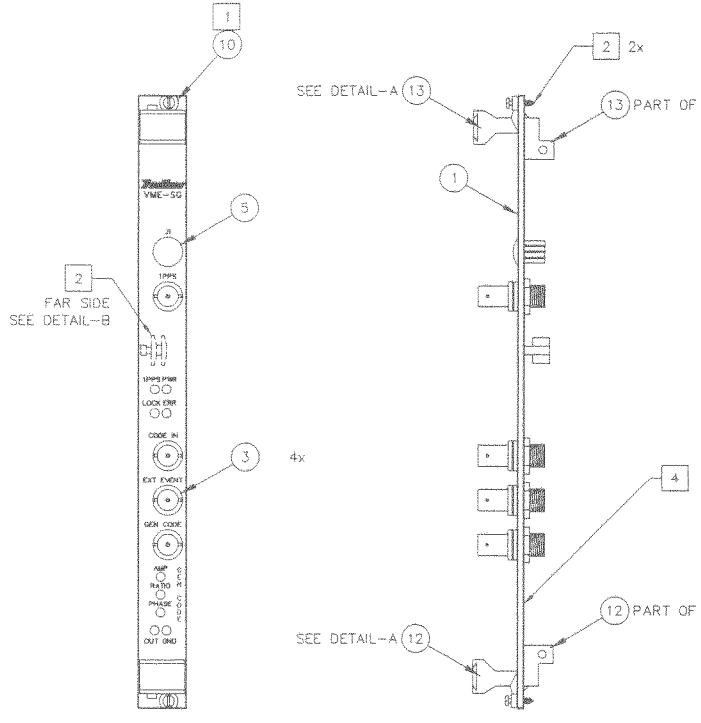
0520	COMP1	057E	COMP2	000D	CR
0818	CRLF	0808	CRTN	01FE	CTCK1
034A	CTCK2	0856	CUP	0874	CUPEX
00AA	DAC	0734	DACOUT	0020	DALL
0024	DALL1	0AAB	DDAC	0882	DELAY
07AE	DSPACE	0702	EXIT	0A0C	FAIL
0A20	FAIL_	0040	FRZ1	0044	FRZ1_
0048	FRZ2_	0A8B	GENMD	00AC	GPRST1
00AE	GPRST2	00B0	GPRST3	00B2	GPRST4
00B4	GPRST5	00B6	GPRST6	00B8	GPRST7
00BA	GPRST8	00BC	GPRST9	0042	GREG1A
0080	GREG1B	0082	GREG1C	0084	GREG1D
0086	GREG1E	0046	GREG2A	0088	GREG2B
008A	GREG2C	008C	GREG2D	008E	GREG2E
0886	HAGAIN	07E4	HEXOUT	0A09	HOM
087A	HOME	07FE	HXOUT1	8002	IOFLAG
03C6	IRATE	046A	ISRV1	04CA	ISRV2
0001	L	000A	LF	0826	LNFD
00A6	LOCAL	0A2E	LOCK	0A3F	LOCK_
07BE	MKASC	089A	MSG1	08C8	MSG2
08F6	MSG3	0922	MSG4	094D	MSG5
0979	MSG6	09A5	MSG7	09C6	MSG8
0704	OMODE	077E	OPACK	079C	OPACK1
072A	OPMD1	0A7E	OPMODE	0414	ORATE
06B8	OSTAT	088E	OSTRNG	0604	OTIME
07C6	OUTPUT	0846	PER	8000	PFLAG

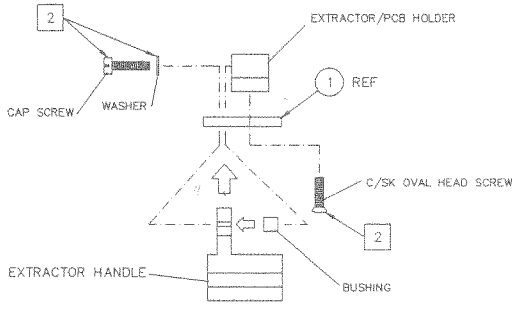
06FA PHLOCK	00A8 RATE	07D4 READY
05E6 RESREG	09D9 RTE0	09E1 RTE1
09E9 RTE2	09F1 RTE3	09F9 RTE4
0A01 RTE5	0094 RTN2	0766 SELTST
00D0 SGCOMP	00D8 SPARE1	00DA SPARE2
00DC SPARE3	0A67 SPFND	048E START2
04EE START3	00DE STEST	0898 STEX
0A50 STFND	0ABF STST	00DC TEST1
0124 TEST2	025E TEST3	035E TEST4
041C TEST5	0394 TMCH4H	038A TMCH4L
0212 TMCHK	0032 TMCHK1	003C TMCHK2
021C TMCK	012E TST2	0268 TST3
0384 TST4	0082 UARTD	0080 UARTS
0000 W	00D8 WAIT2	0120 WAIT3
0466 WAIT5	00BE WARN	03CA WRATE

© TrueTime, Inc. 2000 All Rights Reserved.
PROPRIETARY NOTICE
THIS DOCUMENT, WHETHER PATENTABLE OR NON-PATENTABLE SUBJECT MATTER, EMBODIES PROPRIETARY AND CONFIDENTIAL INFORMATION AND IS THE EXCLUSIVE PROPERTY OF TRUETIME, INC. IT MAY NOT BE REPRODUCED, USED OR DISCLOSED TO OTHERS FOR ANY PURPOSE EXCEPT THAT FOR WHICH IT IS LOANED, AND IT SHALL BE RETURNED UPON DEMAND.

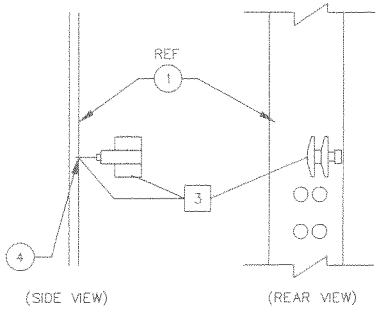
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
B	REDRAWN; ADDED ITEM 10	03-16-94	
C	CAR 605, CAR 606	03-02-98	
D	CAR 874 & CAR 924; REDRAWN	04-24-98	
E	CAR 1429	04-28-99	
F	ADDED NOTE 4	08-28-00	DGK

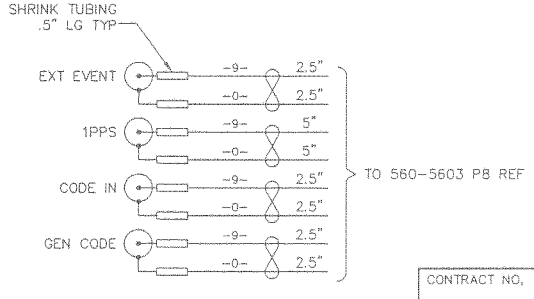




DETAIL-A



DETAIL-B



4 STAMP PART No. AND REV. LEVEL WHERE SHOWN.

3 ALIGN CENTER PCB HOLDER (PART OF ITEM 9) TO DIMPLE ON PANEL AND GLUE TO PANEL USING ITEM 4 ("KRAZY GLUE" OR EQUIV) AS REQUIRED.

2 MOUNTING HARDWARE IS PART OF ITEM 9.

1 REPLACE EXISTING PLASTIC SLEEVES (PART OF ITEM 9) WITH STAINLESS SLEEVES (ITEM 10) AND PRESS INTO FRONT OF PANEL.

NOTES: UNLESS OTHERWISE SPECIFIED

FILENAME: \560\1146
DATE: 08-28-00

CONTRACT NO.	
APPROVALS	DATE
DRAWN BY D. EDILLOR	03-94
CHECKED BY	
APPROVED BY	
NEXT ASSY	

TrueTime®
"Where Customer Satisfaction is our Highest Priority"
2835 Duke Ct. Santa Rosa, CA 95407

ASSEMBLY, FRONT PANEL VME-SG

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		560-1146	F

SCALE NONE SHEET 1 OF 1

R30410

TrueTime, Inc.
Single Level Bill of Material Report

ORIGINAL

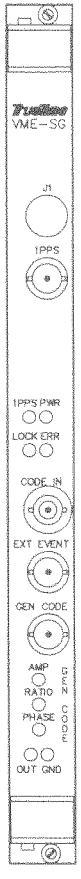
Date - 8/28/00
Time - 17:43:16

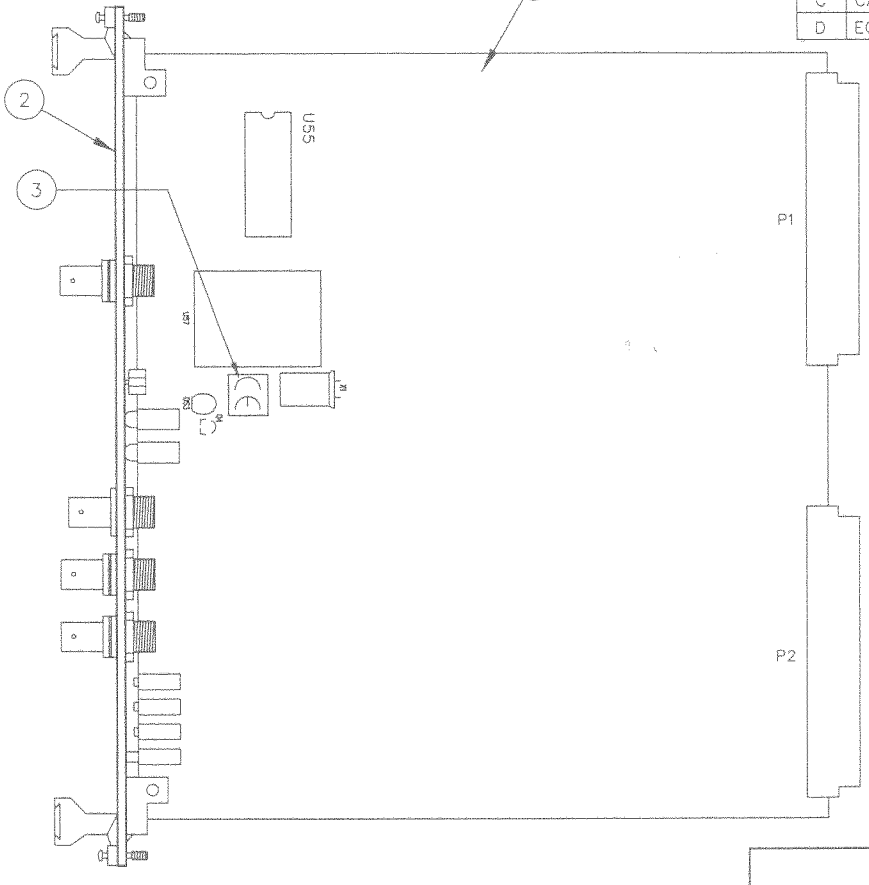
Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Thru
560-1146	ASSY FRONT PNL VME-SG		EA	Type M	Rev [redacted] Draw						
0000-PL	PARTS LIST REV LEVEL	1.00	EA		REV F (08-28-00)	1	S	2.0	M	1/1/00	12/31/10
0000-PRINT	REFERENCE PRINT	1.00	EA		560-1146 REV F	1	S	3.0	M	1/1/00	12/31/10
223-004	HANDLE(TOP) GPS-VME	1.00	EA	13		1	S	4.0	P	1/1/00	12/31/10
223-005	HANDLE (BOTTOM) GPS-VME	1.00	EA	12		1	S	5.0	P	1/1/00	12/31/10
223-006	HARDWARE FRT PNL GPS-VME	1.00	EA	9		1	S	6.0	P	1/1/00	12/31/10
223-464	SLEEVE, STAINLESS	2.00	EA	10		1	S	7.0	P	1/1/00	12/31/10
274-005	PLUG HOLE NYL 3/8 DIA	1.00	EA	5		1	S	8.0	P	1/1/00	12/31/10
284-001	ADHESIVE (SUPER GLUE)	.10	EA	4	AS NEEDED	1	S	9.0	P	1/1/00	12/31/10
315-022-009	WIRE 22AWG PVC INS WHITE	1.50	FT		SEE WIRING	1	S	10.0	P	1/1/00	12/31/10
315-022-010	WIRE 22AWG PVC INS BLACK	1.50	FT		SEE WIRING	1	S	11.0	P	1/1/00	12/31/10
326-001	SHRINK TUBING CLR 3/32 IN	.50	FT		SEE WIRING	1	S	12.0	P	1/1/00	12/31/10
375-014	CONN FM BULKHD RECP INSUL	4.00	EA	3		1	S	13.0	P	1/1/00	12/31/10
560-1145	PANEL,FRONT VME-SG	1.00	EA	1		1	S	14.0	P	1/1/00	12/31/10
560-1146-OSV	ASSY FRONT PNL VME-SG-OSV	1.00	EA			1	S	15.0	P	8/24/00	12/31/10

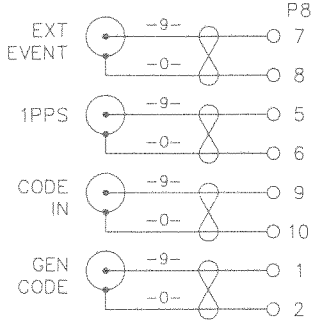
© TrueTime, Inc. 1999 All Rights Reserved.
PROPRIETARY NOTICE
THIS DOCUMENT, WHETHER PATENTABLE OR NON-PATENTABLE SUBJECT MATTER, EMBODIES PROPRIETARY AND CONFIDENTIAL INFORMATION AND IS THE EXCLUSIVE PROPERTY OF TRUETIME, INC. IT MAY NOT BE REPRODUCED, USED OR DISCLOSED TO OTHERS FOR ANY PURPOSE EXCEPT THAT FOR WHICH IT IS LOANED, AND IT SHALL BE RETURNED UPON DEMAND.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	MODIFIED WIRING DETAIL PER 560-5603 REV C	05-10-93	P.E.
B	CAR 644, CAR 605, CAR 606	03-02-98	
C	CAR 1361	01-19-99	J.W.
D	ECO 1227; CHG LABEL TYPE FOR ITEM 3	08-16-99	







WIRING DETAIL
WIRES ARE TO BE SOLDERED DIRECTLY TO PADS

APPROVALS	DATE
DRAWN BY D. EDILLOR	04-93
CHECKED BY	
APPROVED BY	3/99

NEXT ASSY

FILENAME: \560\5608
DATE: 08-16-99

TrueTime®
"Where Customer Satisfaction is our Highest Priority"
2835 Duke Ct. Santa Rosa, CA 95407

ASSEMBLY, VME-SG2

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		560-5608	D

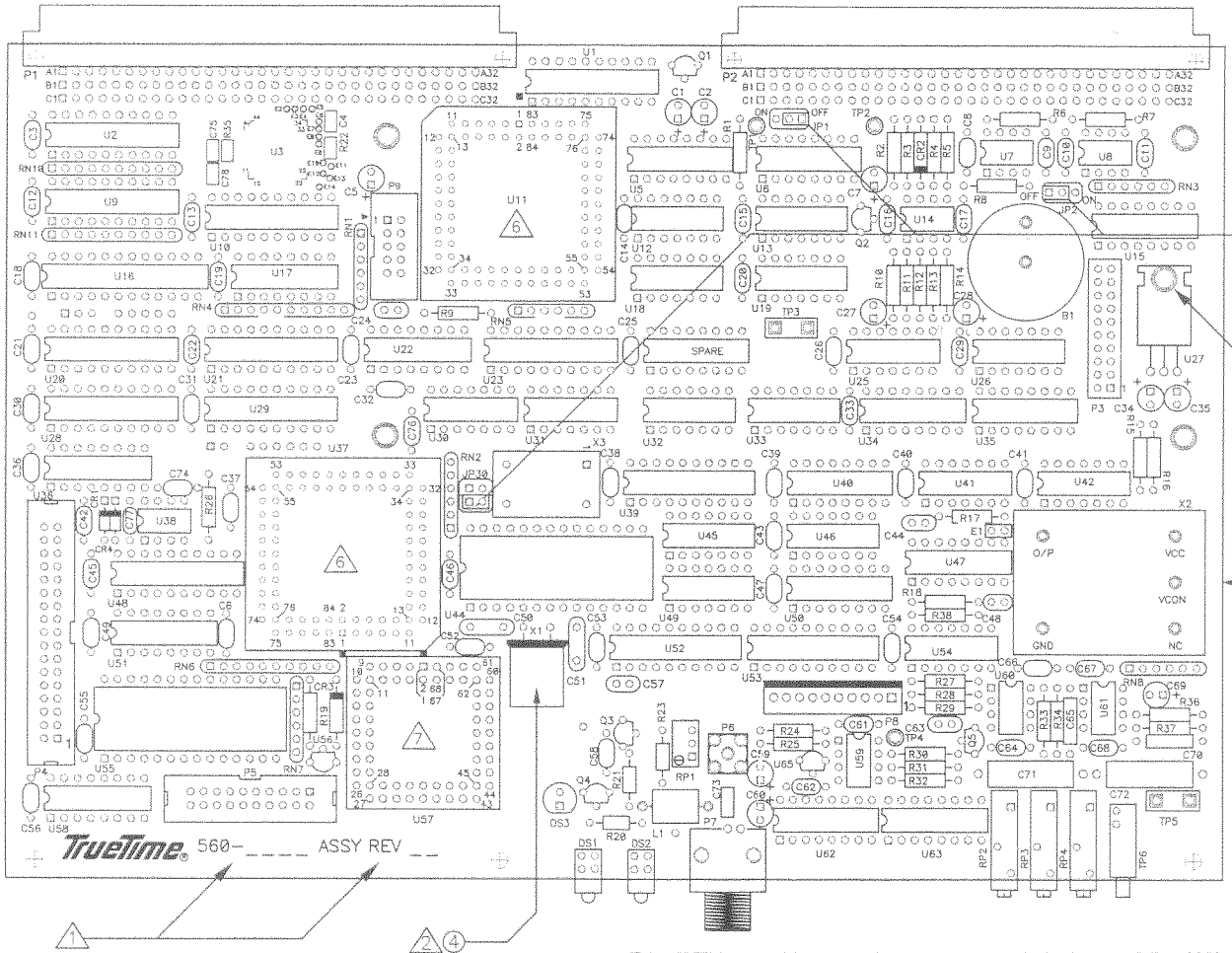
SCALE NONE SHEET 1 OF 1

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
560-5608	FINAL ASSY VME-SG2	VME-SG W/SINGLE-WIDE BRKT				EA		
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		DR 8/99
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV D (08-16-99)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		560-5608 REV D
400-084	LABEL,CE (SMALL)(WHITE)	MADE FROM 400-081	000000		1.0000	EA		03
560-1146	ASSY FRONT PNL VME-SG	SINGLE-WIDE BRKT ASSY	000000		1.0000	EA		02
560-3068	EPROM PROGRAMMING		000000		1.0000	EA		U55 ON 560-5603
560-5603	VME-SG	MADE FROM 560-2600	000000		1.0000	EA		01
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		
OSV560-5608	OUTSIDE LABOR 560-5608	PCA	000000		1.0000	EA		

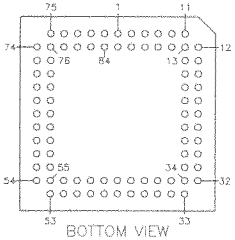
REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
–	SEE HISTORY		
N	ECO 1244	07-27-99	
P	ECO's 1295 & 1296	04-10-00	
R	ECO 1329	05-02-00	

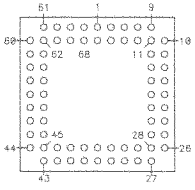


NOTE: UNLESS OTHERWISE SPECIFIED

1. STAMP ASSEMBLY NUMBER AND REVISION
2. INSTALL ITEM 4 BETWEEN X1 AND PC BOARD
3. RESISTOR VALUES IN OHMS, CAPACITORS IN MICRO FARADS
4. ASSEMBLE PER ASSEMBLY REQUIREMENTS DOCUMENT #421-11
5. INSTALL JUMPERS AT JP1,2,30 AS SHOWN.
6. U11 & U37 PIN SEQUENCE



7. U57 PIN SEQUENCE



© TrueTime, Inc. 2000 All Rights Reserved
PROPRIETARY NOTICE
THIS DOCUMENT, WHETHER PATENTABLE OR NON-PATENTABLE SUBJECT MATTER, EMBODIES PROPRIETARY AND CONFIDENTIAL INFORMATION AND IS THE EXCLUSIVE PROPERTY OF TRUETIME, INC. IT MAY NOT BE REPRODUCED, USED OR DISCLOSED TO OTHERS FOR ANY PURPOSE EXCEPT THAT FOR WHICH IT IS LOANED, AND IT SHALL BE RETURNED UPON DEMAND.

CONTRACT NO.		
APPROVALS		DATE
DRAWN BY	R.E.C.	8-23-94
CHECKED		
APPROVED		5-9-00
NEXT ASSY		

TrueTime, Inc.
Santa Rosa, California

Title	ASSEMBLY DRAWING VME PROCESSOR BOARD	
Size	Number	Rev
B	560-5603	R
Date	Fri May 05, 2000	
Filename	2600-J.PCB	Sheet 1 of 12

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
560-5603	VME-SG		EA	Type M	Rev R Draw						
0000-PL	PARTS LIST REV LEVEL	1.00	EA		REV R (08-07-00)	1	S	2.0	M	1/1/00	12/31/10
0000-PRINT	REFERENCE PRINT	1.00	EA		560-5603 REV R	1	S	3.0	M	1/1/00	12/31/10
0000-REV	PCB REV LEVEL HERE >>>>	1.00	EA		560-2600 REV J	1	S	4.0	M	1/1/00	12/31/10
002-051	RES 120 OHM 1/4W 5%	1.00	EA			1	S	5.0	P	1/1/00	12/31/10
	R1										
002-063	RES 390 OHM 1/4W 5% R25J391	1.00	EA			1	S	6.0	P	1/1/00	12/31/10
	R11										
002-073	RES 1K OHM 1/4W 5%	4.00	EA			1	S	7.0	P	1/1/00	12/31/10
	R20 R21 R29 R38										
002-080	RES 2K OHM 1/4W 5%	1.00	EA			1	S	8.0	P	1/1/00	12/31/10
	R25										
002-084	RES 3K OHM 1/4W 5%	1.00	EA			1	S	9.0	P	1/1/00	12/31/10
	R5										
002-089	RES 4.7K OHM 1/4W 5%	5.00	EA			1	S	10.0	P	1/1/00	12/31/10
	R27 R28 R33 R6 R7										
002-097	RES 10K OHM 1/4W 5%	4.00	EA			1	S	11.0	P	1/1/00	12/31/10
	R13 R14 R26 R32										
002-105	RES 22K OHM 1/4W 5%	4.00	EA			1	S	12.0	P	1/1/00	12/31/10
	R17 R18 R4 R9										
002-118	RES 75K OHM 1/4W 5%	1.00	EA			1	S	13.0	P	1/1/00	12/31/10
	R10										
002-121	RES 100K OHM 1/4W 5%	2.00	EA			1	S	14.0	P	1/1/00	12/31/10
	R23 R31										
002-125	RES 150K OHM 1/4W 5%	2.00	EA			1	S	15.0	P	1/1/00	12/31/10

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
	R12 R8										
002-129	RES 220K OHM 1/4W 5%	1.00	EA			1	S	16.0	P	1/1/00	12/31/10
	R19										
002-153	RES 2.2 MEG OHM 1/4W 5%	1.00	EA			1	S	17.0	P	1/1/00	12/31/10
	R2										
008-1001	RES 1K OHM 1/8W 1%	1.00	EA			1	S	18.0	P	1/1/00	12/31/10
	R16										
008-1072	RES 10.7K OHM 1/8W 1%	4.00	EA			1	S	19.0	P	1/1/00	12/31/10
	R3 R34 R36 R37										
008-2210	RES 221 OHM 1/8W 1%	1.00	EA			1	S	20.0	P	1/1/00	12/31/10
	R15										
008-3922	RES 39.2K OHM 1/8W 1%	1.00	EA			1	S	21.0	P	1/1/00	12/31/10
	R30										
008-8061	RES 8.06K OHM 1/8W 1%	1.00	EA			1	S	22.0	P	1/1/00	12/31/10
	R24										
008S-1002	RES 0805 10K OHM 1% 1/8W	1.00	EA			1	S	23.0	P	1/1/00	12/31/10
	R22										
008S-101	RES 0805 100 OHM 5% 1/8W	1.00	EA			1	S	24.0	P	1/1/00	12/31/10
	R35										
011-065-06S	RESNET 470 OHM 6-P ISL	1.00	EA			1	S	25.0	P	1/1/00	12/31/10
	RN8										
011-077-06S	RESNET 1.5K OHM 6-P ISL	1.00	EA			1	S	26.0	P	1/1/00	12/31/10
	RN3										
011-089-06C	RESNET 4.7K OHM 6-P COM	2.00	EA			1	S	27.0	P	1/1/00	12/31/10
	RN1 RN5										

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble / Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
011-089-06S	RESNET 4.7K OHM 6-P ISL	2.00	EA			1	S	28.0	P	1/1/00	12/31/10
	RN2 RN7										
011-089-10C	RESNET 4.7K OHM 10-P COM	4.00	EA			1	S	29.0	P	1/1/00	12/31/10
	RN10 RN11 RN4 RN6										
019-002	POT 5K 20 TURN	2.00	EA			1	S	30.0	P	1/1/00	12/31/10
	RP2 RP3										
019-010	POT 50K 20 TURN T ADJ	1.00	EA			1	S	31.0	P	1/1/00	12/31/10
	RP1										
019-020	POT 20K FRT PNL ADJUSTBL	1.00	EA			1	S	32.0	P	1/1/00	12/31/10
	RP4										
028-008-080	CAP FILM .0047 80V A 10%	2.00	EA			1	S	33.0	P	1/1/00	12/31/10
	C65 C70										
028-021-080	CAP FILM .047 80V A 10%	2.00	EA			1	S	34.0	P	1/1/00	12/31/10
	C71 C72										
029-014	CAP MICA 18PF V R 5%	2.00	EA			1	S	35.0	P	1/1/00	12/31/10
	C50 C51										
036-033	CAP MONO 100PF 50V R	4.00	EA			1	S	36.0	P	1/1/00	12/31/10
	C24 C44 C48 C63										
036-101	CAP MONO .1UF 50V	53.00	EA			1	S	37.0	P	1/1/00	12/31/10
	C10 C11 C12 C13 C14 C15 C16 C17 C18 C19										
	C20 C21 C22 C23 C25 C26 C29 C3 C30 C31										
	C32 C33 C36 C37 C38 C39 C40 C41 C42 C43										
	C45 C46 C47 C49 C52 C53 C54 C55 C56 C57										
	C58 C6 C61 C62 C64 C66 C67 C68 C74 C76										
	C77 C8 C9										
036S-NPO330	CAP 33PF NPO 100V 0805	1.00	EA			1	S	38.0	P	1/1/00	12/31/10
	C78										

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
036S-X7R104-50	CAP .1UF X7R 50V 0805 10%	2.00	EA			1	S	39.0	P	1/1/00	12/31/10
	C4 C75										
037-033	CAP TANT 2.2UF 35V R	8.00	EA			1	S	40.0	P	1/1/00	12/31/10
	C1 C2 C28 C34 C35 C59 C60 C69										
037-041	CAP TANT 10UF 20V R 20%	3.00	EA			1	S	41.0	P	1/1/00	12/31/10
	C27 C5 C7										
039-022	CAP SRF MNT 22PF NPO	1.00	EA			1	S	42.0	P	1/1/00	12/31/10
	C73										
045-2.5	INDUCTOR 2.5UH	1.00	EA			1	S	43.0	P	1/1/00	12/31/10
	L1										
055-914A	DIODE 1V 20MA	2.00	EA			1	S	44.0	P	1/1/00	12/31/10
	CR2 CR3										
058-004	LED RED, SM	1.00	EA			1	S	45.0	P	1/1/00	12/31/10
	DS3										
058-011	LED GREEN/GREEN	1.00	EA			1	S	46.0	P	1/1/00	12/31/10
	DS1										
058-012	LED RED/YELLOW	1.00	EA			1	S	47.0	P	1/1/00	12/31/10
	DS2										
059-1.8432A	XTAL 1.8432 HC18	1.00	EA		X1 SECURE WITH ITEM 04	1	S	48.0	P	1/1/00	12/31/10
065-008	SWITCH DIP 8 POS	1.00	EA			1	S	49.0	P	1/1/00	12/31/10
	U5										
174-XC3042A	XILINX XC3042A	1.00	EA		U11 SOCKETED	1	S	50.0	P	1/1/00	12/31/10
174S-XC4003E	XILINX FPGA PLCC 84-PIN	1.00	EA		U37 SOCKETED	1	S	51.0	P	1/1/00	12/31/10
175-1087	XSISTOR FET P-CHANNEL	1.00	EA			1	S	52.0	P	1/1/00	12/31/10

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
	Q2										
175-3702	XSISTOR MPS3702 (TO-92)	1.00	EA			1	S	53.0	P	1/1/00	12/31/10
	Q4										
175-BS170	XSISTOR TMOS N-CHNL	1.00	EA			1	S	54.0	P	1/1/00	12/31/10
	Q3										
175-J176	XSISTOR FET P-CHANNEL	1.00	EA			1	S	55.0	P	1/1/00	12/31/10
	Q5										
176-082	TL082CP DUAL OP AMP	4.00	EA			1	S	56.0	P	1/1/00	12/31/10
	U14 U59 U60 U61										
176-311	LM311N VOLTAGE COMPARATOR	2.00	EA			1	S	57.0	P	1/1/00	12/31/10
	U7 U8										
176-317	LM317 ADJ. POS REGULATOR	1.00	EA			1	S	58.0	P	1/1/00	12/31/10
	U27										
176-34064	UNDER VOLT.SENSING CKT	1.00	EA			1	S	59.0	P	1/1/00	12/31/10
	U56										
176-431	TL431CLP REGULATOR/3 PIN	1.00	EA			1	S	60.0	P	1/1/00	12/31/10
	U65										
176-6551	UART, 65C51	1.00	EA			1	S	61.0	P	1/1/00	12/31/10
	U44										
176-68HC11F1	IC, CPU	1.00	EA		U57 SOCKETED	1	S	62.0	P	1/1/00	12/31/10
176-79L05	MC79L05ACP -5V REGULATOR	1.00	EA			1	S	63.0	P	1/1/00	12/31/10
	Q1										
176-8923N	DS8923N DIFF LINE DRIVER	1.00	EA			1	S	64.0	P	1/1/00	12/31/10
	U6										
176-GAL16V8	GAL16V8D-25-LP	3.00	EA			1	S	65.0	P	1/1/00	12/31/10

U53 SOCKETED AND PROGRAMMED PER 560-4002 U23 SOCKETED AND PROGRAMMED PER 560-4003 U48 SOCKETED AND

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
PROGRAMMED PER 560-4018											
176-PCM56P	DIGITAL TO ANALOG CONVTR	1.00	EA			1	S	66.0	P	1/1/00	12/31/10
	U62										
176-VME2000	VME2000	1.00	EA			1	S	67.0	P	1/1/00	12/31/10
	U16										
177-27256	CERAMIC 27C256 @ 200NS	1.00	EA			1	S	68.0	P	1/1/00	12/31/10
U55 SOCKETED. PROGRAM AT TRUETIME AT TOP ASSY LEVEL.											
177-74ALS245	74ALS245A-1 BUS XCVR	3.00	EA			1	S	69.0	P	1/1/00	12/31/10
	U10 U2 U9										
177-74ALS374	74ALS374 OCTAL D FLIP FLP	1.00	EA			1	S	70.0	P	1/1/00	12/31/10
	U21										
177-74ALS641	74ALS641 OCTAL BUS XCVR	1.00	EA			1	S	71.0	P	1/1/00	12/31/10
	U1										
178-17C128	FPGA CONFIG EEPROM	1.00	EA			1	S	72.0	P	1/1/00	12/31/10
U38 SOCKETED AND PROGRAMMED PER 184-017											
178-74HC00	MM74HC00N QUAD NAND GATE	1.00	EA			1	S	73.0	P	1/1/00	12/31/10
	U25										
178-74HC08	MC74HC08 QUAD AND GATE	4.00	EA			1	S	74.0	P	1/1/00	12/31/10
	U13 U30 U31 U33										
178-74HC107	74HC107 DUAL JK FLIP-FLOP	2.00	EA			1	S	75.0	P	1/1/00	12/31/10
	U19 U42										
178-74HC138	MC74HC138 1 OF 8 DECODER	3.00	EA			1	S	76.0	P	1/1/00	12/31/10
	U17 U51 U58										
178-74HC14	74HC14 HEX SCHM INVERTER	2.00	EA			1	S	77.0	P	1/1/00	12/31/10
	U45 U49										
178-74HC174	74HC174N HEX D FLIP-FLOP	2.00	EA			1	S	78.0	P	1/1/00	12/31/10
	U50 U63										

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
178-74HC221.7	ONE SHOT TIME CONT T=.7RC	2.00	EA			1	S	79.0	P	1/1/00	12/31/10
	U22 U47										
178-74HC273	74HC273 D FLIP-FLOP	1.00	EA			1	S	80.0	P	1/1/00	12/31/10
	U52										
178-74HC32	MC74HC32 QUAD OR GATE	1.00	EA			1	S	81.0	P	1/1/00	12/31/10
	U32										
178-74HC374	MC74HC374 D FLIP-FLOP	4.00	EA			1	S	82.0	P	1/1/00	12/31/10
	U20 U28 U29 U39										
178-74HC390	74HC390 DUAL BI-QUINARY	2.00	EA			1	S	83.0	P	1/1/00	12/31/10
	U36 U40										
178-74HC4053	74HC4053 MULTIPLEXER	2.00	EA			1	S	84.0	P	1/1/00	12/31/10
	U34 U35										
178-74HC74	MC74HC74 DUAL D FLIP-FLOP	5.00	EA			1	S	85.0	P	1/1/00	12/31/10
	U12 U18 U26 U41 U46										
178-74HC86	74HC86 QUAD EX OR GATE	1.00	EA			1	S	86.0	P	1/1/00	12/31/10
	U54										
178S-MACH211SP	IC, PROGRAMMABLE, CPLD	1.00	EA			1	S	87.0	P	1/1/00	12/31/10
	U3 INSTALL PART. NOT PROGRAMMED. NOTE: THIS PART WILL BE PROGRAMMED AT TRUETIME. AT TRUETIME: DOWNLOAD PROGRAM 560-4031 USING CABLE AND FIXTURE.										
184-017	XILINX DUAL PORT RAM	1.00	EA			1	S	88.0	M	1/1/00	12/31/10
	PROGRAM FOR U38. PROGRAM RESET POLARITY BIT. USE LABEL 400-026, MARK AND AFFIX.NOTE: ECO 1329 CHANGED SOFTWARE REV TO 184-017F										
223-131	SCHROFF TP DUAL	1.00	EA			1	S	89.0	P	1/1/00	12/31/10
	TP6										
240-004-003	SCREW PH PN SS 4-40X3/8	1.00	EA	3		1	S	90.0	P	1/1/00	12/31/10
251-004	NUT KEP SS 4-40	1.00	EA	2		1	S	91.0	P	1/1/00	12/31/10
273-009	TERMINAL TEST POINT	2.00	EA			1	S	92.0	P	1/1/00	12/31/10

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
	TP3 TP5										
273-015	TERM TEST POINT (WHITE)	3.00	EA			1	S	93.0	P	1/1/00	12/31/10
	TP1 TP2 TP4										
290-001	TAPE FOAM DBL SIDE.5X1/16	.20	SI		04 FOR X1	1	S	94.0	P	1/1/00	12/31/10
345-022	OSCILLATOR, 10MHZ(VCTCXO)	1.00	EA			1	S	95.0	P	1/1/00	12/31/10
	X2										
345-042	OSC 40MHZ CMOS	1.00	EA			1	S	96.0	P	1/1/00	12/31/10
	X3										
379-008	SOCKET IC 8 PIN MACHINE	1.00	EA		FOR U38	1	S	97.0	P	1/1/00	12/31/10
379-020	SOCKET IC 20 PIN MACHINE	3.00	EA		FOR U23,48,53	1	S	98.0	P	1/1/00	12/31/10
379-028-001	SOCKET IC 28 PIN MACHINE	1.00	EA		FOR U55	1	S	99.0	P	1/1/00	12/31/10
379-068-002	SOCKET PLCC 68-PIN	1.00	EA		FOR U57	1	S	100.0	P	1/1/00	12/31/10
379-084	SOCKET PLCC 84-PIN	2.00	EA		FOR U11,37	1	S	101.0	P	1/1/00	12/31/10
384-096	CONN 96-P RT ANGLE	2.00	EA			1	S	102.0	P	1/1/00	12/31/10
	P1 P2										
386-010P	CONN 10-P MALE PCB	1.00	EA			1	S	103.0	P	1/1/00	12/31/10
	P9										
386-341	CONN 34-P ML PC MT HDR	1.00	EA			1	S	104.0	P	1/1/00	12/31/10
	P4										
400-026	LABEL,SPCL CONN 1X1/4 IN	5.00	EA			1	S	105.0	P	1/1/00	12/31/10
	FOR PROGRAMMED PARTS. MARK WITH PROGRAM PART NUMBER AND VERSION. EXAMPLE OF MARKING: 560-4002 V.XX										
	CUT TO FIT AND ATTACH TO PROGRAMMED PART.										
401-01-01-34	CONN 36-P HDR SNGL RW W/W	1.00	EA			1	S	106.0	P	1/1/00	12/31/10
	JP1,JP2 (CUT TO FIT). JP30 (CUT TO FIT) AND INSTALL JUMPER JP30 FROM PIN 3 TO PIN 4.										
403-000LP	JUMPER FEMALE LOW PROFILE	3.00	EA			1	S	107.0	P	1/1/00	12/31/10

Parent Item / Component Item	Parent Description / Component Descripiton	Batch Quantity / Quantity Per	UM	Bubble Seq No	Remarks	Level	Ty	Seq	T	Effective From	Effective Thru
INSTALL AT THE FOLLOWING LOCATIONS: JP1 PINS 1,2 JP2 PINS 1,2 JP30 PINS 1,2 ON LOWER HALF OF JP30											
560-2600	PCB VME-SG (GPS COMPAT)	1.00	EA	1		1	S	108.0	P	1/1/00	12/31/10
560-4002	PROG DEV GAL16V8(RAL16R6)	1.00	EA			1	S	109.0	M	1/1/00	12/31/10
PROGRAM FOR U53 (SOCKETED GAL) USE LABEL 400-026, MARK AND AFFIX.											
560-4003	PROG DEV GAL16V8(RAL16R4)	1.00	EA			1	S	110.0	M	1/1/00	12/31/10
PROGRAM FOR U23 (SOCKETED GAL) USE LABEL 400-026, MARK AND AFFIX.											
560-4018	PROGRAMMED PAL	1.00	EA			1	S	111.0	M	1/1/00	12/31/10
PROGRAM FOR U48 (SOCKETED GAL) USE LABEL 400-026, MARK AND AFFIX.											
560-4031	PROGRAM SYNC ADDRESS CODE	1.00	EA			1	S	112.0	M	1/1/00	12/31/10
PROGRAMMED AT TRUETIME. PROGRAM FOR U3 (DOWNLOAD). USE LABEL 400-026, MARK AND AFFIX.											
57-5082-2835	DIODE, SCHOTTKEY LOW VOLT	2.00	EA			1	S	113.0	P	1/1/00	12/31/10
	CR1 CR4										
NOTE 1	NOTE	1.00	EA		U15 IS SPARE	1	S	116.0	M	1/1/00	12/31/10

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP