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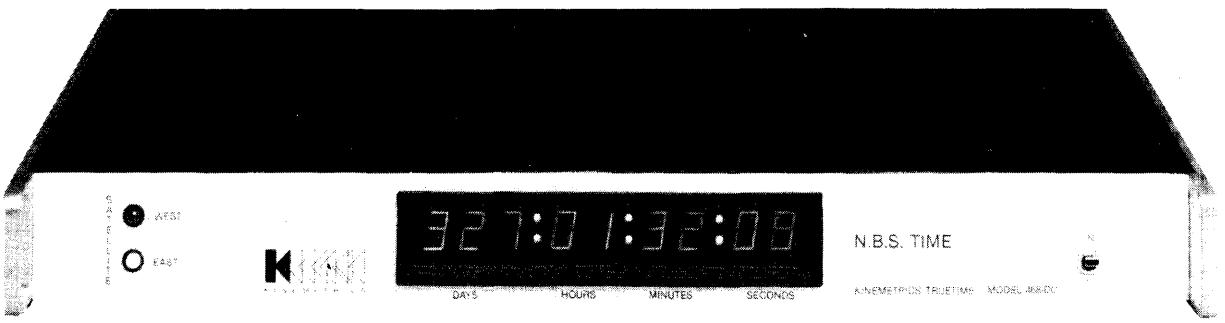
Find the *Microsemi / Truetime / Kinemetrics 468-DC* at our website: ***Click HERE***

KINEMETRICS | TRUETIME

OPERATING AND SERVICE MANUAL

"MODEL 468-DC-MRS"

Satellite Synchronized Clock



KINEMETRICS/TRUETIME: 3243 SANTA ROSA AVE., SANTA ROSA, CA 95407 (707) 528-1230 - TELEX 176687 - FAX (707) 527-6640

MANUAL DATED 10/86

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KINEMETRICS / TRUETIME
3243 Santa Rosa Ave.
Santa Rosa, CA 95407

"References in this manual to:	May be replaced by:
468-DC	468-DC/MM
A-468MS	A-468MS/RK/MM-2
A-468RK	A-468RK/MM-2"

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KINEMETRICS | TRUETIME

MARTIN MARIETTA CORPORATION

SALES ORDER NO. 8255

In 1982 Kinemetrics/TrueTime redesigned the Models A-468MS/RK and A-468RK GOES antenna system. The newer MK II version of the Model A-468MS/RK has a different circuit card and has different dimensions than the MK I. The MK II antenna is still compatible with the MK I Remote Kit, and the MK II Remote Kit is still compatible with the MK I antenna as far as function is concerned. The MK II version of the Remote Kit also has a different circuit card and different dimensions.

When we supplied GOES antennas to Martin Marietta in 1984, we were able to remanufacture MK I kits from resources that were still available to us. Those resources are no longer available. Producing MK I antennas at this point in time would entail an extremely prohibitive expense for Martin Marietta. The MK II GOES antenna system is now the only version available to us. However, we can still accommodate Martin Marietta van application by providing a special adapter plate to be installed on the MK II Remote Kit. This plate will allow the user to interchange both MK I and MK II Remote Kits. Both units are functionally the same as far as input/outputs are concerned.

The mounting holes in the antenna pedestal baseplate have been drilled out to 0.459", and the upright mounting stanchion has been shorted to 9.5" to conform to Martin Marietta Drawing No. 85OMROR0026. Applicable drawings follow this page.

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468DC-MRS SYSTEM DESCRIPTION

ITEM	PART NUMBER	DESCRIPTION
1	468-DC MM	GOES Satellite Synchronized Clock
2.	A-468MS/RK MM 2	GOES Antenna Mark II
3	A-468RK MM	Antenna Remote Kit
4	A-468BP/MM	Base Plate Adapter for Item 3
5	A-468 MM - 1.5	Cable Assembly 1.5 foot length
6	A-468 MM - 20	Cable Assembly 20 Foot length RG 214 with "N" Connectors
7	A-468BC/MM	"N" Bulkhead Connector
8	A-468AP1/MM	Paint Code 17925 for Item 2 (White)
9	A-468PP1/MM	Paint Code 17925 for Item 4 (White)

WARRANTY INFORMATION:

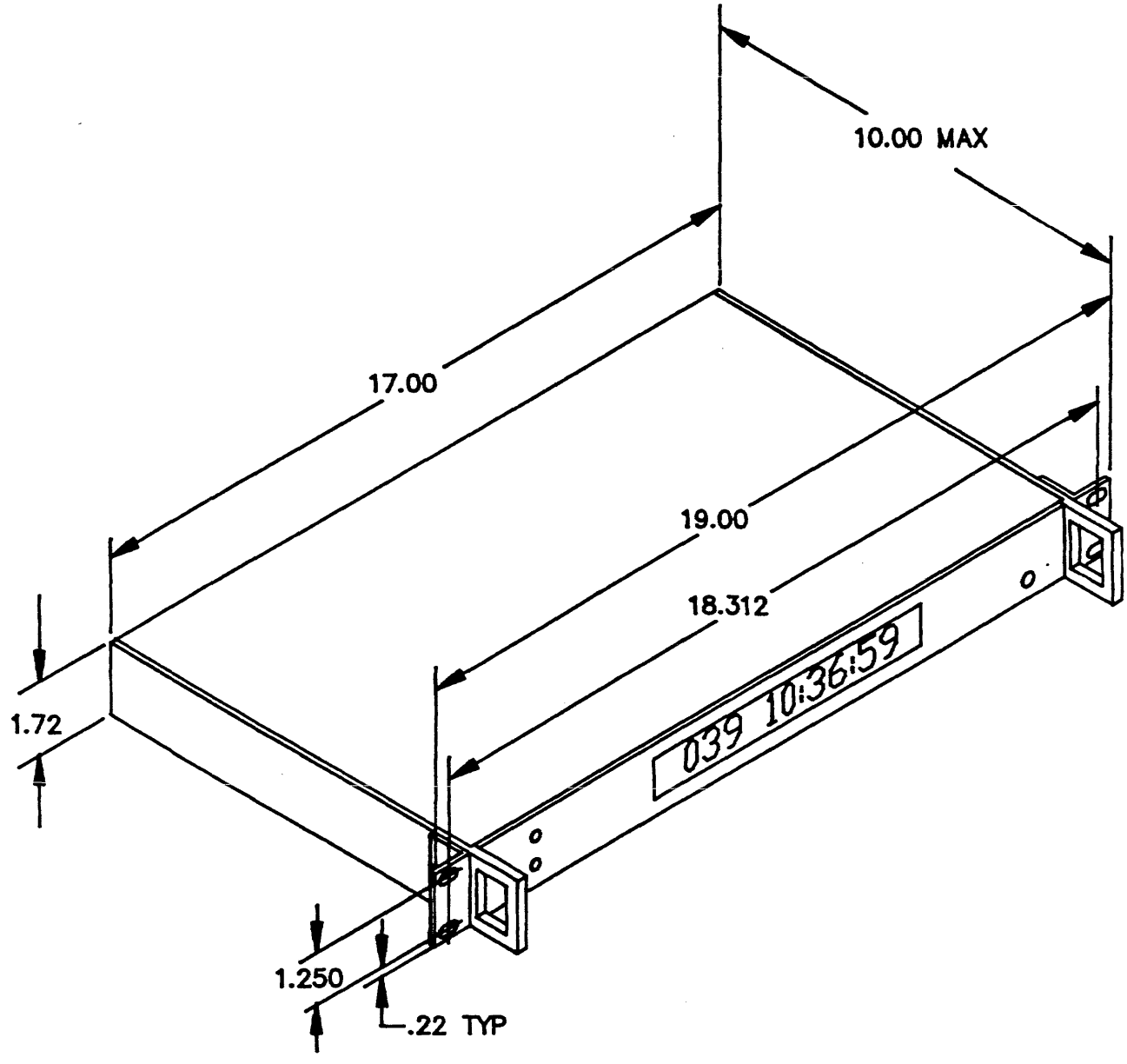
The Kinemetrics/TrueTime design of the 468-DC-MRS is considered proprietary. Kinemetrics/TrueTime's Santa Rosa factory is the only facility authorized to perform warranty repairs. This warranty is transferable from Martin Marietta to their end user. Refer to pages 1 through 3 of this manual for additional details.

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APPENDIX "A"

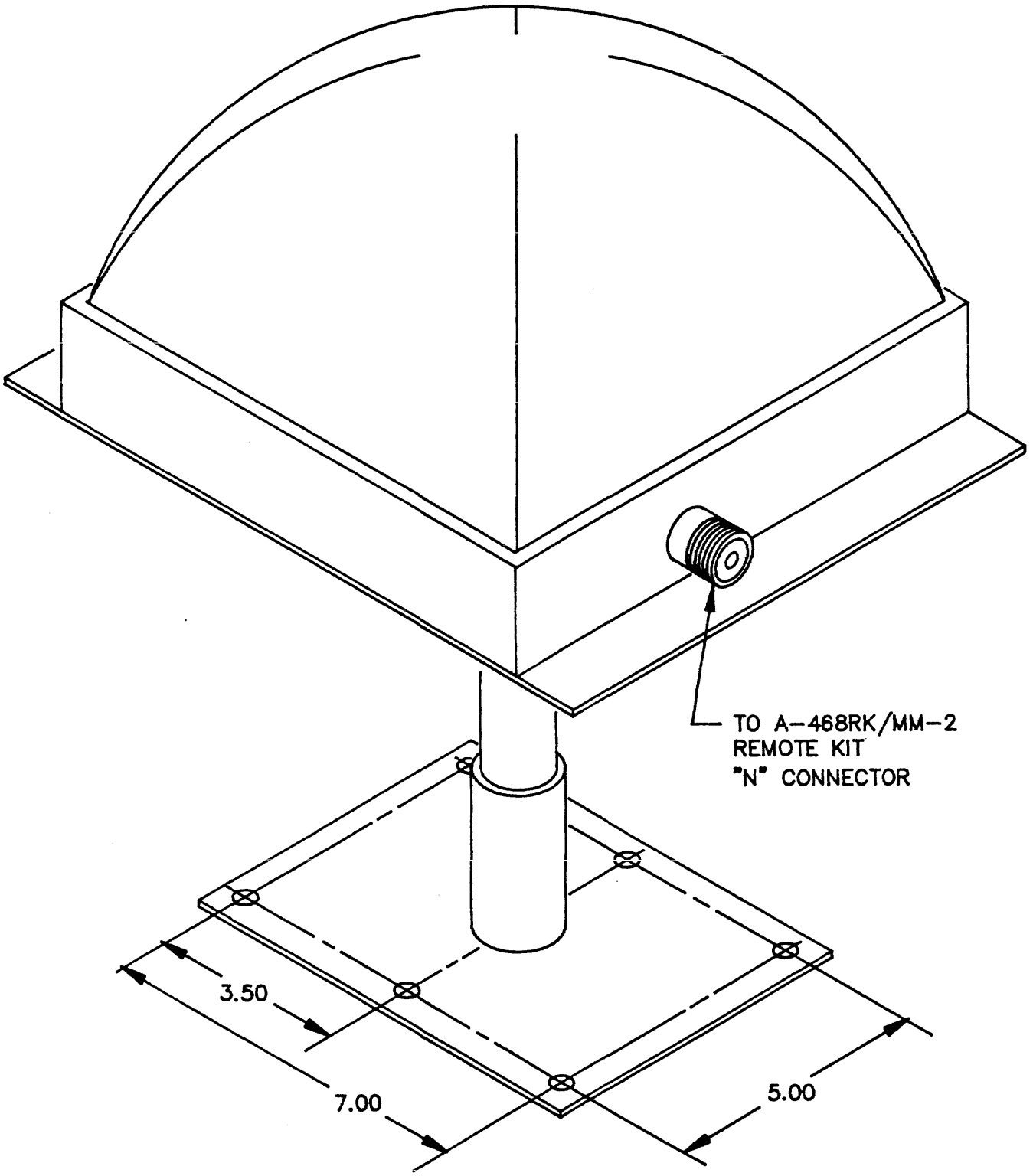
PAGE	DESCRIPTION
1	468-DC/MM
2	A-468MS/ MM
3	A-468RK/MM
4	A-468BP/ MM

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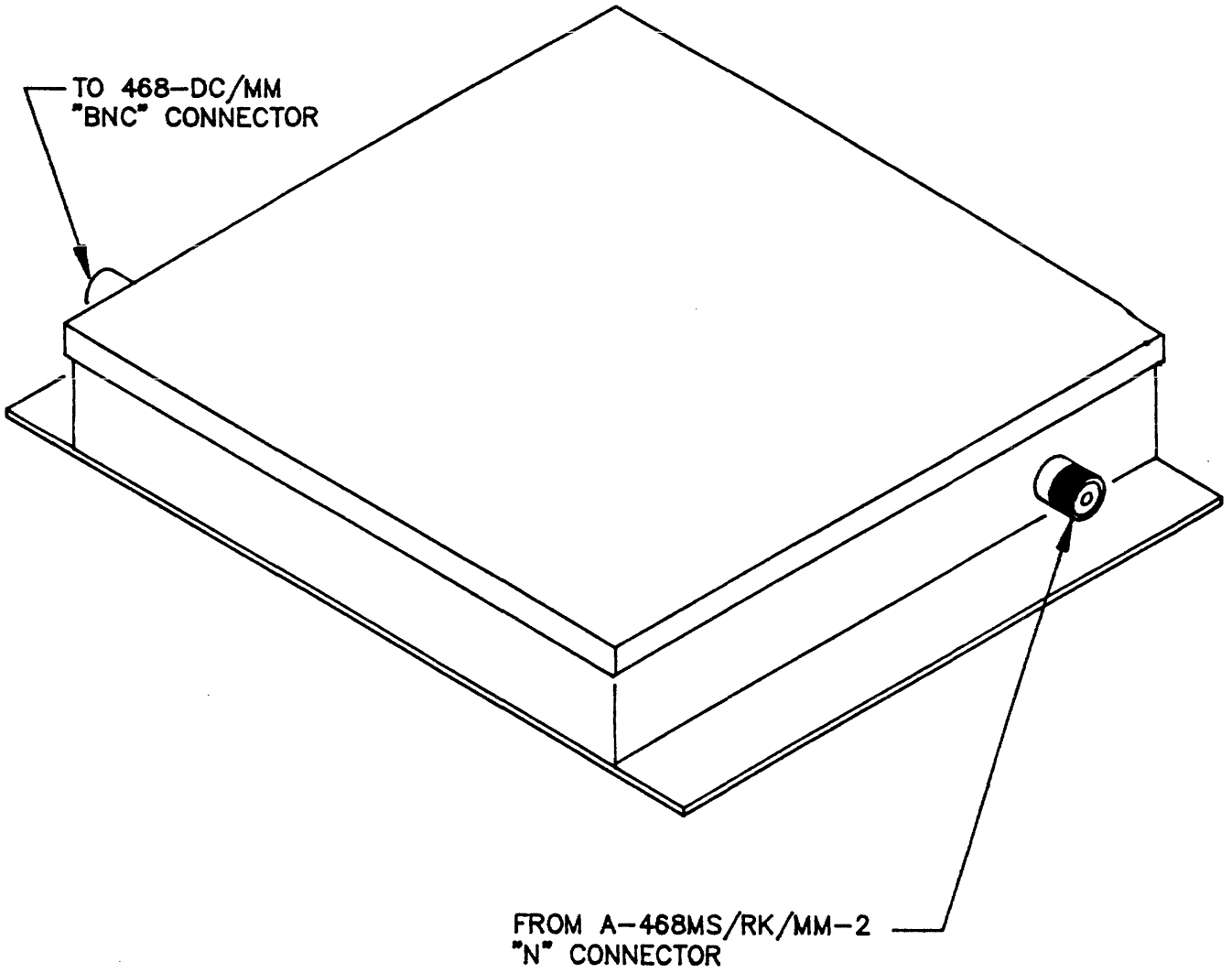
MODEL 468-DC/MM
GOES SATELLITE CLOCK

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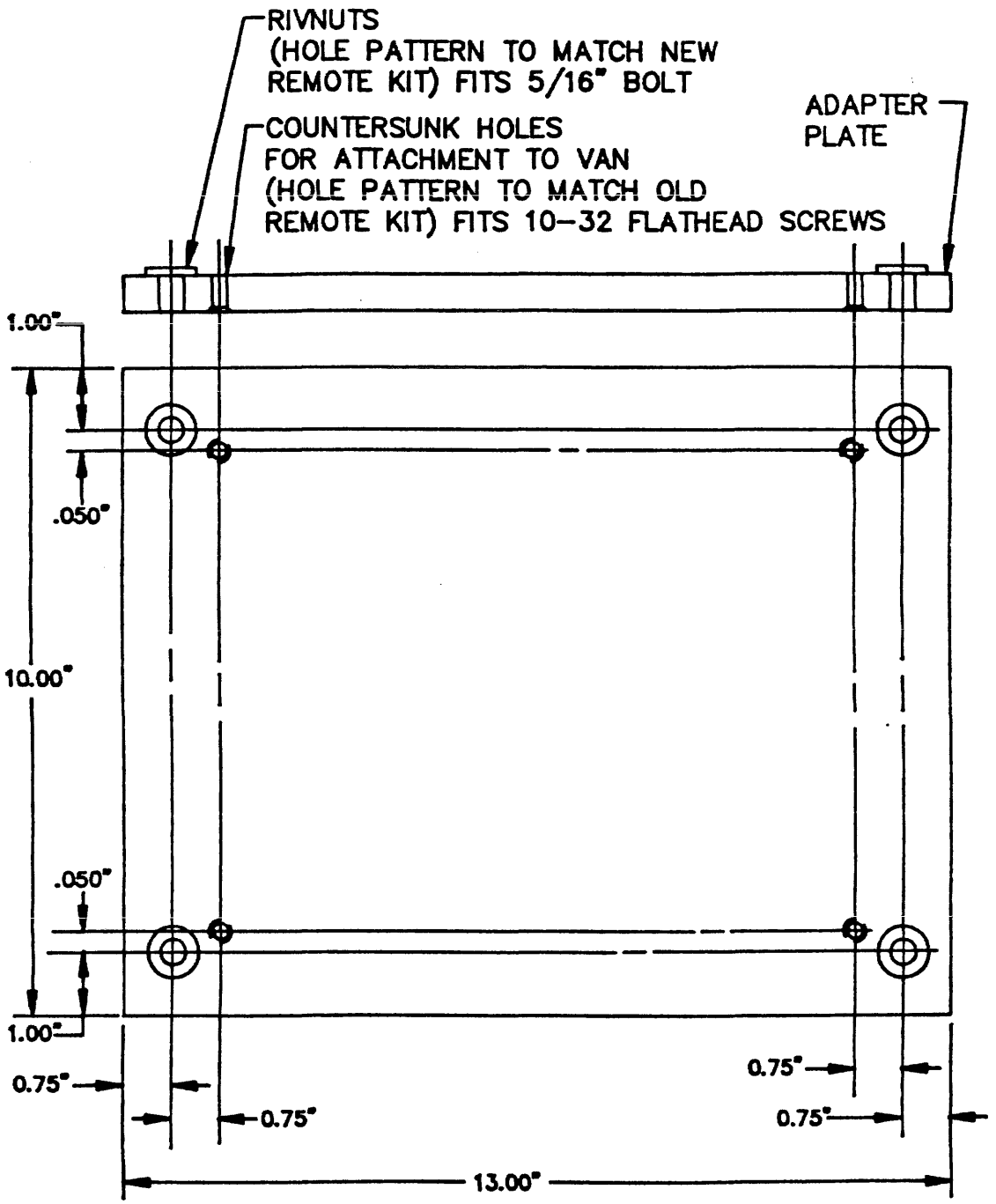
MODEL A-468MS/RK/MM-2
GOES ANTENNA
WITH MOUNTING HARDWARE

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MODEL A-468RK/MM-2 REMOTE KIT

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NOTE: DRAWING NOT TO SCALE

MATERIAL: 1/8" PLATE ALUMINUM, PAINTED

MODEL A-468BP/MM
MK I TO MK II REMOTE ADAPTER PLATE

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SECTION I

GENERAL INFORMATION

1-1 INTRODUCTION

1-2 This manual has been designed and written to provide the owner of the Model 468-DC 'GOES' Satellite Synchronized Clock with all of the data and information needed to operate and utilize all its features.

1-3 The information included in this manual is as complete as possible and includes normal maintenance and adjustment data that may be required to facilitate field repair of the unit.

1-4 The Model 468-DC has been designed to receive the NOAA "GOES" Satellite which transmits on a frequency of 468 MHz and decode the time information from the broadcasts as well as display outputs for supplying the time information to other equipment. The Synchronized Clock in its standard configuration provides a front panel display of days, hours, minutes, and seconds with five rear panel BNC connectors with IRIG B, 1 Hz, 1 kHz, Precision 60 Hz, and Slow Code locked to the electrically outputted time (and options if ordered), may be in either Universal Coordinated Time (UTC), more commonly referred to as Greenwich Mean Time (GMT), or in local time. This is done through the proper time zone offset selected by the rear panel thumbwheel switches. The Model 468-DC is shipped to display the time of year in the twenty-four hour format. By simply removing the cover and switching the position of the small switch on the microprocessor circuit board, the unit can be converted to display and output time in the more conventional twelve hour format.

1-5 This instrument has been designed to be completely automatic requiring only antenna installation and connection of the unit to the power source. Once the instrument is installed and turned on, the microprocessor will lock to the signal from the "GOES" Satellite (either East or West Satellite by sweeping for lock), decode and display the time. From that point on, the unit will require no further attention and will provide time to an accuracy of ± 1.0 ms, continually updated by and phase locked to the transmissions of the "GOES" Satellite. In the event of loss of signal, the unit will continue operation on its internal crystal time base. If power should fail, upon restoration, the unit will again read the time signals and start displaying the time transmitted.

1-6 The Model 468-DC Satellite Synchronized Digital Clock, when using the A-468MS Antenna, is guaranteed to operate at any location within the 5° viewing angle of the satellite as shown on the map enclosed. For viewing angles of 0° - 5° the Model 468-HX should be utilized.

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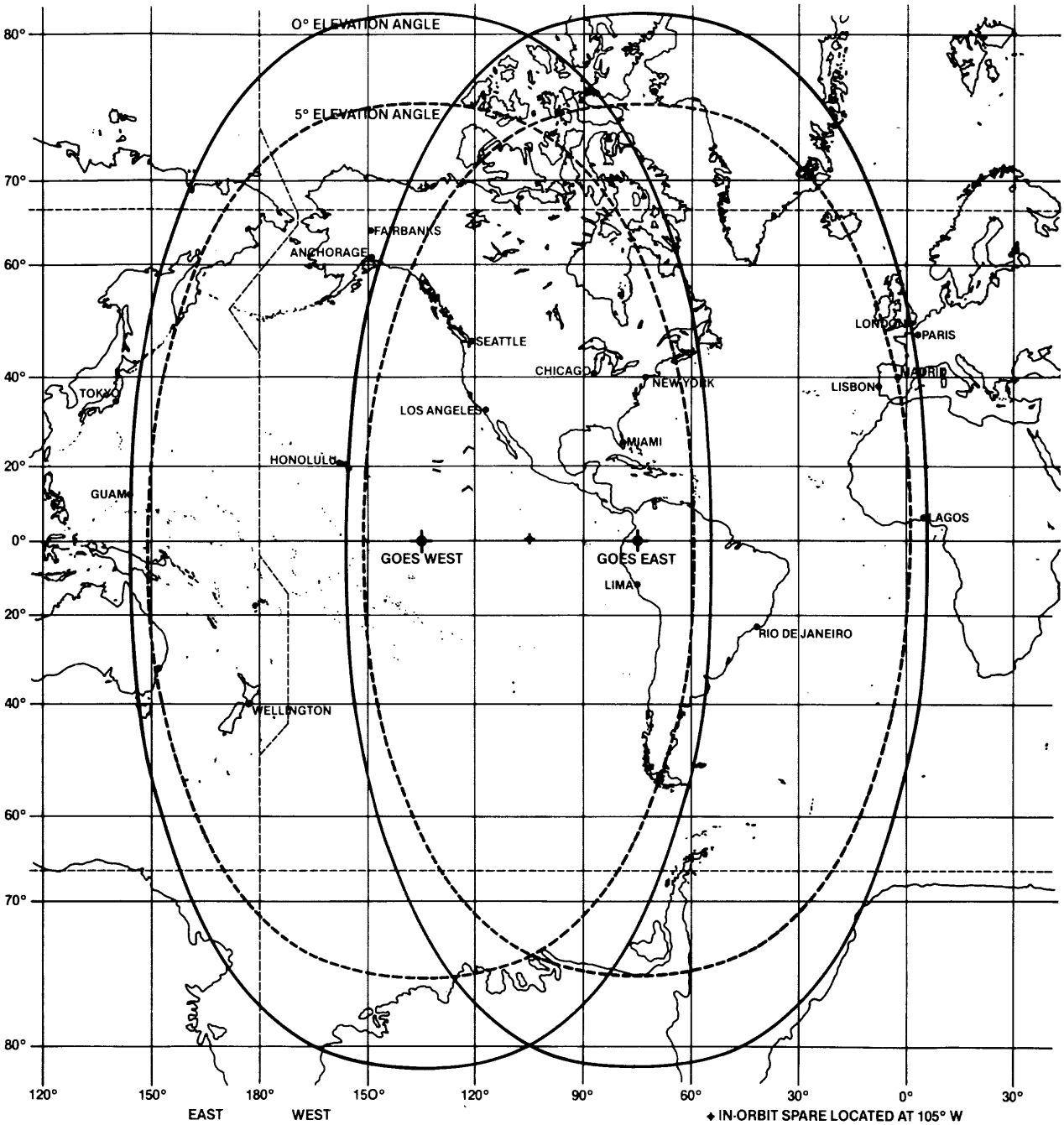


FIGURE 1-1 GOES SATELLITE COVERAGE MAP

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WARRANTY

KINEMETRICS/TRUETIME warrants each instrument it manufactures to be free from defects in material and workmanship for a period of one year from the date of delivery to the original purchaser. Under this warranty, any instrument which is returned to us (freight pre-paid) and is found by us to be defective in material or workmanship will be repaired or replaced (at our option) at no charge to the customer and returned freight pre-paid.

Our obligation under this warranty is limited to servicing or adjustment of any instrument returned. Items not covered by this warranty are: fuses, batteries, and any illuminated parts or damage caused by accident or physical destruction of the instrument.

This warranty is expressly in lieu of all other obligations or liabilities on the part of TrueTime. TrueTime neither assumes nor authorizes any other person to assume for them any other liability in connection with our sales.

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1-8 SPECIFICATIONS

RECEIVER FREQUENCY:	468.8250 and 468.8375 MHz Automatic or Manual select.
SYSTEM SENSITIVITY:	The sensitivity is suitable for proper operation with satellite viewing angle 5° or more above the horizon when using the A-468MS Antenna. (approximately .2uV/m)
SYSTEM NOISE MARGIN:	Operates with 9db attenuator inserted between A-468MS flat plate and preamp input in locations which have a satellite elevation of greater than 15°.
TIMING ACCURACY:	1) ±1.5 ms of UTC/NBS Time when corrected for propagation delay through on-board switches and using the A-468MS Antenna. 2) The time difference between neighboring clocks locked to the same satellite is considerably improved over UTC timing accuracy. Consult the factory for specification and conditions.
PROPAGATION DELAY CORRECTION:	Two internal decade switches provide ±50 ms correction capability in 1 ms steps.
TIME BASE STABILITY:	When not phase locked, crystal controls to ±1 x 10-6. For higher stability time base when not phase locked to satellite, see "External Oscillator Input" Option.
DISPLAY:	1/2" high planar gas discharge. Displays day of year, hours, minutes and seconds.
DISPLAY ACCURACY:	-0 to +100 ms, anytime colons are not flashing.
NOMINAL TURN-ON TIME:	Three minutes from power on and signal reception with 90% confidence under average signal conditions.
OPERATING TEMP:	0° to 50° C.

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REAR PANEL OUTPUTS:

1 Hz:	Rising edge on time, drives ten TTL loads or CMOS. High 10%, Low 90%. See SECTION III, entitled "1 Hz".
1 KHz:	Rising edge on time, drives two TTL loads or CMOS. High 10%, Low 90%. See SECTION III, entitled "1 KHz".
REMOTE DISPLAY DRIVING (IRIG B):	IRIG B Time Code is provided on a rear panel BNC connector. Standard IRIG B Time Code is an amplitude modulated 1 KHz carrier. This output can also be easily field converted to TTL compatible D.C. level shift time code. See Section III, entitled "IRIG-B (REMOTE DISPLAY DRIVING OUTPUT)".
SLOW CODE:	BNC output of 1 pulse per minute (1ppm), 1 pulse per hour (1pph), and 1 pulse per day (1ppd). The pulses go high on time and remain high for 2 seconds for minute mark, 4 seconds for hour mark and 6 seconds for day mark. Capable of sourcing 40 MA at 4.0 volts minimum, and pulled to ground by a 1k ohm resistor. See SECTION III, entitled "SLOW CODE".
60 HZ:	Provided on BNC connector as frequency source to drive a synchronous motor through a power amplifier. Capable of driving 10 TTL loads. The output square wave has an unusual duty cycle. The 60 Hz is a 50% duty cycle over 50 ms (3 cycles). Cycle #1 High 9ms, Low 8ms Cycle #2 High 8ms, Low 9ms Cycle #3 High 8ms, Low 8ms See SECTION III, entitled "60 Hz".
EXTERNAL OSCILLATOR (Option):	Input level of less than 4V and greater than 2.4 volts (TTL) sine wave or square wave is required. Any frequency from 100 KHz to 10 MHz in multiples of 100 KHz is satisfactory. No unit adjustment is needed regardless of frequency. Used as clock time-base when not phase locked to the satellite. See SECTION III, entitled "EXTERNAL OSCILLATOR".

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IRIG H (Option): BNC output of standard IRIG H format TTL DC level shift supplied unless otherwise requested. If 1 KHz amplitude modulated carrier requested, IRIG B will automatically be supplied in D.C. Level Shift format. See SECTION III, entitled "IRIG-H (Special Order Option)".

PARALLEL BCD TIME (Option): If ordered, Parallel BCD time of year is provided on rear panel 50 pin "D" connector. Days, hours, minutes, seconds and milliseconds are provided. Lines indicating worst-case time error of +1, +5, +50 and +500ms drives 15 "LSTTL" loads or 'CMOS'. See SECTION III, entitled "PARALLEL BCD TIME OUTPUT (Special Order Option)".

The High Capacity Parallel BCD drives 100 LSTTL loads.

RS-232 (Option): The displayed time of year is outputted in EIA Standard RS-232C configuration via a "Motorola ACIA". Output format is D D D H H M M S S and an indicator of the time quality, CR/LF. Baud Rate and "ACIA" options are dip switch selectable. See SECTION III, entitled "RS-232 TIME OUTPUT (Options)".

I-MODE (Option): Time can be preset and displayed without synchronization to NBS transmissions.

S-MODE (Option): DAMS/Health Message Software. Assists users of NESS data collection system to check the quality of uplink transmissions.

IEEE-488 (Option): IEEE Buss interface is also available. The time is outputted in ASCII format, with the most significant digit first (100's of days). Among operating modes is time on demand to the millisecond level, or marked time to the milliseconds level. See SECTION III, entitled "IEEE-488 OUTPUT (Option)".

HOURS OFFSET: Rear panel thumbwheel switch allows adjustment of + or - "0" to "11" hours from transmitted UTC time. See SECTION III, entitled "HOURS OFFSET".

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12/24-HR. OPERATION:	Dip Switch located inside unit allows use as 12 hour clock in place of 24 hour format as shipped. See SECTION III, entitled "12/24-HOUR CLOCK OPERATION".

468-DC SYNCHRONIZED DIGITAL CLOCK

SIZE:	1-3/4" x 17" x 10-1/2" (4.4 x 43.2 x 26.7cm) behind panel. Mounts in standard 19" (48.9cm) EIA rack system, hardware included. 24" (60.9) hardware available.
WEIGHT:	7-1/4 lbs. (3.5kg) Ship Wt. 12 lbs. (5.4kg).
POWER (Standard):	96-135VAC, 60-400Hz, less than 25 volt amps. Others available on request.
D.C. POWER INPUT:	When ordered, the standard AC input is replaced with binding posts on 3/4" centers, red is positive, black is negative. Common "Banana Plugs" can be used. Input voltage may be 11 vdc to 32 vdc. Power is approximately 20 watts depending upon option.

A-468MS ANTENNA

SIZE:	10" x 10" high (25.4 cm x 25.4 cm x 30.5 cm).
WEIGHT:	10 lbs(4.5 kg) Ship Wt. 16 lbs.(7.3kg.)

A-468HX ANTENNA

SIZE:	17" x 17" x 43" high (43.2 cm x 43.2 cm x 109 cm) Provided with a universal mounting system and hardware.
WEIGHT:	22 lbs (10 kg) Ship Wt. 66 lbs. (30 kg)

A-468RK DOWN CONVERTER

SIZE:	10" x 13" x 2.4" (2.54 cm x 33.0 cm x 6.1 cm).
WEIGHT:	10 LBS (4.5 KG) Ship Wt. 16 lbs. (7.3 kg).

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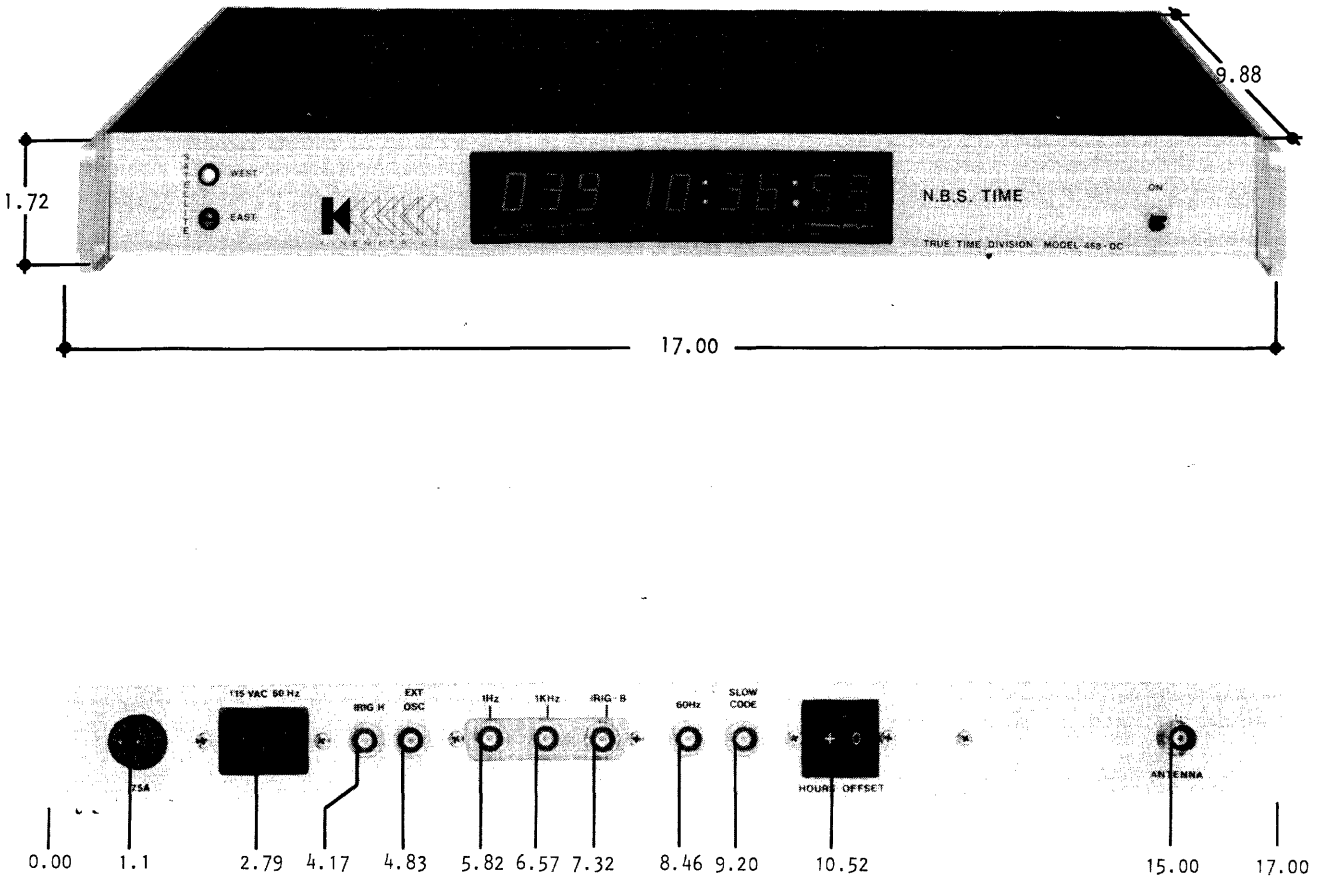


FIGURE 1-2 MODEL 468-DC DIMENSIONS

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SECTION II

INSTALLATION

2-1 ANTENNA INSTALLATION

2-2 The Model 468-DC Synchronized Clock is shipped ready for operation and will require no adjustments. The first step in set-up and operation of the unit is to install the antenna included with the unit. An antenna supplied by KINEMETRICS/TRUETIME for use with the Model 468-DC must be used in conjunction with this receiver/clock as the antenna includes not only a preamp, but receiver controlled frequency conversion circuits. The use of "in antenna conversion" of the 468 MHz frequency to a lower frequency for transmission down the coax allows up to 1000 feet of RG-58/U lead in coax to be used.

2-3 Satellite selection in the Model 468-DC can be either automatic or manual. Maximum time accuracy is obtained in the manual mode where the operator selects either the East or West satellite then sets the propagation delay switches. In the automatic mode the Model 468-DC will try for the East satellite first then the West satellite. If only basic time is required and a change in the received satellite, which can result in a worst case error in propagation delay of 9 milliseconds, is acceptable then the automatic mode can be used and the advantage of automatic scanning is achieved. This scanning allows the receiver to select either receivable satellite in the case of poor or no reception from one. The automatic mode can be used only if a common pointing direction will allow the antenna to receive signals from both satellites. This can be evaluated by the use of the pointing angle maps, FIGURES 2-1 and 2-2. The beamwidth of the A-468MS antenna is approximately 90%. Both satellites can be received by the A-468MS antenna in most areas where there are no obstructions from buildings, trees or mountains. If maximum time accuracy is required with respect to UTC or another 468-DC in the field then either the East or West satellite must be selected, the antenna pointed at the selected satellite, the propagation delay calculated and the internal switches set. SECTION III, PROPAGATION DELAY, gives switch setting instructions.

2-4 Once it is determined which satellite will be received (or if both are to be received) the attached maps can be used to determine the best pointing direction for the users location. In the case of the A-468MS, the antenna should be physically pointed such that the signal from the satellite comes onto the antenna receiving plate through the top of the plastic bubble. The axis of the A-468HX, the Helix, should be pointed at the satellite for best results. Thus, if the user was directly under the satellite, the antenna would be set with it facing straight up. If the satellite was at a 5° angle above the horizon, the antenna must be tipped at 83°.

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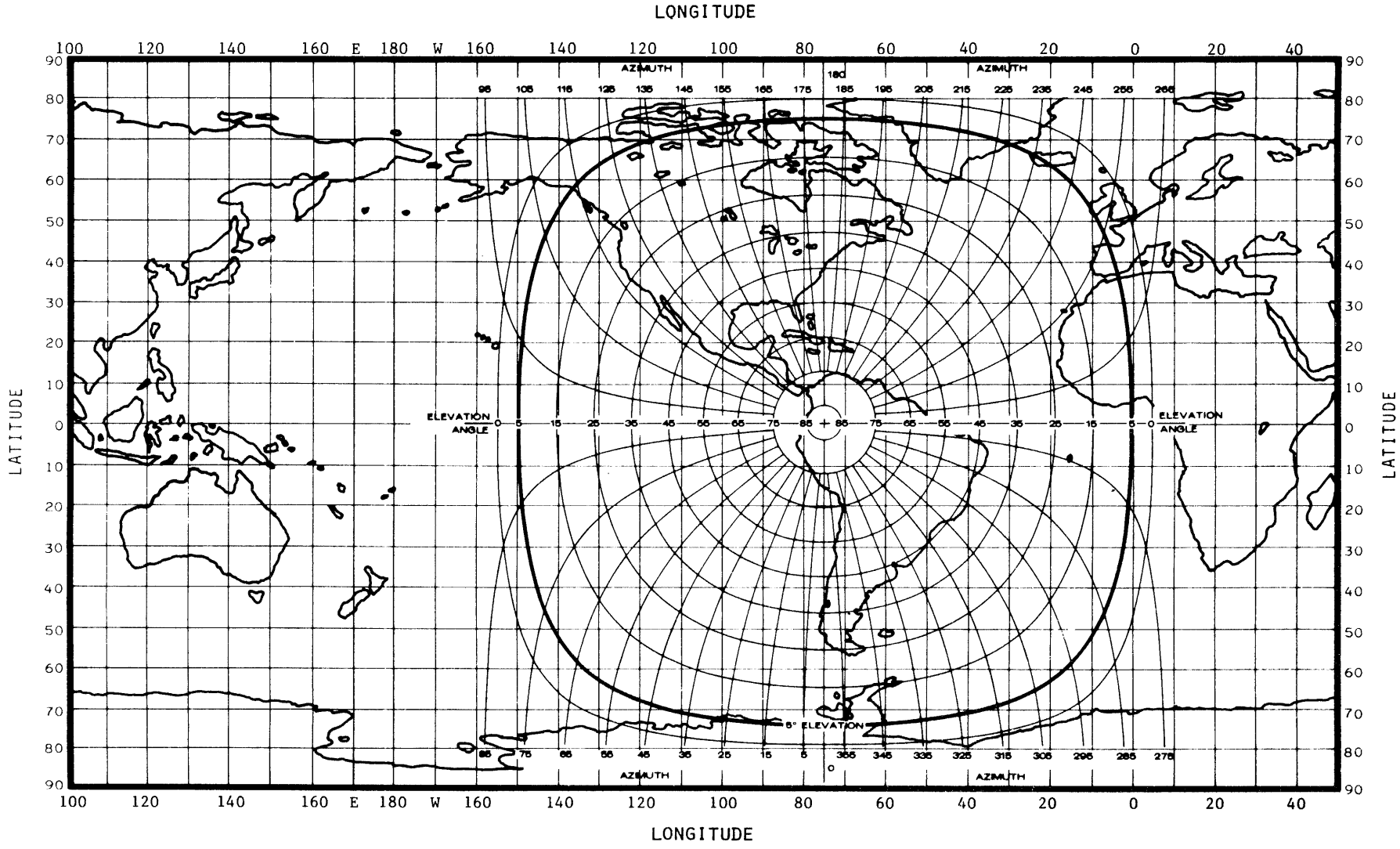
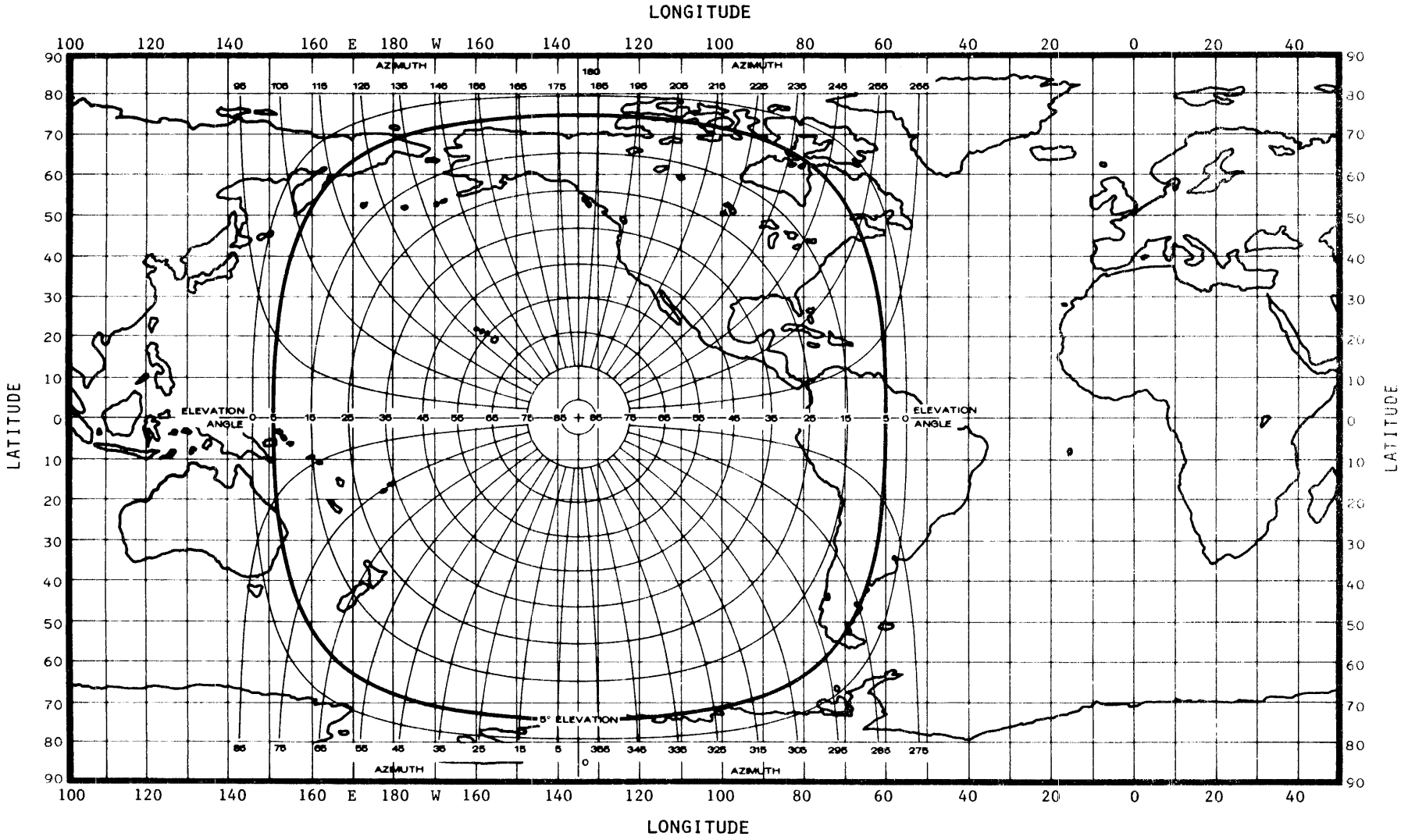


FIGURE 2-1 GOES EAST ANTENNA POINTING ANGLE

EASTERN SATELLITE POINTING ANGLES.

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FIGURE 2-2 GOES WEST ANTENNA POINTING ANGLE



WESTERN SATELLITE POINTING ANGLES.

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2-5 Included with the antenna is a mounting flange with a shaft attached to allow versatile tipping as well as rotation for proper antenna pointing. The stand also allows attachment of this antenna to a flat surface for mounting. See Section VII.

2-6 Once the mounting and pointing of the antenna is complete, attach a lead in coax. For this purpose RG-58/U is available from Kinemetrics/Truetime in 50' and 100' lengths.

2-7 RACK MOUNTING

2-8 If it is desired to mount the Model 468-DC in a standard 19" rack system, use the rack mounting ears provided with the unit. These ears may be attached to the side of the cabinet by removing the two 8-32 flat head screws on the side of the instrument and placing the screws through the counter-sunk hole in the bracket and re-installing the screw. The unit now may be mounted in a 1-3/4" opening in any EIA standard 19" rack system.

2-9 INSTRUMENT START-UP

2-10 After the antenna installation is complete, as described in SECTION II, entitled "Antenna Installation" above, the lead-in coax should be connected to the rear panel BNC connector labeled "ANTENNA". Connect the power cord to the socket on the rear panel and plug the unit into an appropriate power source. The power switch on the front panel may now be turned on.

2-11 When the power is turned on, the initial indication of proper operation of the Model 468-DC is the colons on the display. The colons will blink off and on at about once per second. This indicates to the user that the unit is operating properly and that the receiver is looking for phase lock to the carrier of the signal and then to the 100 Hz data rate of the information broadcast. Next, after the 468-DC has read and recognized the maximum length sequence (MLS) transmitted each 1/2 second, the colons will be locked on solid.

2-12 Following this data lock, the synchronized clock will recognize that it is reading data, a satellite location (as transmitted in the message) will be read. From this information, the 468-DC can determine if it is locked to the "EAST" OR "WEST" Satellite and light the appropriate "LED" on the front panel.

2-13 Finally, after two 30 second long time frames of information of the time of year have been read which agree as to the time, the front panel display will light indicating the correct time of year. At this same time, any options which have been ordered to electrically output the time will begin to function.

2-14 One of the most often overlooked and yet most important factors in the installation and operation of the Model 468-DC is proper antenna installation. Without a proper antenna installation, the signal from the satellite will not be received and thus the unit cannot possibly function properly. In many

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cases "just to try it out", an attempt will be made to operate the unit with the antenna inside a building or without determining the proper antenna pointing angle. This, as often as not, results in inability to lock to the satellite signal, and failure to decode the time.

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SECTION III

OPERATION

3-1 INTRODUCTION

3-2 The Model 468-DC Synchronized Clock provides the user with a means of obtaining time traceable to the U.S. National Bureau of Standards with an accuracy of ±1.5ms. For stability, the time base is phase-locked to the satellite data rate. The time-of-year information broadcast by The National Oceanic and Atmospheric Administration through the "GOES" Satellite is displayed in days, hours, minutes and seconds on the front panel. Also available are outputs of this time information in the form of Remote Display Driving Output (IRIG-B, Parallel BCD Time, or RS-232C compatible interface, or IEEE-488 compatibility). The Model 468-DC has been specifically designed to minimize operator set-up and will provide many years of service without attention.

3-3 SATELLITE EAST-WEST LED

3-4 Located on the lower left hand corner of the front panel are two LED's labeled "Satellite", "WEST" or "EAST". These green LEDs will light anytime the unit is receiving a sufficient signal from one of the satellites to allow the internal time base to phase lock to data frequency of 100 Hz. When the unit is initially turned on, if adequate signal is present, this LED will light within 30 to 45 seconds. If, during the course of operation, phase lock with the satellite is lost long enough for the R.F. Circuits to sweep for phase lock, (about 150 seconds), this light will go out. When phase lock is regained and a satellite position is recognized in the data, the appropriate LED will again light.

3-5 Phase lock will be maintained continually in most areas and the only occasion for loss of lock will be experienced due to local noise interference. The most common source is "land mobile" transmitters on a frequency of 468.8250 MHz which is directly on the Western Satellite frequency.

3-6 The Satellite LED also provides information as to the Satellite position. If the 468-DC is able to read the time of year information but the satellite position informationread in code does not agree with the position shown on the propagation determination maps, (FIGURES 3-1 and 3-2), the LED will blink. If the R. F. carrier on which the time data was found is on the 468.8250 MHz frequency, the West LED will blink, if on 468.8375 MHz, the East LED will blink. This indicates to the user which Satellite is being received, but that propagation delay information may be incorrect and exact satellite position should be determined if accuracies to the millisecond level are desired. Satellite LED blinking also occurs when the unit is in "Automatic" satellite selection, the 468-DC has swept to the other

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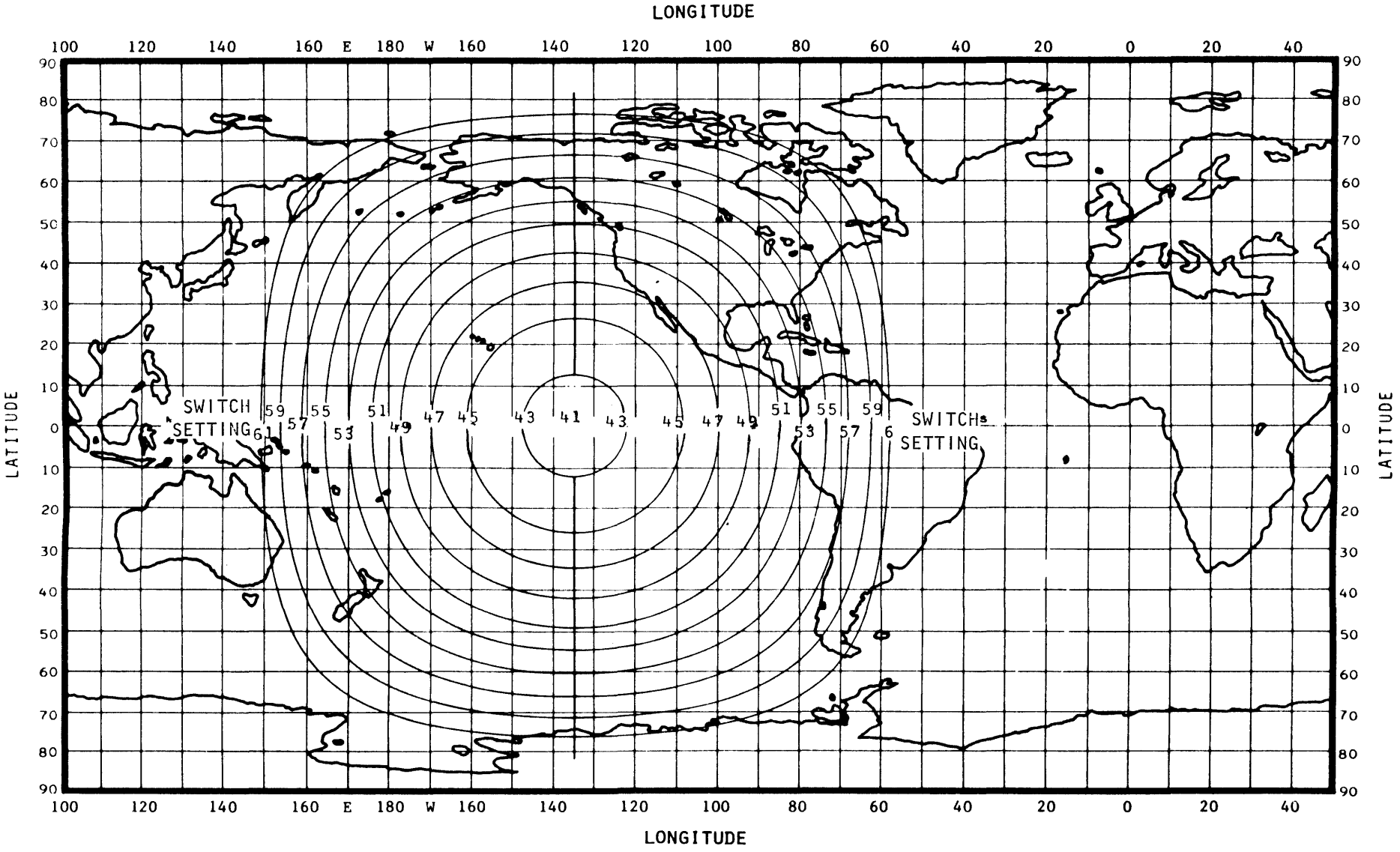


FIGURE 3-1 WESTERN SATELLITE MEAN DELAYS

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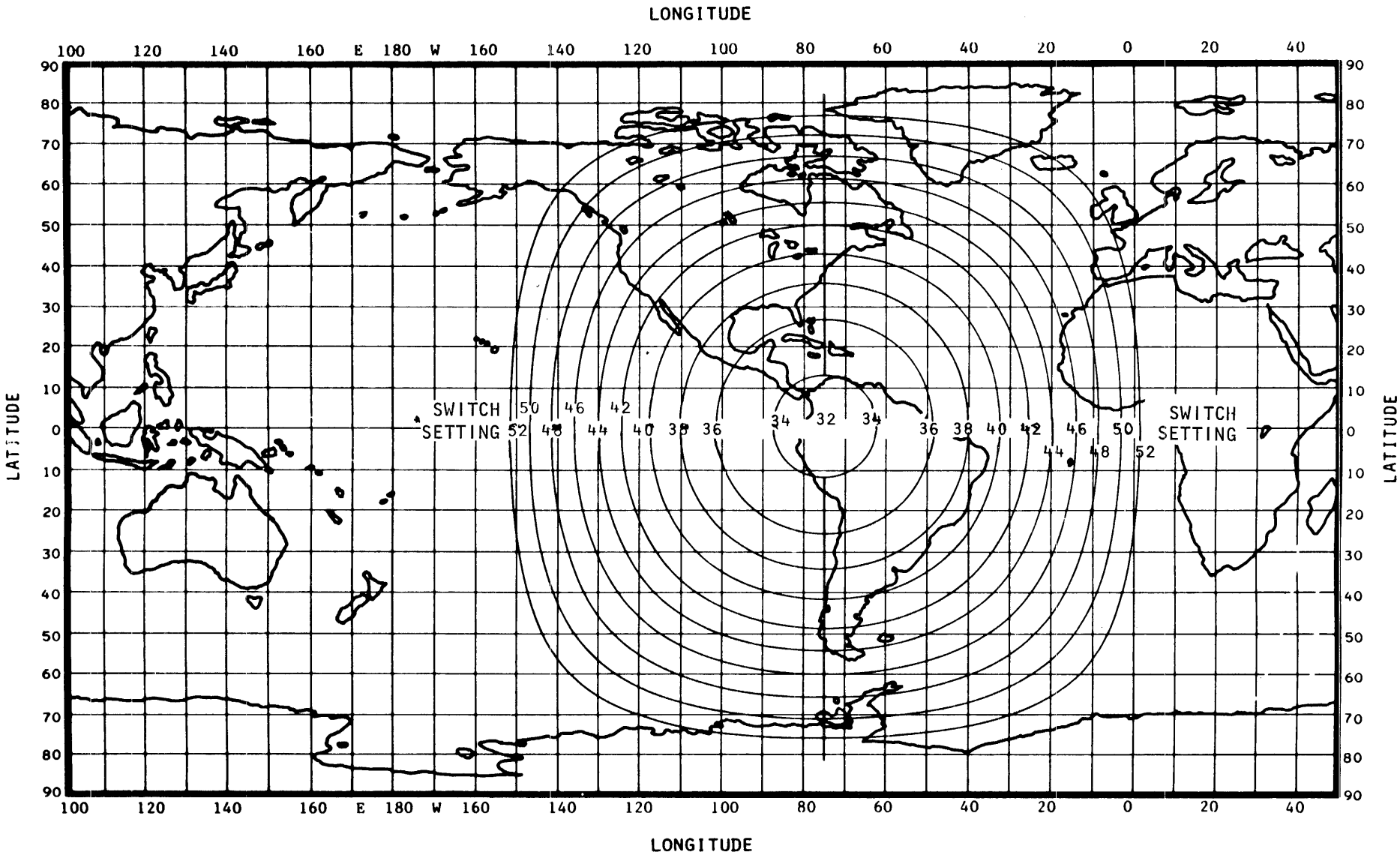


FIGURE 3-2 EASTERN SATELLITE MEAN DELAYS

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satellite, but complete time synchronization is not complete. This usually requires less than 15 minutes to accomplish and then clears the blinking.

3-7 DISPLAY

3-8 The front panel display of time is blank when the unit is initially turned on, because the correct time is not known. The time information broadcast by the "GOES" Satellite is repeated every 30 seconds. The time information is broadcast in the first 11 seconds of each half minute. Requirements for the display to light are: 1) the unit must obtain phase lock with the carrier of satellite, 2) phase lock with the 100Hz data rate must be obtained, and 3) two consecutive frames of time code must be read which agree as to the time. When these three criteria are met, the display will light showing the correct time in days, hours, minutes, and seconds, Universal Coordinated Time (UTC) more commonly referred to as Greenwich Mean Time (GMT). Correction to local time, conversion to a 12-hour clock in place of the 24-hour time base as transmitted and correction for propagation delay are covered in the following sections.

3-9 The display has been designed to indicate to the user the accuracy of the time information being displayed and on the time output lines if ordered. After the display turns on it will indicate the worst case accumulated drift of the time information should phase lock with the satellite be lost. When the unit has accumulated loss of lock for 13.9 hours since the last synchronization to $\pm$5ms., the colons will flash. The flashing colons indicate that the estimate of the worst-case error of the display and outputted time is +50ms. of N.B.S. time. When the unit has been in operation for $\pm$38.9 hours without phase lock since the last synchronization, the complete display will flash. This flashing is certain to attract the operators attention and indicates that the time as displayed and outputted may have a worst-case error of more than $\pm$500ms. (1/2 second).

3-10 Display or colon flashing will stop when the signal from the satellite is regained, phase locked to and the time code is read. Under normal operation this will occur without operator attention. It is very unlikely that either of these conditions will occur under normal conditions. Due to the ability of the unit to phase lock to the carrier frequency down to very low signal levels, persistent flashing of the colons or display may be an indication of poor reception due to local interference or antenna location and/or installation. Refer to SECTION V "Maintenance and Troubleshooting" for additional information on this subject.

3-11 HOURS OFFSET

3-12 Located on the rear panel is a thumbwheel switch labeled "HOURS OFFSET". This switch is set for "0" at the factory which means that the displayed time will be Coordinated Universal Time as broadcast. To change the hours on the display to read

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local time, set the switch to the number of hours your location is offset from Greenwich, England. For example, if you are located in the Eastern Time Zone and desire to display Local Standard Time, the switch should be set for "-5", or for Daylight Savings Time set for "-4". If, in this case, the display was indicating 1800 UTC, the clock would subtract 5 hours and display 1300 hours for Local Standard Time. If the unit has electrically outputted time (IRIG-B, Parallel BCD, RS-232, or IEEE-488), the time supplied on these outputs will agree with the display. Additional information on these outputs is included in the following sections.

3-13 12/24-HOUR CLOCK OPERATION

3-14 The Model 468-DC is shipped from the factory for operation on the 24-hour clock system as broadcast by the National Bureau of Standards. If it is desired to convert the clock to a 12-hour clock display, a small internal switch can be turned.

3-15 To convert a clock to the 12-hour format refer to FIGURE 3-3. Remove the four screws retaining the lid and slide the select switch indicated in the photograph to the 12-hour position. Replace the cover and re-install the screws.

3-16 AUTOMATIC/MANUAL SATELLITE SELECTION

3-17 As described in SECTION II, "ANTENNA INSTALLATION", the Model 468-DC can be used to automatically select the "EAST" or the "WEST" satellite, or can be set manually for lock to either satellite. The receiver, as shipped from the factory, is set for "Automatic" scanning of the satellites. If it is desired to lock the receiver onto either satellite, remove the four screws retaining the lid. By referring to FIGURE 3-1, locate the "EAST" and WEST" Satellite Switch. If it is desired to lock to the East Satellite, turn the "EAST" Switch to "ON", if the 'WEST" Satellite is desired, turn the "WEST" Switch to "ON". With both switches "OFF" the unit will be returned to automatic scanning operation.

3-18 PROPAGATION DELAY

3-19 This feature is included with the Model 468-DC to allow the microprocessor to compensate for the delay in the displayed and outputted time and timing marks due to the time required for the signal to travel to the receiver from the transmitter.

3-20 This feature consists of two switches on the Digital Board Assembly. To adjust these switches, first remove the four screws which hold the top cover in place, remove the lid and set it aside. Refer to FIGURE 3-3 for identification of the "Propagation Delay Switches". The two switches can be combined to provide for a total of 99 ms, propagation delay for the unit. The switch toward the rear panel provides 0 to 9 ms. and the switch toward the front adds to this in steps of ten from 0 to 90 ms. Therefore, if it is desired to compensate for 59 ms. propa-

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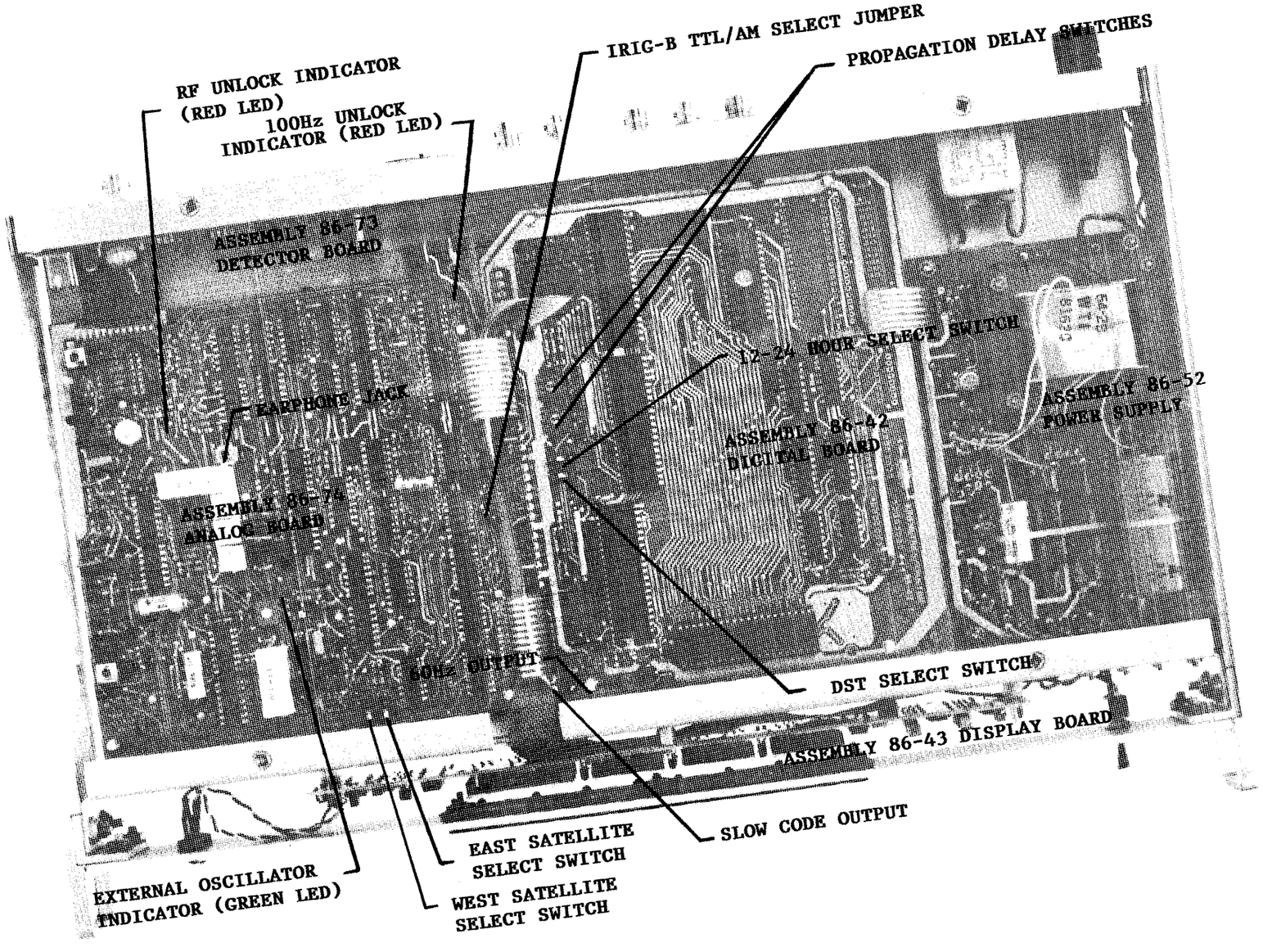


FIGURE 3-3 PARTS LOCATION - MODEL 468-DC

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gation delay, the front switch would be turned to 5 (for 50 ms) and the rear switch to 9 (for 9 ms).

3-21 Through the ground station at Wallops Island, the National Bureau of Standards advances the time sent to the satellite by 260.000 ms. Propagation delay from Wallops Island to the Satellite and back to earth varies between 242.50 and 271.50 ms. depending on satellite position and the receiving location. This results in the receiver signal being advanced up to 17.50 ms. or retarded by 11.50 ms. relative to UTC-NBS depending on receiver location and satellite being received.

3-22 This offset can be compensated for by the propagation delay switches described above. A switch setting of 50 as shipped from the factory, sets the output time of the synchronized clock simultaneous with the received time of the signal. Increasing the propagation delay switch setting advances the output time relative to the received time by 1.0 ms. per step. Thus, a switch setting of 62 advances the time output by 12 ms. as a setting of 32 on the switches retards the output time by 18 ms.

3-23 The appropriate setting of the propagation delay switches can be determined by the use of the attached maps, FIGURES 3-1 and 3-2. If the clock is locked to the "EAST" or "WEST" satellite as described in SECTION III, entitled "AUTOMATIC/MANUAL SATELLITE SELECTION", the delay can be determined relatively accurately. If the unit is left on the "automatic" mode, the best compromise must be determined depending on the receiver location.

EXAMPLE:

1) A user located in the southern tip of Florida, USA and having his unit locked to the "EAST" satellite should set the switches to read 36 ms., "3" on the 10's of milliseconds switch and "6" on the units of millisecond switch.

2) If a unit is located at 120° west longitude and 40° north latitude and left in "automatic" mode, the switches should be set to read 46 or 47 milliseconds at the users option. This would be obtained by setting the 10's of milliseconds switch to "4" and the units switch to "6" or "7".

3-24 1 HZ

3-25 The 1 Hz is provided as a rear panel BNC connector and can be used for a wide variety of timing functions. This output is a pulse going high as the second remains high for 100 milliseconds and going low for the remaining 900 milliseconds. This output is driven from a 2N3904 (Q3) on the microprocessor board (Assembly 86-42, see SECTION V). The collector of Q3 is pulled up to +5VDC with a 3.3K ohm resistor. This output is taken off of Pin #3 of Assembly 86-42 and capable of driving 10 TTL loads.

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3-26 1 KHz

3-27 The 1 KHz rear panel output is similar in form to the 1 Hz above. It is a square wave going high on time, remaining high for 100 microseconds and low the remaining 900 microseconds. This output is driven by U23 on Assembly 86-74 (see SECTION V) which is a CMOS part number 4050. This output is fed to Assembly 86-42 in interconnecting wire(s) and to the rear panel from 86-42 Pin Number #17.

3-28 IRIG B (REMOTE DISPLAY DRIVING OUTPUT)

3-29 The primary purpose of the IRIG-B time code output is to drive slave displays manufactured by Kinemetrics/TrueTime. This output consists of the standard IRIG-B time code. Refer to SECTION VIII for a full description of this code.

3-30 When using this code for other than driving the Kinemetrics/TrueTime Model RD-B, it should be noted that four "Control Functions" are used. These control functions encode estimated time accuracy as fully described in SECTION VII.

3-31 This output is supplied on a rear panel BNC connector. When shipped, this output is in a 1 KHz carrier amplitude modulated format but can be field converted to D.C. level shift code format. In addition to driving remote displays, this output can be used to synchronize commercially available Time Code Generators or direct recording on magnetic tape.

3-32 The modulated 1 KHz format is a sine wave driven by two sections of a Texas Instrument Part Number "TL084" in series with 50 ohm located on Assembly 86-74. The high level of the code is 3.3 volt peak to peak $\pm$0.5V, at the low level it is 1 Volt peak to peak +.2V. This output is fed to Assembly 86-42 via the jumper wire ($\overline{\text{P}}$in Number "P") and to the rear panel from terminal number 18.

3-33 If it is desired to convert the IRIG-B time code from the amplitude modulated 1 KHz form as shipped, to a level shift output, it is necessary to remove the lid and move one wire. To remove the lid, take out the four screws in the cover and set the lid aside. Locate the Analog Board, Assembly 86-74, which can be identified with the assistance of the photograph in FIGURE 3-3 of this manual.

3-34 After locating the Analog Board, Assembly 86-74, note on the right side of the board near the edge a red jumper wire has been installed in two of three holes in a triangular shape pattern. The rear point to which the wire is soldered, labeled "AM", should be unsoldered and swung forward and resoldered into the hold, labeled "TTL" toward the front of the instrument. This connects the lead from the 2N3904 transistor near this hole to pin "P" of the edge connector. Replace the lid and the IRIG-B output will now be in level shift format.

3-35 The Level Shift format is driven by Q100 (2N3904) on

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Assembly 86-74 with 2.2K ohm pull up to +5VDC. This will dr about 10 TTL loads. After leaving Q100, the IRIG-B is transte. red to Assembly 86-42 on jumper wire pin "P" and to the rear panel connector via pin 18 on this assembly.

3-36 SLOW CODE

3-37 The "Slow Code" output from the Model 468-DC has been provided primarily for the purpose of providing timing marks on drum recorders such as the Kinemetrics/TrueTime Model VR-1. This output is a single line which goes high once per minute. On minute marks the output remains high for two seconds, on hour marks the line is held high for four seconds and for the day mark, a six second high is provided.

3-38 This output is driven by Q1 on Assembly 86-42. This is a MPS3702 transistor and will source 40 ma at 4.0VDC. This drive is provided from Pin #2 on the Assembly 86-42 through a wire to the rear panel BNC.

3-39 A second format of this slow code is provided and can be easily field converted. If the wire from Pin #2 of Assembly 86-42 is connected to Pin #1 on the assembly, the complement of Pin #2 described above is provided (see FIGURE 3-3). Pin #1 output is driven by Q2 (2N3904) with approximately 6K ohm pull up to 5VDC. This will drive 2 TTL loads. When wired in this manner, the output on the rear panel BNC will be normally high. On the minute it will go low 2 seconds, 4 seconds on the hour and 6 seconds for a day indicator.

3-40 NOTE: If "External Oscillator" Option is ordered in conjunction with Parallel-BCD, RS-232 or IEEE-488 Output Options, the "Slow Code" Output is not on a rear panel connector but the user is free to lift the lid and obtain this output from Pin #1 or Pin #2 of Assembly 86-42 for use.

3-41 60 Hz

3-42 The precision 60 Hz output on the rear panel BNC, like the Slow Code, has been provided primarily for the purpose of supplying a known 60 Hz signal to drive synchronous motors. This output, when supplied through a power amplifier such as the Kinemetrics Model PA-1, will provide a constant 60 Hz signal for driving drum recorders independent of local power line variations.

3-43 A quasi-square wave is provided for this purpose with transitions on exact milliseconds. The half cycle periods are 8ms, 8ms, 9ms, 8ms, 8ms, and 9ms, etc., then repeating the pattern. This provides exactly a 60 Hz square wave after the average of three cycles.

3-44 Driven by U 11 on Assembly 86-42 (74LS00) this output is capable of driving 5 TTL loads. The output is from the front edge of Assembly 86-42 from a bifurcated terminal labeled "60

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Hz", through a wire to the rear panel connector.

3-45 EXTERNAL OSCILLATOR (Option)

3-46 If optionally ordered, this rear panel input provides for a local lab standard type of oscillator to be utilized as a clock time base during periods when phase lock with the satellite is lost.

3-47 The input frequency for this option may be anywhere between 100 KHz and 10 MHz in increments of 100 KHz. The signal can be a sine wave or square wave with the low level less than 0.4V and the peak greater than 2.4 (TTL). This input is presented from the rear panel BNC through a coax to the input of U 1 (74LS74), which has a 10K ohm pull up to +5VDC. This input therefore is one TTL load.

3-48 Operationally, any time the Model 468-DC is unable to phase lock to the 100 Hz data rate from the satellite, the clock time base will utilize the provided input in the "External Oscillator" BNC connector. If a reference frequency is not provided on this BNC, the 468-DC will continue to operate on its own internal crystal.

3-49 On Assembly 86-74, a green LED has been provided (see FIGURE 3-3) to show the user that the 468-DC recognizes the presence of his External Oscillator. If the LED is not lit, the unit does not recognize the input signal and further investigation will be necessary for proper operation of this option.

3-50 When the situation arises that lock to the satellite is lost, even if a cesium oscillator is used for the External Oscillator, the indications of time drift continue. Therefore, the colons on the display and whole display will blank and flash in the usual manner to indicate loss of satellite reception even in case of a "perfect" external time base. The output time error message in IRIG-B, Parallel BCD, RS-232 and IEEE-488 also function to indicate loss of accuracy.

3-51 IRIG H (Option)

3-52 When ordered, IRIG H is provided on a rear panel BNC. If this is ordered in conjunction with Parallel BCD or RS-232 or IEEE-488, the 1 Hz described in SECTION III is deleted in favor of this output. The 1 Hz is available on assembly 86-42 as described but is not on a rear panel connector. The user can easily open the lid and obtain this 1 Hz if desired.

3-53 The format of the IRIG H time code is covered in Section VIII.

3-54 As shipped from the factory, the IRIG-H code is in DC Level Shift format. This output is provided through a 2N3904 (on Assembly 86-42) with a 3.3K ohm pull up to +5VDC. On request,

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this output can be supplied as a 1 KHz amplitude modulated carrier. In this case, the IRIG-B will be supplied as DC level shift see SECTION III, entitled "IRIG-B (REMOTE DISPLAY DRIVING OUTPUT)". The 1 KHz generation and modulation system, originally used for the IRIG-B, also under "REMOTE DISPLAY DRIVING OUTPUT", will then be used for the IRIG-H, providing a 1 KHz carrier amplitude modulated in IRIG-H format as described in SECTION III, under "IRIG-B (REMOTE DISPLAY DRIVING OUTPUT)".

3-55 PARALLEL BCD TIME OUTPUT (Option)

3-56 The Parallel BCD Time Output option is designed to synchronize other equipment at the time provided by the National Bureau of Standards. This output consists of 42 lines of BCD data from 100's of days to units of milliseconds as shown in FIGURE 3-4. Also included with this option are four lines to indicate the worst case error on the time outputted. Each line has a different error weight, they are: ±500ms, ±50ms, ±5ms and one indicates ±1ms. 1 Hz and 1 KHz lines are available on the output connector which can be used to indicate to the user when the BCD time data on the lines are changing states. If this option is included, a 50 Pin "D" connector will have been installed on the rear panel.

3-57 All of the 42 BCD lines are driven by 74HC244's and are capable of driving fifteen LSTTL equivalent loads. These lines are high (+) to indicate a "1" in that position in the BCD code. The high capacity version of the Parallel BCD Time Output has 74LS244'S as the line drivers. These drivers have the capability to drive 100 LSTTL equivalent loads. For further information regarding the output of these lines and their capabilities, refer to SECTION VI.

3-58 The pin of each output is shown in FIGURE 3-4 on the following page.

3-59 During normal operation, after start-up and synchronization with the Satellite, the four time quality lines will be in a low state. When phase lock with the transmitter is lost, the Model 468-DC will provide the user with a worst-case estimate of the accumulated clock drift based on the VCXO drift rate. This estimate is provided by each of the four lines changing to the high state in turn as the clock time base drifts from synchronization with N.B.S. When the time could be worse than ±1.0ms the output on Pin #50 will go high, at ±5.0ms Pin #14 will go high and on through Pin #17 for worse than +0.5 second accuracy. Each of these lines is driven by an RCA #CD4050 and is capable of driving two TTL loads or multiple CMOS loads. It will be noted that when the +50ms line goes high, the colons on the display will flash and when the ±500ms lines goes high, the complete display will flash.

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PIN #	OUTPUT DATA	PIN #	OUTPUT DATA	PIN #	OUTPUT DATA
1	GROUND	18	2's of 10's of hrs.	34	8's of seconds
2	IRIG B Time Code	19	1's of 10's of hrs.	35	4's of seconds
3	2's of 100's of days	20	8's of hrs.	36	2's of seconds
4	1's of 100's of days	21	4's of hrs.	37	1's of seconds
5	8's of 10's of days	22	2's of hrs.	38	8's of 100's M-sec.
6	4's of 10's of days	23	1's of hrs.	39	4's of 100's M-sec.
7	2's of 10's of days	24	4's of 10's of mins.	40	2's of 100's M-sec.
8	1's of 10's of days	25	2's of 10's of mins.	41	1's of 100's M-sec.
9	1 kHz	26	1's of 10's of mins.	42	8's of 10's of M-sec.
10	8's of units of days	27	8's of minutes	43	4's of 10's of M-sec.
11	4's of units of days	28	4's of minutes	44	2's of 10's of M-sec.
12	2's of units of days	29	2's of minutes	45	1's of 10's of M-sec.
13	1's of units of days	30	1's of minutes	46	8's of units of M-sec.
14	$\pm$5ms. (See Note #3)	31	4's of 10's of sec.	47	4's of units of M-sec.
15	$\pm$50ms. (See Note #3)	32	2's of 10's of sec.	48	2's of units of M-sec.
16	1 Hz	33	1's of 10's of sec.	49	1's of units of M-sec.
17	$\pm$500ms. (See Note #3)			50	$\pm$1.0ms. (See Note 3#)

NOTES: 1) Mating Connector TRW #DD-50P or equivalent.

2) Time accuracy lines in high state indicates time accuracy worse than level specified.

FIGURE 3-4

PIN OUT CONFIGURATION - PARALLEL BCD TIME DATA - MODEL 468-DC

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3-60 When phase lock is regained, the lines will again go low as the unit re-corrects to the proper time. On initial turn-on of the instrument or after a power failure, the ±500ms line will remain in the high state until the display is turned on, thus indicating that the time on the parallel output lines is not correct to the accuracy indicated by the other lines, regardless of their state. This line can therefore be used as a read inhibit line since the data should not be read when this line is in the high state. Refer to the 1 Hz and 1 kHz description below for additional parameters on reading the time of the Parallel Output option.

3-61 The 1 Hz output line on Pin #16 is driven by a #CD4050B and is capable of driving two TTL loads or multiple CMOS loads. This line goes to the high state on time and remains high for 900ms. At any time the 1 Hz line is high, the data on the parallel output lines from the seconds level up is not changing states and is available for reading.

3-62 If it is desired to read the milliseconds lines as well as the seconds through days, the 1 KHz line should be utilized as an indicator that the lines are not changing states. The 800's of milliseconds down to 1's of milliseconds are driven by synchronous counters and may be changing states during the first 1/2 microsecond of any millisecond.

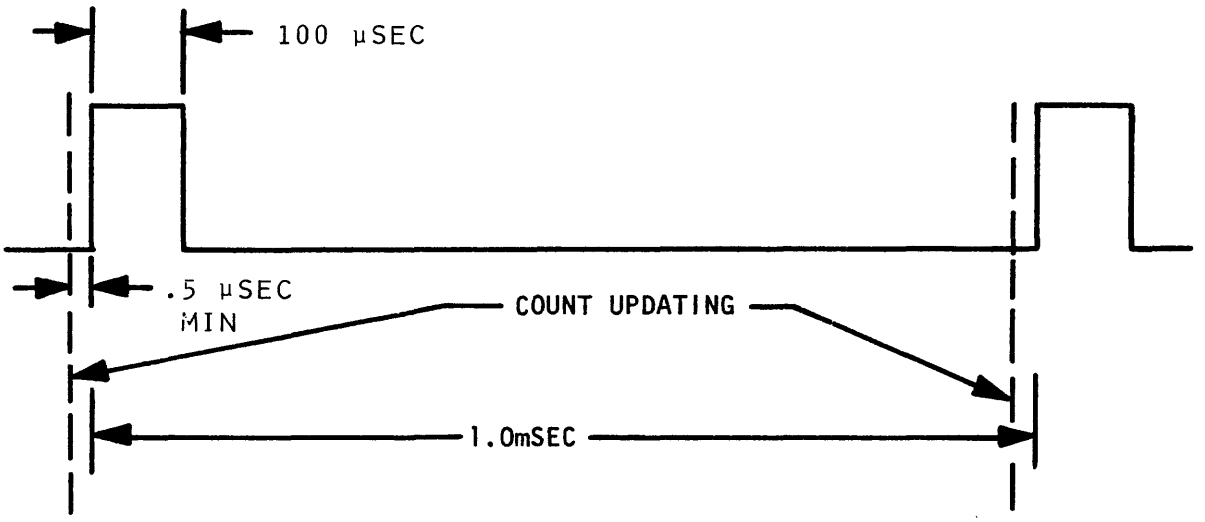
3-63 The 1 KHz line is driven by a #CD4049B and is capable of driving two TTL loads or multiple CMOS loads. The 1 KHz output can provide information to the user in two formats. The first format is as shipped from the factory. The second output format can be converted to in the field by two simple internal modifications. See FIGURE 3-5.

3-64 As supplied from the factory, the 1 KHz output on Pin #9 of the "D" connector goes high on the millisecond for 100 microseconds and then goes low for the remaining 900 microseconds. Since the state of the Parallel Output Time data may be changing state during the first 1/2 microsecond of any millisecond, the transition from the low to the high state has been delayed to allow the milliseconds counter to stabilize. The rising edge of the 1 kHz signal may be used as a Data Strobe. If, rather than one point in time, a time period of when it is "OK" to read is desired, the time period starting at the rise in level of the 1 KHz line and continuing for the next 500 microseconds can be used. This 1 kHz line should be used in conjunction with the ±500ms line as described above to determine if the time data is correct and readable.

3-65 The second format for the 1 kHz output line will provide an output which will go to the high state approximately 3.0 microseconds before the millisecond and low 2 microseconds later. This line will not go to the low state if the estimated time error of the instrument is worse than ±500ms and will also stay in the high state after initial turn-on until the data on the parallel output lines are correct. This line, therefore, pro-

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FIRST FORMAT (AS SHIPPED FROM FACTORY)



SECOND FORMAT (FIELD INSTALLABLE OPTION)

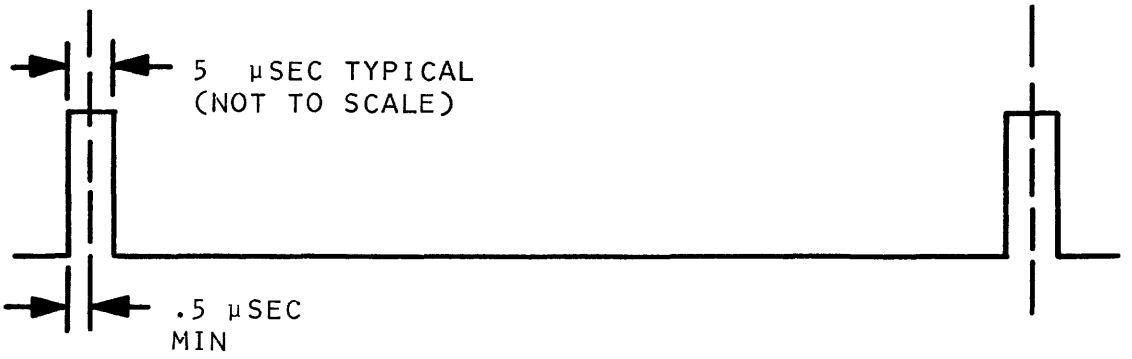


FIGURE 3-5 MILLISECOND COUNTER TIMING DIAGRAM 1 kHz SIGNAL SHOWN (PIN #9 OF OUTPUT CONNECTOR)

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vides one line which,when in the low state, indicates that the time data is "OK" to read. To convert the Model 468-DC to this configuration on the 1 KHz line, remove the bottom cover of the instrument and locate Assembly 86-44. For identification of this Assembly and its parts, see FIGURE 3-6 of this manual. Locate the jumper wires (looks like a 1/4 watt resistor with one black band) labeled JPR3. Unsolder the end connected to the hole labeled "A" and solder it into the hole labeled "B". Unsolder the jumper marked JPR2 and remove it from the board. In the place of JPR2, solder in a 33k ohm resistor (1/4 watt ±5% carbon resistor preferred). Replace the cover and the screws: the conversion is now complete.

3-66 RS-232 TIME OUTPUT (Option)

3-67 The RS-232 Time Output option, available on Model 468-DC, provides time communication to the user via a bi-directional asynchronous RS-232 port. The output is compatable electrically and mechanically with the E.I.A. Standard RS-232C as described for a data terminal. Thus, the rear panel connector is a Cannon #DBP.25PAA or equivalent. Messages are sent and received using ASCII coded characters in most standard data rates and formats.

3-68 Units supplied with this option have a rear panel mounted 25 pin "D" connector with the following pinout:

PIN #	DESCRIPTION
1	Chassis Ground
2	Transmitted Data
3	Received Data
4	*Request to send (internally connected to #5)
5	*Clear to send
6	Not Used
7	Signal Ground
8-24	Not Used
25	*Remote Display Driving (IRIG B)

* These are non-standard connections which are nonetheless compatible with most data terminal equipment.

3-69 The unit as shipped is set for a baud rate of 300, odd parity, one stop bit, and a word length of 8 bits. If it is desired to change these functions, it will be necessary to remove the bottom cover. Remove the four screws which hold the bottom lid on, remove the lid and set it aside. Located on this board are two eight position switch assemblies. One assembly is for the baud rates of 110 to 9600 and the other is to set the parity, number of stop bits, the work length, and other functions as described in the "NOTES" section, See FIGURE 3-7.

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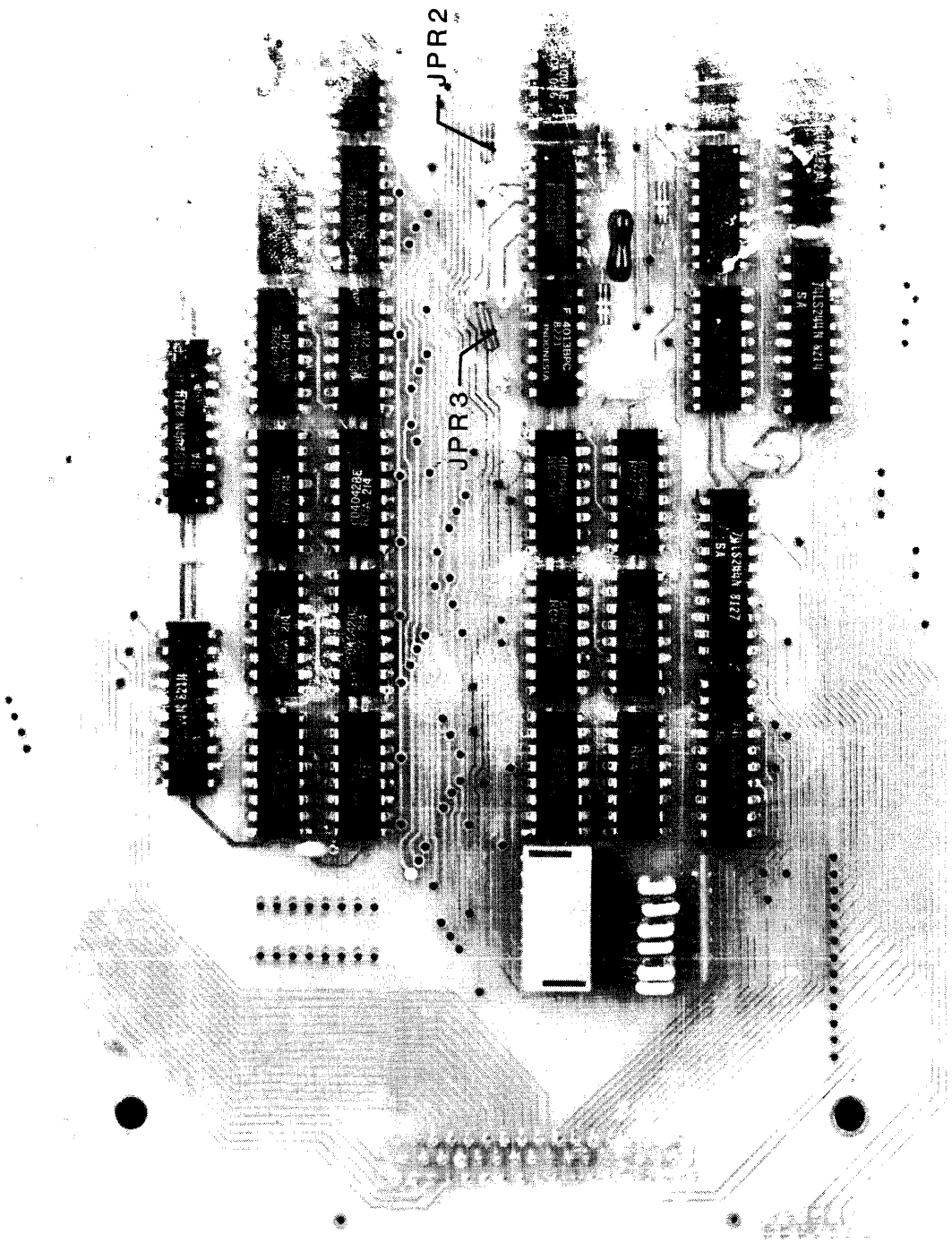


FIGURE 3-6 PARTS LOCATION - PARALLEL BCD OUTPUT OPTION

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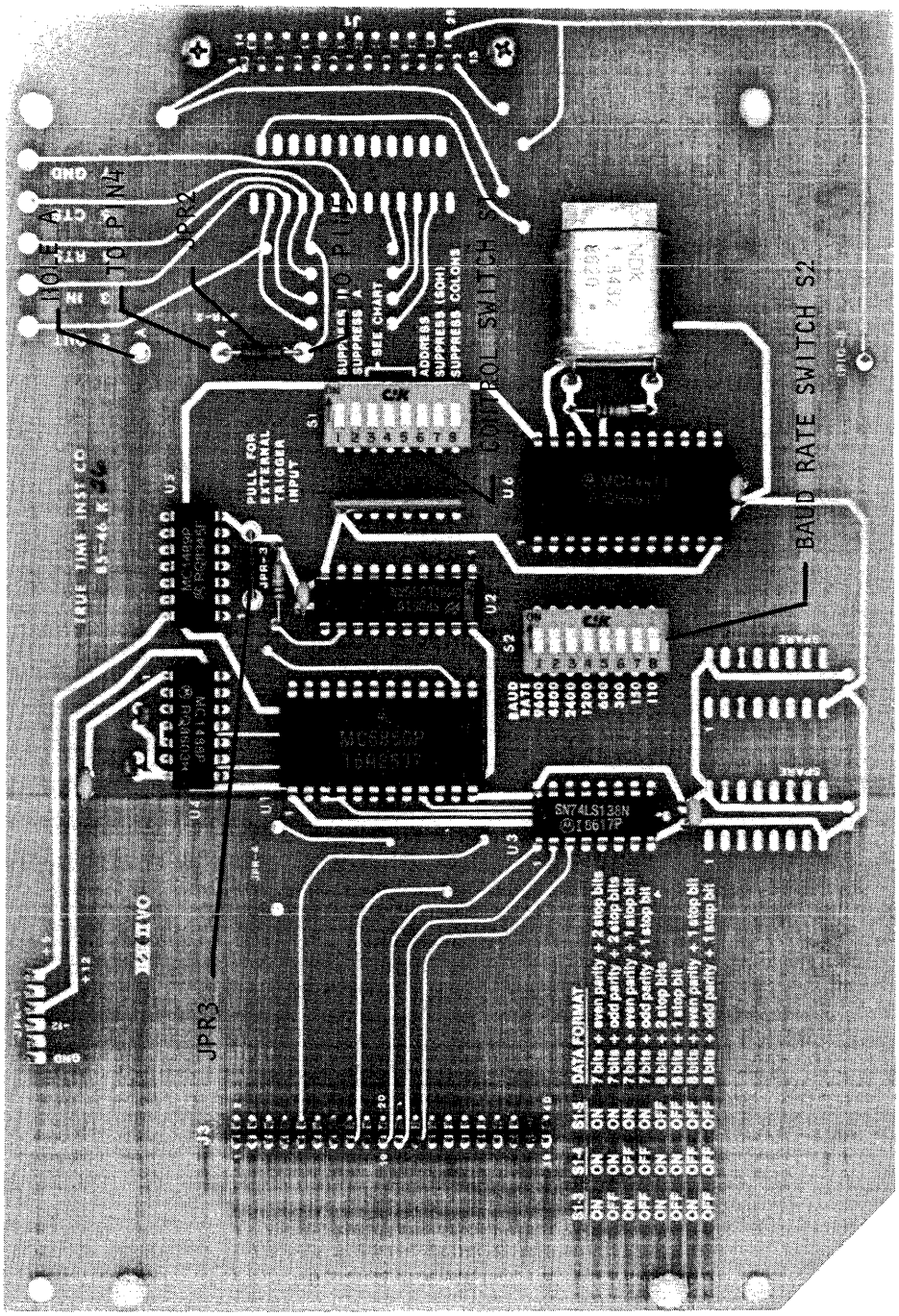


FIGURE 3-7 PARTS LOCATION - RS-232C OUTPUT OPTION

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3-70 The baud rate switch as shipped from thefactory is set for 300, to change the rate simply slide that switch to the off position. Select the desired rate and slide the appropriate switch to the "ON" position. Energize only one switch position at a time.

3-71 Format selection of the parity (odd or even), number of stop bits (1 or 2) and the word length (7 or 8 bits) can be accomplished by the use of the second eight position switch assembly.

PARITY ODD-EVEN	NO. OF STOP BITS 1 - 2	WORD LENGTH 7 - 8	FORMAT
ON	ON	ON	Even Parity + 2 Stop Bits + 7 Bits
OFF	ON	ON	Odd Parity + 2 Stop Bits + 7 Bits
ON	OFF	ON	Even Parity + 1 Stop Bit + 7 Bits
OFF	OFF	ON	Odd Parity + 1 Stop Bit + 7 Bits
ON	ON	OFF	2 Stop Bits + 8 Bits
OFF	ON	OFF	1 Stop Bit + 8 Bits
ON	OFF	OFF	Even Parity + 1 Stop Bit + 8 Bits
OFF	OFF	OFF	Odd Parity + 1 Stop Bit + 8 Bits

3-72 Electrically, the levels of the outputted ASCII code are per EIA Standard RS-232C as available from Electronic Industries Association, Engineering Department, 2001 Eye Street, N.W., Washington, D.C. 20006. This reference is suggested for any user of this system as it is the industry accepted standard for this interface system.

3-73 With the RS-232 output option, several modes of operation are possible. When the clock is initially turned on, the RS-232 option automatically defaults to the once per second output mode of operation. Refer to MODE C, in SECTION III. The RS-232 output option will always (exceptions as in SECTION III, note #4, Position 6.) stay in its then current mode until one of the ASCII control characters (C, T, F, M, P, R, U, I, S) is received to override the previous command. Below is a description of these modes.

MODE	DESCRIPTION
C	Transmission of the time once each second.
T	Transmission of the time on request.
F	Selection of the format for the time message.
M	Transmission of a mark signal at a pre-programmed time.
P	Transmission of the current satellite position.
R	Reset Mode, which resets the format to the "Default Format" and then goes automatically to Mode C.
U	DUT_1 Mode, transmits the DUT_1 as sent by NBS
I	(Option) Display time without synchronization to NBS signals.
S	(Option) DAMS/Health Message software. See standard MODE S description at the end of SECT. III

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3-74 RS-232 MODE DESCRIPTIONS

3-75 MODE C

3-76 When the clock is turned on, the RS-232 option automatically defaults to the once per second output mode of operation in a format as described below:

(CTRL A) DDD:HH:MM:SS Q (CR) (LF)

WHERE: DDD is the 3 digits representing day of year
HH is the 2 digits representing hours
MM is the 2 digits representing minutes
SS is the 2 digits representing seconds
Q is a time quality indicator

The time quality indicators are:

?	indicates a possible error of ±500 milliseconds
#	indicates a possible error of ±50 milliseconds
*	indicates a possible error of ±5 milliseconds
.	indicates a possible error of ±1 millisecond
SPACE	indicates a possible error of less than 1 ms

3-77 When in Mode "C" the carriage return (CR) start bit begins on the second, +0 to 1 bit time. If the maximum timing precision is desired from this output, it is recommended that Mode "M" be used. See the "MODE M" section.

3-78 See Notes 1 and 2, in the "NOTES section.

3-79 MODE T

3-80 When a "T" is received, the time as of 9 bits after the center of the start bit (of the received "T" character) is saved in a buffer. It is then immediately outputted in the current format. No further data is outputted on the RS-232 interface until receipt of one of the valid command character sequences.

3-81 A mode similar to Mode "T" can also be initiated by an external trigger. When the external trigger is used, the current time is noted when the "Clear to Send" line (Pin #5) goes low (TTL or RS-232 levels). No further action occurs until "Clear to Send" goes high, at which point the stored time is outputted in the current format. The unit then awaits further instructions.

3-82 Since this external trigger takes precedence over the other modes, it is normally locked out by a jumper wire on the option board. If it is desired to use this mode, remove the bottom cover of the instrument. The printed circuit board, with the parts facing you, is the RS-232 option card. See FIGURE 3-7. Cut out or unsolder the jumper labeled "Trigger Mode". This mode is now in operation. Remember when this jumper is cut, the external trigger takes precedence over all other modes and all other normal commands are locked out whenever "CTS" is held low.

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3-83 It may also be desirable to remove the jumper at the rear edge of the circuit which connects the "Request to Send" and "Clear to Send" lines together (Pin 4 and 5). This will not affect the operation of the output option but may have an effect on other equipment in the system.

3-84 MODE F

3-85 After an "F" is received, the unit is placed in the "Format Mode", awaiting a time message format string. This format string consists of a 17 character dummy time message consisting of day-of-year through time quality character. As each character is received it controls its respective position in the output format. An "S" in any position suppresses the output of its respective position. In the delimiter positions, any character received for that position will be outputted. In the other non-delimiter positions, any character other than "X" or any of the ASCII control characters, (see Section 3-73), since the clock will see them as a command, allows that position to be outputted as understood by the clock's time system. Be certain not to use an "M" as the unit will see this as a mode change command to Mode "M". The format can be selected within the limits of the maximum format described below:

(CTRL A) DDD__HH__MM__SS__SSS Q (CR) (LF)

3-86 Each __ represents a single delimiter position which can be almost any ASCII character, typically colons, a decimal point, etc.

3-87 This format will now be the format of the outputted time. It should be noted that the milliseconds are not available in Mode "C", even if so formatted.

EXAMPLE:

If the option receives: F 123/12:34:56.789Q, the result will be printing a slash between the days and hours with colons separating hours from minutes and minutes from seconds. A decimal point will be in the seconds between the seconds and hundreds of milliseconds. This string will be preceded by (CTRL A) and followed by a time quality indicator (Q) and (CR) (LF).

Secondly, if F XXXXXXXXXXXXX124X is received, the result will be printing only the fractional part of the seconds, preceded by (CTRL A) and followed by (CR) (LF).

As a check of the entered format, the current time will be sent in the new format after the completion of the 17 character format string.

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3-88 MODE M

3-89 This mode allows the user to preset a time in the future and to be notified when this time occurs. An "M" followed by the desired alarm time presets the time into the unit. The desired time is then echoed, and then the option waits for that time to occur. When the desired time occurs, an "M" is sent (this may be suppressed by the dipswitch position 1 on the option board - See Note 4 in the "NOTES" section.

3-90 As a second indication that the alarm time is present, the unit can be converted to pull Pin #4 low during the alarm time. This is done by moving the jumper connector Pin #4 to Pin #5, to connect Pin #4 to hole "A". See FIGURE 3-7. When this change is made, Pin #4 will be held low through the alarm time and high otherwise. This form of time indication is suggested when the user desires the highest possible time precision from the RS-232 output on the Model 468-DC.

3-91 When one inputs the string for the alarm time, all the delimiters must be included for place holding. An "X" in any position makes that digit a "don't care" digit. If a "Line Feed" is placed in any position, this terminates the string and sets successive set time digits to 0, otherwise all 16 characters including the milliseconds digits of the time must be sent.

EXAMPLE:

M185*11:06:04.387

This would trip the alarm feature at 11:06:04.387 on the 4th of July and an "M" would be sent. If the request to send line had been converted as described above, this would be held low for that millisecond.

M185*11:XX:XX.XXX

This would transmit an "M" at eleven o'clock on the same day and the request to send line would stay low for the hour (through 11:59:59.999).

MXXX*XX:XX:XX (LF)

This input alarm configuration would provide for an "M" at the start of each second and the "Request to Send" line would be held low for one millisecond.

3-92 MODE P

3-93 When ASCII "P" is received on the Model 468-DC, the current position as received from the "GOES" Satellite will be outputted.

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An example of the format is:

13523+013+062

Where in this example:

13523 Represents the longitude of 135.23°

+ can be + or -

013 represents the latitude of +0.13°

+ can be + or -

062 represents +62 microseconds difference in the radius of the satellite from the nominal position

3-94 MODE R

3-95 This mode, when used, is similar to the initial turn on sequence of the instrument. When "R" is received, the unit automatically goes to the "default format" and into Mode "C".

3-96 The initial output string, after an "R" command is received by the synchronized clock, is not reliable either asto data, time or carriage return. This is due to internal sychronization with the data rate. This is also true when the baud rate is changed in the "R" and "C" modes.

3-97 NOTES

1. (CTRL A), (CR) and (LF) are the ASCII characters 01, OD, and OA in hexadecimal form. They are not under format mode control. (CTRL A) is also known as a start of header.

2. During output, Transmissions are continuous, with the end of the top bit of one character coinciding with the beginning of the start bit of the next character.

3. The RS-232 output option will stay in the current mode it is in (default mode at turn on) until one of the valid ASCII control characters (C, T, F, M, P, R, U, I, S) is received to override the previous command.

4. As described in the previous sections of this manual, the dip switch on this option printed circuit card has several functions. The positions and the functions they control are:

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POSITION	FUNCTION
1	Output of an ASCII "M" at the present time, as programmed by Mode M, is suppressed when "ON".
2	NOT USED
3	Parity
4	Number of Stop Bits
5	Number of Data Bits
6	NOT USED
7	Suppress (CTRL A) in default format when "ON"
8	Suppress colons in default format when "ON"

5. Input and output is via an MC6850 ACIA. Refer to manufacturer's (Motorola) data sheet for further information.

6. Effective spring of 1984, the National Bureauof Standards began including extended satellite position data and parity error information for the purpose of providing users with a higher degree of timing precision with respect to UTC. This data is accessible through the use of ASCII control characters "E" and "S". These new modes function in the following manner:

3-98 MODE U - DUT_1 MODE

3-99 When the Model 468-DC receives a "U" over the RS-232 interface, the response will be the current correction to UTC-NBS to obtain UT_1. This correction is transmitted via the GOES Satellite Time Code and is referred to as DUT_1. The RS-232 message consists of 3 items.

1) Sign of correction
2) 3 digit correction in milliseconds
3) (CR) (LF)

3-100 The sign is a "+" or a "-", indicating that the correction must be added to or subtracted from UTC-NBS to obtain the proper value for UT_1.

3-101 The 3 digit correction is normally transmitted as an integral number of hundreds of milliseconds, such as +400. Thus the last two digits should always be zero.

3-102 Four question marks (????) will be transmitted if successive transmissions of DUT_1 do not agree.

3-103 A complete description of the information transmitted by WWVB is described in SECTION IV.

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3-104 MODE E

3-105 When an ASCII "E" is received on the 468-DC, the current satellite position with the extended resolution will be output.

An example of the format is:

123.4567+1.2345-123.4

Where in this example:

123.4567	Represents the longitude of 123.4567 degrees
+	can be + or -
1.2345	Represents the latitude of + 1.2345 degrees
-	can be + or -
123.4	Represents -123.4 microseconds difference in the radius of the satellite from the nominal position.

3-106 I-MODE (Option)

3-107 This option is intended to permit the user to preset the clock to any desired time, without waiting for the clock to automatically synchronize to N.B.S. time. Once preset, the clock outputs will function normally as if N.B.S. sync has been obtained. If an antenna is connected, switchover to N.B.S. time is either automatic or under user control at the user option.

3-108 While the preset time is being output, two indications are provided to alert the user: the time quality character over the RS-232 link to set to "°" and the front panel display is modified; on 468-DC the two satellite indicator LEDS are alternately illuminated.

3-109 An attempt to set the clock after N.B.S. sync has been obtained will result in the response "DO YOU REALLY WANT TO PRESET THE TIME ?" Any answer other than (Y)ES will abort the attempt. A (Y)ES answer will restart the clock as if the power had been interrupted. At this point another "I" will allow presetting the clock, without the previous question.

3-110 To set the time, send an "I" to the clock, followed by the desired preset time in the format DDD:HH:MM:SS. This input line can be edited using a backspace (control H). All characters to the right of the correction made must be re-entered after the correction. When the input line is correct, carriage return enters it into a temporary buffer, and echoes the time for verification. This echoed back time has been examined for valid upper and lower bounds. A question mark (?) will be placed in any location that is not valid. As an example 432:13:10:11 would return ?32:1?:10:11 if the clock is set in 12 hour format and

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?32:13:10:11 if set in 24 hour format. At this point the user must enter the desired preset time, and the same verification process will occur. After a valid time is entered, a line feed will then set the clock if in 24 hour format and ask the following question if in 12 hour format. "IS THE TIME PM?". Any answer other than (Y)ES will be interpreted as AM.

3-111 After the clock has been preset (with the Line Feed) the clock will ask: "AUTOMATIC N.B.S. SYNC ?" A response of (Y)ES will institute an automatic change-over to N.B.S. time when it becomes available. Any response other than (Y)ES will institute a change-over only after the following handshake sequence: when the clock obtains N.B.S. sync, it sends "SYNC OK NOW". From this point the user sends a Line Feed to initiate the change-over.

3-112 When an "R" is entered to initiate the reset mode this will initiate an RS-232 software reset and place the user in "C" MODE under the internal N.B.S. time storage buffer. If the N.B.S. time is valid, the correct time will be displayed on the clock. If the clock does not have valid N.B.S. time, then what ever time is in the buffer will be output. The time quality character will discriminate against the two times. There are three areas in "I" MODE where an "R" will not initiate a reset of the RS-232. These are after the questions "DO YOU REALLY WANT TO PRESET THE TIME?", "AUTOMATIC N.B.S. SYNC ?" and "IS THE TIME PM?". The user must first respond to the question and then may enter an "R" reset.

3-113 During the transition periods of "I" TIME with N.B.S. TIME, all outputs will no longer be valid. The active mode during "I" MODE TIME will also be the active mode after the transfer to N.B.S. TIME. As an example, if "C" MODE is used before the N.B.S. transfer takes place, then after the transfer "C" MODE will still be the active mode.

3-114 DAMS/HEALTH MESSAGE SOFTWARE (Option)

3-115 When this option is ordered with the Kinemetrics/TrueTime Model 468-DC the capabilities of the RS-232 output option described in this section are modified. The purpose of this software package is to assist the users of the National Environmental Satellite Services (NESS) "GOES" data collection system to check the quality of the uplink transmissions of any given platform under actual operating conditions. This can be performed in the lab before an on-site visit or in the field during the actual installation or repair.

3-116 We will first briefly describe how the "DAMS Test Mode" works. This Test Mode utilizes three portions of the NESS ground system to measure, format and transmit this performance information back to the field.

3-117 As each platform message is received at the Wallops Command and Data Acquisition Station, measurements of the signal

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strength, frequency, modulation index and modulation quality are made by the "Data Acquisition and Monitoring Subsystem" (DAMS). This information is passed to the Wallops computer where it is interpreted and, for selected platforms, a command message is formatted. The command is then transmitted back through the "GOES" satellite utilizing the Data Collection Platform Interrogation Transponder. This message appears to the Model 468-DC as a platform address at first glance.

3-118 Since the Test Mode has been designed to provide information to many DCP's at the same time, the command message consists of two parts. The first is an address sequence which identifies the platform for which the data is intended. The second part is one of 4096 unique addresses which have been reserved for this purpose. The Model 468-DC with the DAMS/HEALTH Message Software option has the ability to first select and trap only the message for the platform the user is interested in (based on the user entering his platforms primary address) and to decode the hexadecimal transmission of the platform status or "HEALTH" into English.

3-119 This Test Mode can be used will all types of DCP's interrogated, self-timed, random reporting and international. All that is required to activate the Test Mode for any platform is for the NESS computer system to be told to place that particular platform in the "Test Mode". This can be done by calling the DCS OPERATOR at (301) 763-8351 and giving the platform "PRIMARY ADDRESS" and asking to have this platform placed in the "Test Mode". This also can be done directly by computer, consult your "GOES-DCS USERS INTERFACE MANUAL" for the procedure. After placing the platform in the Test Mode, any DCP message received from that platform will generate a DAMS/HEALTH Message. In addition, if the platform is interrogated or is scheduled to transmit, the NESS computer will transmit DAMS/HEALTH Message even if no message is received. This will tell the technician in the field or lab that the DCP didn't work at all.

3-120 The first step in the use of this unit is to set up the unit as for the reception of time as described in SECTION II of this manual. The second step unique to utilization of the Model 468-DC for the Health Message, is to insure that the proper satellite is selected for reception. Be certain that the "EAST" or "WEST" satellite selection switch is set properly for your application. See the description under "EAST, WEST, AUTO, SATELLITE LOCK SWITCH" operation in this section.

3-121 After the unit has locked onto the proper satellite and the display has come on with the correct time, you are ready to use the Model 468-DC in the DAMS/HEALTH Message Mode. First, an RS-232 terminal must be connected to the output port of the Model 468-DC. For purposes of this manual it will be assumed that a G.R. Electronics Ltd. "Pocket Terminal" is used, use of other terminals will be virtually identical. It should be noted here that one main difference in the Pocket Terminal and other

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terminals is that the display on the Pocket Terminal has only 8 characters visible at one time on its 32 character display memory. Thus the "SL4" (shift left 4) and "SR4" (shift right 4) keys are used to view the complete message as needed.

3-122 When the terminal is first plugged in, you will note that once per second the time is sent to the terminal by the Model 468-DC. You will also note that two flashing decimal points on the display can be moved left and right by using the "SL4" or "SR4" keys. The proper place to start is with the decimals one character from the right (press SR4 several times).

3-123 DAMS/HEALTH MESSAGE SET UP KEY STROKES

3-124 The first step in obtaining the Health Message is to enter the "primary" platform address for the respective platform. The key strokes for platform 75C093C6 would be:

1) "S" This tells the Model 468-DC that the next eight digits will be the primary address of the platform for which data is desired.

2) "75C093C6" This enters the eight digit address of the platform desired.

3) "SHIFT" This prepares the terminal to send an "upper case" of the next key stroke.

4) "CR" This "carriage return" enters into the Model 468-DC the eight digits keyed into the terminal in Step #2.

NOTE: The display on the Model 468-DC has now converted from a nine digit time-of-year display to an eight digit address display. the 9th digit is not significant, and as new platform addresses are received they will be displayed in turn on the panel display. Since it is possible to receive addresses at the rate of one each 1/2 second these digits **may** change at that rate.

3-125 VERIFICATION KEY STROKES

3-126 "X" When this key is struck, the Model 468-DC responds with the current platform primary address for which the unit has been programmed. It is always wise to verify the entered address after the "CR" is entered to assure there are no errors. If you have incorrectly entered the address, simply repeat steps 1) through 4) above.

3-127 "Z" This key stroke will provide the user with one of the following responses:

1) "DAMS FULLY OPNL" This indicates that everything is operating properly, both at the users end and at NESS.

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2) "SCHEDULED S.T. ONLY" Tells the user that a problem exists in the link between the World Weather Building and interrogated platforms are not polled, thus no Health Message is available at this time.

3) "NOT LOCKED TO SATELLITE" This indicates that the Model 468-DC is not locked to a GOES satellite.

4) "DAMS NOT OPNL" This tells the operator that lock is achieved, but no "Health Message" is being transmitted.

3-128 Until the sequence outlined in the following paragraph is complete, striking keys G, H, I, K, or L will result in the terminal response of "NO DATA YET". This indicates that the Model 468-DC has not received the Health Message for the platform yet (in this example 75C093C6).

3-129 At this point the user must wait for the following to happen (or cause it to happen):

1) Your platform to respond through the "GOES" system when it is poled (75C093C6 in this example) or respond in its assigned time slot if a self-timed platform, or be triggered to respond by the field technician.

2) Next the Wallops Command and Data Acquisition Station will receive your message, measure the signal strength, frequency, modulation index, and modulation quality. Once this is done the Wallops computer interprets the data and forms a command message. This message is then transmitted over the Data Collection Interrogation Link which appears at first to be a platform primary address.

3) The Model 468-DC with the DAMS/HEALTH MESSAGE SOFTWARE option will recognize this message as yours (since we keyed in our platform's primary address earlier). The unit will then lock this eight digit ASCII code on the display and decode it into English through the RS-232 terminal. You will note that when this occurs, the left three digits of the clocks display will show "OCd". This is due to the fact that the 9th digit is not used, and the 8th and 7th are always "Cd" for a Health Message.

4) It should be noted that this DAMS/HEALTH MESSAGE will now be locked onto the display (starting with "Cd") and you may scroll through the commands listed below under "DAMS/HEALTH MESSAGE INFORMATION KEY STROKES", as often as needed until

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the unit is reset by one of several commands. See the "OPERATING NOTES" that follow.

3-130 DAMS/HEALTH MESSAGE INFORMATION KEY STROKES

3-131

KEY STROKE	RESPONSE
"G"	"MESSAGE RECEIVED" or "MESSAGE NOT RCVD"
"H"	"MESSAGE GOOD" or "PARITY ERROR(S)"
"I"	"MODULATION GOOD" or "MODULATION BAD"
"J"	"ZERO" or "ONE" (NOT USED)
"K"	"XMIT POWER SB 45-49 IS XX" (Where "XX" is between 26 and 56)
"L"	"XMIT FREQ. SB +250 IS YYY HZ: (Where "YYY" is between +700 and -800)

NOTE: IN ORDER TO VIEW THE COMPLETE ENGLISH MESSAGE AS DESCRIBED ABOVE WHEN USING THE "G.R. ELECTRONICS LTD." TERMINAL IT IS NECESSARY TO SCROLL LEFT (SL4) OR SCROLL RIGHT (SR4).

3-132 It is assumed at this point that the technician has made the needed adjustments to his platform and will desire to reset the Model 468-DC to once again look for the DAMS/HEALTH MESSAGE for his platform. This can be done by one key stroke:

"Y" This will reset previously set platform address into the Model 468-DC to again capture the DAMS/HEALTH MESSAGE for same primary address. (In our example 75C093C6 is automatically re-entered as if the "S" key and the 75C093C6 plus CR were struck).

3-133 OPERATING NOTES:

1) Any RS-232 terminal used with this software option must be set up to operate with this RS-232 output port as described in this section of the manual. If the "G.R. Electronics Ltd." terminal has been purchased from Kinemetrics/TrueTime this set up is complete as received into the panel mounted RS-232 connector.

2) When the "DAMS/HEALTH MESSAGE SOFTWARE" option is ordered, several of the commands described in the previous section "RS-232 TIME OUTPUT (Option)" have been changed to facilitate the use of this software.

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KEY STROKE W/O DAMS (see) RS-232 TIME OUTPUT	DESCRIPTION	NEW KEY STROKE WITH DAMS OPTION
"C"	Time once per second	"O"
"F"	Format time message	"Q"

All other commands described in "RS-232 TIME OUTPUT", this section, are unchanged.

3) Once the Model 468-DC has entered into the "S" Mode by the entry of your platform address and striking the "CR", care should be used in entering any other letters. If any letters other than G, H, I, K, L, X, Y or Z are entered the Model 468-DC will be removed from the "S" Mode and will not trap and retain the Health Message you are interested in.

4) When the system has been properly set up as described above and the Health Message has been "trapped", the "Information Key Strokes" (G, H, I, K and L) can be re-struck as many times as necessary and strolled through time and time again until another key is struck. The next entry might be "Y" since you just made the appropriate adjustment to your DCP and now desire to get another set of data from Wallops after your platform responds again.

3-134 IEEE-488 OUTPUT (Option)

3-135 INTRODUCTION

3-136 The IEEE-488 output option is available on the Model 468-DC to provide the user with a communication port via the IEEE-488 bus. This option is compatible electrically and mechanically with the IEEE-488 standard 488-1978. Messages are sent and received using strings of ASCII coded characters.

3-137 HARDWARE

3-138 The user interface with the option is through a standard IEEE-488 connector. The "BUS ADDRESS" is set by a dip-switch on the output option circuit card. To access this switch, remove the four screws which hold the bottom cover in place and remove the cover. Note the circuit board in the center with the components facing you. Toward the edge of the board nearest the front panel you will find the 8 position switch. The "Address" is set using positions 1-5 of this switch. This switch encodes the address in binary format:

WHEN POSITION #1 IS "ON" A BINARY 1 IS ENCODED
WHEN POSITION #2 IS "ON" A BINARY 2 IS ENCODED
WHEN POSITION #3 IS "ON" A BINARY 4 IS ENCODED
WHEN POSITION #4 IS "ON" A BINARY 8 IS ENCODED
WHEN POSITION #5 IS "ON" A BINARY 16 IS ENCODED
POSITION #6, 7 AND 8 NOT USED
THE ADDRESS OF THE INSTRUMENT IS THEN THE SUM OF THE ENCODED BITS.

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3-139 The Model 468-DC is shipped from the factory with an address of " 5 ". Therefore, switch numbers 1 and 3 are "on" and all others are in the "off" position.

3-140 EXTERNAL TRIGGER

3-141 Also located on this circuit board are two terminals. One is provided for "EXTERNAL TRIGGER IN" and the other "EXTERNAL TRIGGER OUT". These are not provided on rear panel connectors but are available for the user to bring out if he desires. The use of these triggers will be covered under "MODE T".

3-142 SOFTWARE

3-143 Communications over the bus take place using strings of ASCII characters as mentioned earlier. The output strings from the clock are always terminated by a Carriage Return, Line Feed sequence. The Bus management "EOI" is asserted for the line feed character. The longest string of characters output by the clock on the bus is 20 characters including the carriage return and line feed.

3-144 Inputs to the Model 468-DC are also strings of ASCII characters. Whenever a string is input to the unit, a Line Feed or EOI will terminate the string and no action is taken on that string until this termination is received. Input strings are stored in a 32 character buffer which wraps around when overflowed. This will cause the 33rd character received to be stored in the first position and so on.

3-145 Operation of the clock outputs on the bus is organized by six different modes. A particular mode is initiated by sending the clock a string containing a mode-defining character. The first valid mode-defining character in the string received defines the mode the clock will be set in.

The valid mode characters are:

F FORMATTING OF THE TIME MESSAGE

M MARKED TIME (ALARM CLOCK MODE)

N VERIFICATION OF MARKED TIME IN MEMORY

P POSITION INFORMATION OF GOES SATELLITE

T TIME

3-146 MODE F

3-147 This mode allows the user to establish a desired format for the time message. The format is determined by the strings of characters sent to the unit following the receipt of the "F". This format string consists of 17 characters to format the time response of the clock. Each character in the string controls its

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respective position in the new output format of the clock.

3-148 An "X" in any position of this string suppresses the output of its respective position of the time message. The positions between the days and hours, the hours and minutes, the minutes and seconds, and seconds and thousandths are referred to as delimiter positions. Any character inserted in the input string to format the clock in these positions will be repeated in that position.

3-149 The format of the unit can be selected within the limits of the maximum format:

DDD_HH_MM_SS_tttQ

3-150 Each "_" above represents a delimiter position and can be any ASCII character except "X".

EXAMPLE:

If the option port receives: F123/12:34:56.789Q, the resulting response by the clock will be the day of year, a slash, the hours, colons, the minutes, colons, the seconds, a period, the thousandths carriage return and line feed.
Secondly, if FXXXXXXXXXXXXX124X is received by the unit, the resulting response will be printing only the fractional part of the second followed by a carriage return and line feed.

If the format string is terminated short of the 17 characters, the positions in the time string after the termination of the format message will be unchanged by the format operation.

3-151 MODE M

3-152 This mode allows the user to preset a time in the future and to be notified when that time occurs. An "M" followed by the desired alarm time presets that time into the unit. When the desired time occurs, a "service request" is initiated and the external trigger output line (see SECTION III, entitled "EXTERNAL TRIGGER" is set low. When the preset time has passed the external trigger line is returned to the high state.

3-153 The service request will be cleared by a device clear command, by setting a new alarm time, by reading the alarm time using mode "N" (see SECTION III, entitled "MODE N") or by a serial poll. The status byte returned in a serial poll is an ASCII "M". NOTE: This is in conflict with at least Tektronix standards for the IEEE-488 bus.

3-154 When an alarm string is input, all of the delimiters must be included as place holders. An "X" in any position makes

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that digit a "don't care" digit. If a line feed is placed in any position, the string is terminated and sets the successive digits to "0".

EXAMPLE:

M185*11:06:04.387

This input to the unit would trip the alarm feature at 11:06:04.387 on the 4th of July and the external trigger would be held low for that millisecond.

MXXX*XX:XX:XX (line feed)

3-155 This program configuration would provide a service request at the start of each second and the external trigger output line would be held low for one millisecond.

3-156 MODE N

3-157 Mode "N" is provided for the purpose of verifying the alarm time programmed into the unit. When the Model 468-DC receives an "N" the response will be the previously programmed time in the "M" mode. After transmitting the complete time string, the model 468-DC returns to "M" mode.

3-158 MODE P

3-159 Whenthe unit is placed in the "P" mode, the current position of the satellite being received is outputted on the bus. This position information is provided over the satellite link by the National Bureau of Standards for the purpose of determining propagation delay of the received signal at the user's site. This position information is based on predictions of the satellite 30 days in advance and, as such, has obvious limitations. Currently, the National Bureau of Standards only provides certainty that this information is accurate to ±100 microseconds for propagation delay calculations.

3-160 Kinemetrics/Truetime makes no claims as to the accuracy of this information but does provide it as an output for the user interested in this information.

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EXAMPLE OF CLOCK RESPONSE:

10523+013-062 Carriage Return Line Feed

Where:

10523	represents the longitude of 105.23° West
+	Can be + or -
013	represents the latitude of +0.13°
-	can be + or -
062	represents -62 microseconds difference in the radius of the satellite from the nominal position.

3-161 MODE T

3-162 When a "T" is received, the time as of the completion of the handshake of the string terminator (LF or EOI) is saved in a buffer. This saved time can then be read out by addressing the clock as a talker and retrieving the time message. If the unit has not had a format specified by the "M" Mode, the default format of the time response will be:

DDD HH MM SS.tttQ carriage return line feed

This format being day of year, hours, minutes, seconds, milliseconds and time quality character. This is 19 characters incuding the carriage return and line feed.

3-163 "Q" is the time quality character showing the estimate of worst case time error:

WORST CASE ERROR	ASCII CHARACTER
MORE THAN ± 500 ms.	?
MORE THAN ± 50 ms.	#
MORE THAN ± 5 ms.	*
MORE THAN ± 1 ms.	.
LESS THAN ± 1 ms.	(ASCII SPACE)

If a format change is desired see SECTION III, entitled "MODE F".

3-164 Either a Group Execute Trigger command or a positive transition on the External Trigger In line will also catch the time for output when read. If a "T" or a Group Execute Trigger is received, the time will be caught whether or not any previously caught time has been read. The External Trigger In line will ignore the positive transitions after the first one, until the time has been completely read out.

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3-165 SAMPLE PROGRAMS

3-166 To help the user in learning to interface their IEEE-488 System to the Kinemetrics/Truetime Model 468-DC with IEEE-488 output, below are sample programs. These programs are direct print-outs and proven to operate with the Model 468-DC. We trust these will be of assistance. Most of the problems encountered by users in initially interfacing with the Model 468-DC on the "bus" seem to have been in specifying the clock's address, and in properly handling the terminating sequence of <CR>, <LF> which the clock needs and supplies.

1. HP 9825A Program:

```
0: dim M$[20]
1: dim T$[20]
2: ent M$
3: "trig"&wrt
  705,M$
4: red 705,T$
5: dsp T$
6: wait 210
7: gto "trig"
*15336
```

2. HP 9830A Program:

```
REM  **  TRUE TIME 60DC CONTROLLED BY H/P 9830A.  ** 27 FEB 81 **
LIST

5 DIM A$[20]
10 CMD "?U"
20 FORMAT B
30 OUTPUT (13,20)768;
40 CMD "?U%"
50 OUTPUT (13,*)"FDDDDHHHMMMSSS1111"
55 CMD "?U%"
60 OUTPUT (13,*)"T"
65 CMD "?E5"
70 ENTER (13,*)A$
80 DISP "TIME: "A$[1,3]" DAY,"A$[5,6]"HRS "A$[8,9]"MIN'S "A$[11,12]"SEC'S
100 GOTO 55
110 END
```


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3. "PET" Program:

```
Program to set time string format and read time from True Time clock.
via the IEEE-488 bus using a PET

10  OPEN 5,5                        Informs PET of clock"s address on the bus
20  PRINT#5,"FDDDXHHXMMXSSXTTTX"    Sets clock format to omit delimiters.TD flag
30  PRINT#5,"T"                     Instructs clock to catch time
40  INPUT#5,A$                      Reads time from clock
50  PRINT A$                        Displays time
```

4. SYSTRON-DONNER 3520 Program:

```
PROGRAM TO READ TRUE TIME CLOCK USING SYSTRON-DONNER MODEL 3520 'BUSSER'

10      BUS CLEAR           Just in case
20      BUS ADDRESS 00101   5 in binary
30      BUS PRINT"T"        Address clock as listener; send "T<CRLF>"
40      BUS IN              Address clock as talker; read&display time string
```


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3-167 D.C. POWER INPUT (Option)

3-168 The D.C. Supply Option is available at extra cost and is installed in place of the standard 95-135 VAC 60-400 Hz power supply. This option allows the clock to operate from direct current sources of a nominal 12 or 24 VDC ratings. The D.C. Supply option will operate with an input voltage between the absolute limits of 11 and 30 V.D.C. The power required will be approximately 20 watts, depending on the other options installed and the input current will decrease as the input voltage increases.

3-169 Power connection is made through a pair of "5 way binding posts" located on the rear of the unit. They are spaced 3/4" apart to accept the common "double banana plug". The positive terminal is red and the negative terminal is black. Neither is connected to the chassis ground.

3-170 50us TIMING (Option)

3-171 This option may be specified at the time of order when two or more Model 468 Satellite Synchronized Clocks are purchased. It provides for the selection and adjustment of all clocks in the order group to provide the user with 50 microsecond timing correlation between clocks when several operating conditions are met.

3-172 The conditions necessary to assure the 50 microsecond timing correlation are:

1) All clocks are receiving the same satellite (GOES EAST or GOES WEST). See SECTION III, entitled "AUTOMATIC/MANUAL SATELLITE SELECTION".

2) The receiving antenna must be properly aimed at the satellite being received. An error in pointing of no more than 30' is allowable. See SECTION II, entitled "ANTENNA INSTALLATION" for antenna pointing information.

3) Both units have maintained 100 Hz data lock for a minimum of 1/2 hour. Momentary local interference will probably not deteriorate the timing agreement.

4) The antenna of each unit has an unobstructed view of the satellite. This means that there must be no reflecting surfaces which will create strong multipath interference. By multipath, we mean the antenna receiving the satellite signal from both the satellite directly and after bouncing off of a nearby reflective surface.

5) The ambient temperature difference of receiver to receiver is held within 10°C. The ambient temper-

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ature difference of antenna to antenna is also held within 10°C.

6) When the propagation path differences have been properly taken into account. This is intended to be the propagation path from the satellite used to each clock in the system at any time during the period when the 50 microsecond timing accuracy is expected. The distance between clocks over which this "propagation" difference can be held within an acceptable range will vary from one user's network configuration and geographic location to the next. It is therefore recommended that the factory be consulted with the configuration, distances between units, and geographic location for your system to assist in the determination of the applicability of this option to your needs.

3-173 DAYLIGHT SAVINGS TIME CORRECTION

3-174 Effective spring of 1984 the National Bureau of Standards began including two bits in the "GOES" time code to inform the user when the United States is on Daylight Savings Time.

3-175 For users who are operating the Model 468-DC with the "HOURS OFFSET" (See Section III, entitled "HOURS OFFSET") on the rear panel set to "0", this change in the time code will not affect your displayed or output time. This will allow these users to continue to function in "UTC" which is unaffected by the DST laws.

3-176 For those users with the "HOURS OFFSET" Switch set in positions -4 thru -11, the Model 468-DC will automatically correct for the change between DST and Standard Time. Both the displayed time and any electrical output of the time will be changed to provide the user with this change in local time. A small switch, located adjacent to the 12/24 Hour Select Switch on the Digital Board (Assembly 86-42), will enable or inhibit the automatic DST correction. (Refer to FIGURE 3-3). With this switch in the OFF position the automatic DST correction will be applied. Those users located in areas which do not observe U.S. Daylight Savings Time will want to operate the 468-DC with this switch in the ON position to continue to display the correct local time.

3-177 RS-232 STANDARD MODE S

3-178 When an ASCII "S" is received on the 468-DC, an ASCII number from 0 to F or an "*" will be returned. Interpretation of this is as follows:

* Means the clock is currently not synchronized

0 - 7 Represents the satellite position accuracy expectation value. Interpreted as a number N which is used in the

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following equation to give a deviation in microseconds.

2 [2N+1] = ± number of microseconds.

Normally this number will be a 3, which is equivalent to an expected accuracy of no worse than ±128 microseconds.

8 Means that a parity error was detected in the position data.

Combinations of expectation value and parity error are acceptable. For example a "B" would represent a parity error and an expectation value of 3 which is equal to ±128 microseconds.

3-179 ADVANCED PERFORMANCE OPTION

3-180 The 468-DC Advanced Performance Option consists of an additional printed circuit board (86-147), modifications to the analog board (86-74) and digital board (86-42), and additional firmware. The following features are provided by this APO:

1) 10 to 1 improvement in resolution of propagation delay compensation (100 microsecond increments).

2) Automatic selection of proper delay compensation for each of the three GOES satellites (East, West, and Spare).

3) Positive identification of the satellite whose signal is being received.

4) Reduced timing error when switching satellites (1 millisecond or less).

5) Improved internal time base stability (1×10^{-6})

6) Loss of lock indication in IRIG-B time code output.

3-181 FIGURE 3-8 is a block diagram of the baseband data phase-lock-loop circuits. The new circuits for the Advanced Performance Option are shown in the lower right corner, within the dashed lines. The seek/trace, lock/freeze, and fine/coarse switches are solid state switches controlled by signals of the same name that originate at the digital processor board (86-42). The normal acquisition and tracking operation of these switches is explained in SECTION IV of this manual. The switches are shown in their normal tracking position, where the fine phase detector and fine VCXO are part of the data loop.

3-182 A more detailed block diagram of the option circuits only is shown in FIGURE 3-9.

3-183 The 86-147 PCB has nine ten-position switches that are set by the operator. The switches are in groups of three, marked

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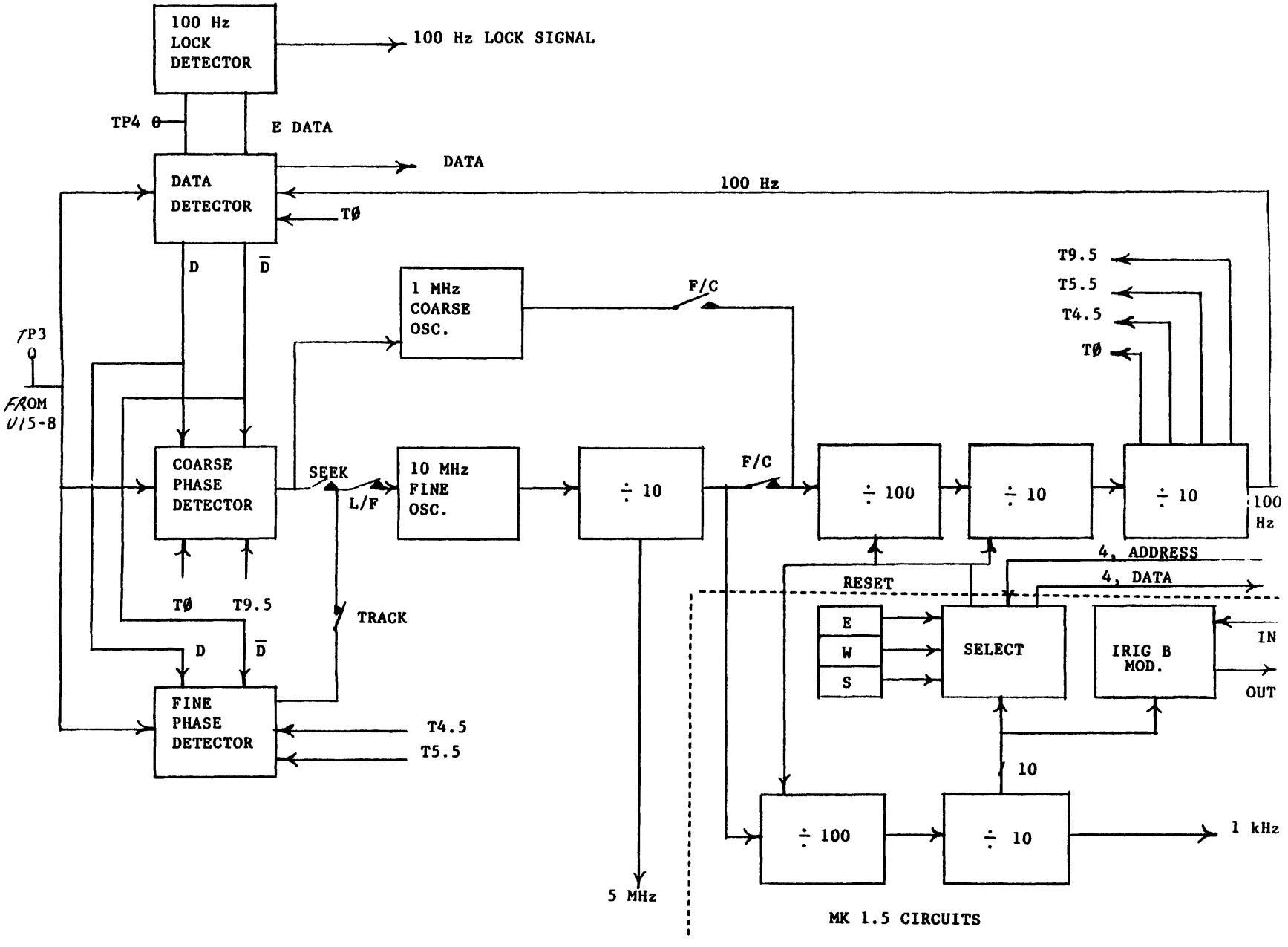
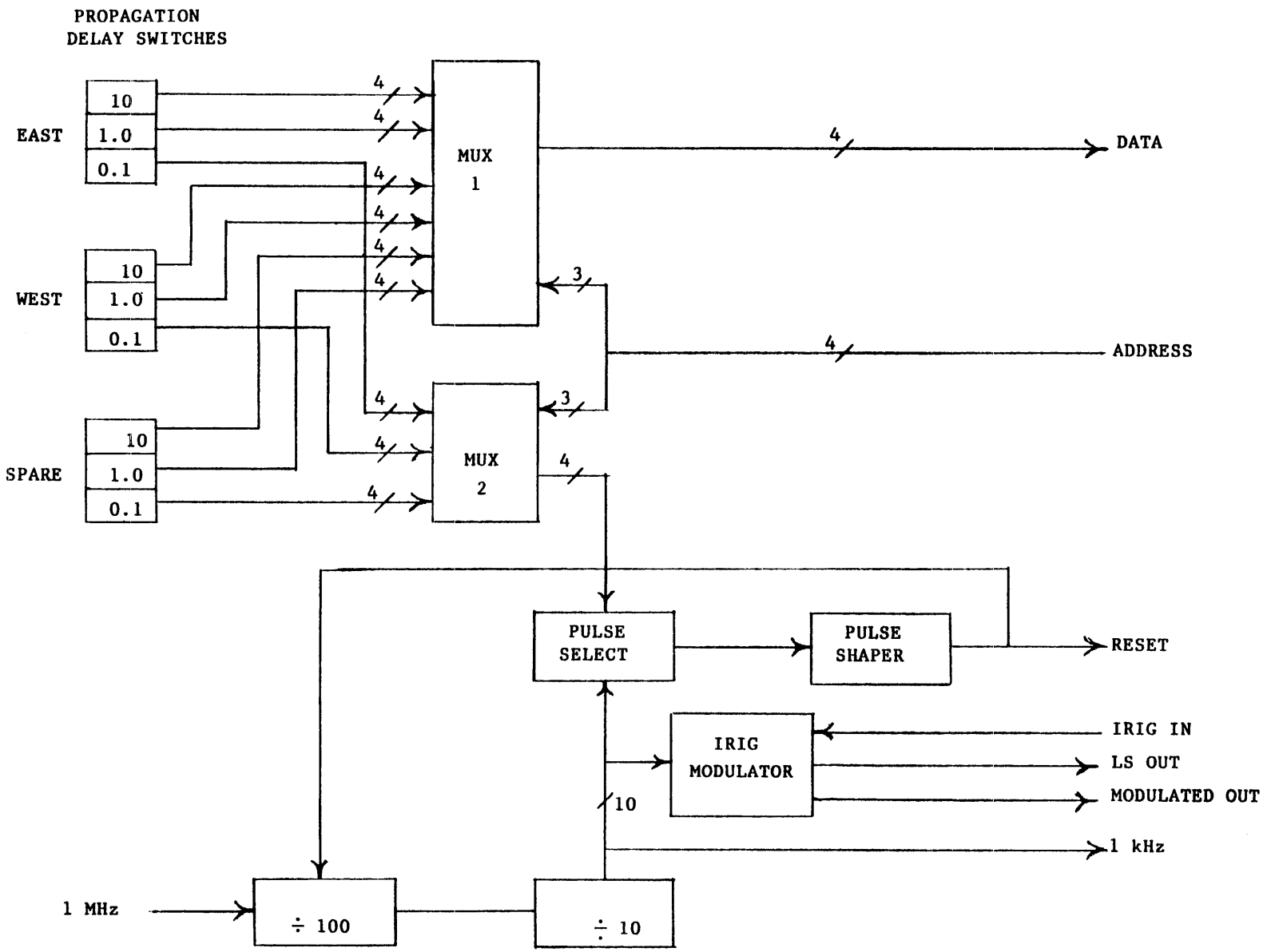


FIGURE 3-8 BASEBAND DATA PHASE-LOCK-LOOP CIRCUITS

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FIGURE 3-9 APO BLOCK DIAGRAM



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'EAST', 'WEST', and 'SPARE', respectively. Each switch is labeled '10', '1.0', or '0.1', indicating the multiplier value of the switch setting in milliseconds.

3-184 The operator must know the 468-DC location to within 18.6 miles (30 km). This is 15 minutes (1/4 degree) of latitude or longitude. The propagation delay can be determined by running the program shown in FIGURE 3-10, or by calling Kinemetrics/TrueTime at 707/528-1230. The operator then sets the switches to the correct setting.

EXAMPLE:

The operator has determined that propagation delay for the East GOES satellite should be 37.4 milliseconds. On the 'EAST' group of switches, the '10' switch would be set to '3', the '1.0' switch to '7', and the '0.1' switch to '4'.

3-185 The satellite selection switches, previously on the digital board assembly, are now on the option board. Operation of the switches is the same as before (see SECTION III, "AUTOMATIC/MANUAL SATELLITE SELECTION").

3-186 The VCXO drift is reduced by clamping the 10 MHz fine oscillator DC input voltage to a fixed value that was set when the receiver was calibrated. Component and crystal aging will still cause an increasing error with time, but clamping the input is more accurate than allowing the integrator to drift to one of the supply voltage rails. The time quality flags are set for an error rate of approximately three milliseconds per hour. This is much worse than actual measurements have shown, and allows for crystal aging. Reference SECTION III, "DISPLAY", SECTION VIII, "CONTROL FUNCTIONS".

3-187 When the operator selects either the East or West satellite, the selection data is compared against the received signal to verify that the receiver is phase locked to the correct satellite signal. The satellite signals contain position information as part of the data stream. This position information is decoded and compared to position data stored in memory. The correct signal is being received when the data stream information and the position data in memory are compared, and found to agree. In non-'Automatic' mode, if the receiver is locked to the wrong signal, the sweep will continue until the correct signal is found. If the receiver has not found the correct signal after 10 to 20 minutes, the operator should check the antenna pointing direction, or select the other satellite. In the 'Automatic' mode the receiver locks to the first satellite signal it finds, whhich can be either East or West.

3-188 With the Advanced Performance Option, timing errors are minimized when the operator switches satellites, or the receiver

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switches satellites due to low signal-to-noise. This has been achieved by the extra propagation delay switches, reduced VCXO drift, and removal from the data loop of the divider circuits that generate the timing 1 KHz. Whenever the 100 Hz lock detector fails to indicate data lock after RF lock has been achieved for more than 3 seconds, the coarse phase detector and coarse VCXO are connected into the data loop (Lock/Freeze opens, Fine/Coarse 2 closes, and Fine/Coarse 1 opens). This allows for faster slewing of the data loop and data acquisition. After data lock has been obtained for 32 seconds, F/C 2 opens, F/C 1 closes, and L/F closes, reconnecting the fine VXCO and fine phase detector into the data loop. Because the fine VXCO has been removed from the data loop during acquisition, its drift is very low; the added error in timing is one millisecond or less, as a result. When a valid relock occurs, there is immediate synchronization to satellite time. After the satellite signal has been identified, multiplexer 2 in FIGURE 3-9 reconnects the correct '0.1' microsecond switch to the select circuit. The select circuit picks one of the ten outputs from the divide-by-ten circuit to reset the three dividers shown. This causes a phase shift in the data loop divide-by-ten circuit, producing the fractional propagation delay.

3-189 The IRIG-B circuits have been moved to the option board to maintain the accuracy during reacquisition time.

3-190 A loss-of-lock bit is added to the IRIG-B Time Code. This bit is located at p_r+530 milliseconds. P_r+530 milliseconds = Control Element 4 (see SECTION VIII, FIGURE 8-1) The loss-of-lock indication is a software modification that indicates loss of carrer lock for more than 150 seconds.

3-191 The program in FIGURE 3-10 provides the user with propagation delay switch settings and antenna elevation angles for use with Kinemetrics/TrueTime Model 468-DC GOES receivers. The program has been written in BASIC and can be run on a CPM 8032 computer.

NOTE 1:

Enter longitude coordinates in terms of West longitude in degrees.

NOTE 2:

Preface Southern latitude coordinates with a minus sign.

A hard copy listing of a more detailed program, complete with operator prompts is available. Contact Kinemetrics/TrueTime for a copy of this program.

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```
8 REM PRGM DATE 1/15/83: L. ELMORE, G. HARDIN
12 REM SETUP
14 PI=3.14159265400001#
20 R0=140580!:REM SAT RADIUS
30 R1=21223:REM EARTH RADIUS
40 L1=75.46*PI/180: REM WALLOPS LONG
42 F1=37.85*PI/180
44 PRINT"ENTER THE FOLLOWING COORDINATES IN DEGREES AND DECIMAL DEGREES:"
47 PRINT:PRINT
56 PRINT"USERS LONGITUDE ";:INPUT L3:L3=L3*PI/180
57 PRINT"USERS LATITUDE ";:INPUT F3:F3=F3*PI/180
58 PRINT:PRINT
68 PRINT"SATELLITE LONGITUDE";:INPUT L2:L2=L2*PI/180
70 PRINT"SATELLITE LATITUDE ";:INPUT F2:F2=F2*PI/180
130 REM CALCULATE WALLOPS>SATELLITE
140 L0=L1
150 F0=F1
160 GOSUB 500:REM RETURN WITH T0=TIME
170 T1=T0
190 REM NOW SATELLITE TO SITE
200 L0=L3
210 F0=F3
220 GOSUB 500
230 T3=T0
250 REM CALCULATE SWITCH SETTING & PRINT
260 T4=100-(310000!-T3-T1)/1000
265 T4=INT(T4)
268 PRINT:PRINT
269 PRINT
274 PRINT"SWITCH SETTING ";T4;"MILLISECONDS
275 GOSUB 600
280 PRINT"ELEVATION ANGLE ";INT((H*180)/PI+.5);"DEGREES"
285 PRINT:PRINT:PRINT:PRINT
286 PRINT
296 PRINT
297 PRINT
300 END
500 REM CALCULATE 1 WAY TRAVEL TIME
510 B=COS(ABS(L2-L0))*COS(F2)*COS(F0)
520 B=B+SIN(F2)*SIN(F0):REM (COS(B) !)
530 T0=SQR(R0*R0+R1*R1-2*R0*R1*B)
535 RETURN
560 RETURN
600 REM CALCULATE ELEVATION ANGLE
601 REM GIVEN B, WHICH IS COS BETA,
602 REM ANGLE AT CENTER OF EARTH
610 C=SQR(1-B*B): REM GET SIN(B)
612 REM TO GET ANGLE AT SATELLITE
620 C=C*R1/T0
630 H=ATN(C/SQR(-C*C+1)):REM ARC SIN
640 REM ANGLE AT SATELLITE
650 B0=-ATN(B/SQR(-B*B+1))+PI/2
652 REM ARCCOSINE
654 H=PI-B0-C:REM SUM OF ANGLES IS 180
660 H=H-PI/2
670 RETURN
```

FIGURE 3-10 COMPUTER PROGRAM

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SECTION IV

THEORY OF OPERATION

4-1 THEORY OF OPERATION MODEL 468-DC

4-2 The 468-DC receiver decodes and outputs the time, using the NBS supported time code transmitted via the "GOES" (Geostationary Operational Environmental Satellite) Satellites, which are operated by NOAA (National Oceanic and Atmospheric Administration).

4-3 The transmission which carries the time code is at a frequency near 468 MHz. The data is encoded by phase shift modulation of the carrier (Manchester encoding) at a 100 bit per second rate. The code format breaks each second down into two 1/2 second sections, each consisting of 50 bits (1/2 of the available 100 bits in the second). During this 1/2 second, the first 4 bits * are used by the National Bureau of Standards for their controlled information.

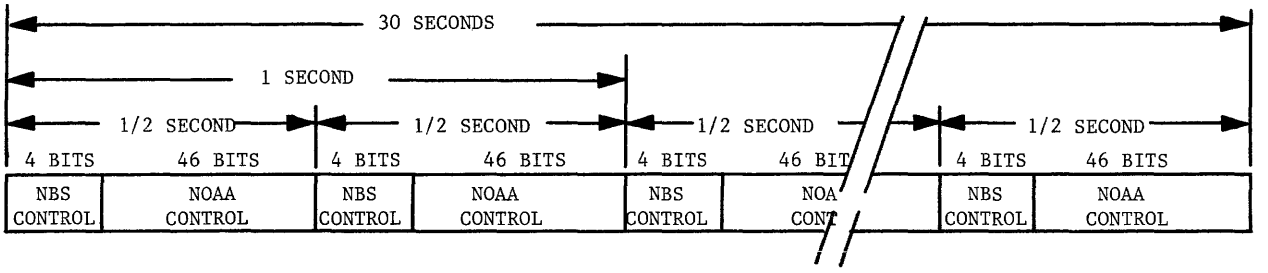


FIGURE 4-1 GOES TRANSMISSION FORMAT

4-4 The NBS Information consists of:

1. Synchronization word
2. Days, hours, minutes, seconds
3. UT1 correction
4. Predicted satellite position
5. Remaining space is used for experimental purposes

This information obviously cannot be conveyed in a single 4 bit character of a 1/2 second, therefore, one character each 1/2 second for 30 seconds is utilized. The data in items 1-5 above is repeated every 30 seconds.

* The remaining 46 of the 50 available bits are used by NOAA for the purpose of "MAXIMUM LENGTH SEQUENCE" (MLS) which is a synchronization word and for data collection platform "Interrogation Address" which is the main purpose of their channel.

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4-5 A phase locked receiver is used to receive and recover raw data from the satellite signal. The raw data is processed by analog circuitry and then passed to a microprocessor for conversion to useful outputs; among which are a visual display, one Hertz and one kilohertz timing pulses, and several optional communication ports. An overall block diagram of the hardware involved is given in FIGURE 4-2.

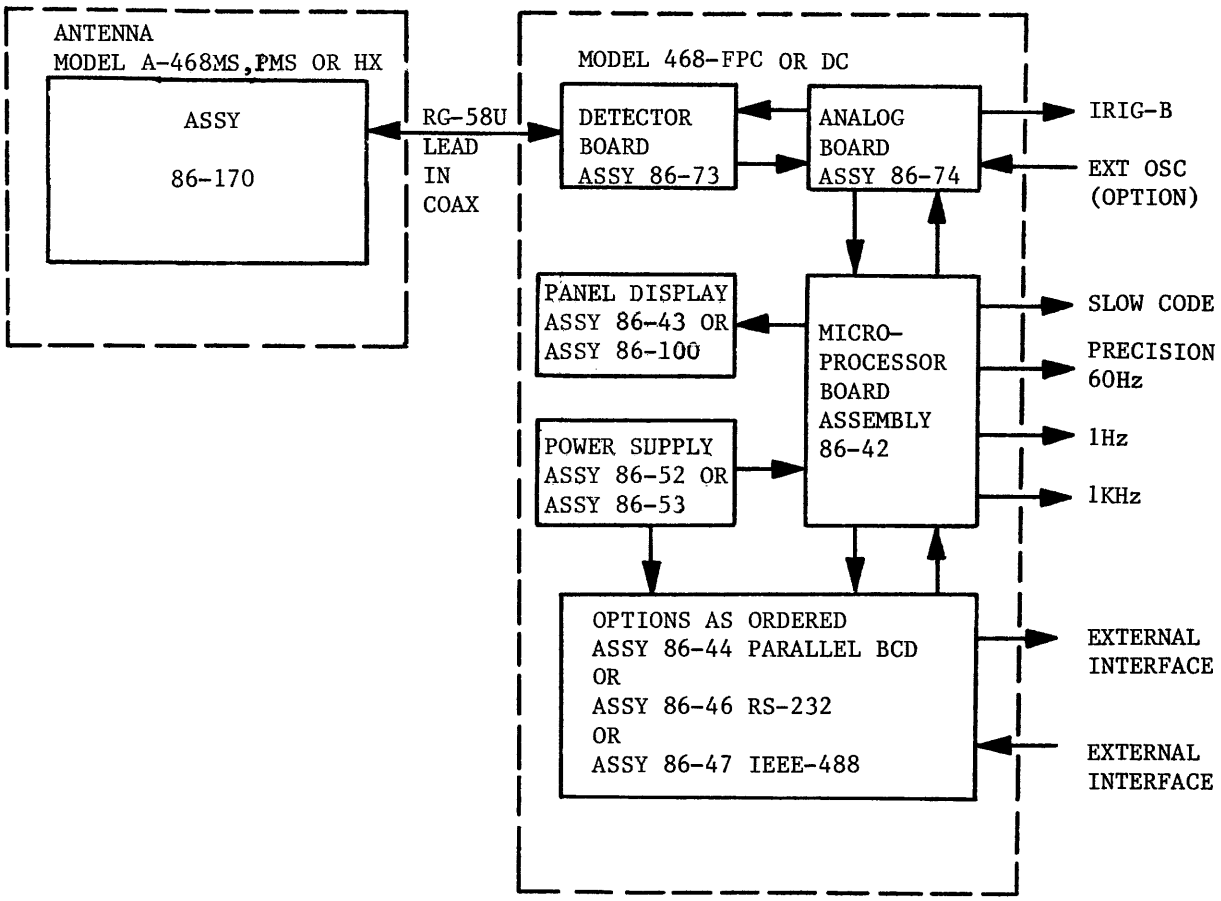


FIGURE 4-2 OVERALL BLOCK DIAGRAM - MODEL 468-DC

4-6 The receiver portion of the clock consists of the active antenna, the detector board (Assembly 86-73), and part of the analog board (Assembly 86-74) - all under control of the program on the digital board (Assembly 86-42). The active antenna receives the satellite signal, amplifies it by about 120 db,

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and translates it in frequency to 4.5 MHz, using the first local oscillator frequency generated on the analog board in the main instrument and sent up the connecting coax together with the 12 VDC power. The second local oscillator is contained in the antenna. A block diagram of the active antenna is shown in FIGURE 4-3.

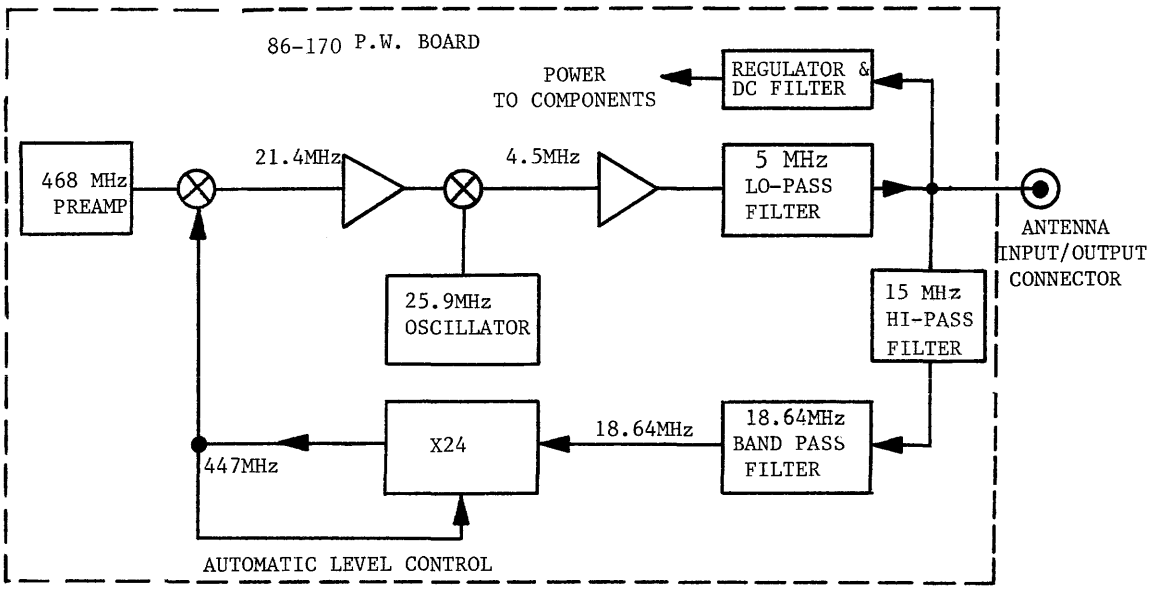


FIGURE 4-3 ACTIVE ANTENNA BLOCK DIAGRAM - MODEL A-468MS

4-7 The 4.5 MHz output of the active antenna comes down the coax to the detector board (Assembly 86-73), where it is translated to baseband using the third local oscillator in conjunction with two balanced modulator/demodulators; one in phase, the other in quadrature with the satellite signal.

4-8 On the analog board, the in-phase baseband signal is an indication of signal strength, and is compared with a reference level to decide whether a satellite signal is being received. This information is passed on to the digital board, as well as being displayed by the LED RF unlock indicator.

4-9 The quadrature baseband signal constitutes the raw Manchester data and goes to the data phase locked loop. It is also used by the RF phase locked loop as the error signal to force the RF loop to stay in lock.

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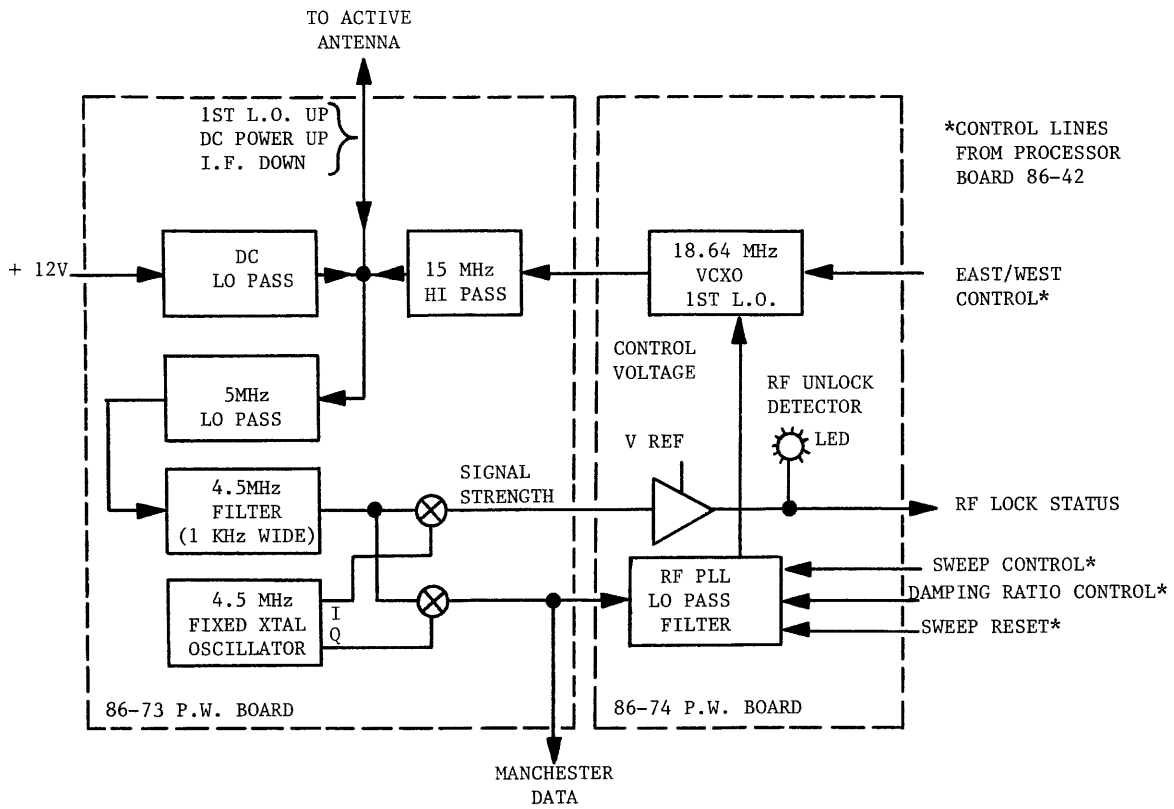


FIGURE 4-4 PHASE LOCK LOOP BLOCK DIAGRAM - MODEL 468-DC

4-10 In order to recover Manchester coded data, two functions must be performed, synchronization (data clock recovering) and data decoding. The data PLL circuitry does both. There are two data PLL circuits, a coarse and a fine. The coarse PLL allows rapid sync to data at turn-on while the fine loop serves for precise sync once coarse sync is obtained. One or the other of these PLL's is always operating, under processor control. Whichever data PLL is selected runs the timing circuitry which supplies the timing for the processor and hence, all clock functions. Data clock recovery is performed by a PLL. At turn- on, a coarse PLL is used to quickly sync to the data. Thereafter, a fine PLL refines and maintains this sync. The fine PLL has three configurations, under processor control:

1. In normal operation, the PLL locks to the incoming data using the fine data phase detector.

2. If satellite signal is lost and if an external oscillator signal is supplied, the PLL locks to the external oscillator. Otherwise, it freezes its present frequency.

3. On re-acquiring satellite signal, the PLL seeks data lock using the coarse data phase detector. See FIGURE 4-5.

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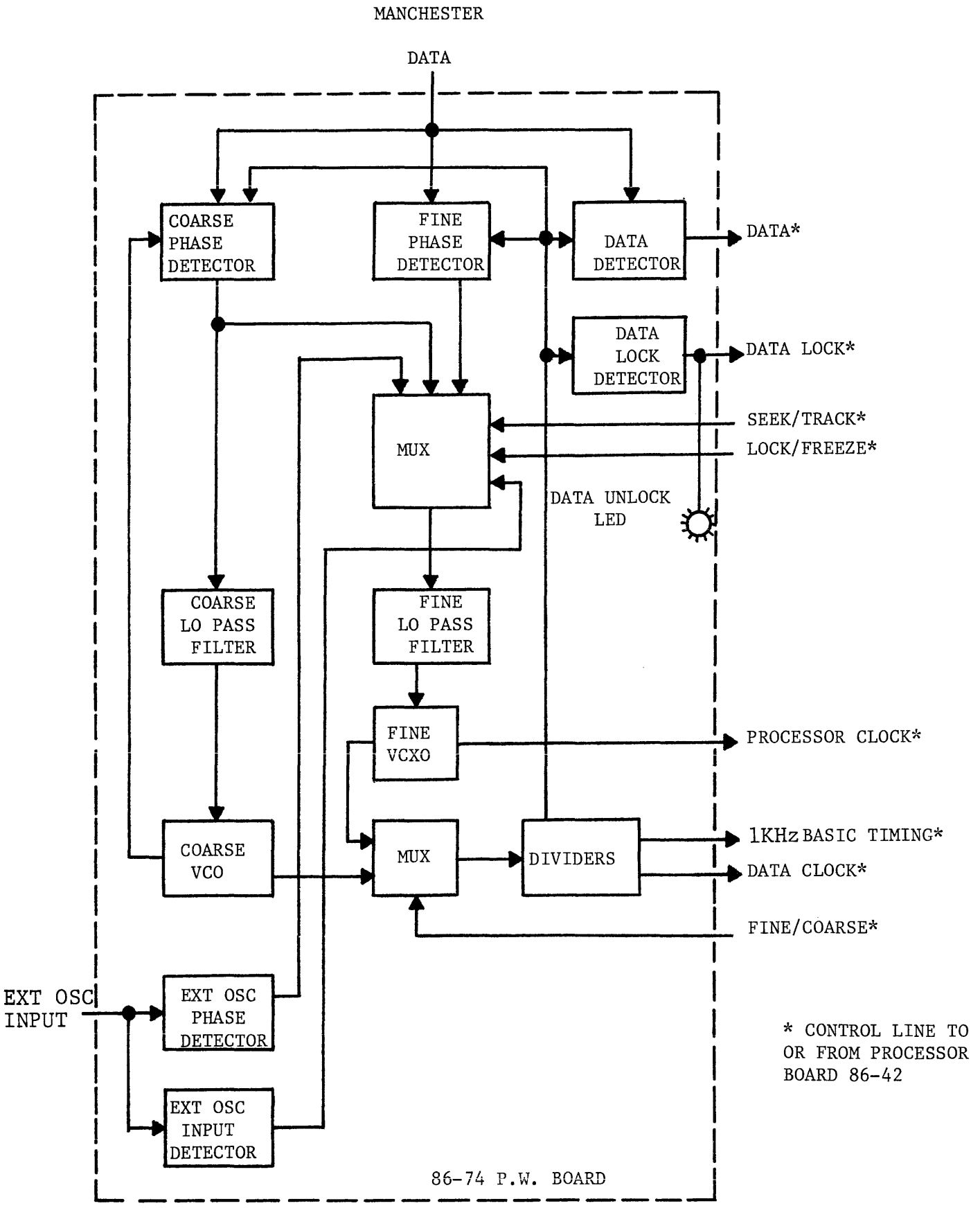


FIGURE 4-5 BASEBAND DATA PHASE LOCK BLOCK DIAGRAM, MODEL 468-DC

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4-11 The data detector which decodes the raw Manchester data is an integrate and dump type, (which constitutes a matched filter for the code) and is located on the analog board. The output of the data detector goes to the processor for further analysis.

4-12 Also on the analog board is the external oscillator input, allowing use of a stable external oscillator during periods of interrupted signal reception; and the modulation circuitry for the IRIG-B time code output.

4-13 The microprocessor Board (Assembly 86-42) controls the whole instrument by means of the program stored in its memory. The program is discussed in the section on software, SECTION IV, entitled "SOFTWARE". All information in the instrument flows through this board. In addition to controlling the receiver's two phase lock loops and recovering the data, the 86-42 board provides all information for the front panel display, generates the several timing outputs of the clock, controls the timebase for the clock, and optionally communicates with the rest of the world via the RS-232, IEEE-488, or Parallel BCD interface.

4-14 The display board is controlled by the digital board. It contains multiplexed planar gas discharge displays and their drivers, providing an easily visible visual display of the time.

4-15 The output options also controlled by this board are the communications options. These boards (only one of which can be installed in an instrument) provide the ability to communicate the time to other instruments finding application in larger systems. Presently available options include Parallel BCD outputs, RS-232 Link, and IEEE-488 Bus capability.

4-16 DETAILED DESCRIPTION OF OPERATION

4-17 ACTIVE ANTENNA ASSEMBLY 86-170

4-18 The active antenna, A-468MS or A-468HX, contains a preamplifier, an IF amplifier and a first L.O. multiplier/mixer. See FIGURE 4-3 for a block diagram and SECTION VI for the schematic of Assembly 86-170.

4-19 PRE-AMPLIFIER

4-20 Helical-tuned resonators provide 50 ohm matching as well as high selectivity at 468.8 MHz. Gain is greater than 8 db and rejection at the image frequency, 426 MHz, exceeds 40 db. TL1 and TL2 are quarter-wave stubs which are used to minimize out-of-band responses.

4-21 1st L.O. MULTIPLIER/MIXER

4-22 The 18.64 MHz first L.O. signal from the main instrument is multiplied by 24 to provide the actual first local oscillator frequency. 468.8 MHz (signal frequency) - 21.4 MHz (first

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intermediate frequency) = 447.4 MHz (first local oscillator frequency). Automatic level control maintains the first L.O. power level at 0 dbm.

4-23 When the 18.64 MHz signal enters the board, it first passes through a high pass and a bandpass filter. Diodes CR4 and CR5 insure a constant drive level at Q3, which quadruples to 55.8 MHz in its collector circuit. Q4, 5 and 6 each act as doublers producing 447.4 MHz which is applied to the final drive stage, Q7. Helical filters, FL5 and FL4, serve to eliminate spurious signals which could cause undesired responses in the output of the mixer. Typically, undesired components are down by at least 60 db. CR1 samples the 447 MHz level for the ALC circuitry.

4-24 Of the four sections of U1, one is the ALC amplifier, one drives the red 1st L.O. unlevel indicator LED, and the remaining two form a window comparator which lights the green "preamp active" indicator, if the preamp supply current demand is between 3 and 7 MA.

4-25 The balanced mixer takes the 447.4 MHz L.O. and the 468.8 MHz satellite signal and converts them to a signal at the 21.4 MHz IF. The output of the ALC amplifier, U1 pin 14, is applied as negative feedback to the emitter of Q5, thus closing the ALC loop.

4-26 INTERMEDIATE FREQUENCY AMPLIFIER

4-27 The 21.4 MHz signal from the mixer passes first through Q2, acting as a buffer, and is then applied to a 13 KHz wide monolithic quartz crystal filter centered on 21.4 MHz (Y1 and Y2). This provides the primary protection against strong nearby signals, which can be common in the 468 MHz land mobile band. Q8 and Q9 and their associated components provide up to 40 db of gain at 21.4 MHz. Y3 and Y4 are a second 21.4 Mhz monolithic quartz filter which further reduce undesired signals, primarily internal receiver noise at this point.

4-28 Q10 is the second mixer. In conjunction with the 25.9 MHz second local oscillator, Q13 and Y5, the frequency is shifted down to 4.5 Mhz, while providing 10 db gain. Q11 and Q12 are the 4.5 MHz amplifier, which provide up to 60 db gain. CR2 is the ACG rectifier. It samples the received signal, and by applying this sample to the ACG line, maintains a constant output level from the IF amplifier.

4-29 L25, C77, L26 match the high impedance 4.5 Mhz output of the IF amplifier to 50 ohms for the transmission down line, and at the same time filter 18.6 MHz power to keep it out of the IF amplifier.

4-30 Power for the active antenna circuitry is provided by U2, an eight volt, three terminal voltage regulator. Nominal current consumption for the entire antenna is approximately 50 MA.

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4-31 DETECTOR BOARD ASSEMBLY 86-73

4-32 Signals pass in both directions through the Detector Board. The 18.64 MHz first L.O. comes from the Analog Board Assembly 86-74, goes through the high pass filter C2, L4, C3 and then goes up the coax to the antenna. See Schematic SECTION VI for Assembly 86-73 and block diagram SECTION IV, FIGURE 4-4.

4-33 The 4.5 MHz signal from the antenna proceeds through the low pass filter L1, C4, L2 into the 4.5 MHz crystal filter T1, Y1, Y2, T2, R4 and then to the two balanced modulator/demodulators U2 and U3. The bandwidth of this filter is narrow, about 1 KHz. Q1, Q2 with Y3 are the third L.O., running at 18 MHz. U1 divides this by four to provide both in-phase and quadrature reference signals for U2 and U3. The frequency of the oscillator is trimmed by C9 to center the received signal in the 4.5 MHz filter passband. U2 and U3 phase detect the signal and output balanced baseband signals to the analog board.

4-34 ANALOG BOARD ASSEMBLY 86-74

4-35 See FIGURES 4-4 and 4-5 for a block diagram and SECTION VI for the schematic of Assembly 86-74.

4-36 RF LOCK DETECTOR

4-37 The in-phase signal from U3 on the detector board is converted to a single-ended signal by U15 (pins 12, 13 and 14). It can be examined at TP2. Typically, this point is at -2.4V when locked to a satellite. Reliable decoding requires less than -1.0V. U15 (pins 1, 2, 3) is the signal strength comparator. The in-phase signal from U15 (pin 14) goes through a low pass filter to reduce the effects of modulation and noise, and is then compared with a reference level fixed at -0.6V. If the in-phase signal is more negative than the reference level, U15 (pin 14) extinguishes the RF unlock indicator (D7) and, through U25 (pins 7, 6) sends this information to the processor board. U25 serves merely as a level translator for signals going to the processor board from the analog board.

4-38 RF LOCK LOOP

4-39 The Quadrature signal from U23 on the detector board is converted to single-ended by U15 (pins 8, 9, 10) and can be examined on TP3. This is the raw Manchester data from the satellite used by the data PLL's and the data detector. See FIGURE 4-6 below which depicts approximately 50 bits of superimposed data.

4-40 The Manchester data is then inverted and level-shifted to compensate for offset voltage by U11 (pins 1, 2, 3) and by R45, the symmetry control. The signal then goes to the RF loop low pass filter, U11 (pins 5, 6, 7).

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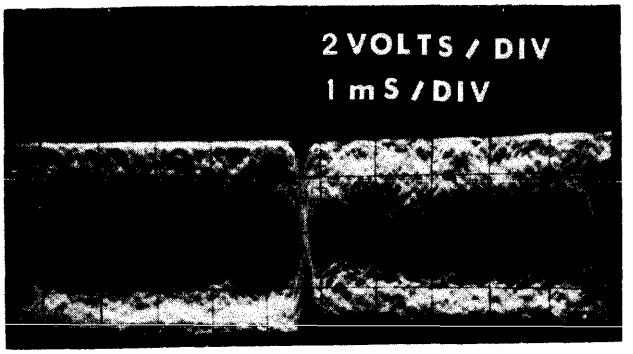


FIGURE 4-6
RAW MANCHESTER DATA (SHOWS APPROXIMATELY 50 BITS SUPERIMPOSED)

4-41 The RF loop low pass filter is an integrator with two inputs. One is the satellite data as described above, the other is a sweep/reset input via U12 (pins 1, 2, 13). When the receiver is locked to a satellite signal, U12 (pins 1, 2) is an open switch, allowing undisturbed phase lock; but when phase lock is not present, the processor can close the switch, allowing current to flow out of the summing node through R31. This forces the output of the integrator, U11 (pin 7) to ramp more positive at about 150mV per second. If a satellite signal is acquired, the processor stops the sweep by opening the switch. If, on the other hand, no satellite signal is detected after the sweep has continued long enough for U11 (pin 7) to approach +5V (it takes 40 seconds), the processor issues a reset pulse through U10 (pins 1, 2, 3). This causes U11 (pin 8) to go high, forcing current into the summing node through R25. This much larger current (than that through R31) rapidly drives U11 (pin 7) negative. The reset ends when the node at R27 and R28 becomes negative enough to pull U11 (pin 10) below ground, thus driving U11 (pin 8) negative, and removing the source of reset current. Meanwhile, the processor, subject to manual override by S1 or S2, can select the other satellite as the target by opening one and closing the other of the analog switches U12 (pins 6, 8, 9) and U2 (pins 3, 4, 5). These switches select one or the other of two DC voltages set by R37 and R38, to be averaged with the output of the RF loop low pass filter to control the frequency of the first local oscillator, Y2, Q5, Q6, D6. The output of this oscillator is sent up to the antenna, thus closing the RF phase locked loop.

4-42 DATA DETECTOR

4-43 See FIGURE 4-5 (the baseband Data Phase Lock Block Diagram) and SECTION VI for the schematic of Assembly 86-74. Also see FIGURE 4-7 for a timing diagram showing T0.0, T4.5, T5.5, T9.5.

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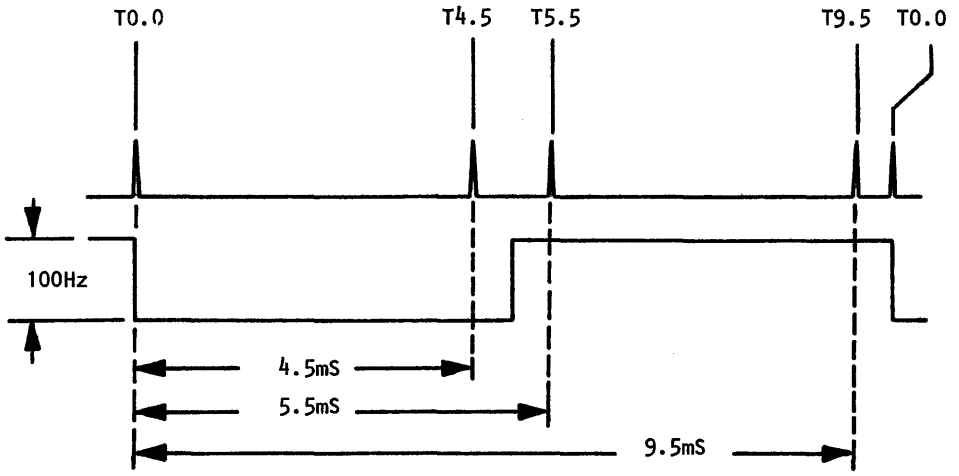


FIGURE 4-7 ANALOG BOARD TIMING

4-44 The heart of the data detector is U30 (pins 12, 13, 14) the data integrator. Its output is available at TP4. The data integrator is reset by switch U29 (pins 6, 8, 9) at the beginning of each data bit time. Its input for the first half of the data bit time is the raw Manchester data, which for a "1" is positive during the first half of the data bit time and negative for the last half. A "0" is negative first, positive last. For the second half of each data bit time, the inverted Manchester data from U28 (pin 1) is applied to the data integrator input. Thus, for a "1", the input is always positive, while for an "0", always negative. The resulting data integrator output is a negative going ramp for a "1" and a positive going ramp for an "0". FIGURE 4-8 shows the data integrator output on the top line, and the raw Manchester data on the bottom.

4-45 The data integrator output is sliced by U30 (pins 1, 2, 3) and sampled near the end of the data bit time by U26 (pins 3, 4, 5) together with C34 and U30 (pins 5, 6, 7).

4-46 U24 inverts the sample so a "1" is positive. U25 (pins 9, 10) buffers the data to the processor and U24 (pins 1, 2, 3) provides inverted data for the data phase detectors.

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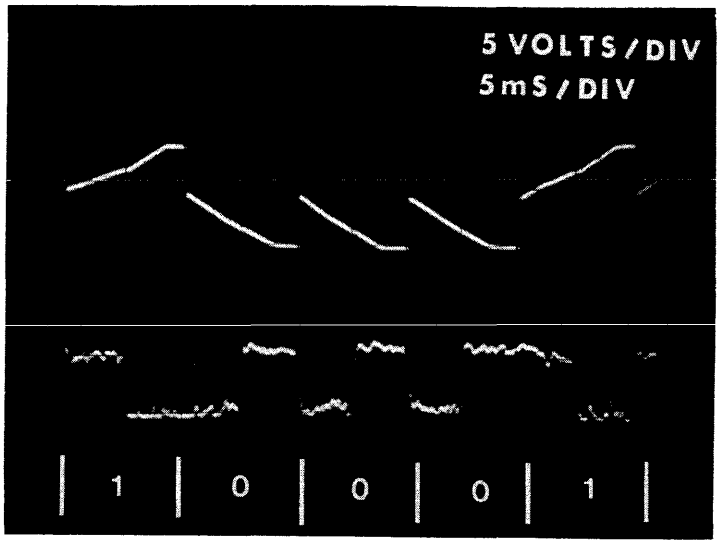


FIGURE 4-8 DATA INTEGRATOR OUTPUT

4-47 DATA LOCK DETECTOR

4-48 There are two slicers operating on the output of the data integrator. They have small opposite offsets so that both have high outputs for zero volts in. U27 (pin 7) is high for "1"s, while U30 (pin 1) is high for "0"s. These outputs are each 'Anded' with a timing pulse (T9.5) near the end of the data bit time and used to sample the output of the data integrator. If the data integrator output is positive at sample time, (data = "0") U26 (pins 10, 11, 12) direct the sample to C32, while if the output is negative, (then, data = "1") U26 (pins 6, 8, 9) directs the sample to C31. Thus C31 accumulates the average final value of the data integrator output for "1"s and C32 for "0"s.

4-49 The diode-resistor networks between each switch and its capacitor serve to weight small (bad) values more heavily than large ones. U27 (pins 8, 9, 10) and U27 (pins 12, 13, 14) are followers to prevent loading of C32 and C31. U27 (pins 1, 2, 3) is a comparator with offset which determines whether the difference between "1"s and "0"s is greater than a threshold value set by R81. If so, D10 is extinguished and the processor is notified via buffer U25 (pins 14, 15) that reliable data lock is obtained (See FIGURE 4-9).

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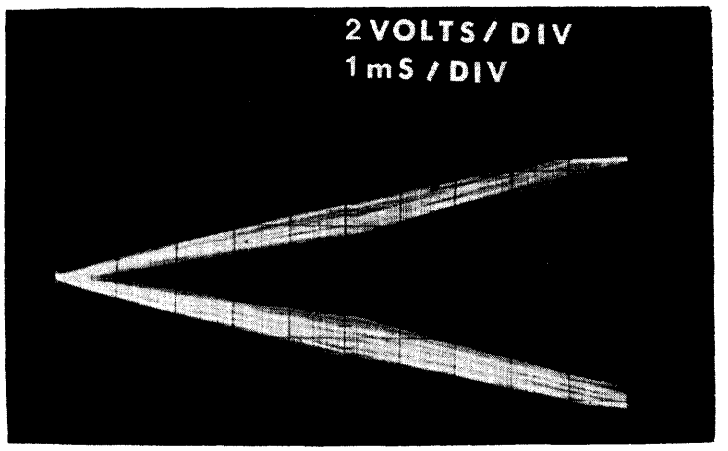


FIGURE 4-9 "CLEAR SIGNAL"

4-50 If the signal-to-noise ratio drops too low, the data integrator output ramps will no longer cleanly separate the "1"s from the "0"s, and the voltages on C31 and C32 will both move in towards zero, eventually causing an out-of-lock condition to be indicated, if the signal becomes too poor for reliable decoding (See FIGURE 4-10).

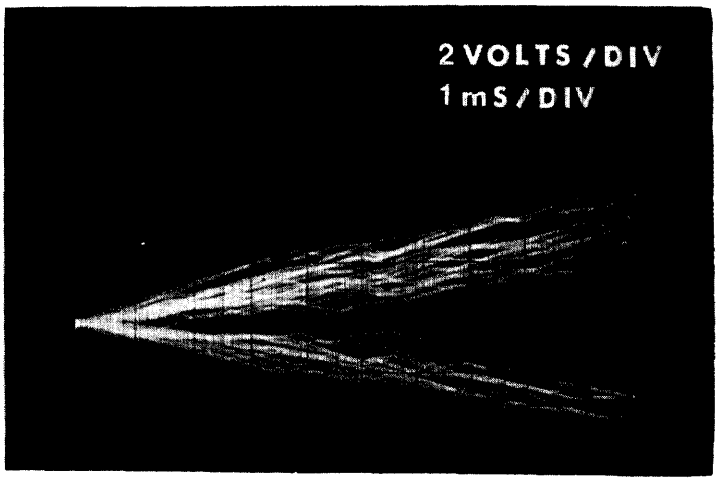


FIGURE 4-10 "POOR SIGNAL"

4-51 If no antenna is connected, the data integrator output is close to zero and both slicers U27 (pins 5, 6, 7) and U30 (pins 1, 2, 3) have high outputs causing both C31 and C32 to discharge, rapidly causing an out-of-lock indication.

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4-52 COARSE PHASE LOCKED LOOP

4-53 The coarse phase detector begins with U28 (pins 5, 6, 7) which slices the Manchester data. This improves the phase detector gain a little for weak signals. Next comes U28 (pins 12, 13, 14), an integrator, reset at the start of each bit time, T0.0 by U31 (pins 6, 8, 9). The output of this integrator is sampled at T9.5, near the end of the data bit time by U31 (pins 10, 11, 12) onto C36. Follower U32 (pins 5, 6, 7) minimizes loading while U32 (pins 8, 9, 10) provides an inverted version of the sample value. Switches U32 (pins 1, 2, 13) and U33 (pins 3, 4, 5) select either the sample or the inverted sample, based on whether the data bit was a "1" or a "0". This results in the desired error voltage, proportional to the phase difference between the local data clock and the incoming data.

4-54 When timing is exactly in phase with incoming data, the output of U28 (pin 14) is a triangle wave; for a "1", the waveform starts out in a positive direction. Then, at mid-bit, it turns back negative going, just reaching zero at the end of bit time. A "0" gives the mirror image. Thus when data and clock are in phase, the detector output is 0V. See FIGURE 4-11.

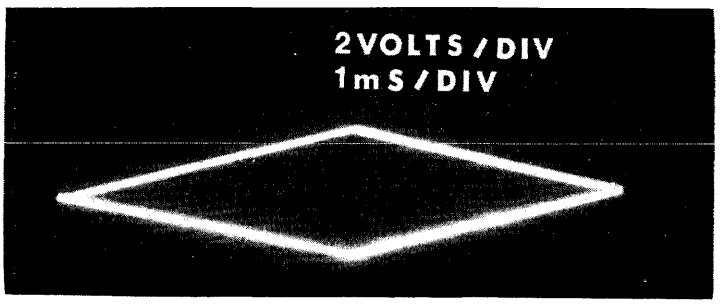


FIGURE 4-11
COARSE DATA PHASE DETECTOR INTEGRATOR OUTPUT (IN LOCK CONDITION)

4-55 If timing is advanced with respect to data, a "1" will contain some contribution from the previous bit, which is uncorrelated and provides no average output, so U28 (pin 14) will, on the average, have insufficient time to get back to zero, and a net positive charge will be stored on C36. A "0" will leave a negative charge, for this timing. A data "1" will, however, select the inverted sample for output, while a "0" uses the non-inverted sample; the end result for either case is a negative output for timing advanced with respect to data. A similar argument shows that for timing retarded with respect to data a positive output results.

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4-56 The above argument strictly holds only for the second of two same bits, a bit following its complement produces no net contribution. The coding scheme on the satellite has been designed with this in mind. The complete coarse phase detector characteristic is shown in FIGURE 4-12.

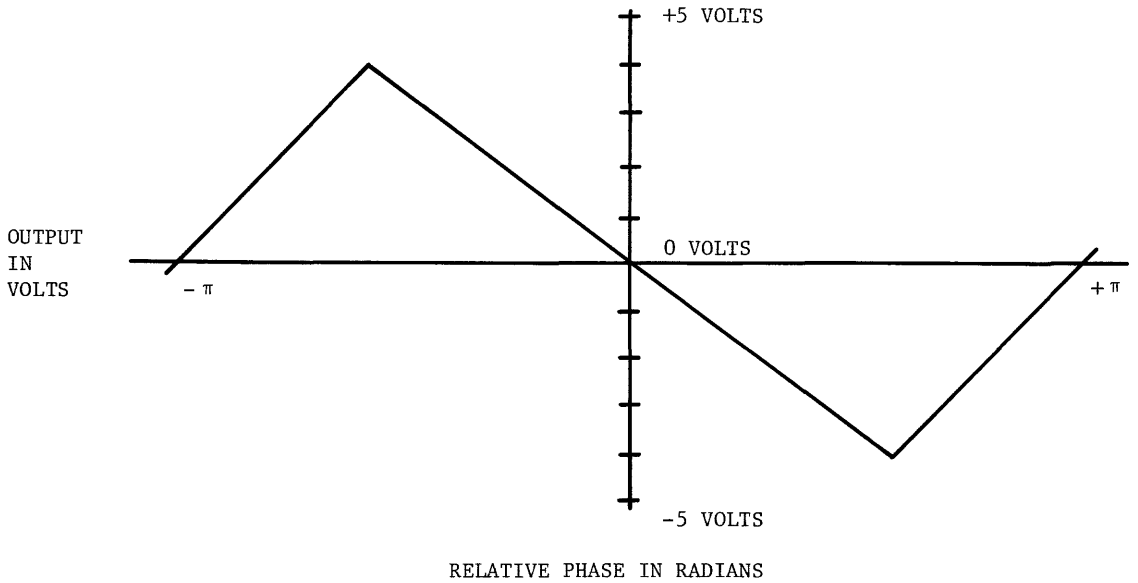


FIGURE 4-12 COARSE DATA PHASE DETECTOR CHARACTERISTIC

4-57 Pins 8, 9, 10 of U4 is the coarse low pass filter. Its output is clamped at zero by the processor via U3 (pins 8, 9, 10) and U3 (pins 1, 2, 13) until the coarse timebase is selected. This speeds coarse data lock acquisition by guaranteeing an initial frequency close to the correct value. Q1, Q2, D1 comprise the coarse data clock oscillator. It is controlled in frequency by the output of U4 (pin 8) and runs at 1 MHz +2%. When the coarse oscillator is selected by the processor, it provides all the timing for the analog board and for program execution on the processor board. Selection is controlled via U5 (pins 3, 4, 5) and U6 (pins 6, 8, 9).

4-58 FINE DATA PHASE LOCKED LOOP

4-59 The fine phase detector operates similarly to the coarse detector, but with two notable exceptions; it has no slicer at the input, and its timing is such that integration takes place only during the central millisecond of the data bit time. These differences tend to reduce the effects of noise and of op-amp offsets on the systematic sync error; but they also destroy the detector's effectiveness far away from lock. FIGURE 4-12 shows the output of the fine phase detector integrator for many cycles, all superimposed. It is clamped until T4.5 and sampled at T5.5. These times correspond to 4.5 and 5.5 divisions on the scope. The fine phase detector's characteristic is shown in FIGURE 4-13.

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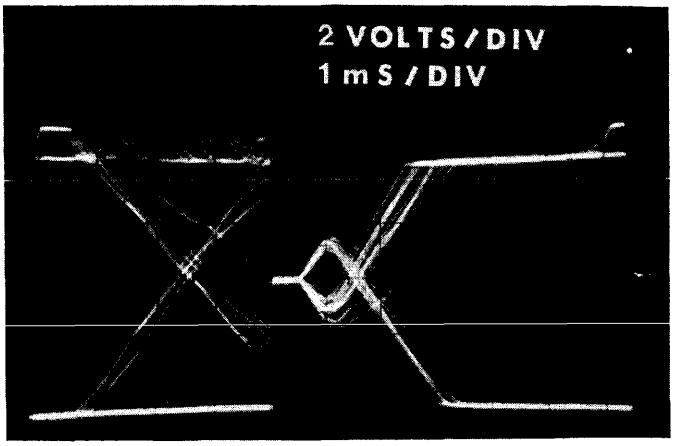


FIGURE 4-13 FINE DATA PHASE DETECTOR INTEGRATOR OUTPUT

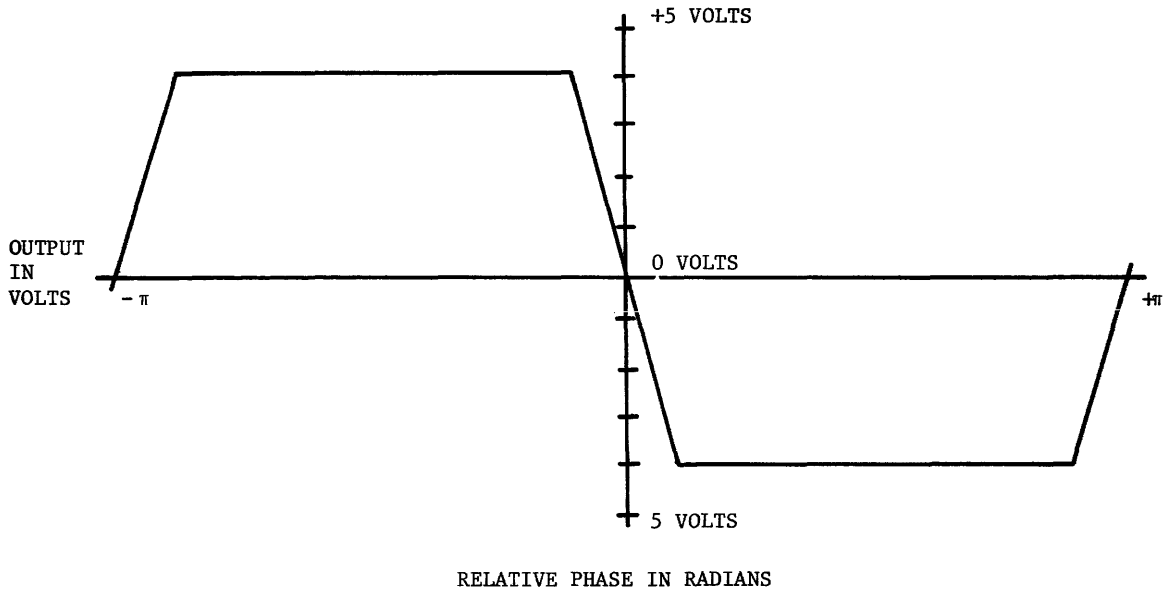


FIGURE 4-14 FINE DATA PHASE DETECTOR CHARACTERISTIC

4-60 The output of the fine phase detector can be applied to the input of the fine PLL low pass filter through U6 (pins 1, 2, 13) and U3 (pins 10, 11, 12). Opening this switch enables the processor to open the loop and freeze the data clock oscillator frequency at its present value, in case of interference.

4-61 EXTERNAL OSCILLATOR INPUT (Option)

4-62 As an alternative, the output of the coarse phase detector, or an external input phase detector can be selected as

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the input to the fine loop via U6 (pins 10, 11, 12), or U3 (pins 3, 4, 5) respectively. The coarse detector is used to re-acquire data lock after it has been lost. The external input phase detector will be selected during a "freeze" condition, but only if an external oscillator is connected. This is accomplished by gating in U9 (pins 1-10) and Q500, the "External Oscillator" detector. Q7 (pins 8, 9, 12) serves to provide a 50% duty cycle for pins 2, 3, 5, 6, the external input phase detector. U4 (pins 12, 13, 14) converts the balanced output of this detector to single ended form. The external input phase detector is edge sensitive and locks to even harmonics of its reference frequency of 10 kHz.

4-63 U4 (pins 1, 2, 3) with R13, R14, and C10 is the fine loop low pass filter. Its output (available at TP8) is averaged with the fine trim voltage from R17 to control the frequency of the fine data clock oscillator. The fine data clock oscillator consists of Q3, Q4, Y1 and D2. It runs at 10 MHz $\pm$7 PPM, and is divided by two, in U8, to provide 5 MHz for the processor and also is divided by ten in U8 to provide 1 MHz for the timing chain.

4-64 TIMING CHAIN

4-65 U18 divides whichever 1 MHz source is selected by 100 to provide 10 KHz. Its output is level-shifted by C26, R63 and R64 from 5V/0V levels to $\pm$2.5V levels which drive U19. U19 provides a further division by 10, and provides timing for generation of a stepwise approximation of the 1 KHz sinewave carrier, using R107 through R116, used in generation of IRIG-B. This stepwise approximation is smoothed and buffered by U100 (pins 12, 13, 14) and then modulated by the processor using U102 (pins 1, 2, 13), R104 and R105. This modulated code is buffered by U100 (pins 1, 2, 3) and U100 (pins 5, 6, 7) for output.

4-66 If level-shift code is desired, output transistor Q100 provides TTL signal levels. 1 KHz timing for the processor also comes from U19. This is the basic timing for all processor activity. This output, along with all other outputs to the processor, is buffered by U21.

4-67 U20 divides the 1 KHz output of U19 by ten to provide the 100 Hz timing for the processor and also, with U21, timing for data lock and detection circuitry.

4-68 DIGITAL BOARD - ASSEMBLY 86-42

4-69 See SECTION VI, Assembly 86-42, for schematic of the digital board. The digital board utilizes a M6802 microprocessor as the central processor. The processor controls data flow over a multiline bus in a typical microprocessor configuration as a controller, stored program memory, read/write data memory, and input/output interface. U2, U3, U4 are the I/O interface devices. All communications with the other areas flow through them. U12, U13 are type 2114 rams and comprise the read/write memory used

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for storage of program variables. U5 and U7 2716 EPROMS, are used for program storage. U9, U10, U11, and U15 perform address decoding to direct data flow to and from the proper devices. U14 generates a reset pulse to ensure orderly start of operating at turn-on.

4-70 The function of the 86-42 board is determined within a wide range by the program stored in U5-U8. It is beyond the scope of this manual to describe in detail the operation of this program, however, a general outline is provided in the software section to aid in the understanding of the clock's behavior.

4-71 POWER SUPPLY - ASSEMBLY 86-52

4-72 See SECTION VI, Assembly 86-52, for schematic of power supply assembly.

4-73 The power supply itself is a standard design and needs no explanation.

4-74 The reset circuit, U6, senses ripple on either of the +5V supplies and generates a negative going pulse which goes to the reset flip-flop on Assembly 86-42, forcing a program reset as long as ripple is present on either +5V line. This protects against erratic operation during times of low line voltage.

4-75 DISPLAY BOARD - ASSEMBLY 86-43

4-76 See SECTION VI, Assembly 86-43, for schematic of display board assembly. The display board provides a visual display controlled by the processor. The display is multiplexed by pairs of digits. A given pair is selected by the processor via Q1-Q10 driving the anode to +180V. At the same time, the desired digits are presented in BCD to the decoder-drivers, U1 and U2. Unblanking, colon, and satellite LED indicator drives are encoded and latched by U5 as the absent left hand digit of the pair of digits of which the 100's of days is the right hand digit.

4-77 PARALLEL BCD TIME OUTPUT (Option) - ASSEMBLY 86-44

4-78 See SECTION VI, Assembly 86-44, for schematic. The parallel output option provides logic level output of the same time as shown on the display. It does this by demultiplexing the display data lines and latching the data in a buffer consisting of U8-U9 and U22-U24. On the second, the data in the output buffer is sent to the outside world through drivers 74HCC244 to provide increased drive capability.

4-79 A millisecond counter, U25-U27, together with drivers U29-U31, provide milliseconds output, and also control loading of time into the output buffer. This counter is synchronized with NBS time via the "time ok" line through trigger latch U19.

4-80 The function of U21 and its associated circuitry, is to provide either an edge or a level for controlling sampling of the

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BCD output lines. U29 is an output driver for several miscellaneous outputs. A timing diagram, showing the relationship of the 1 KHz line to the data output lines is shown in SECTION III, to assist in reading the lines during the time when they are stable.

4-81 RS-232 INTERFACE (Option) - ASSEMBLY 86-46

4-82 See SECTION VI, Assembly 86-47, for schematic. U1, a Motorola MC6850 ACIA, handles the conversion between processor bus data and serial data. U4 and U5, line driver and receiver type 1488 and 1489 respectively, convert between NMOS and RS-232 signal levels. U6, a Motorola MC14411 BAUD rate generator with Y1 provides an assortment of clock rates, one of which is selected by S2 to drive the ACIA. U3, a 74LS138, decodes addresses to direct information flow; while U2, a 81LS96, permits reading of the option switches, S1.

4-83 Use of this option is covered in SECTION III, entitled "RS-232 TIME OUTPUT" (Option).

4-84 DAMS/HEALTH MESSAGE (Option)

4-85 This option is designed to aid users of the National Environmental Satellite Service GOES Data Collection System. It allows users concerned with Data Collection Platform performance to check the quality of the uplink transmissions under actual operating conditions.

4-86 Use of this option is under program control and is described separately. See SECTION III, under "DAMS/HEALTH MESSAGE".

4-87 IEEE-488 INTERFACE (Option) - ASSEMBLY 86-47

4-88 See SECTION VI, Assembly 86-47, for schematic. The IEEE-488 (GPIB, HPIB) interface uses U1, a Motorola MC68488 GPIA, to handle the handshaking and other bus management activities. Interface to the bus is through U4-U7, MC3448 bus transceivers, with U8, a 74LS138, provides address decoding; while U9, a MC6821, allows for reading the device address switches, and for sending and receiving external triggers.

4-89 Use of the option is under program control and is described separately. See SECTION III, entitled IEEE-488 (Option).

4-90 D.C. POWER INPUT (Option)

4-91 This additional cost option allows clock operation with a variety of motor vehicle, uninterruptable and portable battery power sources.

4-92 The circuit is the "Flyback Switching" type with complete D.C. isolation between power source and clock chassis.

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4-93 The input filter consists of C15, C16, C25 and L. CR6 protects against the application of reversed polarity power. U2 provides a constant 8 volts for the operation of the starting and transistor drive circuits.

4-94 Q2 is the power switching element, and T1 and U2 provide isolation between the power source and the clock circuits.

4-95 The supply is started by circuits U10, U11 and U13. When applied voltage is sufficient for clock operation (approximately 10.5 volts), pin 4 of U13 goes low and in 11 of U10 goes high, and the multivibrator (consisting of U10-10, U11-9, R38 and C20) starts to oscillate. The signal labeled STLC* (for starting clock) is applied to U8, Q3, and Q4 etc. and turns Q2 on with an approximately 20% duty cycle at a rate of about 20 KHz.

4-96 The energy stored in T1 is transferred to the secondary windings, and capacitors C5, C6, C7 and C8 are charged to provide operating power for the load and also to the switching regulator U5. When the voltage across C4 rises to approximately 3.5 volts, the circuit of U5 will begin to oscillate with a 50% duty cycle signal which is coupled through U7 to U10-6 and U11-5. The signal at U10-6 is input to the drivers of Q2 and the same signal is applied to U11-5, which sets U11-7 into a low state each cycle of the regulator's output. U11 is re-triggerable and the period of R36 and C18 is sufficiently long, that while U5 oscillates, the starting clock is continually inhibited.

4-97 The voltage across C7 will continue to rise until it reaches the regulator set-point, approximately 5.25 VDC. When this voltage is reached, the regulator will reduce the duty-cycle of its output waveform to maintain the output voltage at this desired value.

4-98 During trouble-shooting, R11, which sets the regulator output, should never be changed unless it is certain that the regulator is working properly. The supply also should never be operated without a load, as normal operation cannot be determined under no-load conditions, and damage may result as a result of application of over-voltage to some components.

4-99 The current through Q2 is monitored by comparing the voltage across R27 with the voltage across the lower portion of R26. U6 re-sets U9-1 when the current exceeds the value pre-set with R-26, interrupting the current through Q2. The next pulse from U5 again sets U9 allowing the drive circuit to again turn Q2 on. This provides over-current protection to Q2.

4-100 U4 provides a RESET* signal to the processor with a signal which goes high when the 5 VDC voltage exceeds about 4.7 VDC.

4-101 U1, U3 and U12 are each conventional I.C. regulators which provide the -12, -5 and +12 volt power to the clock.

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4-102 SOFTWARE

4-103 PROGRAM DESCRIPTION

4-104 The Model 468-DC program can be divided into three broad areas. All, of course, being controlled by the microprocessor on the Assembly 86-42.

1. Control of the receiver and processing of satellite data

2. Generation of the various timing outputs

3. Communications via an optional interface board (RS-232 or IEEE-488)

4-105 RECEIVER CONTROL AND DATA PROCESSING

4-106 Receiver control can be considered as three levels of synchronization:

Synchronization to the RF carrier

Synchronization to the 100 Hz data rate

Synchronization to the transmitted time code

There is no clean division between synchronization to the time code and decoding the time. Each level of sync is contingent on the preceeding levels. A series of state diagrams attempts to describe these levels. See FIGURE 4-15 and 4-16.

4-107 DESCRIPTION OF THE STATE DIAGRAMS

4-108 The state diagrams present a view of the internal states of the program along with the conditions for transitions between the states. Also shown are the external effects of the internal states. A state definition is represented by information enclosed by a line. The format is:

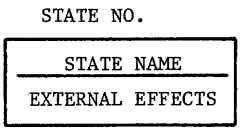


FIGURE 4-15 STATE DIAGRAM

Transitions between states are represented by lines connecting two states with an arrow indicating the direction of the transition and with the condition causing the transition indicated alongside the line.

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FIGURE 4-16 STATE DIAGRAM

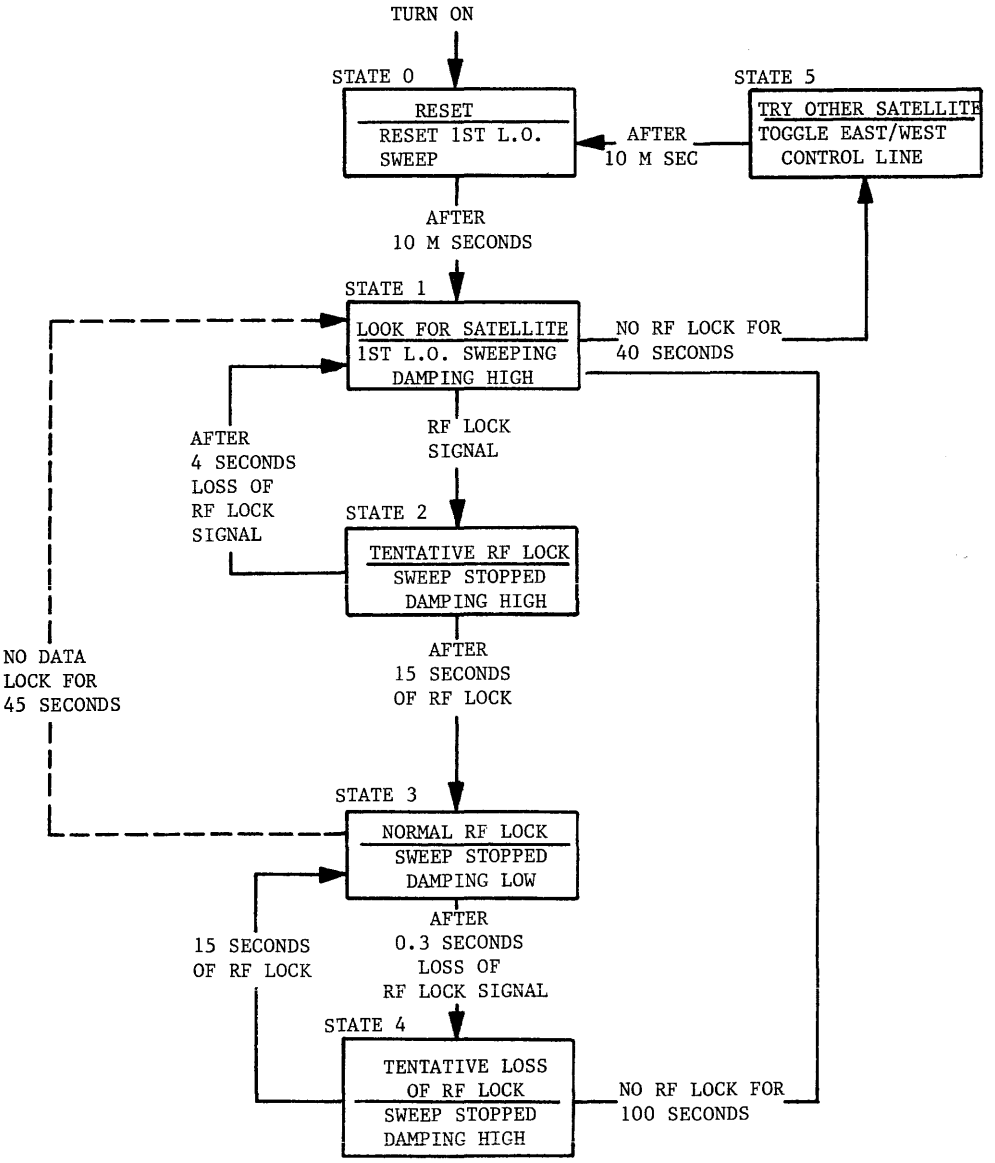


FIGURE 4-17 RF LOCK STATE DIAGRAM

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4-109 Normally, the clock will start at state 0 and quickly pass to state 1. RF lock will be obtained usually in about 20 seconds, causing a transition to state 2, which allows the RF lock loop to stabilize. Fifteen seconds later, state 3 will be entered, and normal operation proceeds.

4-110 The reverse linkages in the diagram are there to recover from problems that may arise; primarily interference by land mobile service. The link from state 3 to state 1 prevents lock to unmodulated carriers. State 4 facilitates RF lock after a short burst of interference.

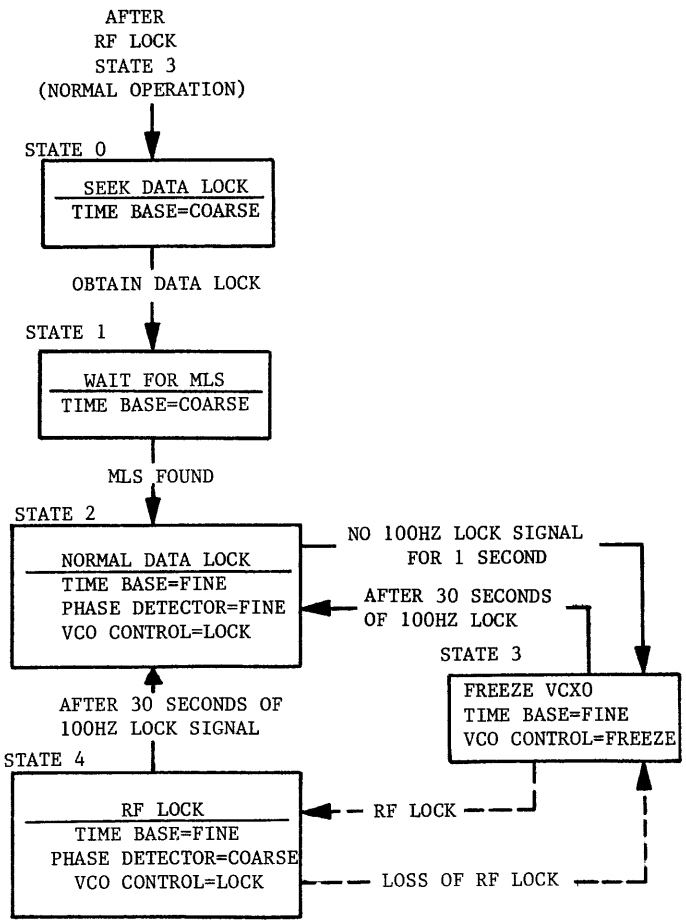


FIGURE 4-18 100Hz DATA LOCK STATE DIAGRAM

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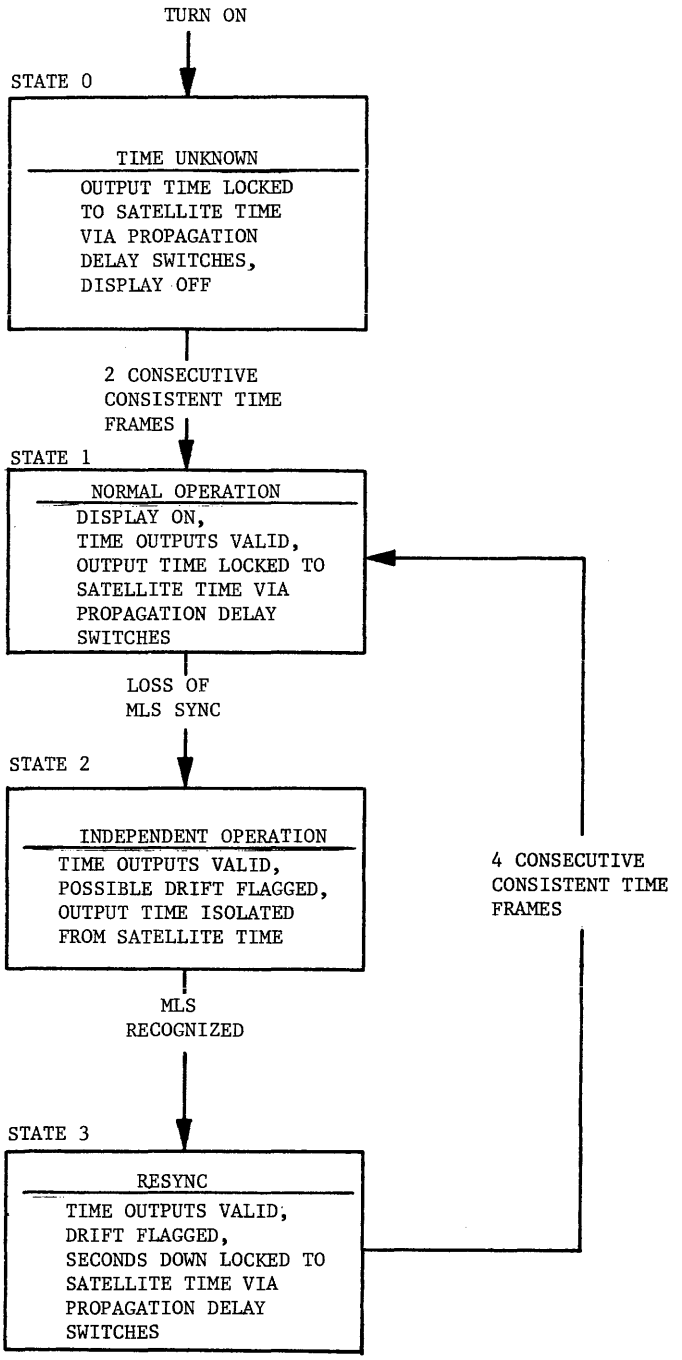


FIGURE 4-19 FRAME SYNC CONTROL STATE DIAGRAM

4-111 Understanding of FIGURE 4-18 and 4-19 will be facilitated by reference to FIGURE 4-20, which is a description of the format of the satellite signal.

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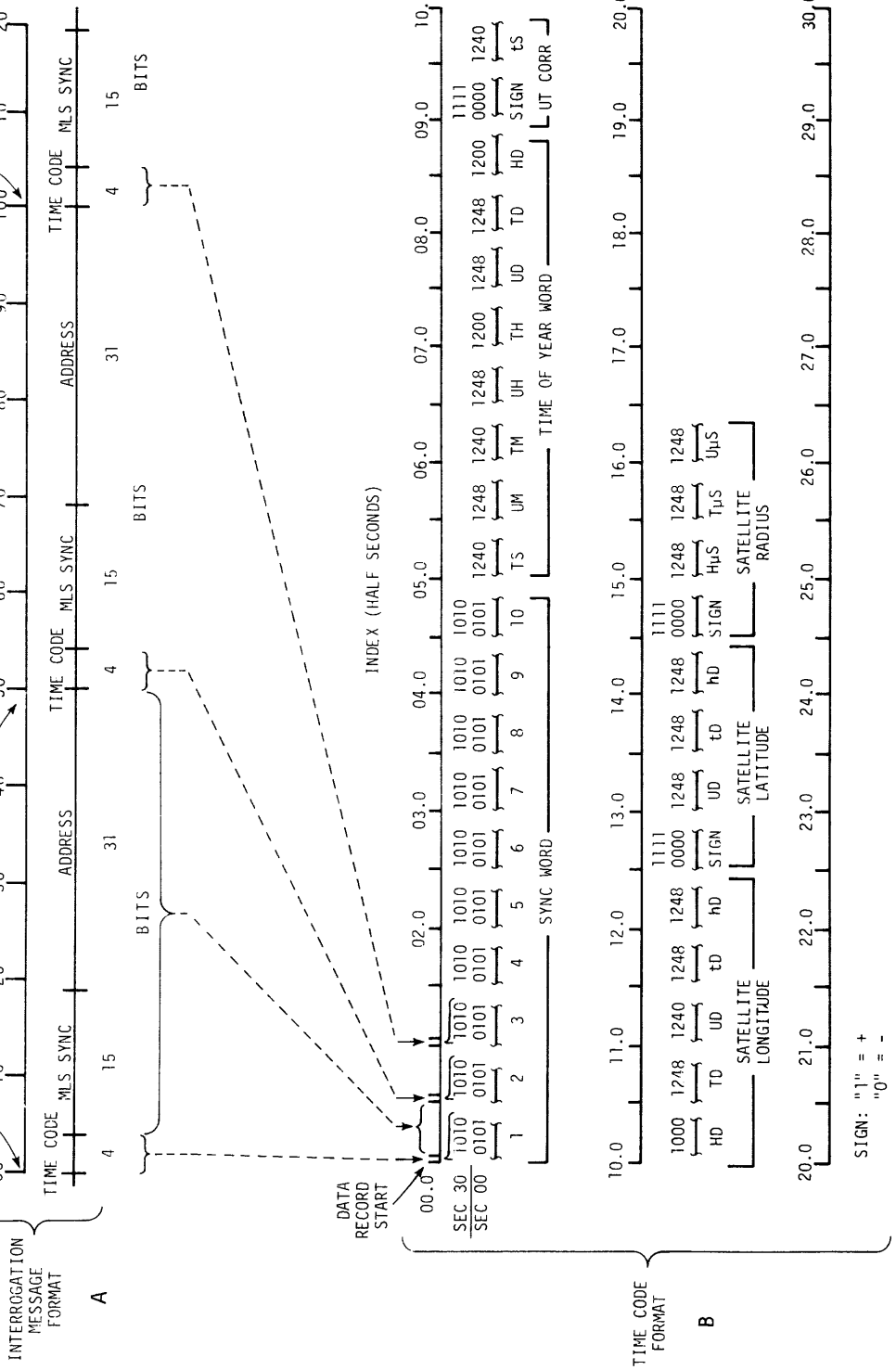


FIGURE 4-20 INTERROGATION MESSAGE AND TIME CODE FORMATS FROM N.B.S.TECHNICAL NOTE 681

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4-112 State 0 is entered a few seconds after normal RF lock is attained. The detection of MLS is an almost certain indication that lock to a functioning satellite has been obtained. There is no return to state 1, so the coarse timebase will not be used again.

4-113 When interference causes loss of lock during normal operation, state 3 is entered, freezing the timebase oscillator at its present frequency (or switching to an external timebase if one is provided). State 4 permits re-lock to the data after protracted loss of data lock has caused the timebase to drift out of the acquisition range of the fine data phase detector.

4-114 In state 0 at turn-on, "output time" commences from zero, indicating elapsed time, but is not displayed on the front panel. When two successive time frames agree, this time replaces the elapsed time, the time quality flags are brought low, and the display comes on.

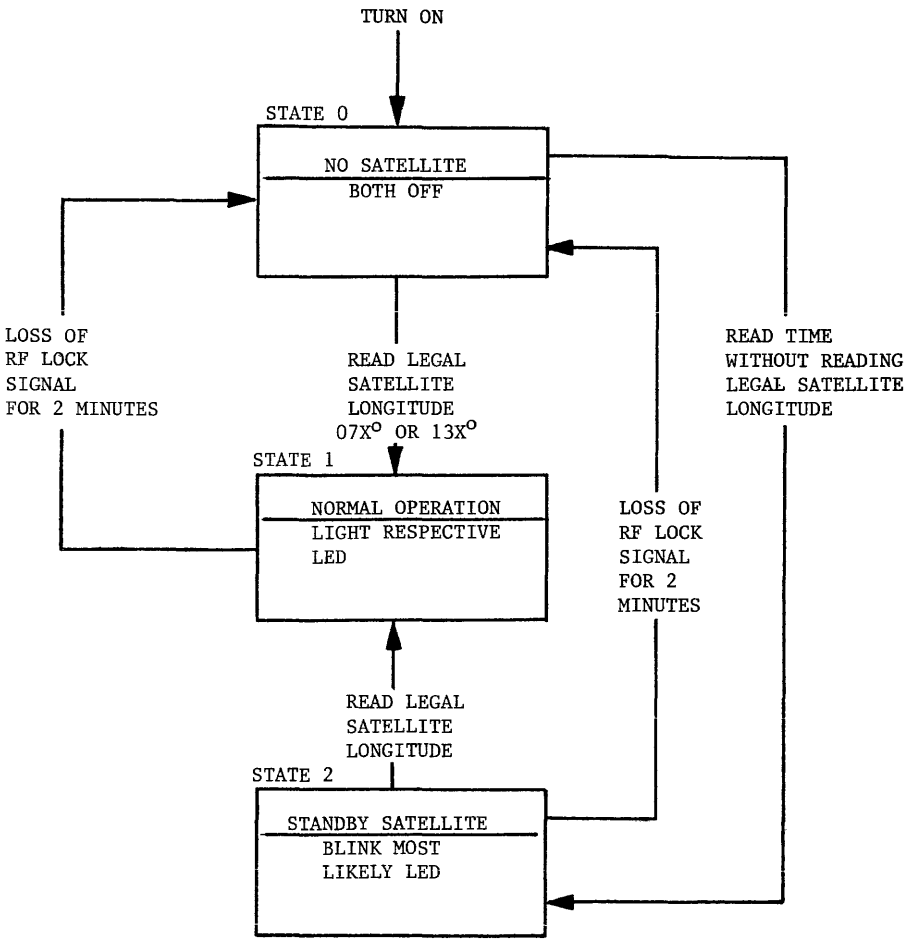


FIGURE 4-21 SATELLITE LED STATE DIAGRAM

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4-115 If satellite signal is lost, output time continues to update via the internal (or external) timebase. Meanwhile, the clock searches for the satellite signal and re-syncs to it without affecting the output time. This independence is achieved by not applying the propagation delay correction while in mode 2 unless the switch setting is changed. Since the timebase oscillator must still gain phaselock with the data, a slow drift of up to five milliseconds can occur during this time.

4-116 Once data lock is re-established, no further adjustments to the output time will occur until four (4) consecutive frames agree. At this point, the time quality flags go low and a time jump of an integral number of milliseconds can occur, to bring output time in sync with the new frame. Re-sync to the time frame requires four consistant frames to reduce the probability of incorrect time during adverse conditions.

4-117 The satellite LEDS are controlled by the received satellite longitude data. A position between 70 and 79 degrees west will light the east LED, while 130 to 139 degrees west lights the west LED.

4-118 A blinking LED indicates time lock without a legal longitude. The most common cause of this condition is reception of the back-up satellite at 105 degrees west during problems with one of the main satellites. East or west blinking merely indicates which sweep the processor is attempting; if the manual override switch on the analog board is in effect, no significance attaches to which of the two LEDs is blinking.

4-119 TIMING OUTPUTS

4-120 The timing outputs under software control are:
One Hertz
Slow Code
60 Hertz
IRIG-B
IRIG-H

4-121 One Hertz,the Slow Code, and 60 Hertz are all present beginning at power on. The IRIG time code outputs start after NBS time has been acquired. The IRIG-B time code transitions are within 40 microseconds of the data clock, the other outputs may lag by up to 300 microseconds. This difference arises from the fact that the IRIG-B output is pre-computed and output immediately after the data clock interrupt occurs, while the others are output as they are computed during the interrupt service.

4-122 Operation of the communications options, RS-232C and IEEE-488 are described separately. The program controlling these options runs with lowest priority on the 1 KHz interrupt, so there may be up to 300 microseconds jitter in these outputs.

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SECTION V

MAINTENANCE AND TROUBLESHOOTING

5-1 MAINTENANCE - MODEL 468-DC

5-2 Equipment needed:

1. RF Sweep Generator...HP8601A or equivalent
2. Oscilloscope.....1 MHz or greater bandwidth
3. Digital voltmeter....Greater than 10 Meg. input impedance
4. Frequency counter....Fluke 1900A or equivalent
5. Spectrum analyzer....HP 8558B/182T or equivalent

5-3 The Model 468-DC has been designed to provide maintenance free operation. The main instrument contains only seven adjustments, most of which will never require resetting. They are:

1. Third IF trim, a ceramic trimmer capacitor on Assembly 86-73, C9
2. Data symmetry, a trimpot on Assembly 86-74, R45
3. East sweep trim, a trimpot on Assembly 86-74, R38
4. West sweep trim, a trimpot on Assembly 86-74, R37
5. 10 MHz fine timebase trim, a trimpot on Assembly 86-74, R17
6. 1 MHz coarse timebase trim, a tunable coil on Assembly 86-74, L1
7. First L.O. peaking, a tunable coil on Assembly 86-74, T1

5-4 THIRD I.F. TRIM - ASSEMBLY 86-73

5-5 The sweep generator and the scope are needed for this adjustment which sets the third intermediate frequency to the center of the passband of the 4.5 MHz crystal filter T1, Y1, Y2, etc.

5-6 Connect the sweeper RF output through a blocking capacitor (0.1 UF) to the antenna input BNC. Set up the scope so the sweep output gives full scale horizontal deflection connecting the X axis to the sweep output, and 2V to 5V gives full vertical deflection. Connect the scope vertical input to TP3 on Assembly 86-74, the Analog Board. Set the sweeper to 4.500 MHz, 10 kHz sweep width, about 5 sweeps per second sweep rate, and -40 dbm output level. A faster sweep rate will distort the picture.

5-7 The display should appear as in FIGURE 5-1. The zero beat must occur in the center of the filter passband. If the zero beat is outside the -3 db points, C9 on Assembly 86-73 must be adjusted to bring it back into the center. This adjustment also affects receiver delay by up to 100 microseconds.

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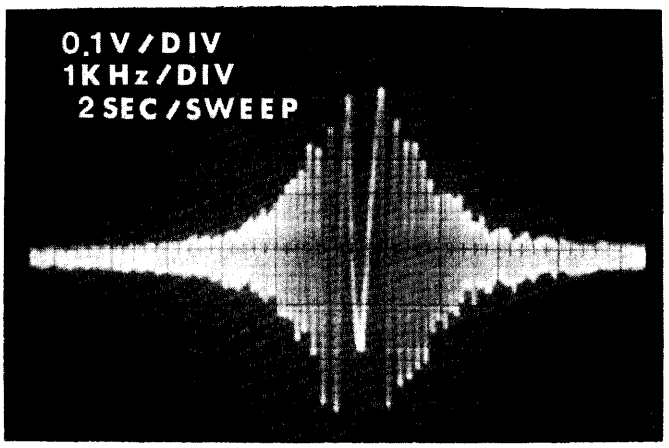


FIGURE 5-1 THIRD LOCAL OSCILLATOR ADJUSTMENT

5-8 DATA SYMMETRY ADJUSTMENT - ASSEMBLY 86-74

5-9 To adjust data symmetry, R45, the clock must be locked to a satellite. Connect the voltmeter to TP3, on Assembly 86-74 (see SECTION VI). A 6 second low pass is helpful for this adjustment. The FIGURE 4-23 shows the low pass filter which can be used. Adjust R45 (Assembly 86-74) for 0±0.2V. This adjustment also affects receiver delay up to 100 microseconds.

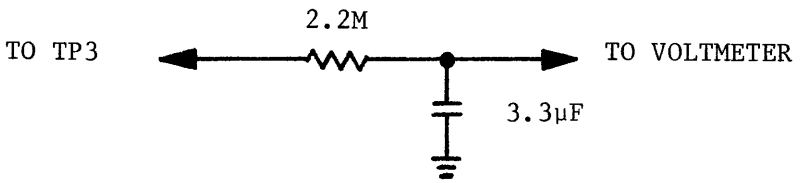


FIGURE 5-2 LOW PASS FILTER

5-10 EAST SWEEP TRIM - ASSEMBLY 86-74

5-11 Connect the frequency counter to the antenna input BNC (after removing the sweeper). Ground TP6 on the Analog Board (Assembly 86-74) and select the East Satellite with S2 (labeled "E"). Adjust R38, the center of the three-in-a-row trimpots, for a frequency of 18,643,400 +50 Hz. See SECTION VI, Assembly 86-74, for parts location of TP6, R38 and S2.

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5-12 WEST SWEEP TRIM - ASSEMBLY 86-74

5-13 Select the west sweep with S1 (labelled "W") and adjust R37 for a frequency of 18,642,650 ±50 Hz.

5-14 10 MHz FINE TIMEBASE TRIM, ASSEMBLY 86-74.

5-15 Ground TP8, attach the counter to TP12. Adjust R17 for 10,000,000 ±10 Hz (1 PPM). See SECTION VI, Assembly 86-74, for parts location.

5-16 1 MHz COARSE TIMEBASE, ASSEMBLY 86-74.

5-17 Ground the coarse oscillator control voltage at TP13. Connect the counter TP11. Adjust L1 (the shield can nearer the front of the instrument) for 1.000 MHz ±0.001 MHz.

5-18 FIRST LOCAL OSCILLATOR PEAKING, ASSEMBLY 86-74.

5-19 If a spectrum analyzer covering 18-40 MHz with 50 Ohm AC coupled input is available, see two sections below.

5-20 Connect the spectrum analyzer to the antenna input BNC connector. Tune T1 (the can near the back of the instrument) to minimize 37.3 MHz output while maximizing the 18.64 MHz output. The 18.64 MHz component will be about +15 dbm, the 37.3 MHz component about -15 dbm.

5-21 If no analyzer is available, make a dummy load using a 50 Ohm resister in series with a 0.1 micro F capacitor (see FIGURE 5-4). Connect this load to the antenna input BNC. Look at TP1 with a scope capable of responding to 20 MHz and tune T1 for maximum output.

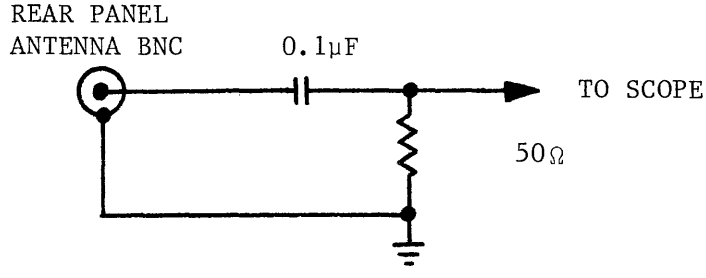


FIGURE 5-3 50 OHM DUMMY LOAD

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5-22 TROUBLESHOOTING

5-23 No exhaustive troubleshooting tree has been prepared. It is believed that a more effective approach is to give some hopefully useful hints to be used in conjunction with the "Theory of Operation" section. The circuitry in the instrument is relatively straightforward. Interaction with the program may vary with the options supplied. Therefore, in case of trouble:

5-24 First, make sure that suitable power is supplied to the instrument (fuse, switch).

5-25 Second, verify that an antenna is connected and that it has a relatively clear view of a satellite. (Trees can obstruct the signal, as will buildings). A DC voltmeter should read approximately +12V at the antenna end of the lead-in coax.

5-26 In some locations, land-mobile service interference on the west satellite frequency greatly delays time acquisition. Try the east.

5-27 When the clock is first turned on, the colons should blink; on one second, off one second, etc. If they don't, the program is probably not running. Take the cover off. Check that all connectors inside are making proper contact. With no antenna, both unlock LED'S on the analog board should be lit.

5-28 At this point, check all ten power supply voltages:

On the digital board ... +5V,-5V, +12V, -12V.

On the analog board ... +12V, +8V, two +5V, one -6V.

On the display board ... +180V (Red Wire).

5-29 If the processor board is running, as evidenced by blinking colons, check further in this section, if not, see next paragraph.

5-30 Check for 1 KHz interrupt at U4 (pin 19) on the processor board. If none present, look for trouble in the timing chain on the analog board.

5-31 Check that the processor clock at U1 pin 38 is 5.0 MHz and that U1 pin 37 is 1.24 MHz.

5-32 Check that reset (pin 40) is low for a fraction of a second at turn-on, then goes cleanly high and stays high.

5-33 Remove and re-insert the socketed chips in their sockets.

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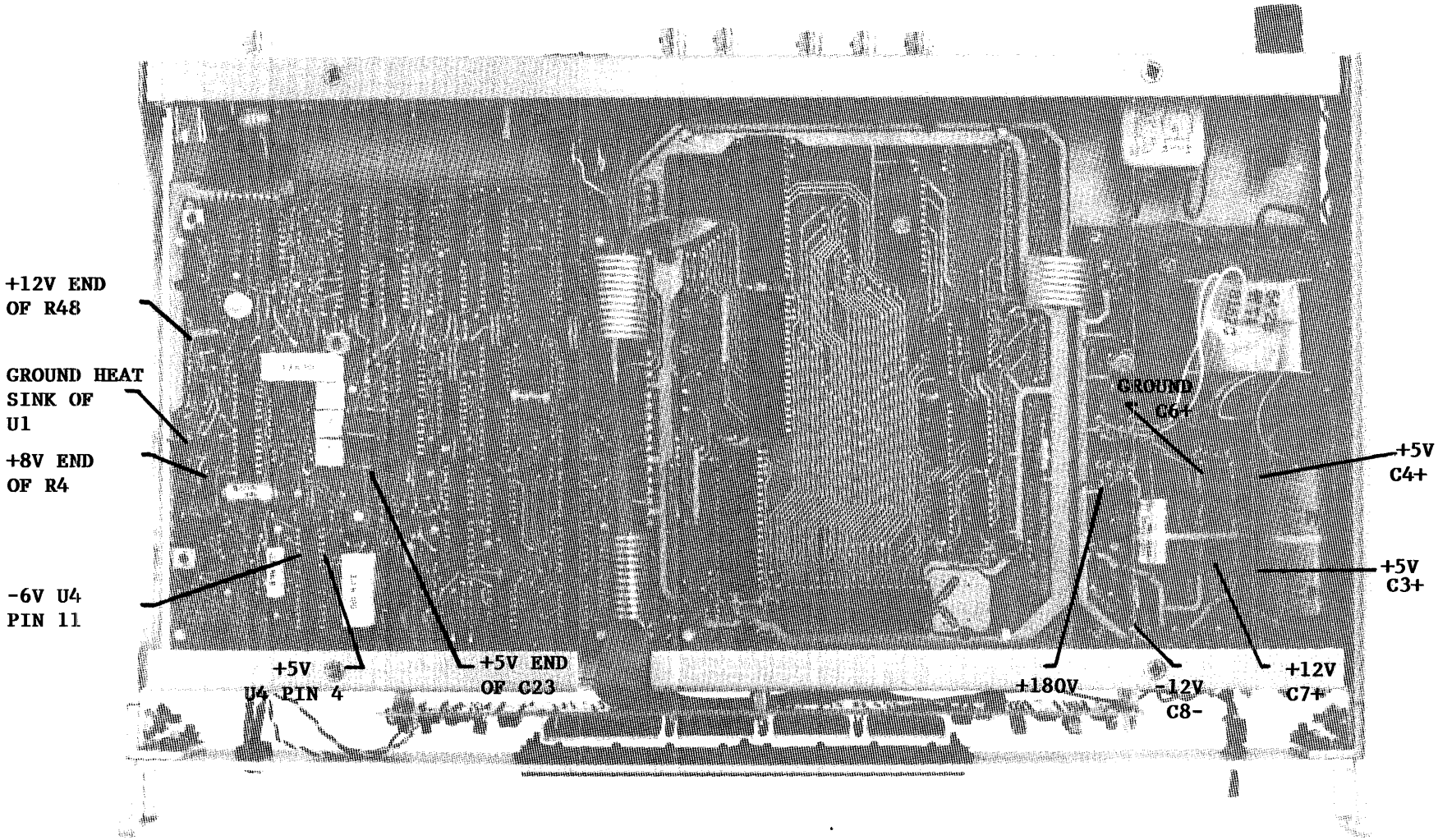


FIGURE 5-4 VOLTAGE TEST POINT LOCATIONS - MODEL 468-DC

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5-34 Check for the presence of the 1st local oscillator sweep voltage on TP6 of the analog board. This should be a slowly ramping DC voltage which begins at approximately -3.5v and ramps to approximately 4.0v. The period should be 40 seconds.

5-35 If the program is running, but no time comes on the display after a few minutes, look at or listen to J2 on the analog board.

5-36 At turn-on, there should be a few volts of audible noise present. You can easily see/hear the satellite signal as the receiver sweeps to it and locks. A marginally weak signal is hard to discern on the scope but easily audible on the speaker. A cassette tape of typical signal and interference conditions (with earphone) is available from the factory for this checkout. Contact Kinemetrics/TrueTime directly for this tape and earphone set. If no signal is present, there is probably a problem in the antenna. If a strong signal is observed, the antenna is OK and the problem is probably on the analog board (see paragraph later in this section).

5-37 If the antenna appears to be malfunctioning, and you don't want to return it to the factory, it is possible to open and check it. To open the antenna, cut the silicone rubber seal around the edge of the plastic bubble, pry off the bubble and take the flat plate antenna off the metal box, too. You should be looking at the 86-170 board.

5-38 If the green LED is lit and the red LED is not, the 86-70/71 board is probably OK. Also, if no noise was apparent at the TP3 on the analog board, the problem is likely in the I.F. amplifier, Q8 thru Q12.

5-39 Use of an RF sweeper greatly eases diagnosis and treatment of the I.F. board. Inject 21.4 MHz at the mixer I.F. port (end of R5 nearest the mixer). Locate R56 and ground the end which is nearest the center of the board. This is the AGC line.

5-40 Set the sweep width to 100 KHz and set the level to -37 dbm (3mv). You should get a rectangular passband 13 KHz wide at about 300 mv p-p when observing the drain of Q9 (end of R49 nearest edge of board) using a x10 scope probe.

5-41 If that's ok,move the scope probe to the drain of Q10. Here you should get a similiar passband and about 2 volts p-p amplitude with an input of -47 dbm (1 mv). If the second L.O. isn't running, no signal will be observed here.

5-42 Check the last two 4.5 MHz stages by looking at the drain of Q12. Here you should see about 2 volts p-p with an input of -97 dbm (3uv).

5-43 Remove the AGC ground. If the AGC and the control gates of the dual-gate mosfets are operating properly, you should see about 15 volts p-p of noise at the drain of Q12.

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5-44 If the problem is in L.O.multiplier, reference to the voltage chart, FIGURE 5-5, may prove useful. If proper operation cannot be obtained by replacing a defective transistor, it is recommended that the unit be returned to the factory for repair, since tuning of the UHF circuits is critical and inter-active. To use FIGURE 5-5, it is necessary to disable ALC on the multiplier chain. Do this by grounding TP2.

Supply Volts = 12.0
18.64 MHz Level = +12dbm

MEASUREMENT POINT	VOLTAGE	TOLERANCE
TP3	0.5v	0.1v
TP4	0.5v	0.1v
TP5	0.8v	0.2v
TP6	0.8v	0.2v
Q7 Collector	7.1v	0.4v
TP1	0.4v	0.1v

FIGURE 5-5 ASSEMBLY 86-71 VOLTAGE CHART

5-45 To continue, you will need the sweeper and spectrum analyzer.

5-46 Inject 18.64 MHz, sweep width 1 MHz, level 0 dbm into the multiplier input. Check the input high pass and bandpass filters by observing the base of Q3. You should see a peaked response at 18.64 MHz with a bandwidth (-6 db points) of approx. 1 MHz. Next look successively at the emitter current test points for the multiplier stages. Adjust each stage for widest peak of emitter current in the succeeding stage. Then adjust the 447 MHz helical filters for widest leveled response at TP8. Use of a spectrum analyzer will aid in avoiding the possibility of spurious responses.

5-47 Troubles on the detector board, Assembly 86-73, will show up as loss of signal going one direction or the other, and as mistuning of the third L.O., covered under "Maintenance".

5-48 Troubles on the analog board generally are due to op-amp outputs being stuck high or low, or analog switches latching up or leaking excessively. These kinds of problems can often be isolated by feeling the IC's for hot ones and by looking for stuck op-amp outputs with inputs inconsistent with the output state. Refer also to the "Theory of Operation" section for description of proper waveforms on the test points.

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5-49 TROUBLESHOOTING THE EXTERNAL OSCILLATOR (OPTION)

5-50 If D500 won't light when the external oscillator is connected, look at U7 (pin 9). You should see approximate TTL levels at half frequency. If D500 lights, but the clock doesn't appear to lock to the external oscillator when the antenna is pulled, check for drift between the waveforms at U7 (pin 3), 10 KHz, and U7 (pin 8), ext/2. Also check that U3 (pins 5 and 12) both go high.

5-51 TROUBLESHOOTING THE D.C. SUPPLY (OPTION)

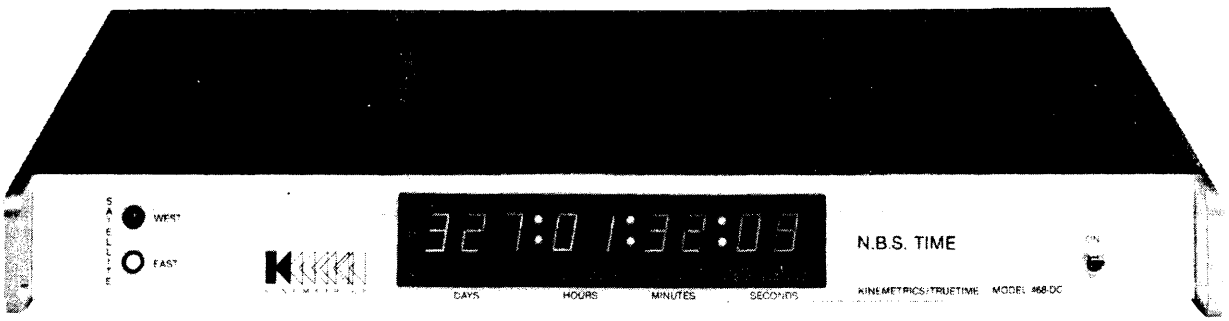
5-52 See SECTION IV, entitled D.C. POWER INPUT (Option).

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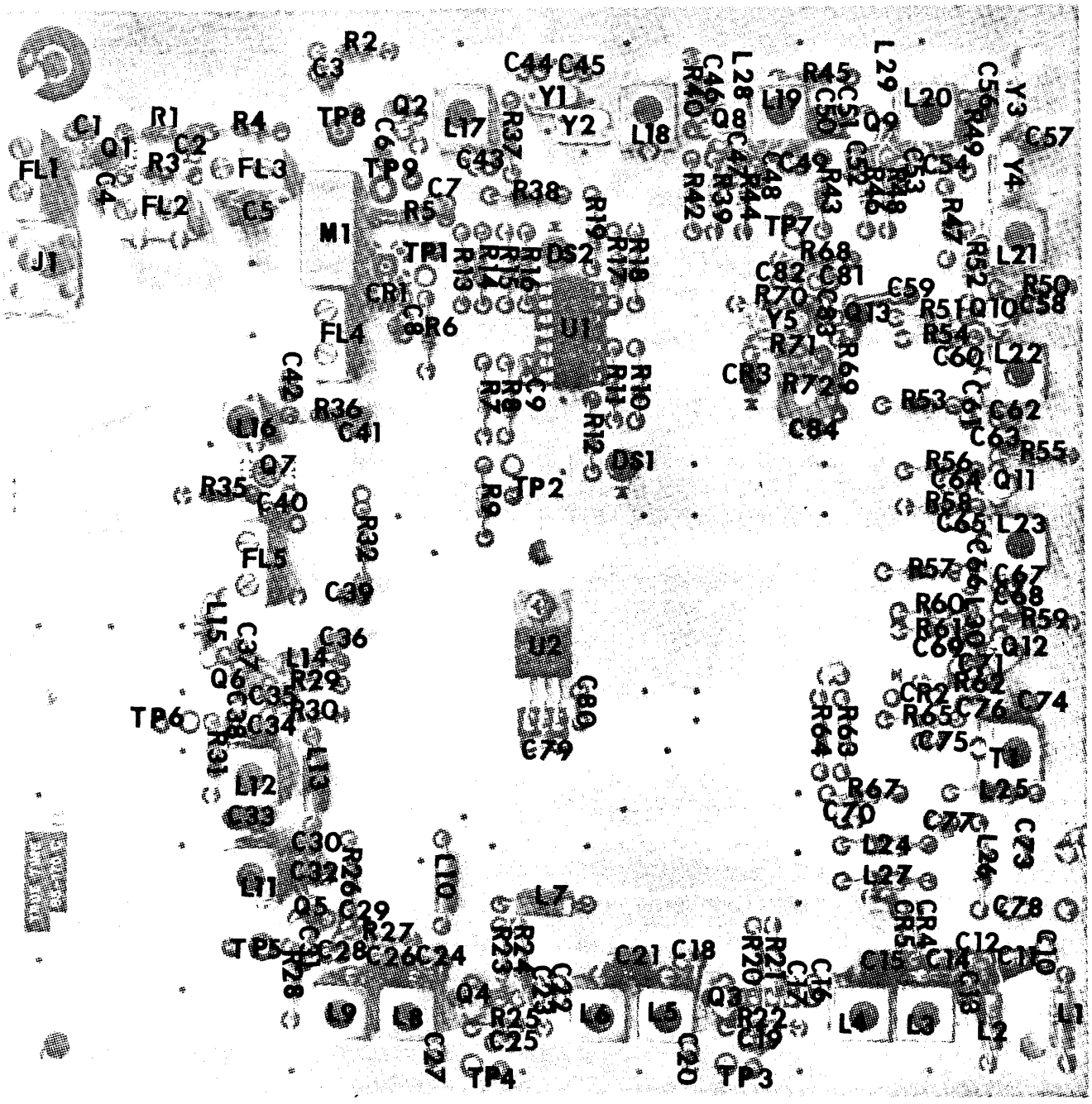
SECTION VI

SCHEMATICS AND PARTS LIST

MODEL 468-DC

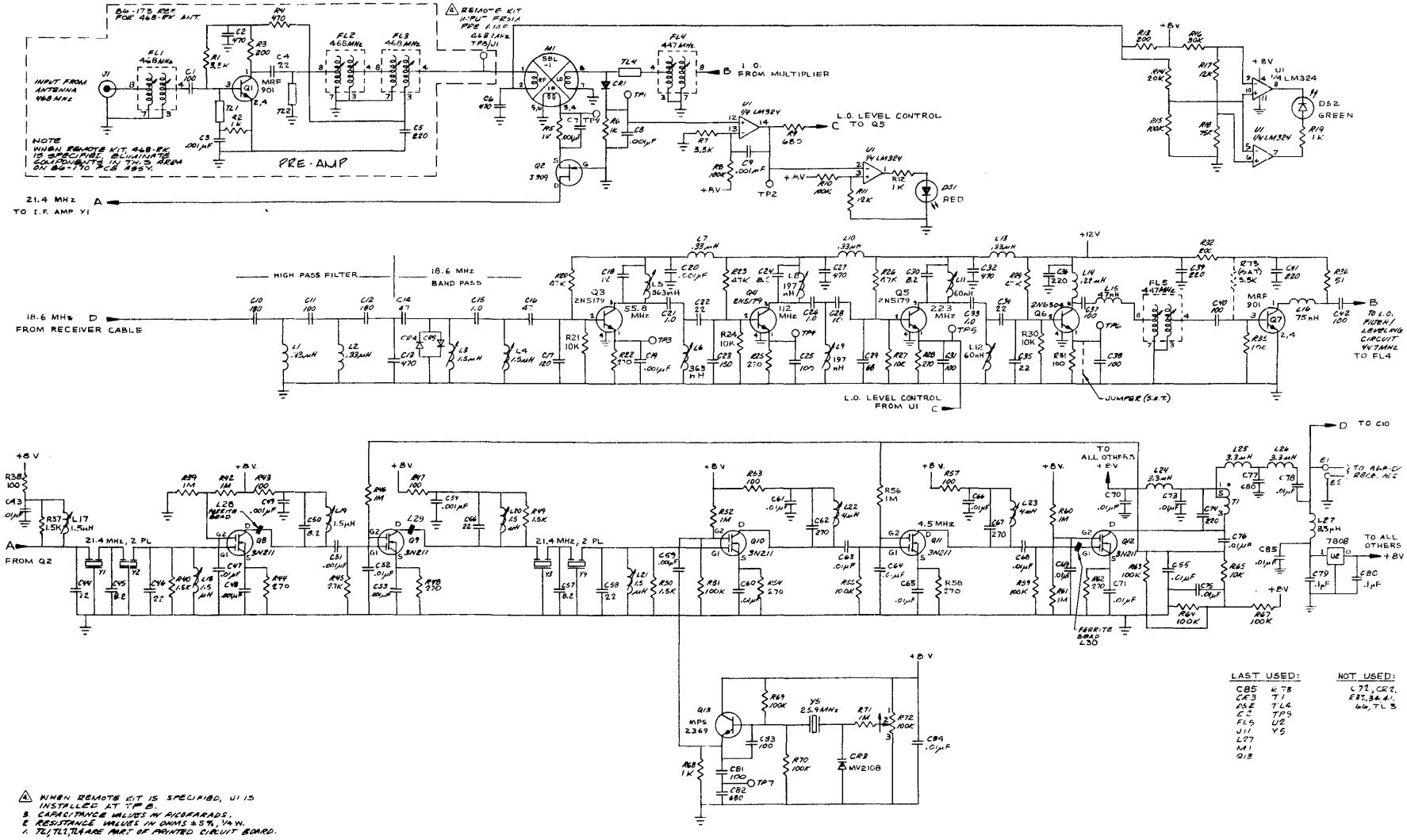


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6-1 PARTS LOCATION - ASSEMBLY 86-170

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6-2 SCHEMATIC - ASSEMBLY 86-170

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6-3 SYMBOL DESIGNATION REFERENCE 86-170

SYMBOL	KINEMETRICS/ TRIETIME PART NUMBER	DESCRIPTION
PCB	85-170	468MS MK II PCB
C1	36-33	Cap., Monolithic 100pF
C2	36-50	Cap., Monolithic 470pF
C3	36-58	Cap., Monolithic .001pF
C4	36-16	Cap., Monolithic 22pF
C5	36-41	Cap., Monolithic 220pF
C6	36-50	Cap., Monolithic 470pF
C7	36-58	Cap., Monolithic .001uF
C8	36-58	Cap., Monolithic .001uF
C9	36-58	Cap., Monolithic .001uF
C10	36-39	Cap., Monolithic 180pF
C11	36-33	Cap., Monolithic 100pF
C12	36-39	Cap., Monolithic 180pF
C13	36-50	Cap., Monolithic 470pF
C14	36-24	Cap., Monolithic 47pF
C15	36-01	Cap., Monolithic 1.0pF
C16	36-24	Cap., Monolithic 47pF
C17	36-35	Cap., Monolithic 120pF
C18	36-12	Cap., Monolithic 12pF
C19	36-58	Cap., Monolithic .001uF
C20	36-58	Cap., Monolithic .001uF
C21	36-01	Cap., Monolithic 1.0pF
C22	36-16	Cap., Monolithic 22pF
C23	36-37	Cap., Monolithic 150pF
C24	36-08	Cap., Monolithic 8.2pF
C25	36-33	Cap., Monolithic 100pF
C26	36-01	Cap., Monolithic 1.0pF
C27	36-50	Cap., Monolithic 470pF
C28	36-10	Cap., Monolithic 10pF
C29	36-29	Cap., Monolithic 68pF
C30	36-08	Cap., Monolithic 8.2pF
C31	36-33	Cap., Monolithic 100pF
C32	36-50	Cap., Monolithic 470pF
C33	36-01	Cap., Monolithic 1.0pF
C34	36-16	Cap., Monolithic 22pF
C35	36-16	Cap., Monolithic 22pF
C36	36-41	Cap., Monolithic 220pF
C37	36-33	Cap., Monolithic 100pF
C38	36-33	Cap., Monolithic 100pF
C39	36-41	Cap., Monolithic 220pF
C40	36-33	Cap., Monolithic 100pF
C41	36-41	Cap., Monolithic 220pF
C42	36-33	Cap., Monolithic 100pF
C43	36-83	Cap., Monolithic .01uF
C44	36-16	Cap., Monolithic 22pF
C45	36-08	Cap., Monolithic 8.2pF
C46	36-16	Cap., Monolithic 22pF
C47	36-58	Cap., Monolithic .001uF
C48	36-58	Cap., Monolithic .001uF
C49	36-58	Cap., Monolithic .001uF
C50	36-08	Cap., Monolithic 8.2pF
C51	36-58	Cap., Monolithic .001uF
C52	36-83	Cap., Monolithic .01uF
C53	36-58	Cap., Monolithic .001uF
C54	36-58	Cap., Monolithic .001uF
C55	36-83	Cap., Monolithic .01uF
C56	36-16	Cap., Monolithic 22pF
C57	36-08	Cap., Monolithic 8.2pF
C58	36-16	Cap., Monolithic 22pF
C59	36-58	Cap., Monolithic .001uF
C60	36-83	Cap., Monolithic .01uF
C61	36-83	Cap., Monolithic .01uF
C62	36-44	Cap., Monolithic 270pF
C63	36-83	Cap., Monolithic .01uF
C64	36-83	Cap., Monolithic .01uF
C65	36-83	Cap., Monolithic .01uF
C66	36-83	Cap., Monolithic .01uF
C67	36-44	Cap., Monolithic 270pF
C68	36-83	Cap., Monolithic .01uF
C69	36-83	Cap., Monolithic .01uF
C70	36-83	Cap., Monolithic .01uF
C71	36-83	Cap., Monolithic .01uF
C72		NOT USED
C73	36-83	Cap., Monolithic .01uF
C74	36-41	Cap., Monolithic 220pF
C75	36-83	Cap., Monolithic .01uF
C76	36-83	Cap., Monolithic .01uF
C77	36-54	Cap., Monolithic 680pF
C78	36-83	Cap., Monolithic .01uF
C79	36-95	Cap., Monolithic .1uF
C80	36-95	Cap., Monolithic .1uF
C81	36-33	Cap., Monolithic 100pF
C82	36-54	Cap., Monolithic 680pF
C83	36-33	Cap., Monolithic 100pF
C84	36-83	Cap., Monolithic .01uF
C85	36-83	Cap., Monolithic .01uF
CR1	57-5082-2800	Diode, Sch., H.P. 5082-2800
CR2	NOT USED	
CR3	35-8	Diode, Varicap, 2112
CR4	57-5082-2800	Diode, Sch., H.P. 5082-2800
CR5	57-5082-2800	Diode, Sch., H.P. 5082-2800
DS1	58-5	LED, Red, MV5053
DS2	58-1	LED, Green, MV5253
FL1	342-3	Filter, Hex. 468MHz
FL2	342-3	Filter, Hex. 468MHz
FL3	342-3	Filter, Hex. 468MHz
FL4	342-4	Filter, Hex. 447MHz
FL5	342-4	Filter, Hex. 447MHz
J1	381-1A	Connector, SMA, Flange Mt.
L1	45-.33	Choke, RF, .33uH, Molded
L2	45-.33	Choke, RF, .33uH, Molded
L3	45-1.5	Coil, 1.5uH, Var.
L4	45-1.5	Coil, 1.5uH, Var.
L5	45-.363	Coil, 363nH, Var., 9-1/2 Turns
L6	45-.363	Coil, 363nH, Var., 9-1/2 Turns
L7	45-.33	Choke, RF, .33uH, Molded
L8	45-.197	Coil, 197nH, Var., 5-1/2 Turns
L9	45-.197	Coil, 197nH, Var., 5-1/2 Turns
L10	45-.33	Choke, RF, .33uH, Molded
L11	45-.06	Coil, 60nH, Var., 1-1/2 Turns
L12	45-.06	Coil, 60nH, Var., 1-1/2 Turns
L13	45-.33	Choke, RF, .33uH, Molded
L14	45-.22	Choke, .22uH, RF, Molded

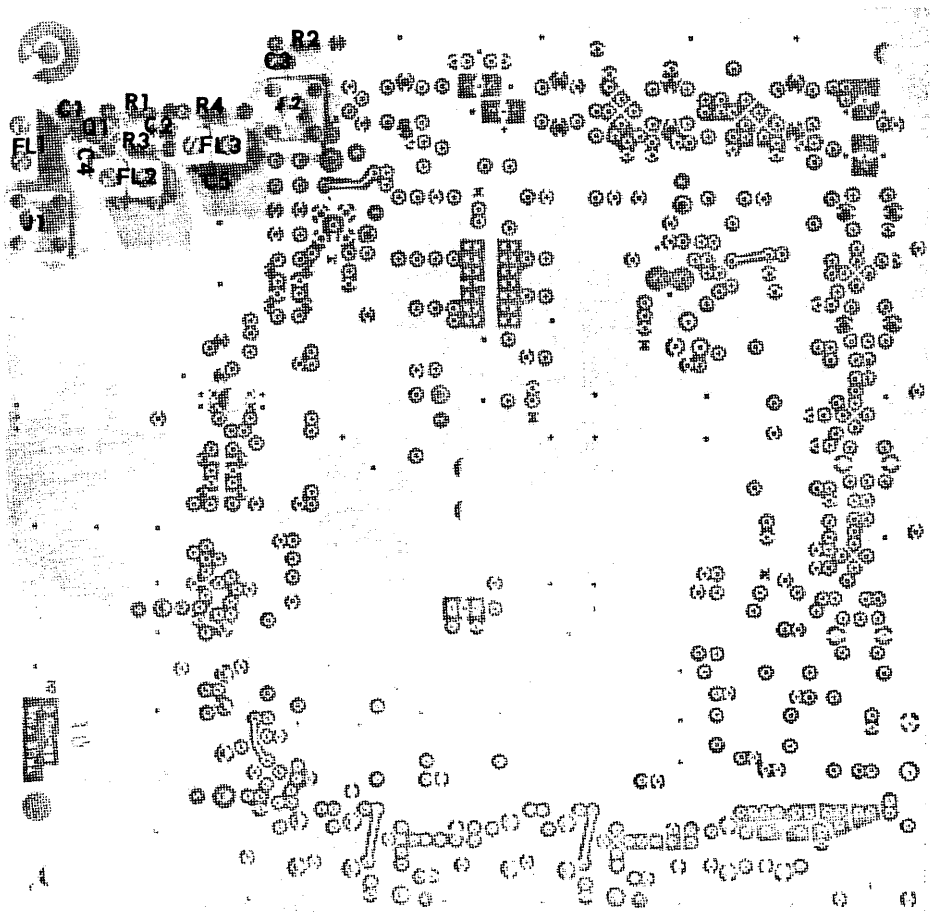
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SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
L15	45-.047	Choke, 47nH, RF, Molded
L16	45-.075	Coil, 75nH, Core Removed
L17	45-1.5	Coil, 1.5uH, Var.
L18	45-1.5	Coil, 1.5uH, Var.
L19	45-1.5	Coil, 1.5uH, Var.
L20	45-1.5	Coil, 1.5uH, Var.
L21	45-1.5	Coil, 1.5uH, Var.
L22		See "T" Section
L23		See "T" Section
L24	45-3.3	Coil, 3.3uH, RF, Molded
L25	45-3.3	Coil, 3.3uH, RF, Molded
L26	45-3.3	Coil, 3.3uH, RF, Molded
L27	45-3.3	Coil, 3.3uH, RF, Molded
L28	41-0	Ferrite Bead (For Q8)
L29	41-0	Ferrite Bead (For Q9)
L30	41-0	Ferrite Bead (For Q12)
M1	50-1	Mixer, 1-500 MHz, SBL-1
Q1	175-901	Transistor, H.F., NPN, MRF901
Q2	175-309	Transistor, JFET, TO-92,J309
Q3	175-5179	Transistor, NPN, TO-72, 2N5179
Q4	175-5179	Transistor, NPN, TO-72, 2N5179
Q5	175-5179	Transistor, NPN, TO-72, 2N5179
Q6	175-6304	Transistor, High Freq., NPN, 2N6304
Q7	175-901	Transistor, H.F., NPN, MRF901
Q8	175-211	Transistor, MOSFET, TO-72, 3N211
Q9	175-211	Transistor, MOSFET, TO-72, 3N211
Q10	175-211	Transistor, MOSFET, TO-72, 3N211
Q11	175-211	Transistor, MOSFET, TO-72, 3N211
Q12	175-211	Transistor, MOSFET, TO-72, 3N211
Q13	175-2369	Transistor, Sw., NPN,TO-92, MPS2369
ALL RESISTORS 1/4 WATT, +5% CARBON COMP. UNLESS OTHERWISE NOTED.		
R1	02-85	Resistor, 3.3K
R2	02-73	Resistor, 1K
R3	02-56	Resistor, 200 ohms
R4	02-65	Resistor, 470 ohms
R5	02-73	Resistor, 1K
R6	02-73	Resistor, 1K
R7	02-85	Resistor, 3.3K
R8	02-121	Resistor, 100K
R9	02-69	Resistor, 680 ohms
R10	02-121	Resistor, 100K
R11	02-99	Resistor, 12K
R12	02-73	Resistor, 1K
R13	02-56	Resistor, 200 ohms
R14	02-104	Resistor, 20K
R15	02-121	Resistor, 100K
R16	02-108	Resistor, 30K
R17	02-99	Resistor, 12K
R18	02-118	Resistor, 75K
R19	02-73	Resistor, 1K
R20	02-113	Resistor, 47K
R21	02-97	Resistor, 10K
R22	02-59	Resistor, 270 ohms
R23	02-113	Resistor, 47K
R24	02-97	Resistor, 10K
R25	02-59	Resistor, 270 ohms
R26	02-113	Resistor, 47K
R27	02-97	Resistor, 10K

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
R28	02-59	Resistor, 270 ohms
R29	02-113	Resistor, 47K
R30	02-97	Resistor, 10K
R31	02-49	Resistor, 100 ohms
R32	02-56	Resistor, 200 ohms
R33		NOT USED
R34		NOT USED
R35	02-49	Resistor, 100 ohms
R36	02-42	Resistor, 51 ohms
R38	02-49	Resistor, 100 ohms
R37	02-77	Resistor, 1.5K
R39	02-145	Resistor, 1M
R40	02-77	Resistor, 1.5K
R41		NOT USED
R42	02-145	Resistor, 1M
R43	02-49	Resistor, 100 ohms
R44	02-59	Resistor, 270 ohms
R45	02-83	Resistor, 2.7K
R46	02-145	Resistor, 1M
R47	02-49	Resistor, 100 ohms
R48	02-59	Resistor, 270 ohms
R49	02-77	Resistor, 1.5K
R50	02-77	Resistor, 1.5K
R51	02-121	Resistor, 100K
R52	02-145	Resistor, 1M
R53	02-49	Resistor, 100 ohms
R54	02-59	Resistor, 270 ohms
R55	02-121	Resistor, 100K
R56	02-145	Resistor, 1M
R57	02-49	Resistor, 100 ohms
R58	02-59	Resistor, 270 ohms
R59	02-121	Resistor, 100K
R60	02-145	Resistor, 1M
R61	02-145	Resistor, 1M
R62	02-59	Resistor, 270 ohms
R63	02-121	Resistor, 100K
R64	02-121	Resistor, 100K
R65	02-97	Resistor, 10K
R66		NOT USED
R67	02-121	Resistor, 100K
R68	02-73	Resistor, 1K
R69	02-121	Resistor, 100K
R70	02-121	Resistor, 100K
R71	02-145	Resistor, 1M
R72	20-7	Potentiometer, 100K
T1	52-4	Transformer, 4uH, 4.5 MHz
L22	52-4	Transformer, 4uH, 4.5 MHz
L23	52-4	Transformer, 4uH, 4.5 MHz
U1	176-324	I.C., Op. Amp., LM324
U2	176-7808	I.C., Reg., LM7808
Y1	59-21400	Crystal, Monolithic, Filter, 21.4 MHz
Y2	59-21400	Crystal, Monolithic, Filter, 21.4 MHz
Y3	59-21400	Crystal, Monolithic, Filter, 21.4 MHz
Y4	59-21400	Crystal, Monolithic, Filter, 21.4 MHz
Y5	59-25900	Crystal, Osc., 25.9 MHz

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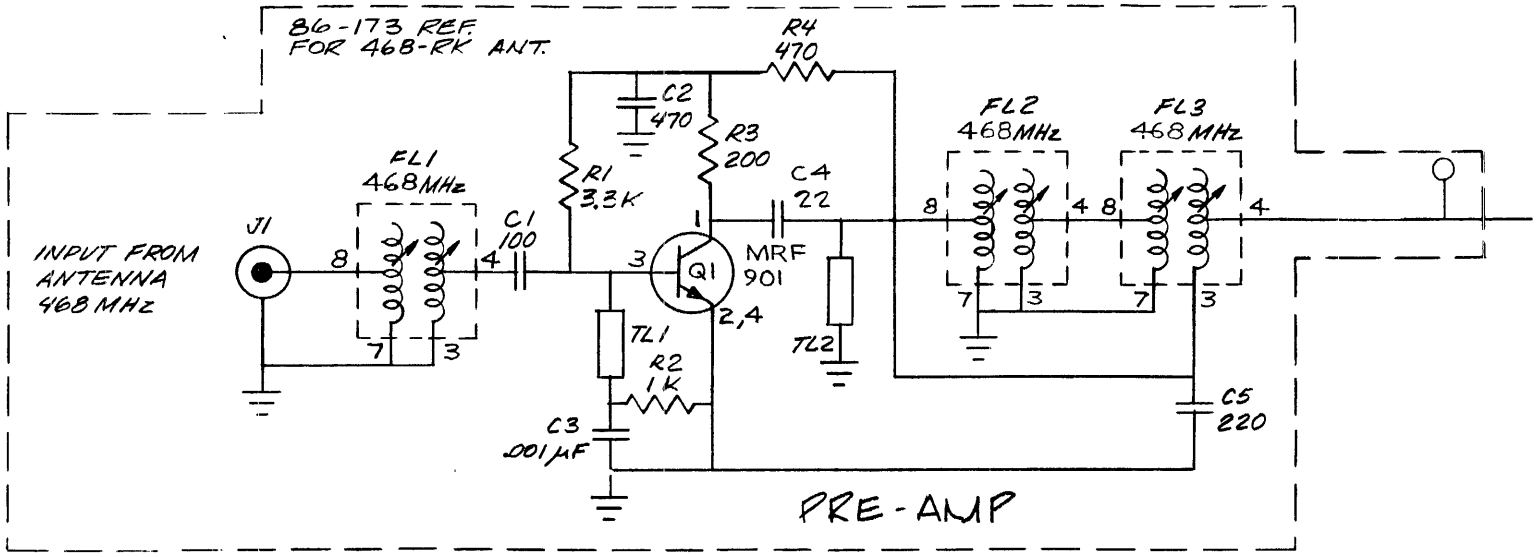
6-4 PARTS LOCATION - ASSEMBLY 86-173



6-5 SYMBOL DESIGNATION REFERENCE 86-173

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	36-33	Cap., Monolithic, 100pF
C2	36-50	Cap., Monolithic, 470pF
C3	36-58	Cap., Monolithic, .100pF
C4	36-33	Cap., Monolithic, 100pF
C5	36-41	Cap., Monolithic, 220pF
FL1	342-3	Filter, Hex. 468 MHz
FL2	342-3	Filter, Hex. 468 MHz
FL3	342-3	Filter, Hex. 468 MHz
J1	381-1A	Connector, Receptacle
J2	381-1A	Connector, Receptacle
PCB	85-170	468 MHz Pre-Amp PCB Fab.
Q1	175-901	Transistor, MRF 901
	ALL RESISTORS 1/4 WATT, +5% CARBON COMP. UNLESS OTHERWISE NOTED.	
R1	2-85	Resistor, 3.3K
R2	2-73	Resistor, 1K
R3	2-56	Resistor, 200 ohm
R4	2-65	Resistor, 470 ohm

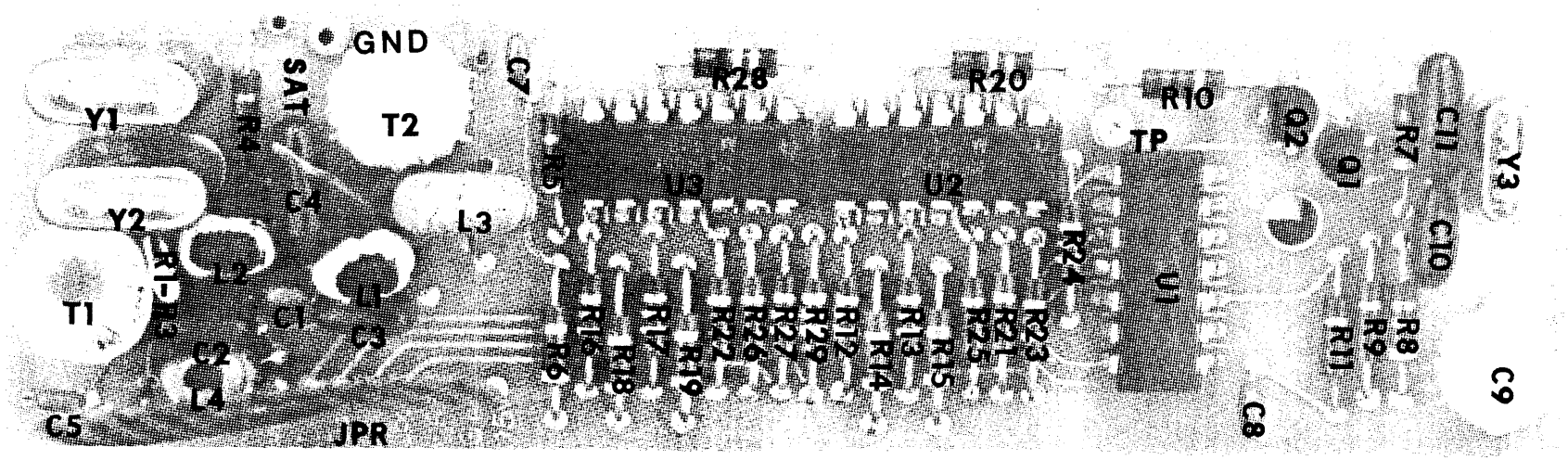
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6-6 SCHEMATIC - ASSEMBLY 86-173

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6-7 PARTS LOCATION - ASSEMBLY 86-73



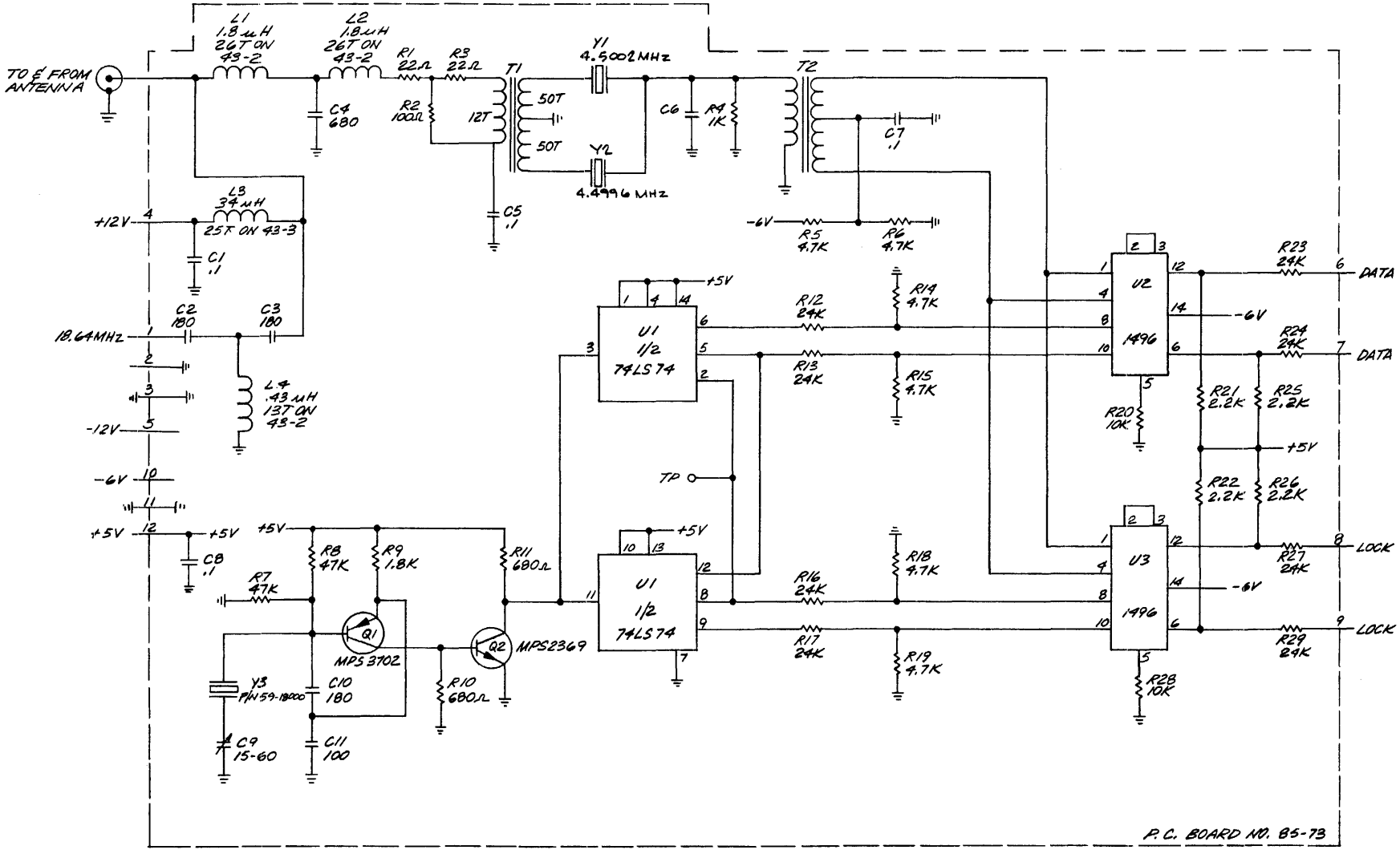
6-8 SYMBOL DESIGNATION REFERENCE 86-73

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	36-95	Cap., Monolithic .1uF
C2	29-39	Cap., Dipped Mica 180pF
C3	29-39	Cap., Dipped Mica 180pF
C4	29-54	Cap., Dipped Mica 680pF
C5	36-95	Cap., Monolithic .1uF
C6		SELECT AT TEST
C7	36-95	Cap., Monolithic .1uF
C8	36-95	Cap., Monolithic .1uF
C9	33-60	Cap. Cer. Var. 15-60pF
C10	29-30	Cap., Dipped Mica 180pF
C11	29-33	Cap., Dipped Mica 100pF
JPR	387-12	"Flexstrip" Jumper, 12 Pin
L1	43-2	Coil Assembly (42-40)
L2	43-2	Coil Assembly (42-40)
L3	43-3	Coil Assembly (42-38)
L4	43-2	Coil Assembly (42-35)
PCB	85-73	Detector PCB FAB
Q1	175-3702	Transistor MPS3702
Q2	175-2369	Transistor MPS2369

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
ALL RESISTORS 1/4 Watt, ±5% CARBON COMP. UNLESS OTHERWISE NOTED.		
R1	2-33	Resistor, 22 ohm
R2	2-49	Resistor, 100 ohm
R3	2-33	Resistor, 22 ohm
R4	2-73	Resistor, 1K
R5	2-89	Resistor, 4.7K
R6	2-89	Resistor, 4.7K
R7	2-113	Resistor, 47K
R8	2-113	Resistor, 47K
R9	2-79	Resistor, 1.8K
R10	2-69	Resistor, 680 ohm
R11	2-69	Resistor, 680 ohm
R12	2-106	Resistor, 24K
R13	2-106	Resistor, 24K
R14	2-89	Resistor, 4.7K
R15	2-89	Resistor, 4.7K
R16	2-106	Resistor, 24K
R17	2-106	Resistor, 24K
R18	2-89	Resistor, 4.7K
R19	2-89	Resistor, 4.7K
R20	2-97	Resistor, 10K

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
R21	2-81	Resistor, 2.2K
R22	2-81	Resistor, 2.2K
R23	2-106	Resistor, 24K
R24	2-106	Resistor, 24K
R25	2-81	Resistor, 2.2K
R26	2-81	Resistor, 2.2K
R27	2-106	Resistor, 24K
R28	2-97	Resistor, 10K
R29	2-106	Resistor, 24K
T1	43-3	Toroid (42-42)
T2	43-3	Toroid (42-43)
U1	176-74LS74	I.C. 74LS74
U2	176-1496	I.C. 1496
U3	176-496	I.C. 1496
Y1	59-4499A	Crystal 4.5002 MHz
Y2	59-4499	Crystal, 4.4996 MHz
Y3	49-18000	Crystal, 18.000 MHz
	43-100	Base, Toroid

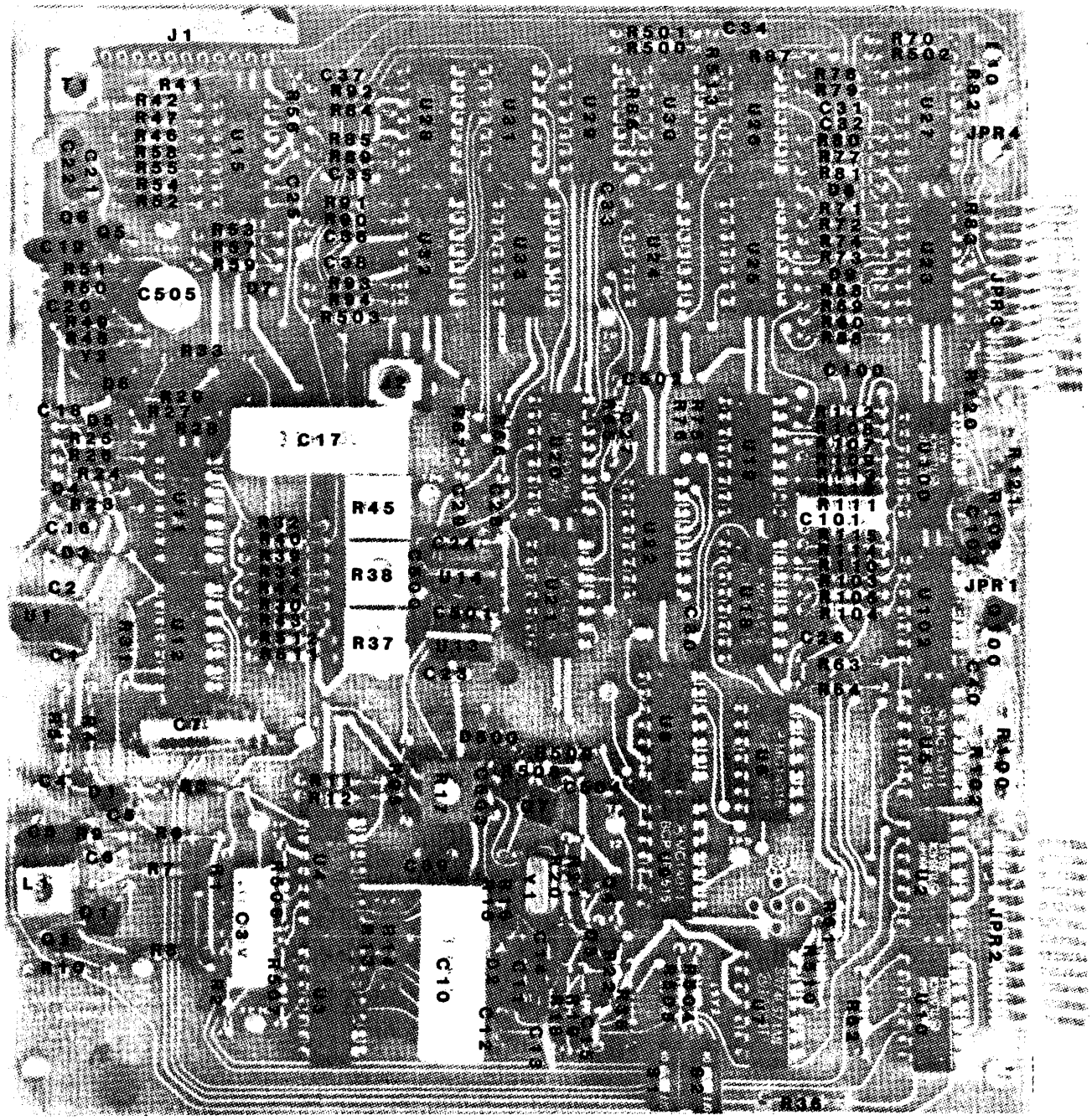
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6-9

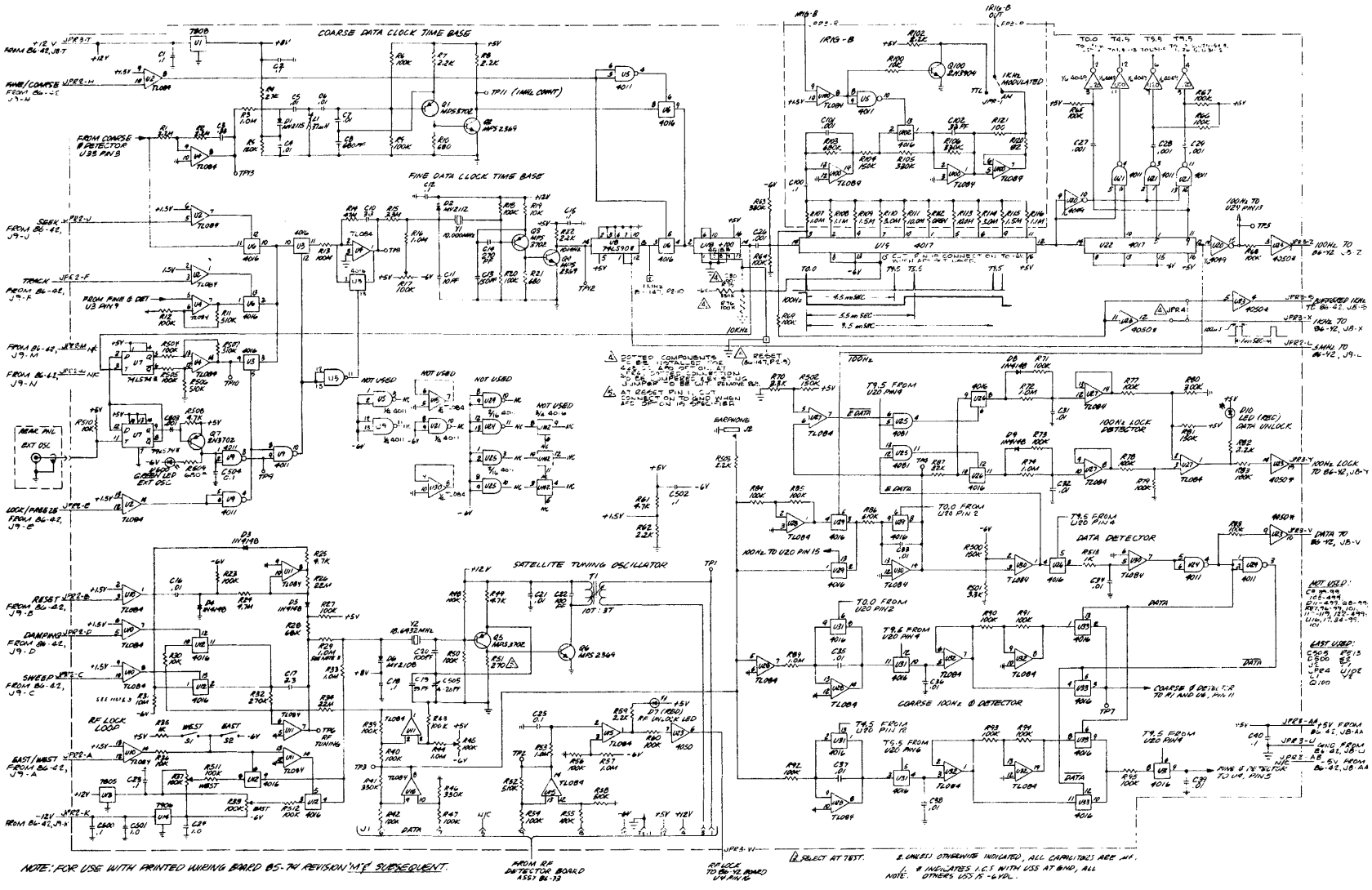
6-9 SCHEMATIC - ASSEMBLY 86-73

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6-10 PARTS LOCATION - ASSEMBLY 86-74

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6-11 SCHEMATIC - ASSEMBLY 86-74

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6-12 SYMBOL DESIGNATION REFERENCE 86-74

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	36-95	Cap., Monolithic .1uF
C2	36-95	Cap., Monolithic .1uF
C3	36-32	Cap., Film, .33uF
C4	36-83	Cap., Monolithic .01uF
C5	36-83	Cap., Monolithic .01uF
C6	36-83	Cap., Monolithic .01uF
C7	24-13	Cap., Polystyrene .01uF
C8	29-54	Cap., Dipped Mica 680pF
C9		NOT USED
C10	28-43	Cap., Film 3.3uF
C11	29-10	Cap., Dipped Mica 10pF
C12	36-95	Cap., Monolithic .1uF
C13	29-37	Cap., Dipped Mica 150pF
C14	29-44	Cap., Dipped Mica 270pF
C15	36-95	Cap., Monolithic .1uF
C16	36-83	Cap., Monolithic .01uF
C17	28-43	Cap., Film 3.3uF
C18	36-95	Cap., Monolithic .1uF
C19	29-22	Cap., Dipped Mica 39pF
C20	29-33	Cap., Dipped Mica 100pF
C21	36-83	Cap., Monolithic .01uF
C22	29-33	Cap., Dipped Mica 100pF
C23	36-95	Cap., Monolithic .1uF
C24	32-29	Cap., Tant 0.1uF
C25	36-95	Cap., Monolithic .1uF
C26	24-1	Cap., Polystyrene .001uF
C27	24-1	Cap., Polystyrene .001uF
C28	24-1	Cap., Polystyrene .001uF
C29	24-1	Cap., Polystyrene .001uF
C30		NOT USED
C31	36-83	Cap., Monolithic .01uF
C32	36-83	Cap., Monolithic .01uF
C33	36-83	Cap., Monolithic .01uF
C34	36-83	Cap., Monolithic .01uF
C35	36-83	Cap., Monolithic .01uF
C36	36-83	Cap., Monolithic .01uF
C37	36-83	Cap., Monolithic .01uF
C38	36-83	Cap., Monolithic .01uF
C39	36-83	Cap., Monolithic .01uF
C40	36-95	Cap., Monolithic .1uF
C41-99		NOT USED
C100	36-95	Cap., Monolithic .1uF
C101	24-1	Cap., Polystyrene .001uF
C102	29-20	Cap., Dipped Mica 33pF
C103-499		NOT USED
C500	36-95	Cap., Monolithic .1uF
C501	32-29	Cap., Tant. 0.1uF
C502	36-95	Cap., Monolithic .1uF
C503	36-58	Cap., Monolithic .001uF
C504	36-95	Cap., Monolithic .1uF
C505	33-20	Cap., Cer. Var. 4-20pF
D1	35-15	Varicap MV2115
D2	35-12	Varicap MV2112
D3	57-4148	Diode 1N4148
D4	57-4148	Diode 1N4148
D5	57-4148	Diode 1N4148
D6	35-8	Varicap MV2108
D7	58-4	LED-Red
D8	57-4148	Diode 1N4148
D9	57-4148	Diode 1N4148
D10	58-4	LED-Red
D11-499		NOT USED
D500	58-1	LED-Green
J1	318-25	Socket, 12 Pin Strip (318-12)
J2	369-2	Jack, Earphone
JPR-1	387-12	"Flexstrip - 12 Pin
JPR-2	387-12	"Flexstrip - 12 Pin
JPR-3	387-12	"Flexstrip - 12 Pin
L1	41-6A	Coil, R.F. 942-44)
PCB	85-74	Analog PCB Fabrication
Q1	175-3702	Transistor MPS3702
Q2	175-2369	Transistor MPS2369
Q3	175-3702	Transistor MPS3702
Q4	175-2369	Transistor MPS2369
Q5	175-3702	Transistor MPS3702
Q6	175-2369	Transistor MPS2369
Q7	175-3702	Transistor MPS3702
Q8-99		not used
Q100	175-3904	Transistor 2N3904

NOTE: ALL RESISTORS ARE 1/4 WATT, 5% CARBON COMP. UNLESS OTHERWISE NOTED.

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
R1	2-153	Resistor, 2.2M
R2	2-153	Resistor, 2.2M
R3	2-145	Resistor, 1.0M
R4	2-107	Resistor, 27K
R5	2-123	Resistor, 120K
R6	2-121	Resistor, 100K
R7	2-81	Resistor, 2.2K
R8	2-81	Resistor, 2.2K
R9	2-121	Resistor, 100K
R10	2-69	Resistor, 680 ohm
R11	2-138	Resistor, 510K
R12	2-121	Resistor, 100K
R13	2-203	Resistor, 100M
R14	2-186	Resistor, 47M
R15	2-157	Resistor, 3.3M
R16	2-145	Resistor, 1.0M
R17	20-7	100K Var. Pot.
R18	2-121	Resistor, 100K
R19	2-97	Resistor, 10K
R20	2-121	Resistor, 100K
R21	2-69	Resistor, 680 ohm
R22	2-81	Resistor, 2.2K
R23	2-121	Resistor, 100K
R24	2-161	Resistor, 4.7M
R25	2-89	Resistor, 4.7K
R26	2-177	Resistor, 22M
R27	2-121	Resistor, 100K
R28	2-117	Resistor, 68K
R29	2-145	Resistor, 1.0M
R30	2-97	Resistor, 10K
R31	2-169	Resistor, 10M
R32	2-131	Resistor, 270K
R33	2-145	Resistor, 1.0M
R34	2-177	Resistor, 22M
R35	2-73	Resistor, 1K
R36	2-97	Resistor, 10K
R37	20-7	Pot., 100K Var.
R38	20-7	Pot., 100K Var.
R39	2-121	Resistor, 100K
R40	2-121	Resistor, 100K
R41	2-133	Resistor, 330K
R42	2-121	Resistor, 100K
R43	2-121	Resistor, 100K

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SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
R44	2-145	Resistor, 1.0M
R45	20-7	Pot., 100K Var.
R46	2-133	Resistor, 330K
R47	2-121	Resistor, 100K
R48	2-121	Resistor, 100K
R49	2-89	Resistor, 4.7K
R50	2-121	Resistor, 100K
R51	2-59	Resistor, 270 ohm
R52	2-138	Resistor, 510K
R53	2-145	Resistor, 1.0M
R54	2-121	Resistor, 100K
R55	2-121	Resistor, 100K
R56	2-121	Resistor, 100K
R57	2-145	Resistor, 1.0M
R58	2-138	Resistor, 510M
R59	2-81	Resistor, 2.2K
R60	2-121	Resistor, 100K
R61	2-89	Resistor, 4.7K
R62	2-81	Resistor, 2.2K
R63	2-133	Resistor, 330K
R64	2-121	Resistor, 100K
R65	2-121	Resistor, 100K
R66	2-121	Resistor, 100K
R67	2-121	Resistor, 100K
R68	2-121	Resistor, 100K
R69	2-121	Resistor, 100K
R70	2-85	Resistor, 100K
R71	2-121	Resistor, 100K
R72	2-145	Resistor, 1.0M
R73	2-121	Resistor, 100K
R74	2-145	Resistor, 1.0M
R75	2-133	Resistor, 330K
R76		NOT USED
R77	2-121	Resistor, 100K
R78	2-121	Resistor, 100K
R79	2-121	Resistor, 100K
R80	2-132	Resistor, 300K
R81	2-125	Resistor, 150K
R82	2-81	Resistor, 2.2K
R83	2-121	Resistor, 100K
R84	2-121	Resistor, 100K
R85	2-121	Resistor, 100K
R86	2-138	Resistor, 510K
R87	2-105	Resistor, 22K

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
R88	2-121	Resistor, 100K
R89	2-145	Resistor, 1.0M
R90	2-121	Resistor, 100K
R91	2-121	Resistor, 100K
R91	2-121	Resistor, 100K
R92	2-121	Resistor, 100K
R93	2-121	Resistor, 100K
R94	2-121	Resistor, 100K
R95	2-121	Resistor, 100K
R96-99		NOT USED
R100	2-97	Resistor, 10K
R101		NOT USED
R102	2-81	Resistor, 2.2K
R103	2-141	Resistor, 680K
R104	2-125	Resistor, 150K
R105	2-133	Resistor, 330K
R106	2-133	Resistor, 330K
R107	2-145	Resistor, 1.0M
R108	2-146	Resistor, 1.1M
R109	2-149	Resistor, 1.5M
R110	2-156	Resistor, 3.0M
R111	2-169	Resistor, 10M
R112		Selected in test
R113	2-169	Resistor, 10M
R114	2-156	Resistor, 3.0M
R115	2-149	Resistor, 1.5M
R116	2-146	Resistor, 1.1M
R117-119		NOT USED
R120	2-47	Resistor, 82 ohm
R121	2-49	Resistor, 100 ohm
R122-499		NOT USED
R500	2-125	Resistor, 150K
R501	2-85	Resistor, 3.3K
R502	2-125	Resistor, 150K
R503	2-81	Resistor, 2.2K
R504	2-121	Resistor, 100K
R505	2-121	Resistor, 100K
R506	2-138	Resistor, 510K
R507	2-138	Resistor, 510K
R508	2-89	Resistor, 4.7K
R509	2-69	Resistor, 680 ohm
R510	2-97	Resistor, 10K
R511	2-121	Resistor, 100K
R512	2-121	Resistor, 100K
R513	2-73	Resistor, 1K

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
S1	65-1	Switch, SPST, DIP
S2	65-1	Switch, SPST, DIP
T1	41-6A	Transformer (42-45)
U1	176-7808	I.C. 7808
U2	176-084	I.C. TL084
U3	176-4016	I.C. 4016
U4	176-084	I.C. TL084
U5	176-4011	I.C. 4011
U6	176-4016	I.C. 4016
U7	176-74LS74	I.C. 74LS74
U8	176-74LS90	I.C. 74LS90
U9	176-4011	I.C. 4011
U10	176-084	I.C. TL084
U11	176-084	I.C. TL084
U12	176-4016	I.C. 4016
U13	176-7805	I.C. 7805
U14	176-7906	I.C. 7906
U15	176-084	I.C. TL084
U16		NOT USED
U17		NOT USED
U18	176-4518	I.C. 4518
U19	176-4017	I.C. 4017
U20	176-4049	I.C. 4049
U21	176-4011	I.C. 4011
U22	176-4017	I.C. 4017
U23	176-4050	I.C. 4050
U24	176-4011	I.C. 4011
U25	176-4081	I.C. 4081
U26	176-4016	I.C. 4016
U27	176-084	I.C. TL084
U28	176-084	I.C. TL084
U29	176-4016	I.C. 4016
U30	176-084	I.C. TL084
U31	176-4016	I.C. 4016
U32	176-084	I.C. TL084
U33	176-4016	I.C. 4016
U34-99		NOT USED
U100	176-084	I.C. TL084
U101		NOT USED
U102	176-4016	I.C. 4016
Y1	59-10000	Crystal 10.000 MHz
Y2	59-186432	Crystal 18.6432 MHz

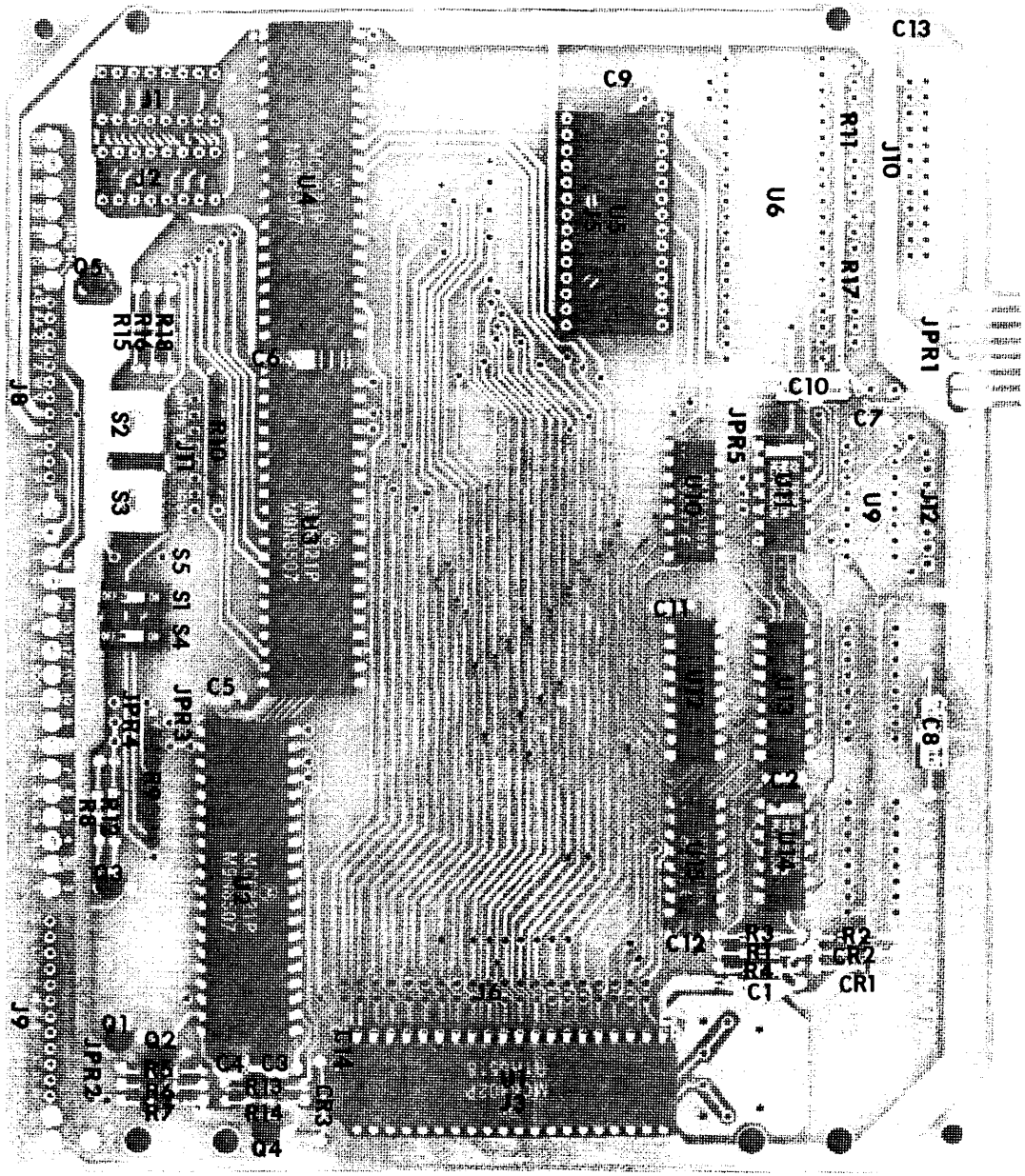
NOTE: The following items are installed when the Advanced Performance Option (APO) is specified.

C30	36-58	Cap., .001 uf, Mono
R76	2-121	Resistor, 100 K
JPR4	315-26-2	Jumper, 26 AWG, Red, 2" Lg. (Remove: R69)

6-12 SYMBOL DESIGNATION REFERENCE 86-74 (cont.)

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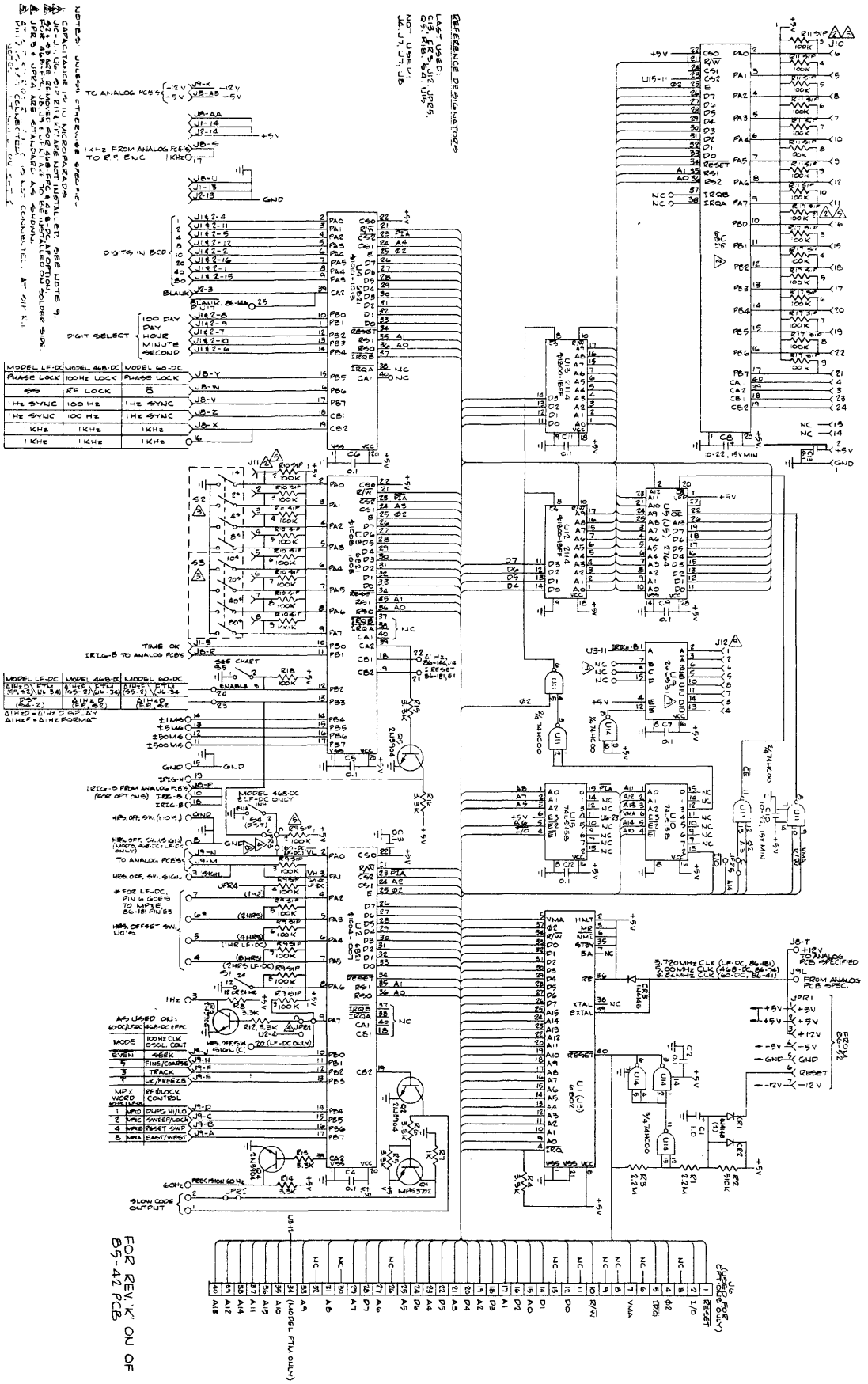
6-13 PARTS LOCATION - ASSEMBLY 86-42



6-14 SYMBOL DESIGNATION REFERENCE 86-42

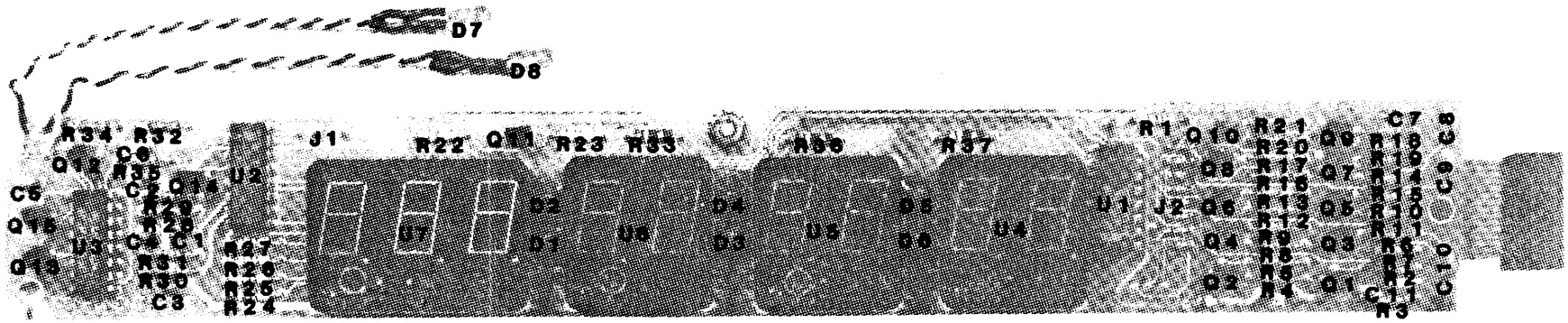
SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	32-29	Cap., Tant. 1.0uF
C2	36-95	Cap., Monolithic .1uF
C3	36-95	Cap., Monolithic .1uF
C4	36-95	Cap., Monolithic .1uF
C5	36-95	Cap., Monolithic .1uF
C6	36-95	Cap., Monolithic .1uF
C7	36-95	Cap., Monolithic .1uF
C8	23-10-25 *	Cap., Electro 10uF 25V
C9	36-95	Cap., Monolithic .1uF
C10	23-10-25 *	Cap., Electro 10uF 25V
C11	36-95	Cap., Monolithic .1uF
C12	36-95	Cap., Monolithic .1uF
C13	36-95	Cap., Monolithic .1uF
	* 32-45	Cap., Tant 22uF 15V (May be used
CR1	57-4148	Diode, 1N4148
CR2	57-4148	Diode, 1N4148
CR3	57-4148	Diode, 1N4148
J1	379-16	Socket, 16 Pin Dip
J2	379-16	Socket, 16 Pin Dip
J3	379-40	Socket, 40 Pin Dip
J4	379-24	Socket, 24 Pin Dip
J5	379-28-1	Socket, 28 Pin Dip
J6,7		NOT USED
J8	318-25	Socket, 12 Pin (318-12)
J9	318-25	Socket, 12 Pin (318-12)
JPR	387-14	Jumper (387-7)
PCB	85-42	Digital PCB FAB.
Q1	175-3702	Transistor, MPS3702
Q2	175-3904	Transistor, 2N3904
Q3	175-3904	Transistor, 2N3904
Q4	175-3904	Transistor, 2N3904
Q5	175-3904	Transistor, 2N3904
NOTE: All Resistors are 1/4 Watt, 5% Carbon Comp. unless otherwise noted.		
R1	2-153	Resistor, 2.2M
R2	2-138	Resistor, 510K
R3	2-177	Resistor, 22M
R4	2-85	Resistor, 3.3K
R5	2-85	Resistor, 3.3K
R6	2-85	Resistor, 3.3K
R7	2-73	Resistor, 1K
R8	2-85	Resistor, 3.3K
R9	11-121-10	Resistor, 100K SIP
R10	11-121-10	Resistor, 100K SIP
R11		NOT USED
R12	2-85	Resistor, 3.3K
R13	2-85	Resistor, 3.3K
R14	2-85	Resistor, 3.3K
R15	2-85	Resistor, 3.3K
R16	2-85	Resistor, 3.3K
R17		NOT USED
R18	2-121	Resistor, 100K
S1	65-1	Switch, SPST, DIP
S2	63-2	Switch, 10 Pos. Rotary
S3	63-2	Switch, 10 Pos. Rotary
U1	176-6802	I.C. MC6802
U2	176-6821	I.C. MC6821
U3	176-6821	I.C. MC6821
U4	176-6821	I.C. MC6821
U5-9		NOT USED
U10	176-74LS138	I.C. 74LS138
U11	176-74HC00	I.C. 74HC00
U12	176-2114	I.C. 2114
U13	176-2114	I.C. 2114
U14	176-4011	I.C. 4011
U15	176-74LS138	I.C. 74LS138

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6-16 PARTS LOCATION - ASSEMBLY 86-43



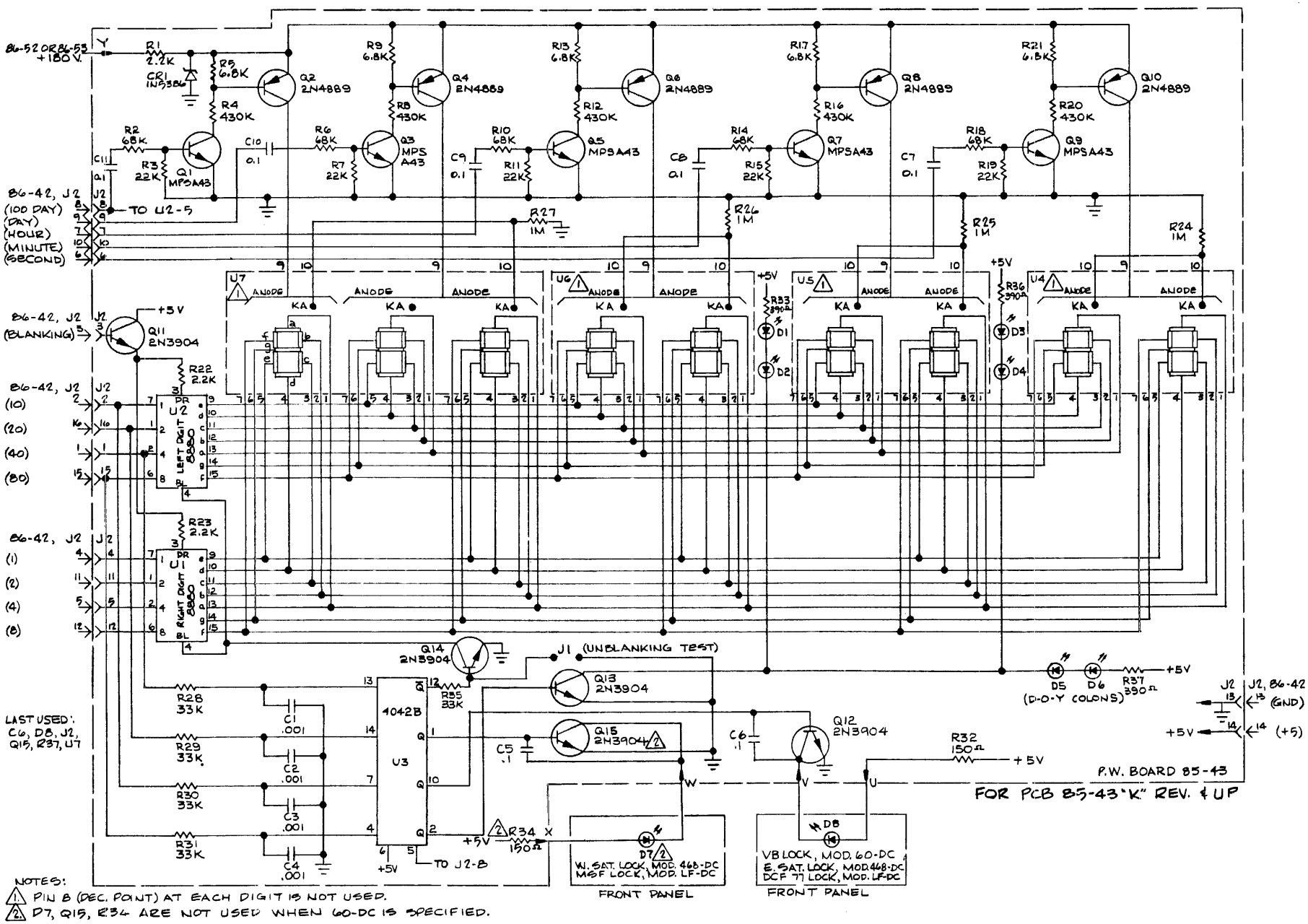
6-17 SYMBOL DESIGNATION REFERENCE 86-43

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	36-58	Cap., Monolithic .001uF
C2	36-58	Cap., Monolithic .001uF
C3	36-58	Cap., Monolithic .001uF
C4	36-58	Cap., Monolithic .001uF
C5	36-95	Cap., Monolithic 0.1uF
C6	36-95	Cap., Monolithic 0.1uF
C7	36-95	Cap., Monolithic 0.1uF
C8	36-95	Cap., Monolithic 0.1uF
C9	36-95	Cap., Monolithic 0.1uF
C10	36-95	Cap., Monolithic 0.1uF
C11	36-95	Cap., Monolithic 0.1uF
CR1	55-5386	Diode, Zener 1N5386
D1	58-4	LED, Red
D2	58-4	LED, Red
D2	58-4	LED, Red
D3	58-4	LED, Red
D4	58-4	LED, Red
D5	58-4	LED, Red
D6	58-4	LED, Red
D7	58-1	LED, Green
D8	58-1	LED, Green
PCB	85-43	Display PCB. Fab.
Q1	175-MPSA43*	Transistor MPSA43
Q2	176-4889	Transistor 2N4889
Q3	175-MPSA43*	Transistor MPSA43
Q4	175-4889	Transistor 2N4889
Q5	175-MPSA43*	Transistor MPSA43
Q6	175-4889	Transistor 2N4889
Q7	175-MPSA438	Transistor MPSA43
Q8	175-4889	Transistor 2N4889
Q9	175-MPSA43*	Transistor MPSA43
Q10	175-4889	Transistor 2N4889
Q11	175-3904	Transistor 2N3904
Q12	175-3904	Transistor 2N3904
Q13	175-3904	Transistor 2N3904
Q14	175-3904	Transistor 2N3904
Q15	175-3904	Transistor 2N3904

NOTE: ALL RESISTORS 1/4 WATT, 5% CARBON COMP. UNLESS OTHERWISE NOTED.

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
R1	2-81	Resistor, 2.2K
R2	2-117	Resistor, 68K
R3	2-105	Resistor, 22K
R4	2-136	Resistor, 430K
R5	2-93	Resistor, 6.8K
R6	2-117	Resistor, 68K
R7	2-106	Resistor, 22K
R8	2-136	Resistor, 430K
R9	2-93	Resistor, 6.8K
R10	2-117	Resistor, 68K
R11	2-105	Resistor, 22K
R12	2-136	Resistor, 430K
R13	2-93	Resistor, 6.8K
R14	2-117	Resistor, 68K
R15	2-106	Resistor, 22K
R16	2-136	Resistor, 430K
R17	2-93	Resistor, 6.8K
R18	2-117	Resistor, 68K
R19	2-105	Resistor, 22K
R20	2-136	Resistor, 430K
R21	2-93	Resistor, 6.8K
R22	2-81	Resistor, 2.2K
R23	2-81	Resistor, 2.2K
R24	2-145	Resistor, 1M
R25	2-145	Resistor, 1M
R26	2-145	Resistor, 1M
R27	2-145	Resistor, 1M
R28	2-109	Resistor, 33K
R29	2-109	Resistor, 33K
R30	2-109	Resistor, 33K
R31	2-109	Resistor, 33K
R32	2-53	Resistor, 150 ohm
R33	2-63	Resistor, 390 ohm
R34	2-53	Resistor, 150 ohm
R35	2-109	Resistor, 33K
R36	2-63	Resistor, 390 ohm
R37	2-63	Resistor, 390 ohm
U1	176-8880	I.C. 8880
U2	176-8880	I.C. 8880
U3	176-4042	I.C. 4042
U4	189-1	Digit Display 20 Pin (2 Digit)
U5	189-1	Digit Display 20 Pin (2 Digit)
U6	189-1	Digit Display 20 Pin (2 Digit)
U7	189-2	Digit Display 30 Pin (3 Digit)

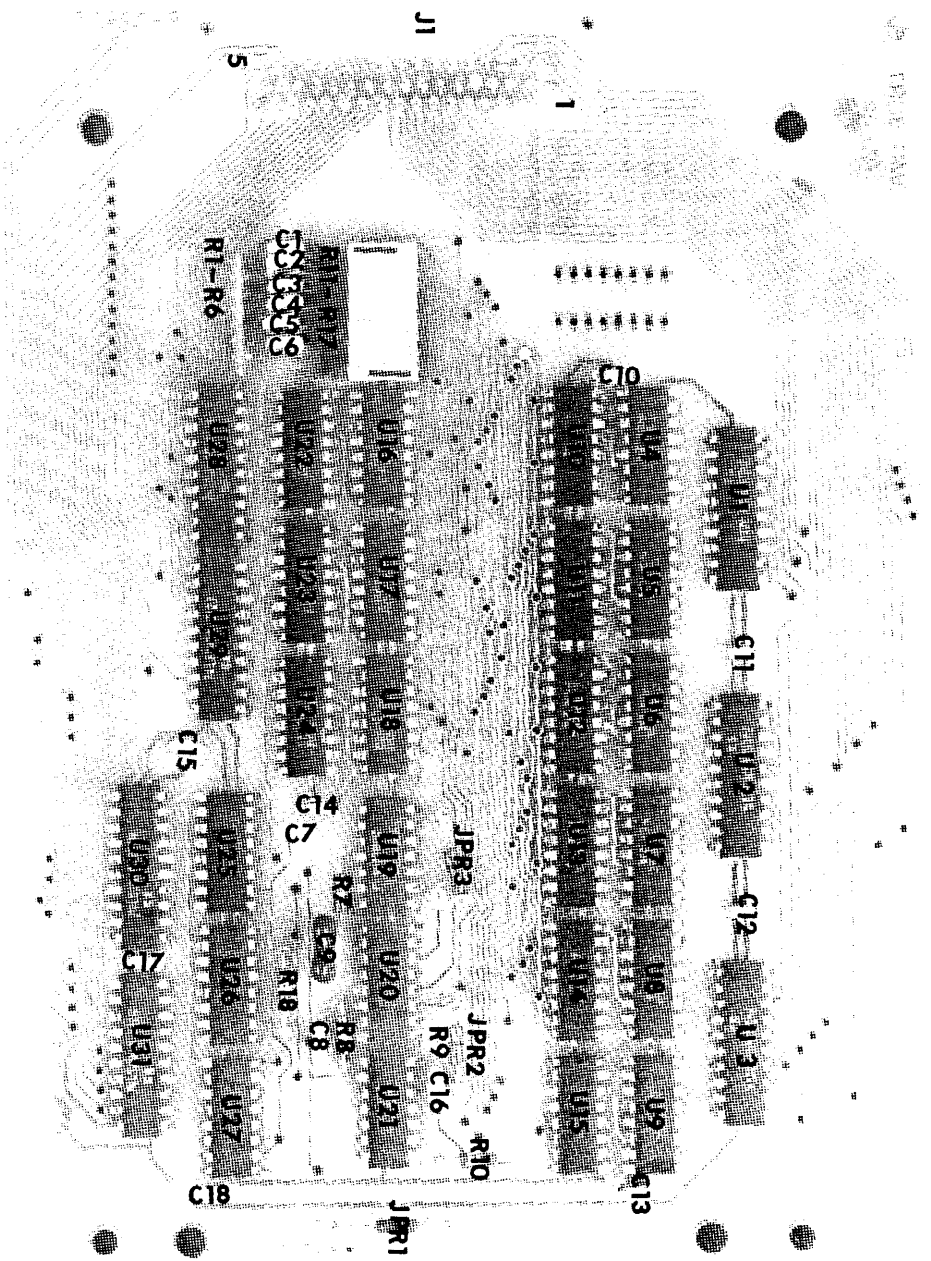
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6-18 SCHEMATIC - ASSEMBLY 86-43

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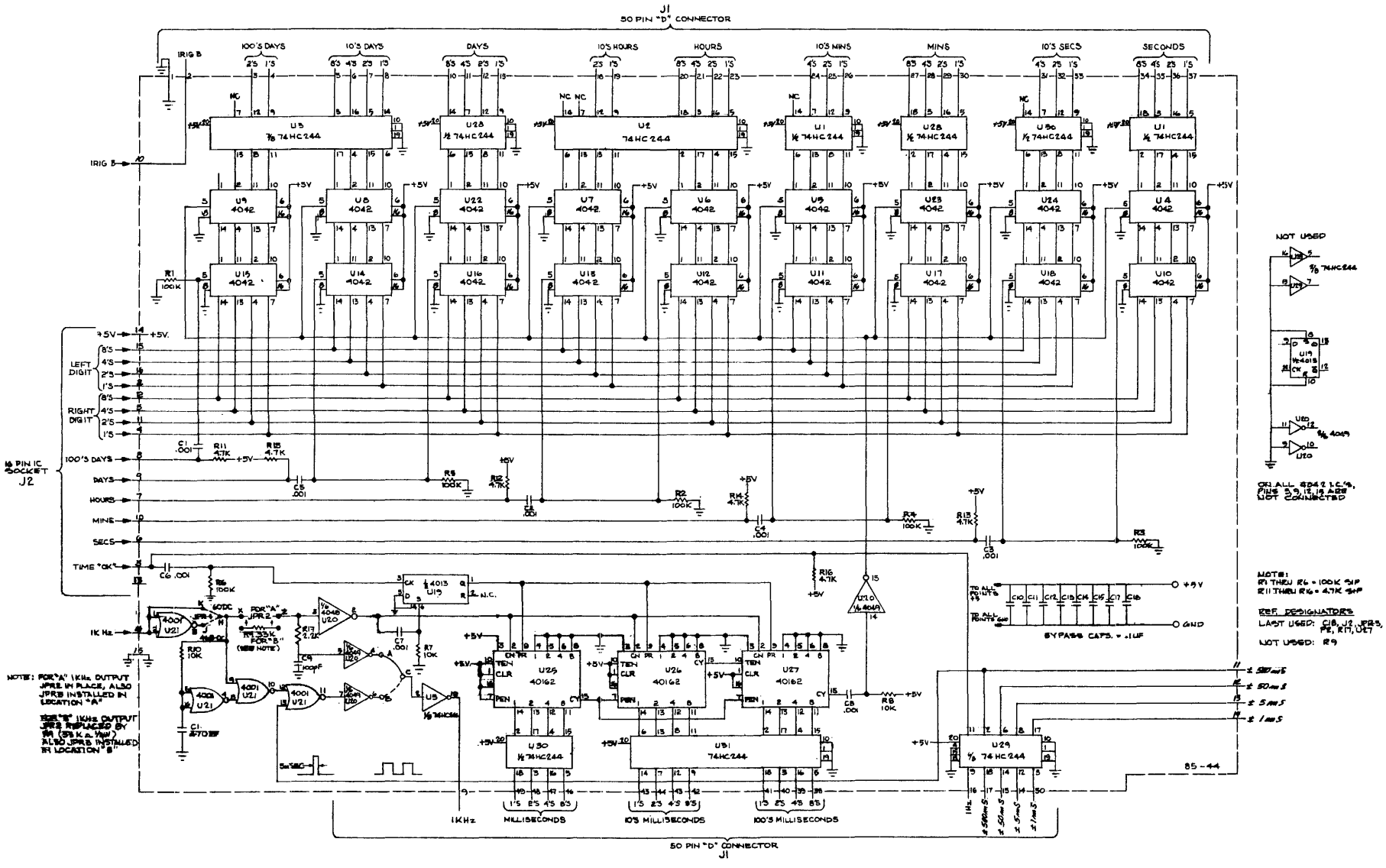
6-19 PARTS LOCATION - ASSEMBLY 86-44



6-20 SYMBOL DESIGNATION REFERENCE 86-44

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	36-58	Cap., Monolithic .001uF
C2	36-58	Cap., Monolithic .001uF
C3	36-58	Cap., Monolithic .001uF
C4	36-58	Cap., Monolithic .001uF
C5	36-58	Cap., Monolithic .001uF
C6	36-58	Cap., Monolithic .001uF
C7	36-58	Cap., Monolithic .001uF
C8	36-58	Cap., Monolithic .001uF
C9	29-33	Cap., Dipped Mica 100pF
C10	36-95	Cap., Monolithic 0.1uF
C11	36-95	Cap., Monolithic 0.1uF
C12	36-95	Cap., Monolithic 0.1uF
C13	36-95	Cap., Monolithic 0.1uF
C14	36-95	Cap., Monolithic 0.1uF
C15	36-95	Cap., Monolithic 0.1uF
C16	36-50	Cap., Monolithic 470pF
C17	36-95	Cap., Monolithic 0.1uF
C18	36-95	Cap., Monolithic 0.1uF
J1	372-1505	Connector 50 Pin D Ft. Ang.
J2	379-16	ocket, 16 pin DIP
JPR1	2-0	Jumper
JPR2	2-0	Jumper
JPR3	2-0	Jumper
PCB	85-79	Buff. Parallel BCD Time Output PCB
P1	389-1-1	Cable Assy. DIP to DIP
P2	389-1-1	Cable Assy. DIP to DIP
NOTE:	All resistors are 1/4 Watt 5% Carbon Comp. unless otherwise noted.	
R1	11-121-8	S.I.P. 100K
R2	11-121-8	S.I.P. 100K
R3	11-121-8	S.I.P. 100K
R4	11-121-8	S.I.P. 100K
R5	11-121-8	S.I.P. 100K
R6	11-121-8	S.I.P. 100K
R7	2-97	Resistor, 10K
R8	2-97	Resistor, 10K
R9	2-109 *	Resistor, 33K
R10	2-97	Resistor, 10K
R11	22-89-8	S.I.P. 4.7K
R12	22-89-8	S.I.P. 4.7K
R13	22-89-8	S.I.P. 4.7K
R14	22-89-8	S.I.P. 4.7K
R15	22-89-8	S.I.P. 4.7K
R16	22-89-8	S.I.P. 4.7K
R17	2-105	Resistor, 22K
* Option replacing JPR-2 (Special Order Only).		
U1	178-74HC244	I.C., 74HC244
U2	178-74HC244	I.C., 74HC244
U3	178-74HC244	I.C., 74HC244
U4	176-4042	I.C. 4042
U5	176-4042	I.C. 4042
U6	176-4042	I.C. 4042
U7	176-4042	I.C. 4042
U8	176-4042	I.C. 4042
U9	176-4042	I.C. 4042
U10	176-4042	I.C. 4042
U11	176-4042	I.C. 4042
U12	176-4042	I.C. 4042
U13	176-4042	I.C. 4042
U14	176-4042	I.C. 4042
U15	176-4042	I.C. 4042
U16	176-4042	I.C. 4042
U17	176-4042	I.C. 4042
U18	176-4042	I.C. 4042
U19	176-4013	I.C. 4013
U20	176-4049	I.C. 4049
U21	176-4001	I.C. 4001
U22	176-4-42	I.C. 4042
U23	176-4-42	I.C. 4042
U24	176-4-42	I.C. 4042
U25	176-40162	I.C. 40162
U26	176-40162	I.C. 40162
U27	176-40162	I.C. 40162
U28	178-74HC244	I.C., 74HC244
U29	178-74HC244	I.C., 74HC244
U30	178-74HC244	I.C., 74HC244
U31	178-74HC244	I.C., 74HC244

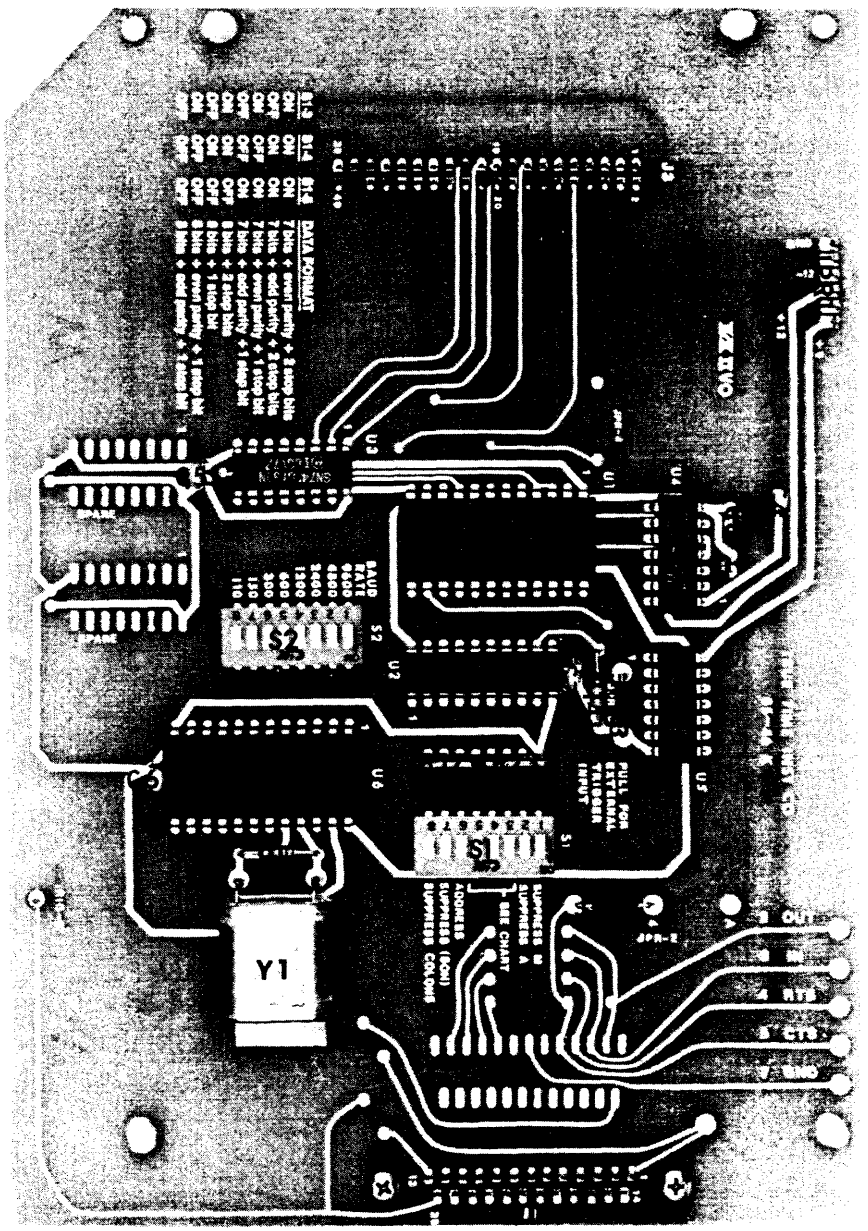
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6-21 SCHEMATIC - ASSEMBLY 86-44

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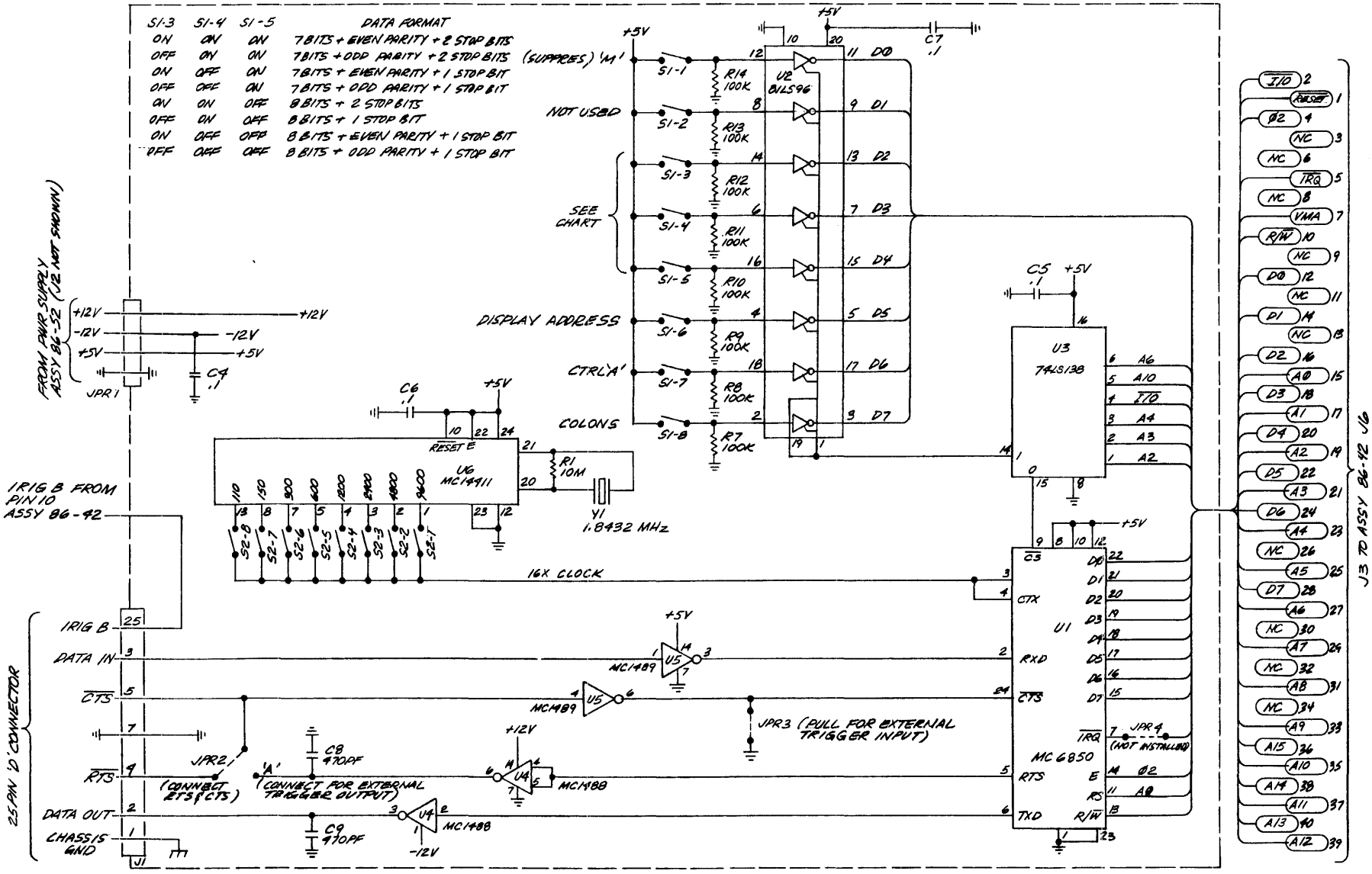
6-22 PARTS LOCATION - ASSEMBLY 86-46



6-23 SYMBOL DESIGNATION REFERENCE 86-46

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1		NOT USED
C2		NOT USED
C3		NOT USED
C4	36-95	Cap., Monolithic .1uF
C5	36-95	Cap., Monolithic .1uF
C6	36-95	Cap., Monolithic .1uF
C7	36-95	Cap., Monolithic .1uF
C8	36-50	Cap., Monolithic 470pF
C9	36-50	Cap., Monolithic 470pF
J1	372-125P	Conn., 25 Pin, Male 'D', Rt. Angle
J2		NOT USED
J3	404-1-2-20	Conn., 40 Pin, Female
J4		NOT USED
J5		NOT USED
J6	401-1-2-20	CONN., 40 Pin, Male
JPR-1	387-12	"Flexstrip" Jumper 6 Cond. (387-6)
JPR-2	2-0	Jumper
JPR-3	2-0	Jumper
PCB	85-46	PCB, RS232 Output
NOTE:	All resistors are 1/4 Watt, 5% Carbon Comp. unless otherwise noted.	
R1	2-169	Resistor, 10 M
R2-R13		NOT USED
R14	2-121	Resistor, 100K
R15		NOT USED
R16		NOT USED
R17	11-121	Resistor, S.I.P. 100K
R18	11-121	Resistor, S.I.P. 100K
R19	11-121	Resistor, S.I.P. 100K
R20	11-121	Resistor, S.I.P. 100K
R21	11-121	Resistor, S.I.P. 100K
R22	11-121	Resistor, S.I.P. 100K
R23	11-121	Resistor, S.I.P. 100K
S1	65-8	Switch, 8 Pos. SPST DIP
S2	65-8	Switch, 8 Pos. SPST DIP
U1	176-6850	I.C. 6850
U2	176-81LS96	I.C. 81LS96
U3	176-74LS138	I.C. 74LS138
U4	176-1488	I.C. 1488
U5	176-1489	I.C. 1489
U6	176-14411	I.C. 14411
U7		NOT USED
U8	177-2716	I.C. 2716
Y1	59-1843	Crystal, 1.8432 MHz

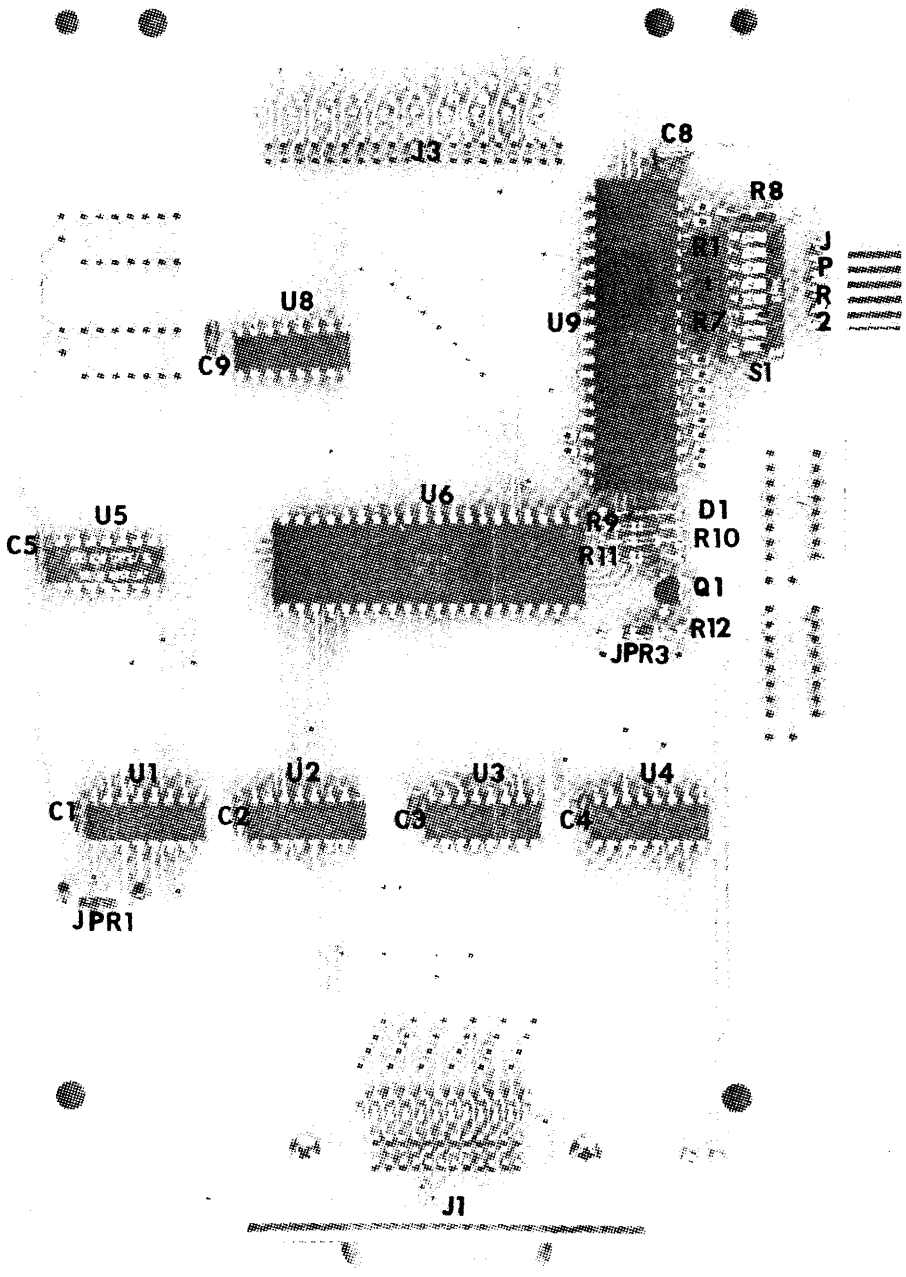
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6-24 SCHEMATIC - ASSEMBLY 86-46

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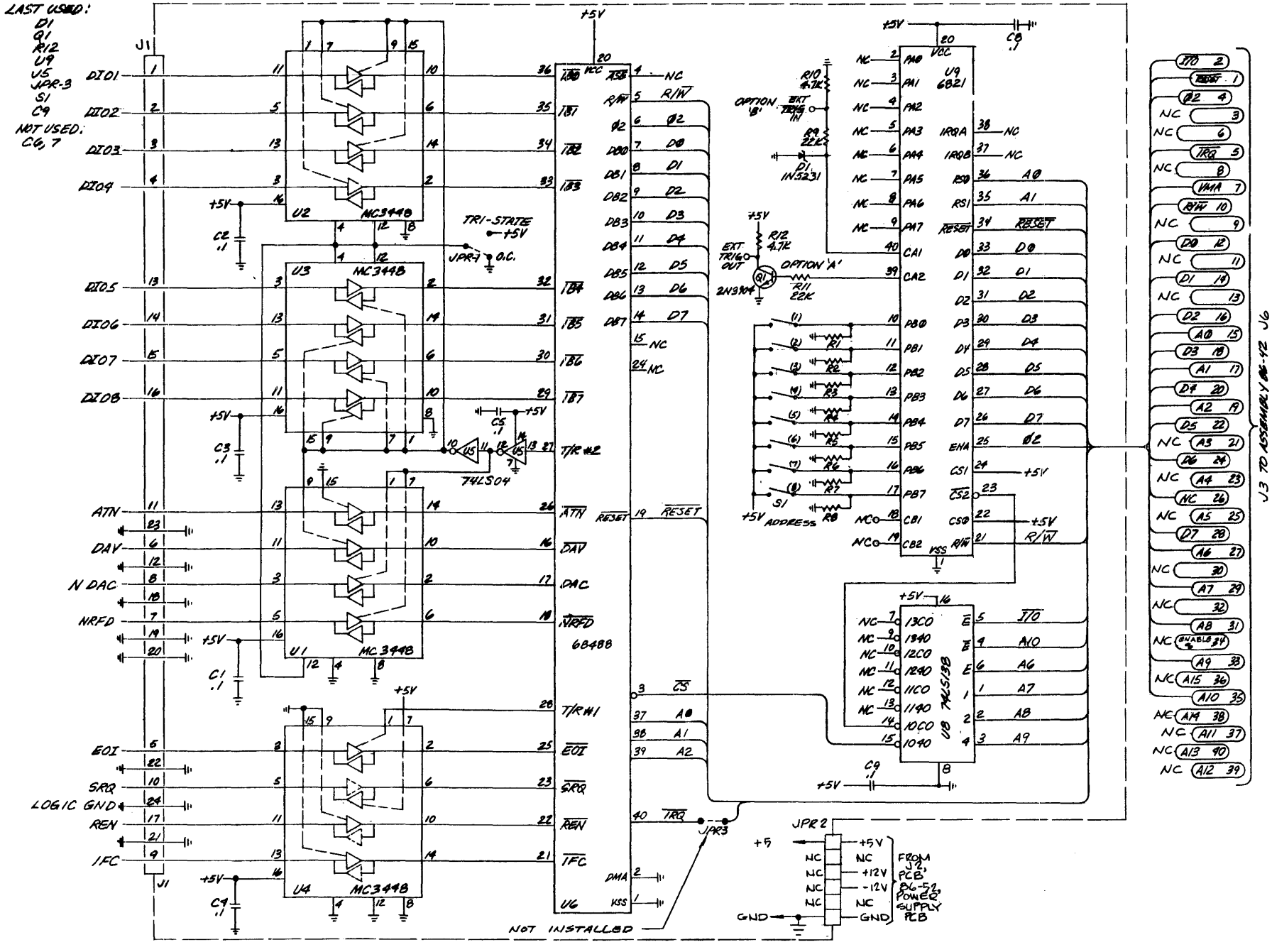
6-25 PARTS LOCATION - ASSEMBLY 86-47



6-26 SYMBOL DESIGNATION REFERENCE 86-47

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	36-95	Cap., Monolithic .1uF
C2	36-95	Cap., Monolithic .1uF
C3	36-95	Cap., Monolithic .1uF
C4	36-95	Cap., Monolithic .1uF
C5	36-95	Cap., Monolithic .1uF
C6		NOT USED
C7		NOT USED
C8	36-95	Cap., Monolithic .1uF
C9	36-95	Cap., Monolithic .1uF
D1	55-5231	Diode 1N5231
J1	384-24	Header, 24 Pin, Male
J2		NOT USED
J3	404-1-2-20	Conn., 40 Pin, Female
J4		NOT USED
J5		NOT USED
J6	401-1-2-20	Conn., 40 Pin, Male
JPR-1	2-0	Jumper
JPR-2	387-12	Jumper 1/2
PCB	85-47	IEEE-488 Time Output PCB Fab.
Q1	175-3904	Transistor, 2N3904
NOTE:	All resistors are 1/4 Watt, 5% Carbon Comp. unless otherwise noted.	
R1	11-89	Resistor, S.I.P., 4.7K
R2	11-89	Resistor, S.I.P., 4.7K
R3	11-89	Resistor, S.I.P., 4.7K
R4	11-89	Resistor, S.I.P., 4.7K
R5	11-89	Resistor, S.I.P., 4.7K
R6	11-89	Resistor, S.I.P., 4.7K
R7	11-89	Resistor, S.I.P., 4.7K
R8	2-89	Resistor, 4.7K
R9	2-105	Resistor, 22K
R10	2-89	Resistor, 4.7K
R11	2-105	Resistor, 22K
R12	2-89	Resistor, 4.7K
S1	65-8	Switch, 8 Pos., SPST, DIP
U1	176-3448	I.C. 3448
U2	176-3448	I.C. 3448
U3	176-3448	I.C. 3448
U4	176-3448	I.C. 3448
U5	176-74LS04	I.C. 74LS04
U6	176-68488	I.C. 68488
U7		NOT USED
U8	176-74LS138	I.C. 74LS138
U9	176-6821	I.C. 6821

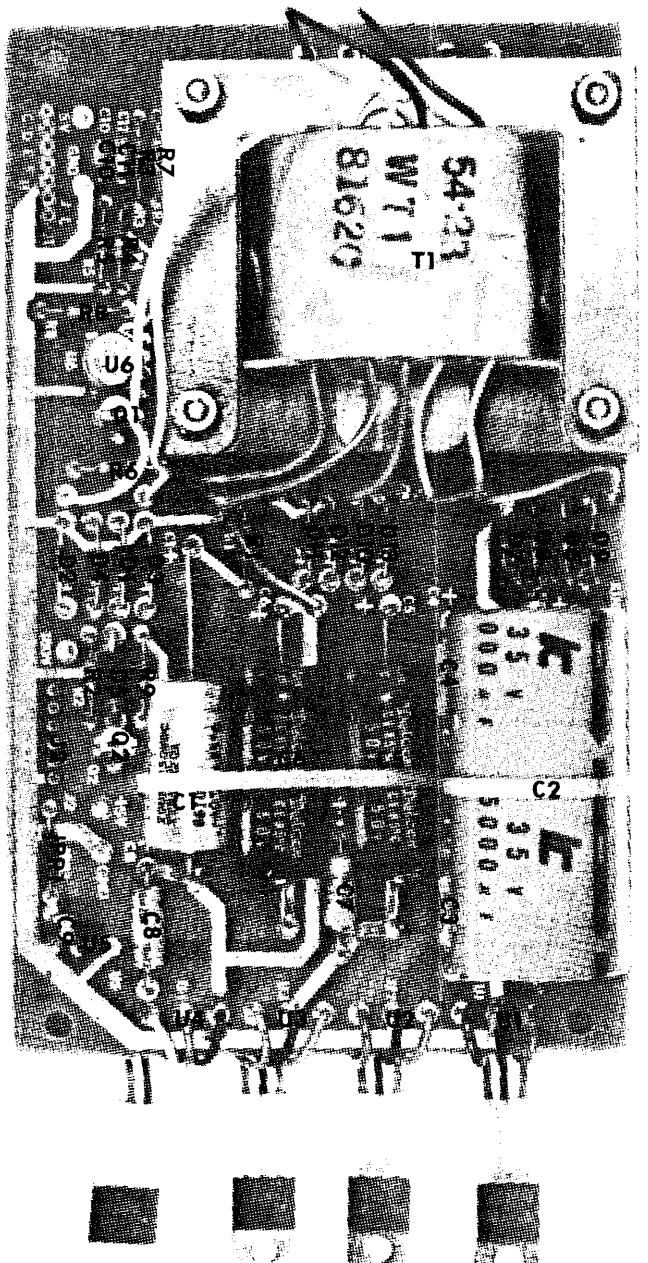
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6-27 SCHEMATIC - ASSEMBLY 86-47

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6-28 PARTS LOCATION - ASSEMBLY 86-52

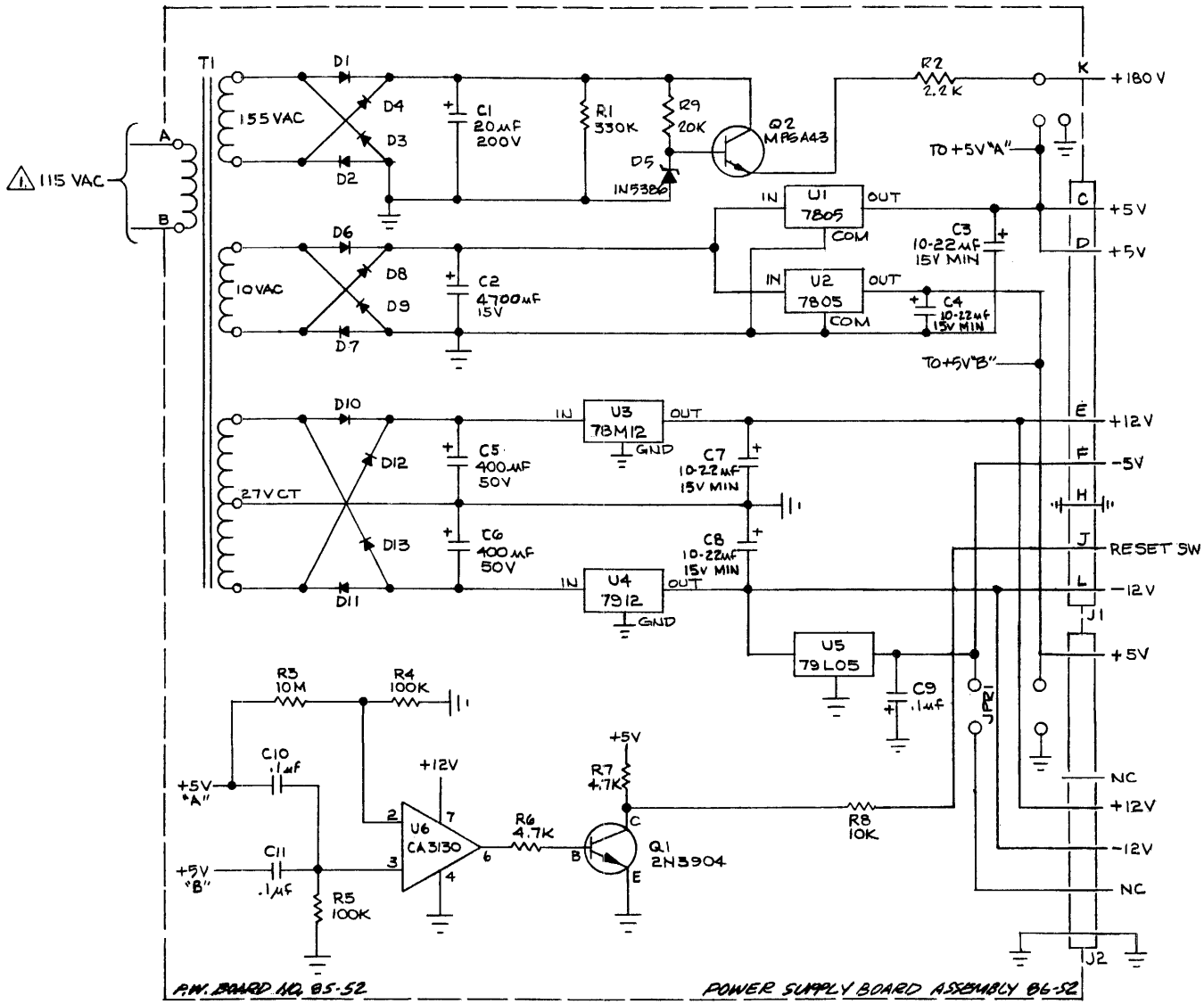


6-29 SYMBOL DESIGNATION REFERENCE 86-52

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	23-20-200	Cap., Electro 20uF 200V
C2	23-4700-25	Cap., Electro 4700 uF 25V
C3 *	23-10-25	Cap., Electro 10uF 25V
C4 *	23-10-25	Cap., Electro 10uF 25V
C5	23-400-50	Cap., Electro 400uF 50V
C6	23-400-50	Cap., Electro 400uF 50V
C7 *	23-10-25	Cap., Electro 10uF 25V
C8 *	23-10-25	Cap., Electro 10uF 25V
C9	36-95	Cap., Monolithic .luF
C10	36-95	Cap., Monolithic .luF
C11	36-95	Cap., Monolithic .luF
D1	57-4005	Diode 1N4005
D2	57-4005	Diode 1N4005
D3	57-4005	Diode 1N4005
D4	57-4005	Diode 1N4005
D5	55-5386	Diode 1N5386
D6	57-4005	Diode 1N4005
D7	57-4005	Diode 1N4005
D8	57-4005	Diode 1N4005
D9	57-4005	Diode 1N4005
D10	57-4005	Diode 1N4005
D11	57-4005	Diode 1N4005
D12	57-4005	Diode 1N4005
D13	57-4005	Diode 1N4005
J1	318-25	Socket, 7 Pin Strip (318-7)
J2	318-25	Socket, 6 Pin Strip (318-6)
JPR-1	2-0	Jumper
PCB	85-52	PCB, Power Supply
Q1	175-3904	Transistor, 2N3904
Q2	175-MPSA43	Transistor, MPSA43
NOTE:	All resistors are 1/4 Watt, 5% Carbon Comp. unless otherwise noted.	
R1	2-133	Resistor, 330K
R2	2-81	Resistor, 2.2K
R3	2-169	Resistor, 10MEG
R4	2-121	Resistor, 100K
R5	2-121	Resistor, 100K
R6	2-89	Resistor, 4.7K
R7	2-89	Resistor, 4.7K
R8	2-97	Resistor, 10
R9	2-104	Resistor, 20K
T1	54-2	Transformer
U1	176-7805	I.C. +5V Reg., LM7805
U2	176-7805	I.C. +5V Reg., LM7805
U3	176-78M12	I.C. +12V Reg., LM78M12
U4	176-7912	I.C. -12V Reg., LM79M12
U5	176-79L05	I.C. 3 Pin Case
U6	176-3130	I.C. 8 Pin Metal Can

* Cap. Tant. 22UF 15V Part # 32-45 may be used.

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NOTE: DIODES D1 THRU D4 & D6 THRU D13 = IN4005

LAST USED:
D13
R9
C10
Q2
U6
T1
JPR-2
J2

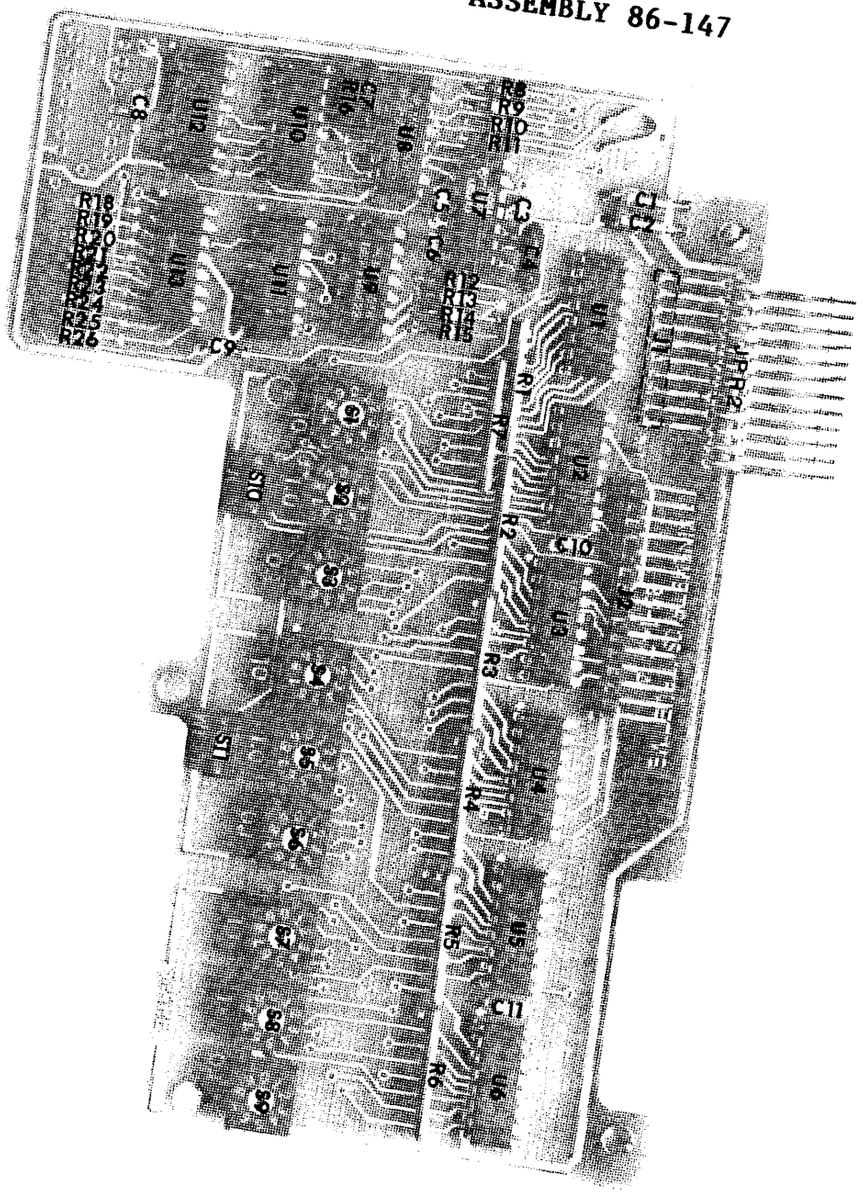
NOTES: UNLESS OTHERWISE SPECIFIED

⚠1 WHEN 220 VAC, 50 Hz IS SPECIFIED, USE PART NO. 54-8 IN PLACE OF PART NO. 54-2 FOR T1.

6-30 SCHEMATIC - ASSEMBLY 86-52

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6-31 PARTS LOCATION - ASSEMBLY 86-147



6-32 SYMBOL DESIGNATION REFERENCE 86-147

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
PCB	85-147	MK 1.5 Option PCB Fab.
C1	32-29	Cap., 1.0 uf, 35V, Tant.
C2	32-29	Cap., 1.0 uf, 35V, Tant.
C3	36-95	Cap., 0.1 uf, Mono.
C4	29-20	Cap., 33 pf, Dipped Mica
C5	36-95	Cap., 0.1 uf, Mono.
C6	36-58	Cap., .001 uf, Mono.
C7	29-31	Cap., 82 pf, Dipped Mica
C8	36-95	Cap., 0.1 uf, Mono.
C9	36-95	Cap., 0.1 uf, Mono.
C10	36-95	Cap., 0.1 uf, Mono.
C11	36-95	Cap., 0.1 uf, Mono.
JPR2	387-12	"Flexstrip" Jumper, 12 Cond.
J1	318-12	Socket, 12 Pin Strip
J2	401-2-1-15	Header, 15 Pin Strip Rt. Ang.

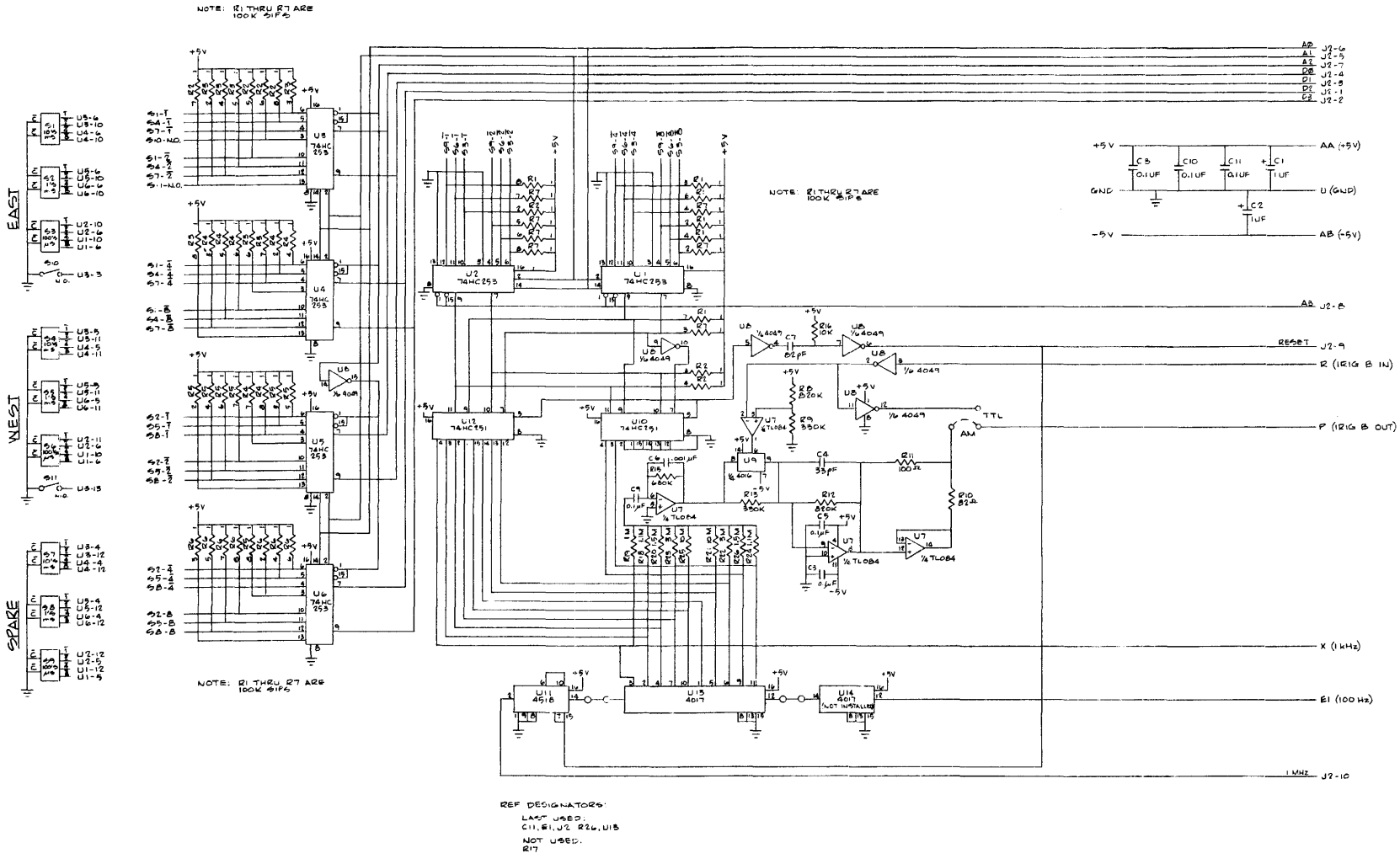
NOTE: All resistors 1/4 Watt, ±5%, Carbon Comp. unless otherwise noted.

R1	11-121	Resistor, 100K SIP
R2	11-121	Resistor, 100K SIP
R3	11-121	Resistor, 100K SIP
R4	11-121	Resistor, 100K SIP
R5	11-121	Resistor, 100K SIP
R6	11-121	Resistor, 100K SIP
R7	11-121	Resistor, 100K SIP
R8	2-143	Resistor, 820K
R9	2-133	Resistor, 330K
R10	2-47	Resistor, 82 ohm
R11	2-49	Resistor, 100 ohm
R12	2-143	Resistor, 820K
R13	2-133	Resistor, 330K
R14	2-125	Resistor, 150K
R15	2-141	Resistor, 680K
R16	2-97	Resistor, 10K
R17		NOT USED
R18, R19	2-146	Resistor, 1.1M
R20	2-145	Resistor, 1.0M
R21	2-149	Resistor, 1.5M
R22	2-169	Resistor, 10.0M
R23	2-156	Resistor, 3.0M
R24	2-156	Resistor, 3.0M
R25	2-146	Resistor, 1.1M
R26	2-169	Resistor, 10.0M
	2-149	Resistor, 1.5M

S1	63-2	Switch, 10 Pos. Rotary
S2	63-2	Switch, 10 Pos. Rotary
S3	63-2	Switch, 10 Pos. Rotary
S4	63-2	Switch, 10 Pos. Rotary
S5	63-2	Switch, 10 Pos. Rotary
S6	63-2	Switch, 10 Pos. Rotary
S7	63-2	Switch, 10 Pos. Rotary
S8	63-2	Switch, 10 Pos. Rotary
S9	63-2	Switch, 10 Pos. Rotary
S10	65-1	Switch SPST
S11	65-1	Switch SPST

U1	178-74HC253	I.C. 74HC253
U2	178-74HC253	I.C. 74HC253
U3	178-74HC253	I.C. 74HC253
U4	178-74HC253	I.C. 74HC253
U5	178-74HC253	I.C. 74HC253
U6	178-74HC253	I.C. 74HC253
U7	176-084	I.C. TL084
U8	176-4049	I.C. 4049
U9	176-4016	I.C. 4016
U10	178-74HC251	I.C. 74HC251
U11	176-4518	I.C. 4518
U12	178-74HC251	I.C. 74HC251
U13	176-4017	I.C. 4017

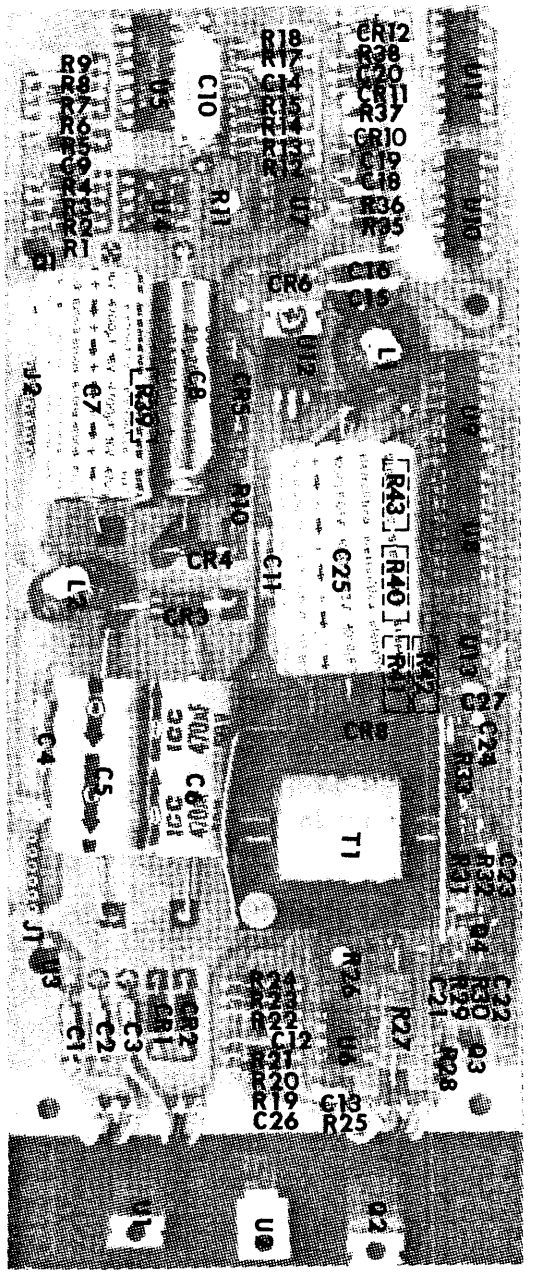
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6-33 SCHEMATIC - ASSEMBLY 86-147

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6-34 PARTS LOCATION - ASSEMBLY 86-53



6-35 SYMBOL DESIGNATION REFERENCE 86-53

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
C1	32-29	Cap., 1.0uF Tant.
C2	32-29	Cap., 1.0uF Tant.
C3	32-29	Cap., 1.0uF Tant.
C4	32-45	Cap., 22uF Tant.
C5	23-400-50	Cap., 400uF 50V Alum. Electro
C6	23-400-50	Cap., 400uF 50V Alum. Electro
C7	23-4700-25	Cap., 4700uF 25V Alum. Electro
C8	23-20-200	Cap., 20uF 200V Alum. Electro
C9	36-95	Cap., 0.1uF Monolithic
C10	24-13	Cap., .01uF Polystyrene
C11	32-45	Cap., 22uF Tant.
C12	36-50	Cap., 470pF Monolithic
C13	36-50	Cap., 470pF Monolithic
C14	36-83	Cap., .01uF Monolithic
C15	36-83A	Cap., .02uF, 1000V Ceramic
C16	36-83A	Cap., .02uF, 1000V Ceramic
C17		NOT USED
C18	36-83	Cap., .01uF Monolithic
C19	36-58	Cap., .001uF Monolithic
C20	36-58	Cap., .001uF Monolithic
C21	36-91	Cap., .047uF Monolithic
C22	36-78	Cap., .0056uF Monolithic
C23	36-58	Cap., .001uF Monolithic
C24	36-83	Cap., .01uF Monolithic
C25	23-1000-50	Cap., 1000uF 50V Alum. Electro
C26	36-95	Cap., 0.1uF Monolithic
C27	36-95	Cap., 0.1uF Monolithic
CR1	57-4934	Diode, IN4934
CR2	57-4934	Diode, IN4934
CR3	57-ERC82-004	Diode, ERC81-004
CR4	57-FR107	Diode, FR107
CR5	55-5386	Diode, IN5386
CR6	57-5391	Diode, IN5391
CR7		NOT USED
CR8	57-4934	Diode, IN4934
CR9		NOT USED
CR10	57-4148	Diode, IN4148
CR11	57-4148	Diode, IN4148
CR12	57-4148	Diode, IN4148
J1	318-25	Strip Connector (Cut into 6 & 7 conductor pieces)
J2	318-25	Strip Connector (Cut into 6 & 7 conductor pieces)
L1	43-6	Coil Assy. Inductor (42-58)
L2	43-6	Coil Assy. Inductor (42-58)

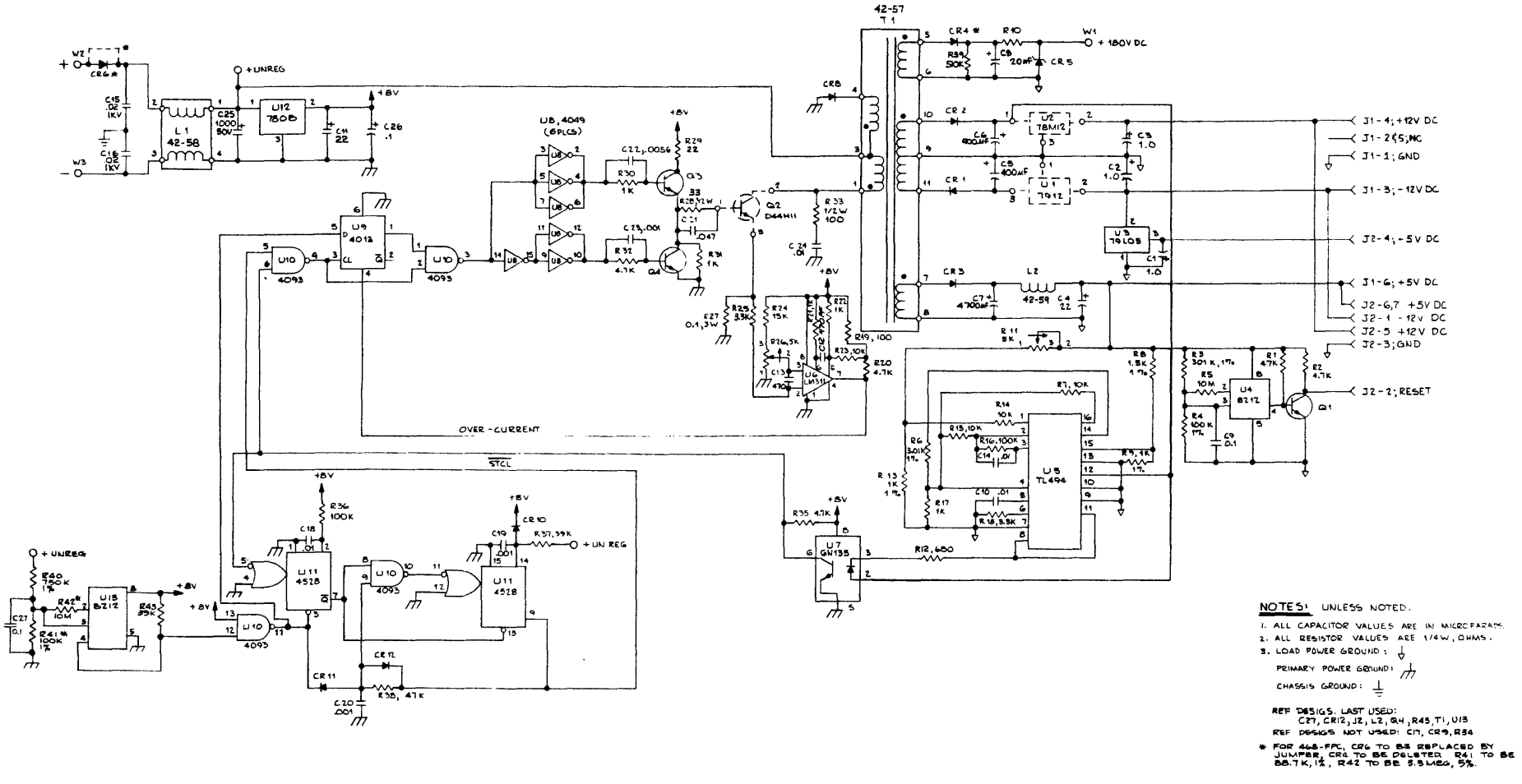
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SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
PCB	85-53	Printed Circuit Board
Q1	175-3904	Transistor 2N3904
Q2	175-D44H11	Transistor D44H11
Q3	175-3904	Transistor 2N3904
Q4	176-3904	Transistor 2N3904
NOTE:	All resistors are 1/4 Watt, 5% Carbon Comp. unless otherwise noted.	
R1	211-3	Resistor, 47K
R2	2-89	Resistor, 4.7K
R3	8-3013	Resistor, 301K, 1/8 W, 1% Film
R4	8-1003	Resistor, 100K, 1/8 W, 1% Film
R5	2-169	Resistor, 10M
R6	8-3011	Resistor, 3.01K, 1/8 W, 1% Film
R7	2-97	Resistor, 10K
R8	8-1501	Resistor, 1.5K, 1/8 W, 1% Film
R9	8-1001	Resistor, 1.0K, 1/8 W, 1% Film
R10	2-77	Resistor, 1.5K
R11	20-9	Pot., 5.0K Cermet
R12	2-69	Resistor, 680 ohm
R13	8-1001	Resistor, 1.0K, 1/8 W, 1% Film
R14	2-97	Resistor, 10K
R15	2-97	Resistor, 10K
R16	8-1003	Resistor, 100K, 1/8 W, 1% Film
R17	1--1	Resistor, 1.0K, 1/8 W, 1% Film
R18	2-85	Resistor, 3.3K
R19	2-49	Resistor, 100 ohm
R20	2-89	Resistor, 4.7K
R21	8-1001	Resistor, 1.0K, 1/8 W, 1% Film
R22	8-1001	Resistor, 1.0K, 1/8 W, 1% Film
R23	2-97	Resistor, 10K
R24	2-101	Resistor, 15K
R25	2-85	Resistor, 3.3K
R26	20-9	Pot., 5.0K Cermet
R27	10-1R-3	Resistro, 0.1 ohm, 3W, WW Carbon
R28	2-37	Resistor, 33 ohm
R29	2-33	Resistor, 22 ohm
R30	8-1001	Resistor, 1.0K, 1/8 W, 1% Film
R31	8-1001	Resistor, 1.0K, 1/8 W, 1% Film
R32	2-89	Resistor, 4.7K
R33	3-1000-0.5	Resistor, 100 ohm, 1/2 W
R34		NOT USED
R35	2-89	Resistor, 4.7K
R36	8-1003	Resistor, 100K, 1/8 W, 1% Film
R37		NOT USED
R38	2-113	Resistor, 47K
R39	2-138	Resistor, 510K
R40	8-7503	Resistor, 750K, 1/8 W, 1% Film

SYMBOL	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION
R41	8-1003	Resistor, 100K, 1/8 W, 1% Film
R42	2-169	Resistor, 10meg.
R43	2-111	Resistor, 39K
T1	42-57	Transformer
U1	176-7912	I.C. 7912, -12V Reg.
U2	176-78M12	I.C. 7812, +12V Reg.
U3	176-79L05	I.C. 79L05, -5V Reg.
U4	176-8212	I.C. ICL8212, Volt Monitor
U5	176-TL494	I.C. 494, Switch Reg.
U6	176-LM311	I.C. LM311N, Comparator
U7	176-6N135	I.C. 6N135, Opto. Isolator
U8	176-4049	I.C. 4049, Hex Buffer
U9	176-4013	I.C. 4013, Dual D F/F
U10	176-4093	I.C. 4093, Quad 2 Schmit
U11	176-4528	I.C. 4528, Dual 1 Shot
U12	176-7808	I.C. 7808, +12V Reg.
QTY		
1	370-1	Binding Post (Red)
1	370-2	Binding Post (Black)
1	363-2.0	Fuse, Slo Blo 2.0 amp
2	253-4	Washer, #4 Flat
2	251-4	Kepnut, #4
NOTE:	**The following items are omitted or added when the DC Power supply is installed.**	
OMIT		
	363-.750	Fuse, 3AG, 3/4A
	342-1	Power Plug
	86-52	P.W. Board Assy. Power Supply
	315-20-4	Wire, #20AWG, Yellow
	315-20-7	Wire, #20AWG, Violet
ADD		
	315-20-2	Wire, #20AWG, Black
	315-20-0	Wire, #20AWG, Red

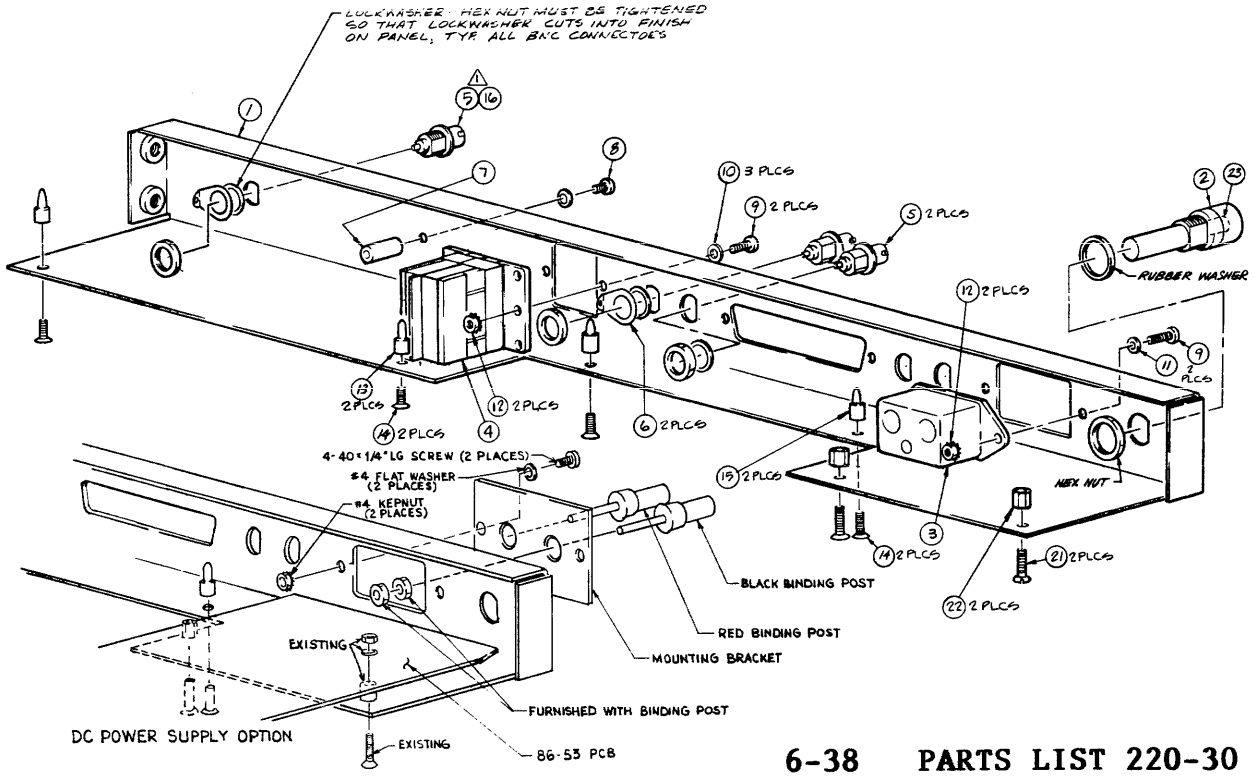
6-35 SYMBOL DESIGNATION REFERENCE 86-53 (cont.)

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6-36 SCHEMATIC - ASSEMBLY 86-53

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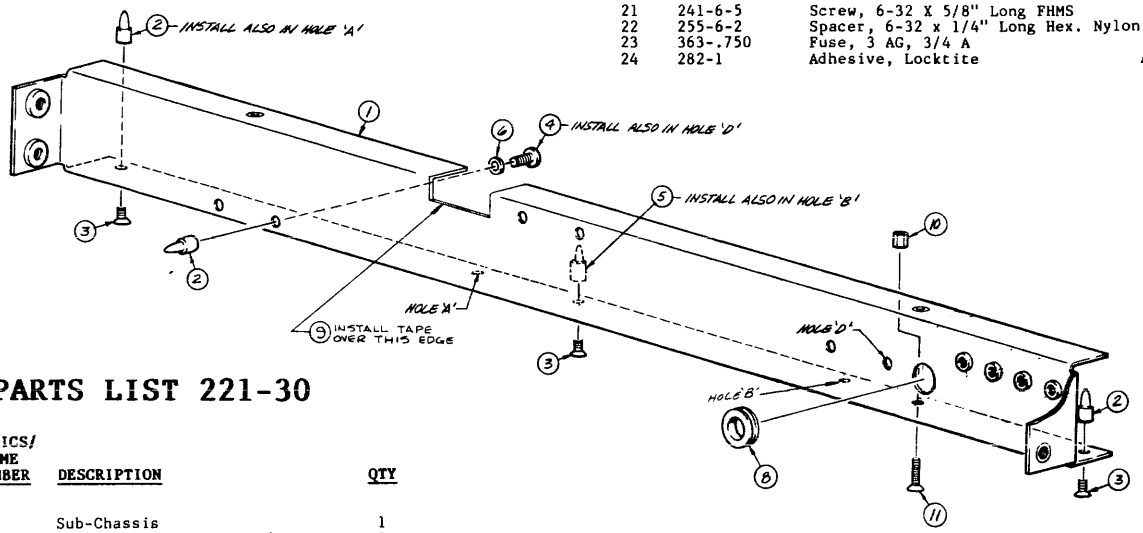


6-37 REAR PANEL ASSEMBLY 220-30

6-38 PARTS LIST 220-30

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
1	216-30	Rear Panel	1
2	365-1	Fuse Holder	1
3	342-1	Power Socket & Line Filter	1
4	61-14	Thumb Wheel Switch (+,- and 0-9)	1
5	375-1	BNC Connector	3
6	256-.375	Solder Lug. .375" I.D.	2
7	255-4-4	Spacer, 4-40 x 1/2" Threaded	1
8	240-4-2	Screw, 4-40 x 1/4" Long PHMS	1
9	240-4-3	Screw, 4-40 x 3/8" Long PHMS	4
10	253-4	Washer #4 Flat	3
11	265-4	Lockwasher #4 Internal Teeth	2
12	251-4	Kepnut, 4-40	4
13	277-2	Spacer, Circuit Board, 1/4" Lg.	2
14	241-6-2	Screw, 6-32 x 1/4" Long FHMS	4
15	277-6	Spacer, PCB 3/8" Lg.	2
16		NOT USED	0
17		NOT USED	0
18	134-24	Wiring Harness (Not Shown)	1
19		NOT USED	0
20		NOT USED	0
21	241-6-5	Screw, 6-32 X 5/8" Long FHMS	2
22	255-6-2	Spacer, 6-32 x 1/4" Long Hex. Nylon	2
23	363-.750	Fuse, 3 AG, 3/4 A	1
24	282-1	Adhesive, Locktite	A/R

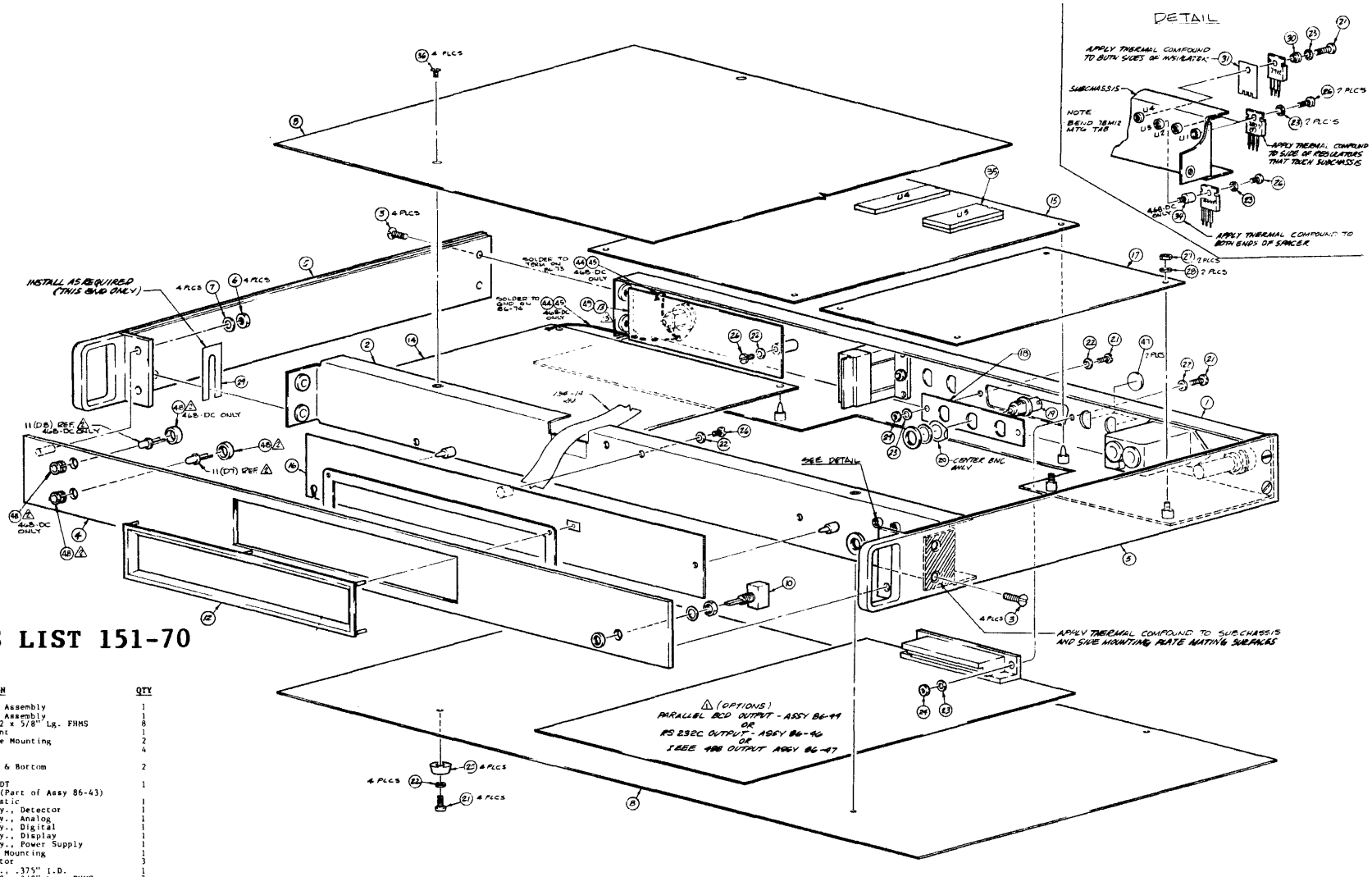
6-39 SUBCHASSIS ASSEMBLY 221-30



6-40 PARTS LIST 221-30

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
1	215-30	Sub-Chassis	1
2	277-2	Spacer, P.W. Board 1/4" Long	5
3	247-6-2	Screw, 6-32 X 1/4" Long FHMS	5
4	240-6-2	Screw, 6-32 x 1/4" Long PHMS	2
5	277-6	Spacer, P.C.B. Support, 3/8 Lg.	2
6	253-6	Washer, #6 Flat	2
7	282-1	Adhesive, Locktite	A/R
8	73-16	Grommet, Rubber	1
9	289-1	Tape, Adhesive, 1/4" W., Mylar	A/R
10	268-6-2	Spacer, 6-32 x 1/4" Lg., Nylon	1
11	241-6-5	Screw, 6-32 x 5/8" Lg., FHMS	1

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6-42 PARTS LIST 151-70

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
1	220-30	Rear Panel Assembly	1
2	221-30	Subchassis Assembly	1
3	241-8-5	Screw, 8-32 x 5/8" Lg. FHMS	8
4	100-70	Panel, Front	1
5	217-30	Plate, Side Mounting	2
6	251-8	Kepnut, #8	4
7		NOT USED	
8	203-6	Cover, Top & Bottom	2
9		NOT USED	
10	60-1	Switch, SPDT	1
11		LED, GRN. (Part of Assy 86-43)	
12	210-2	Bezel, Plastic	1
13	86-73	PC Bd. Assy., Detector	1
14	86-74	PC Bd. Assy., Analog	1
15	86-42	PC Bd. Assy., Digital	1
16	86-43	PC Bd. Assy., Display	1
17	86-52	PC Bd. Assy., Power Supply	1
18	206-30	* Plate, BNC Mounting	1
19	375-1	* BNC Connector	3
20	256-.375	* Solder Lug, .375" I.D.	1
21	240-4-3	Screw, 4-40 x 3/8" Lg., PHMS	7
22	253-4	Washer, #4 Flat	12
23	265-4	* Lockwasher, #4 Int. Teeth	6
24	252-4	* Nut, 4-40 Hex	2
25	261-1	Rubber Feet	4
26	240-4-2	Screw,4-40 x 1/4" Lg., PHMS	4
27	251-6	Kepnut, #6	2
28		NOT USED	
29	263-1	Chassis Shim	A/R
30	271-4	Shoulder Washer, #4	1
31	272-2	Insulator, Mica	1
32		NOT USED	
33		NOT USED	
34	255-100	Spacer, 4-40 x 1/4" Lg.	1
35	177-2764	I.C., 2764 (U5, Installed on 86-42)	1
36	249-1	Screw, 4-40 x 1/4" Lg., FHMS, Blk	8
37	332-2	Power Cord (Not Shown)	1
38	206-1	Bracket, Rack Mtg. (Not Shown)	2
39	400-1	Name Plate, Product I.D.	1
40	281-1	Compound, Thermal (Not Shown)	A/R
41	282-2	Adhesive, Locktite (Not Shown)	A/R
42		NOT USED	
44	320-1	Braid, Tinned Copper	A/R
45	326-4	Sleeving, 1/8" Dia. Shrinkable	A/R
46	400-2	Label, Prod. Warr. (Not Shown)	1
47	274-5	Hole Plug	A/R
48		Mtg. Hardware for P/N 58-1	2 Set

NOTE: When Option Assembly 86-44, 86-46 or 86-47 is ordered, items 18, 19 and 20 will be deleted. Two each of items 23 and 24 will be deleted and replaced with P/N 251-4, #4 Kepnut.

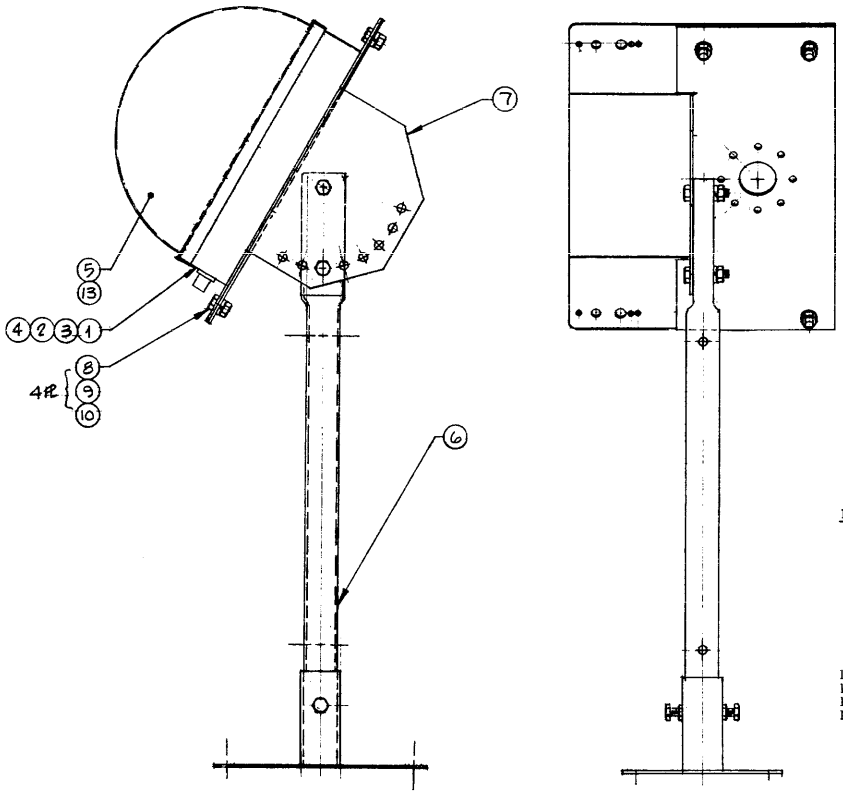
NOTE: When RS-422 Option is specified, the following items will be installed.

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
		On 86-42:	
49		Header, 8 Pin	
	401-2-1-15	(401-2-1-8) (J12)	1
50	176-26LS31	I.C., (U9) 26LS31	1
		On 220-30:	1
51	392-5	Cable Assy., RS-422 (P12)	1
52	206-24	Mtg. Bracket	1
53	240-4-3	Screw, 4-40 x 3/8" Lg.,PHMS	4
54	253-4	Washer, #4 Flat	4
55	251-4	Kepnut, 4-40	4
56	366-2.0	Circuit Brkr., 2A (Install in place of fuse & fuseholder)	1

6-41 MODEL 468-DC FINAL ASSEMBLY 151-70

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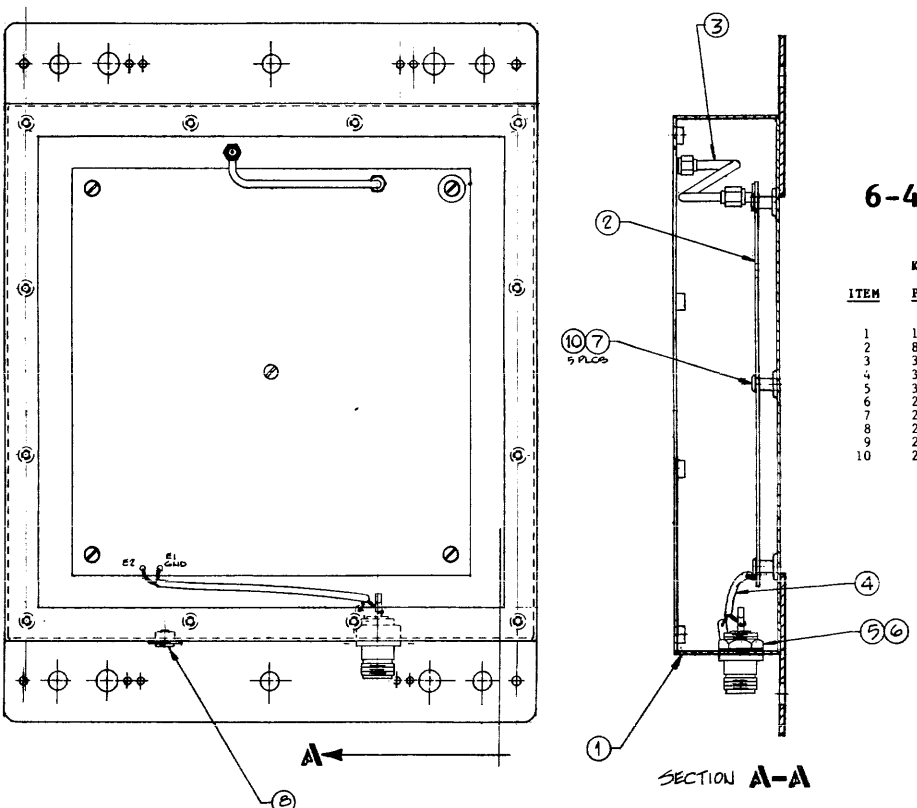
6-43 MODEL A-468MS FINAL ASSEMBLY 142-170



6-44 PARTS LIST 142-170

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
1	141-170	Antenna Sub-Assy.	1
2	138-171	Cover (NOT SHOWN)	1
3	85-13	Satellite Antenna PCB	1
4	381-1A	Connector, SMA Flange Mt.	1
5	227-16	Dome Cover	1
6	141-173	Antenna Mtg. Kit	1
7	138-174	Pivot Bracket	1
8	248-.31-8	Screw, Hex 5/16-18 x 1" Lg.	4
9	254-.312	Lockwasher, 5/16 Split	4
10	252-.312	Hex Nut 5/16-18	4
11	400-2	Label, Product Warranty (NOT SHOWN)	1
12	400-1	Label, Product I.D. (NOT SHOWN)	1
13	285-1	Sealant, Silicone	A/R

6-45 MODEL A-468MS SUB-ASSEMBLY 141-170

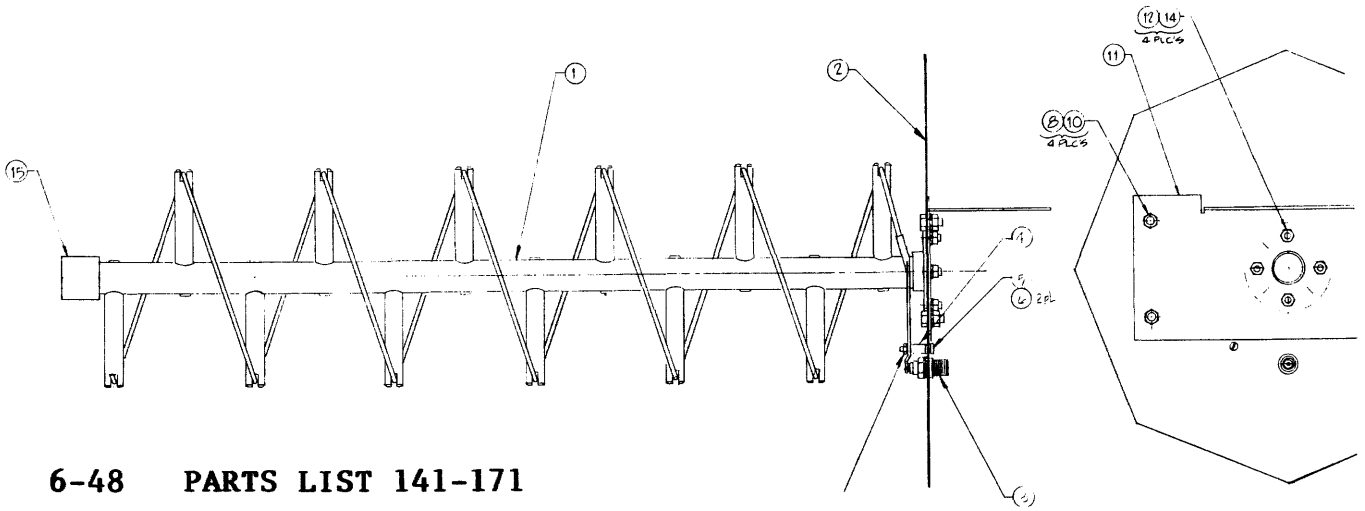


6-46 PARTS LIST 141-170

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
1	138-170	Antenna Box	1
2	86-170	468MHz Down Converter PCB Assy.	1
3	339-6-0	Cable Assy. (Male SMA to Male SMA)	1
4	337-4	Cable, Coax RG 188 A/U	A/R
5	383-1	Connector N (Solder Cup)	1
6	256-.625	Solder Lug, 5/8" I.D.	1
7	240-6-2	Screw, PAN HD, 6-32 x 1/4 Lg.	5
8	240-8-4	Screw, PAN HD, 6-32 x 1/2 Lg.	1
9	257-8	Washer, Seal #8	1
10	265-6	Lockwasher, #6 Int. Teeth	5

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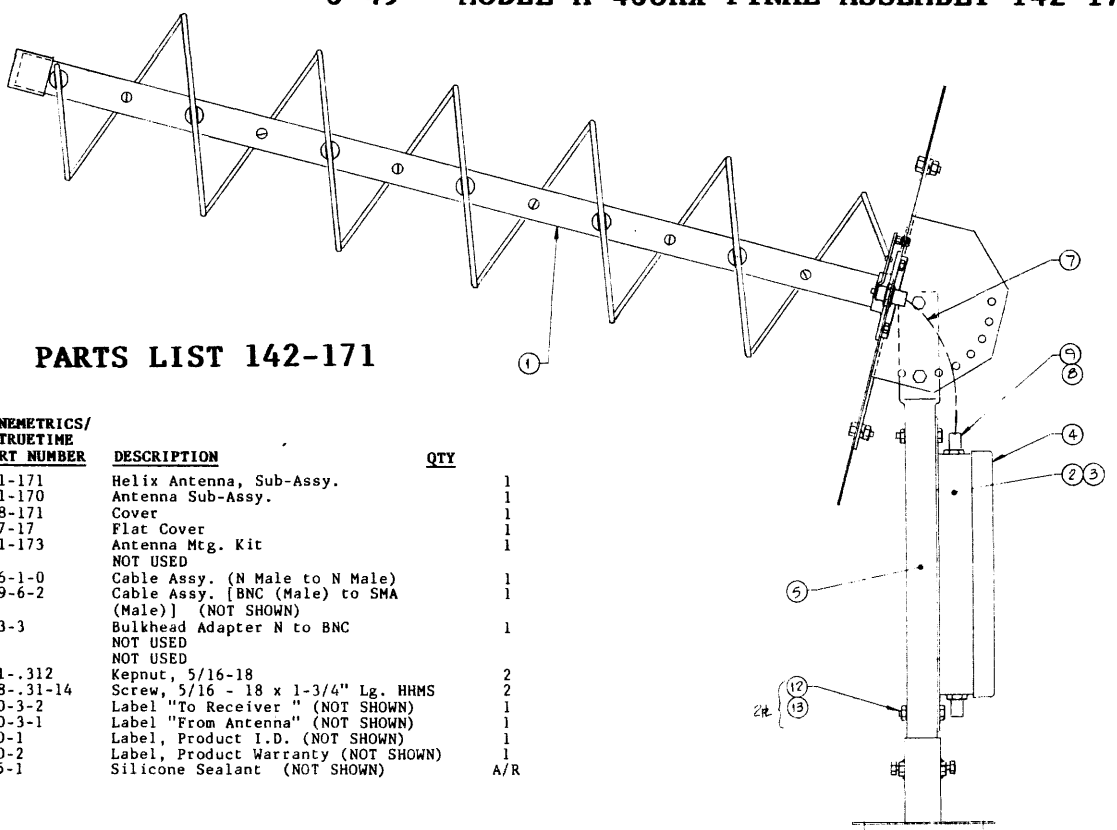
6-47 MODEL A-468HX SUB-ASSEMBLY 141-171



6-48 PARTS LIST 141-171

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
1	141-172	Helix Antenna Coil Sub-Assy.	1
2	138-177	Helix Ground Plane	1
3	383-1	Connector 'N' (Solder Cup)	1
4	255-6-13	Spacer #6 x 3/8" Lg. (Alum.)	1
5	240-6-6	Screw, 6-32 x 3/4" Lg. PHMS	1
6	271-6	Shoulder, Washer, #6 Nylon	2
7	251-6	Kepnut, 6-32	1
8	241-.25-6	Screw, 1/4-20 X 3/4" LG", FHMS	4
9		NOT USED	
10	251-.250	Kepnut, 1/4-20	4
11	138-174	Pivot Bracket	1
12	248-.31-6	Screw, 5/16 - 18 x 3/4" Lg., HHMS	4
13		NOT USED	
14	251-.312	Kepnut, 5/16-18	4
15	227-13	End Cap, Plastic	1

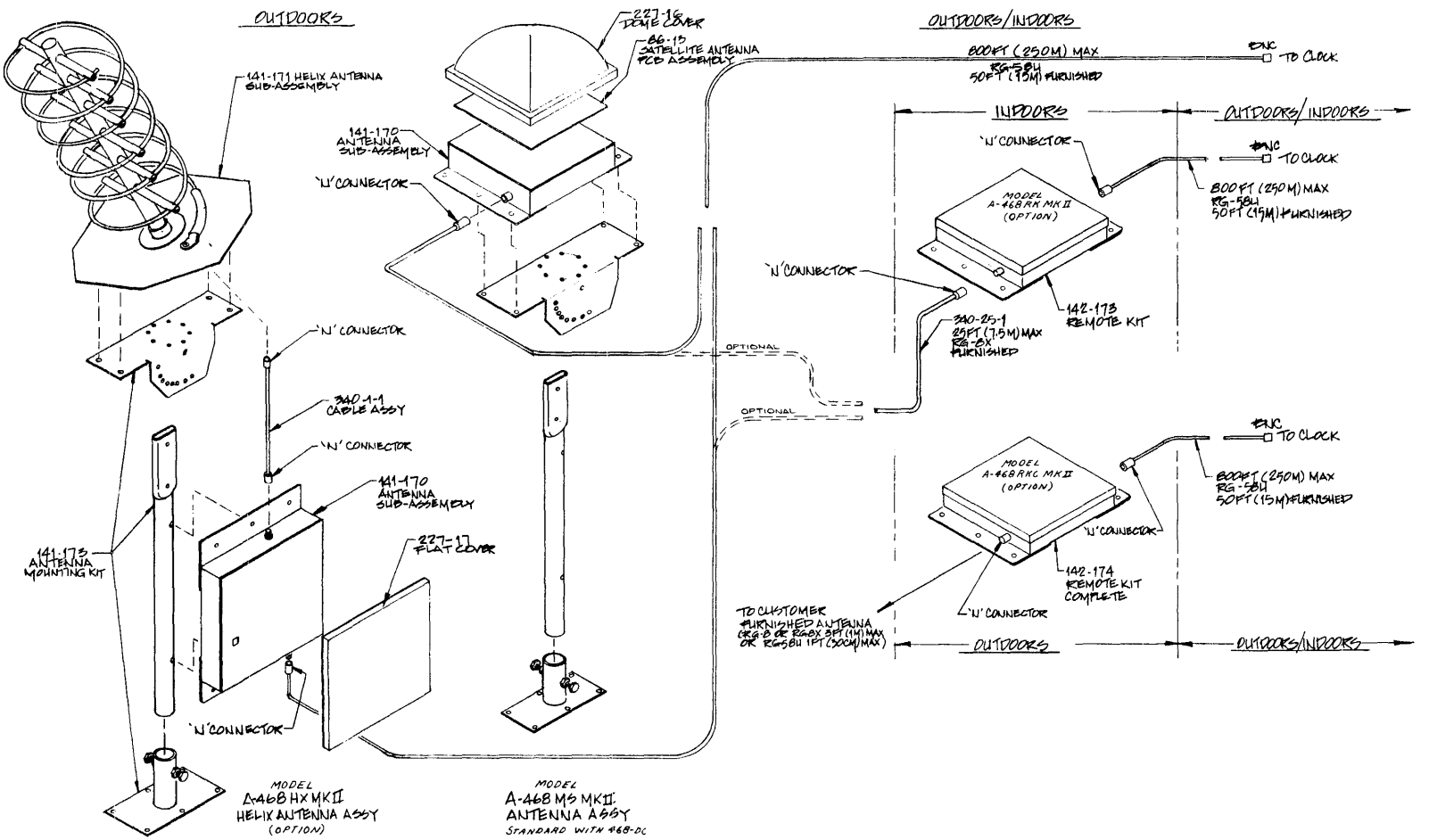
6-49 MODEL A-468HX FINAL ASSEMBLY 142-171



6-50 PARTS LIST 142-171

ITEM	KINEMETRICS/ TRUETIME PART NUMBER	DESCRIPTION	QTY
1	141-171	Helix Antenna, Sub-Assy.	1
2	141-170	Antenna Sub-Assy.	1
3	138-171	Cover	1
4	227-17	Flat Cover	1
5	141-173	Antenna Mtg. Kit	1
6		NOT USED	
7	336-1-0	Cable Assy. (N Male to N Male)	1
8	339-6-2	Cable Assy. [BNC (Male) to SMA (Male)] (NOT SHOWN)	1
9	383-3	Bulkhead Adapter N to BNC	1
10		NOT USED	
11		NOT USED	
12	251-.312	Kepnut, 5/16-18	2
13	248-.31-14	Screw, 5/16 - 18 x 1-3/4" Lg. HHMS	2
14	400-3-2	Label "To Receiver " (NOT SHOWN)	1
15	400-3-1	Label "From Antenna" (NOT SHOWN)	1
16	400-1	Label, Product I.D. (NOT SHOWN)	1
17	400-2	Label, Product Warranty (NOT SHOWN)	1
18	285-1	Silicone Sealant (NOT SHOWN)	A/R

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6-51 A-468 ANTENNA SYSTEMS

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SECTION VII

ANTENNA INSTALLATION

FOR

MODEL A-468MS
MODEL A-468MS/RK
MODEL A-468HX
MODEL A-468RK
MODEL A-468RKC
EXTERNAL ANTENNA INPUT

7-1 GENERAL INFORMATION

7-2 All of the above antennas and kits are specifically for use with the Kinemetrics/TrueTime Model 468-DC Satellite Synchronized Clocks. Since these antennas include receiver controlled frequency conversion circuits, they must be used with the TrueTime Receiver/Clocks.

7-3 SECTION II of the 468-DC Synchronized Clock Operating and Service Manual contains the necessary information for determining the correct antenna pointing angle. This section provides information as to the physical size and mounting dimensions.

7-4 MODEL A-468MS

7-5 The Model 468-DC Synchronized Clock is normally shipped with the Model A-468MS Antenna unless the customer requests the Model A-468HX (see SECTION entitled, MODEL A-468HX), or the Model A-468RKC (see SECTION entitled MODEL A-468RKC).

7-6 FIGURE 7-1 provides the physical dimensions of the Model A-468MS to assist in installation. When a Model A-468MS is ordered, the following items are supplied:

1) Receiving antenna (Model A-468MS)

2) Base, Antenna Mounting

3) Shaft, Antenna Mounting

4) Antenna Mounting Hardware Kit

5) Lead-in Coax, 50 ft of RG-58/U.

7-7 FIGURE 7-2 provides the mounting hole pattern used for the base which is used to mount the Model A-468MS and Model A-468HX.

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FIGURE 7-1 MODEL A-468MS AND MODEL A-468 MS/RK DIMENSIONS

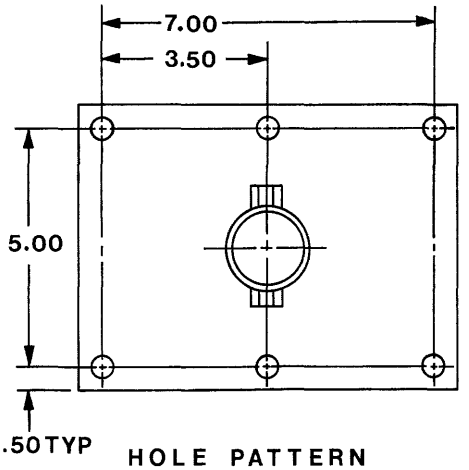


FIGURE 7-2 BASE, ANTENNA MOUNTING DIMENSIONS

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7-8 The Antenna Mounting Hardware Kit provided to mount the base consists of:

1) Four (4) each 5/16" dia., 2" long bolts with nuts and washers.

2) Four (4) each 5/16" dia., 3.5" long lag screws.

This kit should provide for universal mounting of the base at most locations.

7-9 INSTALLATION:

1) Select an installation site with a clear view of the satellite(s) which you plan to be receiving. The viewing angle of the satellites is provided in SECTION II of this manual.

2) Using the Mounting Hardware Kit provided, secure the base to an appropriate surface.

3) Attach the "Shaft" provided to the "Pivot Bracket" attached to the back of the Antenna Package. Install one bolt through the top hole in the shaft and through the center hole of the "Pivot Bracket".

4) Slip the free end of the shaft into the tubing in the base previously mounted in Step 2 above.

5) Rotate and pivot the antenna in the base to the proper orientation for satellite reception. Install the remaining bolt through the "Shaft" and "Pivot" bracket as well as the two bolts in the base to secure the Shaft. Tighten all bolts.

6) Connect the supplied 50 ft. coax to the antenna. The "N" connector connects to the A-468MS antenna and the end with the "BNC" connects directly to the Model 468 "ANTENNA" connector. Additional cable in 50 and 100 foot lengths can be obtained from TrueTime. These additional lengths have "BNC" connectors on both ends and includes a jack-to-jack adapter allowing the cables to be connected end to end.

7-10 MODEL A-468HX

7-11 The Model A-468HX is available as an extra cost option in place of the MODEL A-468MS. The A-468HX is normally only required when the viewing angle of the satellite is less than 5° above the horizon. Since the satellite signal is attenuated by the increased travel distance through the atmosphere at these low angles, the added 6 db of gain provided by the helix can be of benefit to the user. In addition, whenever local interference of

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"land mobile" transmitters is a significant problem, the narrower beam width of the helix can aid in such signal rejection.

7-12 For shipment, the A-468HX is packed in one wooden crate and includes the following:

1) Helix Antenna Sub Assembly (including the Pivot Bracket).

2) Shaft, Antenna Mounting.

3) Antenna electronics package including 1 ft. interconnecting cable).

4) Base, Antenna Mounting (including Mounting Hardware Kit).

5) Lead-in coax, 50 ft. of RG-58/U.

7-13 A photograph of the assembled MODEL A-468HX, including dimensions, is provided in FIGURE 7-3.

7-14 INSTALLATION:

1) Keeping in mind the viewing angle of the satellite as determined from SECTION II of this manual, select a suitable installation site for the antenna.

2) Using the Antenna Mounting Hardware Kit provided, securely mount the "Base" in the selected site. The dimensions for this base are provided in FIGURE 7-2.

3) Remove the shaft and antenna electronics package from the shipping crate. Slip the round end of this shaft into the base. Bolt the antenna electronics package to the shaft with the hardware provided. NOTE: The "N" connector labeled "FROM ANTENNA" must bolted toward the "flattened" end of the shaft. Refer to FIGURE 7-3.

4) Remove the Helix Antenna from the shipping crate. Using one of the bolts provided, connect the center hole in the pivot bracket on the back of the helix, to the top hole in the shaft.

5) Pivot the helix to the correct elevation for satellite reception and install a second bolt through the pivot bracket and through the shaft. Select the hole in the pivot bracket closest to the elevation required for your location. NOTE: REGARDLESS OF THE ACTUAL ELEVATION OF THE SATELLITE, NEVER AIM THE ANTENNA LESS THAN 15' ABOVE THE HORIZON. AN ANGLE OF LESS THAN 15' WILL RESULT IN RECEPTION OF EARTH GENERATED "THERMAL

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NOISE". THIS WILL INTERFERE WITH THE "GOES" SIGNAL AND DEGRADE THE UNIT PERFORMANCE.

Tighten the two pivot bracket bolts just installed.

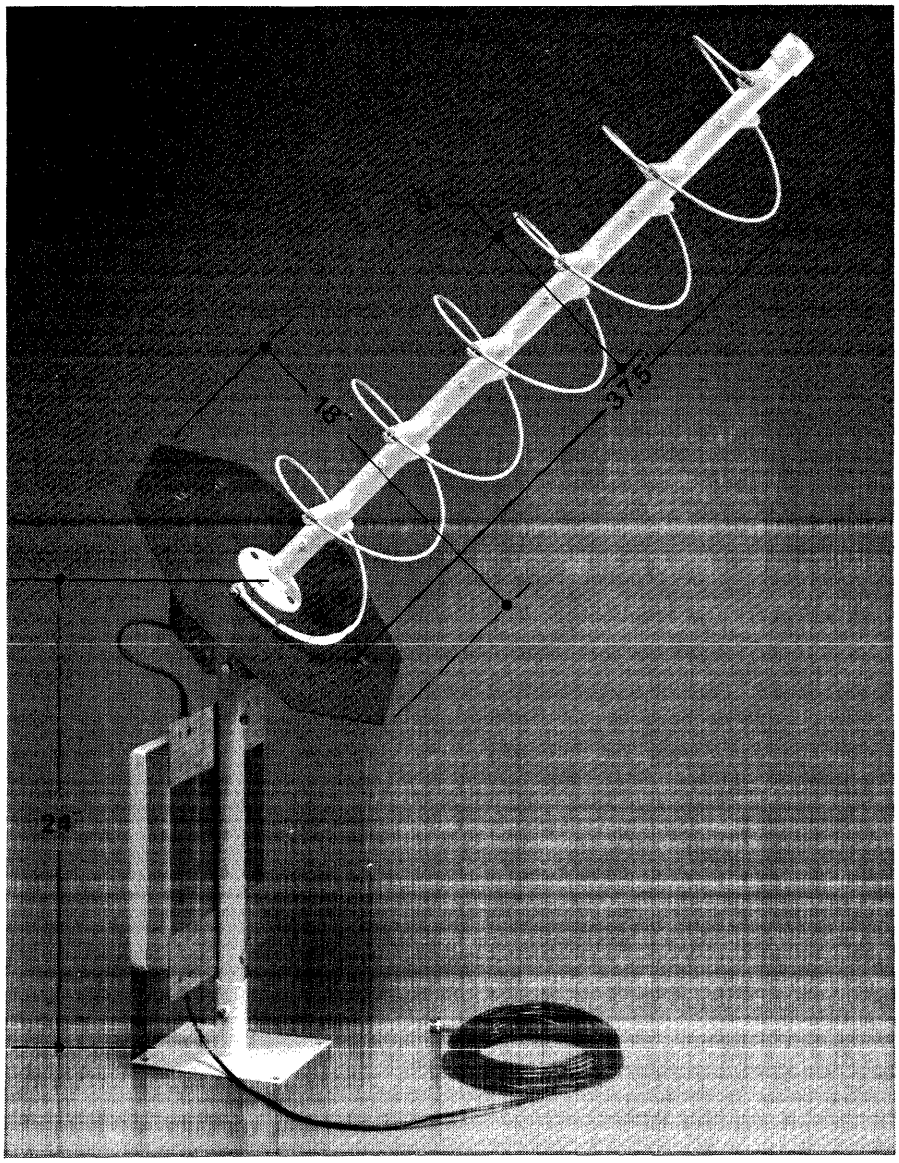


FIGURE 7-3 MODEL A-468HX ANTENNA DIMENSIONS

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6) Rotate the helix to the proper compass heading for satellite reception and install the two bolts provided through the base to secure the rotation of the helix.

7) Connect the free end to the 1 ft. cable (which is factory connected to the top end of the antenna electronics package) labeled "FROM ANTENNA" to the "N" connector on the back of the Helix Antenna.

8) Connect the 50 ft. lead-in coax from the "N" connector on the bottom of the antenna electronics package (labeled "TO RECEIVER") to the "ANTENNA" BNC on the MODEL 468-DC. Additional cable in 50 and 100 foot lengths can be obtained from TrueTime. These additional lengths have BNC connectors on both ends and includes a jack-to-jack adapter allowing the cables to be connected end to end.

7-15 MODEL A-468RK

7-16 The Model A-468RK Remote Kit is available as an extra cost option for the Model A-468MS or A-468HX. This is generally ordered when the user expects to encounter temperatures below 0°C or above 50°C. This "REMOTE KIT" provides an in-line housing for the temperature sensitive components in the antenna. This in-line housing can be up to 25 feet from the A-468 when using the supplied cable. The 25 foot cable supplied with this option should not be shortened or lengthened. The intention of this 25 foot addition to the cable is to permit the user to place this housing in a more protected environment (under the eaves, in the attic, or in the actual users building).

7-17 When the Model A-468RK is ordered with the Model A-468MS or 468-HX, in addition to the items received as described in SECTION VII under MODEL A-468MS or MODEL A-468HX, the following items will be included:

1) Antenna electronics housing (A-468RK)

2) Special 25 ft. interconnecting cable

7-18 The user should note that the A-468RK will only operate with the TrueTime Model A-468MS or A-468HX which has been prepared to operate with the Model A-468RK at the factory. Such units are labeled as "MODEL A-468MS/RK" and "MODEL A-468HX/RK" respectively.

7-19 FIGURE 7-4, on the next page, is a dimensioned photograph of the Model A-468RK to assist in mounting of this housing. FIGURE 7-5 provides a complete mounting hole pattern for preparation in bolting this housing in place.

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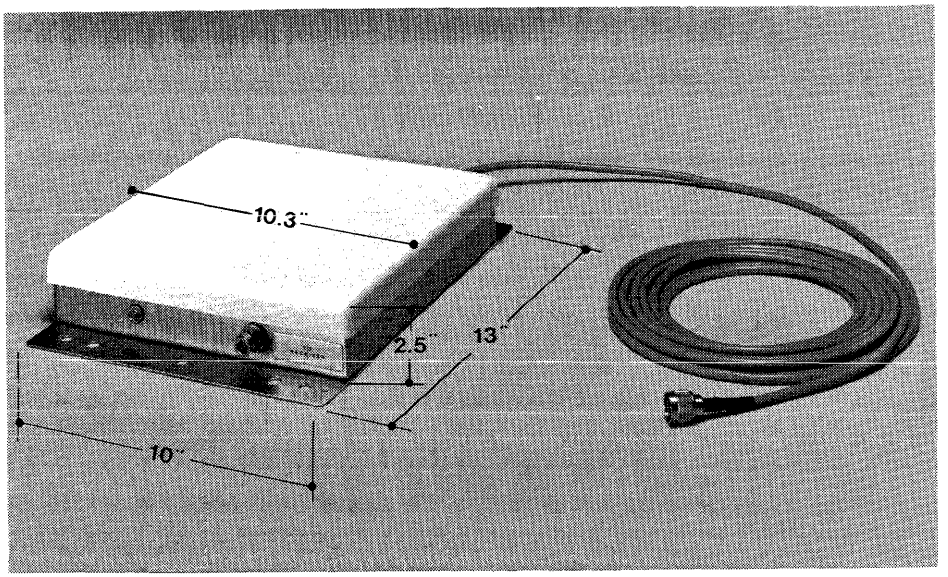


FIGURE 7-4 MODEL A-468RK AND MODEL 468-RKC DIMENSIONS

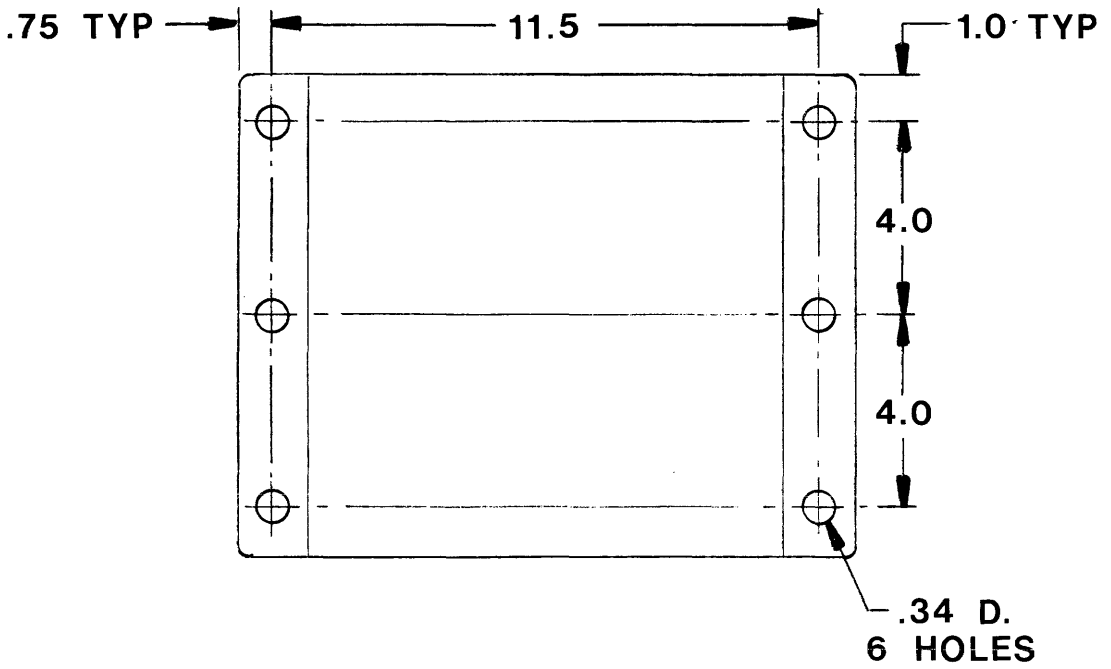


FIGURE 7-5 A-468RK AND A-468RKC MOUNTING DIMENSIONS

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7-20 Once the Model A-468MS or A-468HX is mounted and installed, as described earlier in this section, the Model 468-RK should be mounted within the 25 ft. cable run of the antenna. To connect the system:

1) Using the provided 25 foot cable (RG-8U), connect one end of the cable to the receiving antenna output "N" connector. Connect the other end to the A-468RK "N" connector labeled "FROM ANTENNA".

2) Connect the 50 ft. lead-in coax (RG-58/U) to the "N" connector labeled "TO RECEIVER". The remaining end of this 50 ft. cable is provided with a BNC for connection to the "ANTENNA" input on the Model 468-DC Synchronized Clock.

7-21 MODEL A-468RKC

7-22 The Model A-468RKC is normally ordered as a "no-charge" option whenever the user wishes to use his own signal receiving medium, such as an aircraft fin antenna. This A-468RKC consists of all the same electronics housed in the Model A-468MS or A-468HX antenna, but repackaged in a single housing without the receiving medium.

7-23 When a Model 468-RKC is ordered, the following items are supplied:

1) Antenna electronics housing (Model A-468RKC)

2) 50 ft lead-in coax, RG-58/U

7-24 The input connector for the A-468RKC is an "N" connector to accept the 468MHz signal from the users antenna. The input cable from your receiving medium should be kept as short as possible. It is recommended that RG-8 or RG8X cable be used and kept less than 3 feet. If RG-58/U is used, a length of less than 1 foot must be used.

7-25 The A-468RKC is identical in size and mounting pattern as the A-468RK as shown in FIGURES 7-4 and 7-5.

7-26 For the ouput from the A-468RKC, a 50 foot length of RG-58/U is provided. From the connector labeled "TO RECEIVER", connect the appropriate end of this lead-in coax. Connect the other end to the Model 468 "ANTENNA" input connector (BNC). Additional cable in 50 and 100 foot lengths can be obtained from TrueTime. These additional lengths have BNC connectors on both ends and includes a jack-to-jack adapter allowing the cables to be connected end to end.

7-27 EXTERNAL ANTENNA INPUT

7-28 This option can be ordered in conjunction with the standard Model A-468MS, or A-468HX antenna. When ordered, it

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allows the unit to operate as a standard antenna or through the use of an input from an "external antenna".

7-29 With this option, two "N"connectors are factory installed on the side of the antenna case and a short coax is connected between them. When the signal is received in the helix or through the microstrip, the signal goes out through the connector labeled "FROM ANTENNA", through the short coax and into the unlabeled "N" connector. If the jumper is disconnected from the unlabeled "N" connector, the external antenna can be fed directly into the pre-amp.

7-30 This option allows versatile input to the pre-amp and basically allows the standard unit to be used as a Model 468-RKC. The size and installation of the Model A-468MS or A-468HX is unchanged by this option.

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SECTION VIII

IRIG-B AND IRIG-H TIME CODE FORMAT

8-1 INTRODUCTION

8-2 The IRIG-B Time Code as outputted from the Model 468-DC and IRIG-H if optionally ordered, is as described in "IRIG STANDARD TIME FORMATS" Tele-Communications Working Group, Inter-Range Instrumentation Group, Range Commanders Council, IRIG Document 104-70. This document is published by Secretariat, Range Commanders Council, White Sands Missile Range, New Mexico, 88002 dated August 1970.

8-3 The standard time formats described in this publication were designed for use in missile, satellite and spaceresearch programs which require the use of a standardized time format for the efficient interchange of test data among the various users of the data. These formats are suitable for recording on magnetic tape, oscillographs, film and for real-time transmission in both automatic and manual data reduction. The IRIG-B format from the Model 468-DC is suitable for remote display driving, recording on magnetic tape and many other uses. When the output is used as IRIG-B in the strict sense as described by the above mentioned document, the output must be in Universal Coordinated Time (UTC) and not converted to 12-hour basis or local time zone as is the capability of this instrument. The same is, of course, true of the IRIG-H output.

8-4 IRIG CODE FORMAT

8-5 The IRIG-B and IRIG-H Time Code as provided by the Model 468-DC is a serial time format with two coded expressions. The first expression is a time-of-year code word in Binary Coded Decimal (BCD) notation as days, hours, minutes and seconds. The second expression used here is a set of elements for encoding control functions which are used in the Model 468-DC to provide the user with worst case estimate of the timing accuracy. The estimate for this timing accuracy is discussed in SECTION III, entitled DISPLAY and also PARALLEL BCD TIME OUTPUT (Special Order Option), of this manual. The third expression sometimes found in the IRIG code, which is an expression of time-of-day in Straight Binary Seconds (SBS) notation, is not outputted by the Model 468-DC.

8-6 Each pulse, or element, in the format of the level-shift encoded signal has a leading edge which is "on time". The repetition rate of the elements in the IRIG-B is 100 pulses per second and 1 pulse per second in IRIG-H. The index count interval, or the time between the leading edges of two consecutive elements, is 0.01 seconds with IRIG-B and 1 second with IRIG-H.

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8-7 The time frame format begins with a frame reference marker and consists of all the elements between two consecutive frame reference markers. This frame reference marker consists of a consecutive position identifier element and a "P" reference element each having a duration of 0.008 seconds in IRIG-B and .8 seconds in IRIG-H. The on time reference point of time frame is the leading edge of the second pulse. The repetition rate of the time frame called the "time frame rate" is 1 fps (frame per second) with IRIG-B and 1 fpm (frame per minute) with IRIG-H. P_0 occurs one index count interval before the frame reference point and each succeeding position identifier (P_1, P_2, P_3, P_4, etc.) occurs every succeeding tenth element. The repetition rate then, of the position identifiers, is 10 pps in IRIG-B and 6 ppm in IRIG-H. There are seven position identifiers per IRIG-H frame and 11 position identifiers per IRIG-B frame.

8-8 The BCD time-of-year code word is pulse width coded. A binary "1" element has a duration of 0.005 seconds, a binary "0" has a duration of 0.002 seconds for IRIG-B. IRIG-H in .5 seconds for a "1" and .2 seconds for a "0". This format is then used to encode the BCD time-of-year code word which consists of decimal digits in a 1-2-4-8 binary sequence.

8-9 When the IRIG-B from the Model 468-DC is in the amplitude modulated 1 KHz format, the sine wave carrier frequency is synchronized to have a positive going axis crossing coincident with the leading edge of the modulating format elements. The IRIG-H format is D.C. level shift format as supplied by the factory. See SECTION III, entitled IRIG-H (Special Order Option).

8-10 FIGURE 8-1 on the following page depicts the IRIG-B Time Code, and FIGURE 8-2 depicts IRIG-H.

8-11 CONTROL-FUNCTIONS

8-12 The control functions provide the user of the IRIG-B Time Code with a record in their recording of the estimated worst case accuracy of the Model 468-DC time information. This is more fully covered in SECTION III, under DISPLAY and PARALLEL BCD TIME OUTPUT (Special Order Option). A "1" or .005 second pulse width in the following locations signify the accuracy specifically.

Control Function Element 4 (or time P_r+530ms) in-lock indicator
Control Function Element 6 (or time P_r+550ms) indicates $\pm$1.0ms worst case
Control Function Element 7 (or time P_r+560ms) indicates $\pm$5.0ms worst case
Control Function Element 8 (or time P_r+570ms) indicates $\pm$50.0ms worst case
Control Function Element 9 (or time P_r+580ms) indicates $\pm$500.0ms worst case

8-13 This information is also utilized by the TrueTime Model RD-B to duplicate the display of the 468-DC Master Clock. At $\pm$50ms the colons are flashed, and at $\pm$500ms the display will blink on the Model RD-B.

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8-14 The IRIG-H Time Code does not contain these control bits. These have not been included due to the relative time frames and usage of this code as opposed to the IRIG-B Code.

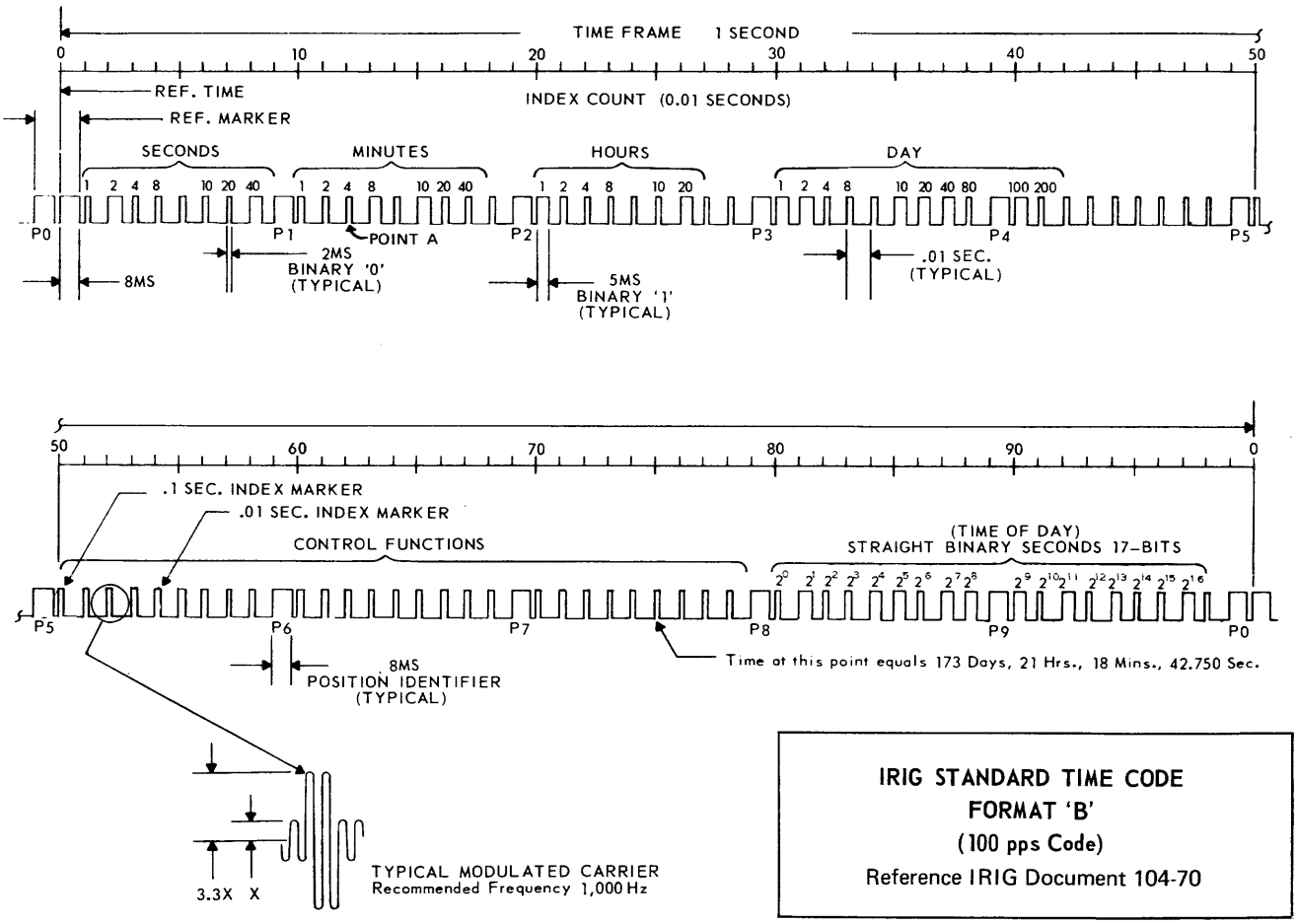
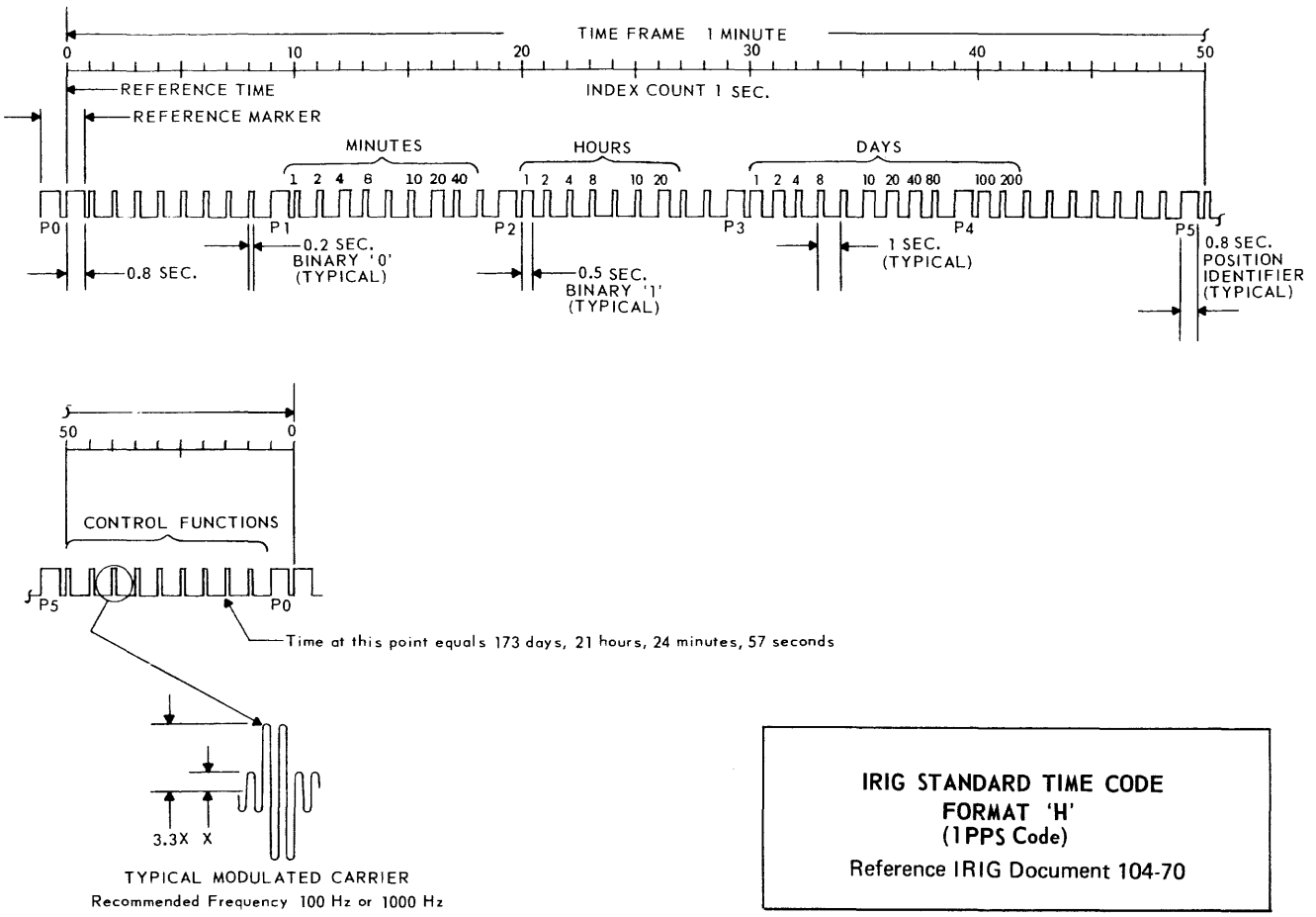


FIGURE 8-1 IRIG-B TIME CODE FORMAT

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IRIG STANDARD TIME CODE
FORMAT 'H'
(1PPS Code)
Reference IRIG Document 104-70

FIGURE 8-2 IRIG-H TIME CODE FORMAT

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IN CASE OF FAILURE

MODEL_____ S/N_____ OPTIONS_____

First contact the Service Department at Kinemetrics/True Time at (707) 528-1230. Complete this form, attach to instrument and forward to Kinemetrics/TrueTime.

Failure Mode is:
Constant ☐
Intermittent ☐

Describe Problem/Symptoms:
_____
_____
_____

NAME_____ COMPANY_____

STREET_____ CITY_____

STATE_____ ZIP_____ PHONE NO._____

IN CASE OF FAILURE

MODEL_____ S/N_____ OPTIONS_____

First contact the Service Department at Kinemetrics/True Time at (707) 528-1230. Complete this form, attach to instrument and forward to Kinemetrics/TrueTime.

Failure Mode is:
Constant ☐
Intermittent ☐

Describe Problem/Symptoms:
_____
_____
_____

NAME_____ COMPANY_____

STREET_____ CITY_____

STATE_____ ZIP_____ PHONE NO._____

FOLLOW UP INFORMATION EXCHANGE

MODEL_____ S/N_____ OPTIONS_____

Please fill in and mail on _____(One Year).

1. How is the instrument used?_____
_____

2. Describe any problems or changes you would like to see
_____
_____
_____

NAME_____ COMPANY_____

STREET_____ CITY_____

STATE_____ ZIP_____ PHONE NO._____

USER REGISTRATION

MODEL_____ S/N_____ OPTIONS_____

Please complete this card and return to Kinemetrics/True Time. This will allow us to keep you directly informed of any manual corrections or additions and application notes which apply to your particular instrument.

NAME_____ COMPANY_____

STREET_____ CITY_____

STATE_____ ZIP_____ PHONE NO._____

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