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Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
D-82054 Sauerlach
Germany

declare that the product

IP 360

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date: 17.01.1997

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User's Manual

IP 360 Rev. 6

1st edition

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1. Introduction

1.1 Short Description

The **IP360** is another excellent product out of the MicroSys' **Single Euro** VME line. The board uses the powerful **32 bit MC68360** communication controller from Motorola. The IP360 offers a 16 bit wide VMEbus shared **SRAM** area, one or two 32 bit wide **DRAM** banks and a 32 bit wide **FLASH** memory bank.

A 32 pin JEDEC socket for an 8 bit ROM, PROM or FLASH device can be used for the board firmware. The **SRAM** as well as the onboard **real time clock** can be supported with either a rechargeable NiCd battery, a long time standing Lithium Cell or a service free goldcapacitor. A serial **EEPROM** allows the power free storage of board or user specific data.

The board contains **two** piggyback slots according to the Green Spring Logic Interface Specification Revision 0.7.1 for **IP modules**. It was designed to work as an intelligent carrier board for 'IndustryPack' modules in embedded, stand-alone or multiprocessing applications. The various communication functions of the MC68360 can be supported by an additional slot for special I/O modules, which offers all kind of EIA interface standards or network facilities. The **background debug port**, the JTAG test port, and the in-system-programming port of the onboard logic can be used for board maintenance and software debug purposes.

The VMEbus interface contains a single level arbiter and requester with a four level ROR option, a programmable 7 level **VMEbus interrupter** and interrupt handler and a memory mapped **mailbox** with interrupt capability. The two SMC serial interface channels of the MC68360 with RS232 standard are direct available onboard the IP360 via two connectors.

The **variable front end** of the IP slot area can be fitted out with various adapter boards out of the IPAxx series with different connector types. This allows also for low cost custom designed front ends.

The IP360 will take a maximum of **8 MBytes** of **DRAM, 1 MBytes** of **EPROM, 8 MBytes** of **Flash** memory and up to **1 MBytes** of **SRAM.**

The complete board is implemented in **CMOS technology**, which allows for a power consumption as low as: **5V / 3W @ 33MHz** CPU speed.

The 5 volt board supply voltage is protected by a transient suppresser diode against overvoltage or wrong polarity.

The IP360 conforms to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297.

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1.2 Options

- different IPAxx front adapter board solutions
- different DRAM sizes with one or two banks populated
- different FLASH memory sizes by different package types
- different SRAM memory sizes by different package types
- different IP compatible modules
- different IE36x communication piggyback boards

1.3 Specifications

The power requirements for the IP360 board are shown in the following table. The given values are valid for the IP360 with two populated DRAM banks. The power consumption of the optionally used IP-Modules and I/O-Module must be added to the given values.

–	Power Requirements:	+5V, +5/-2.5%,	400mA + used IP or I/O modules
		+12V, +5/-2.5%	0mA + used IP or I/O modules
		-12V, +5/-2.5%	0mA + used IP or I/O modules

The IP 360 can be supplied with single 5 volts, if neither the optional IP modules nor the optional I/O module uses the 12 volts supply.

1.4 Related Documentation

The following manual are applicable to the IP 360:

- VMEbus Specification Manual ANSI/IEEE STD1014-1987
- Green Spring IndustryPack Logic Interface Specification
- M68360 QUICC User's Manual
- Real-time Clock Module RTC-72423 Application Manual
- XICOR X24C16 serial EEPROM Data Sheet

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2. Delivery

2.1 Items shipped with this unit

- User's Manual IP360 Hardware
- MicroSys shipping carton



ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys Shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

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3. Installation

3.1 Items required for IP 360 installation

For installation of the IP 360, the following items are required.

– Card cage or housing

– VMEbus motherboard

– Adequate rated power supply

3.2 Points to be observed

Before the unit is inserted into the card cage, the following points should be observed.

– Unit requires +5V (+ 5 %, - 2,5 %),

– Unit requires optional +/-12V (+ 5 %, - 2,5 %),

– Mounted IP-Modules may require +/-12V.

– Be sure voltage is of correct polarity.

– Unit should only be inserted into, and removed from card cage when power is off.

– The IP-Modules must only be inserted or removed during power off.

– The card cage should be well ventilated. The operating temperature should never exceed it’s specified range.

– Check default jumper or switch setting.



GUARANTEE IS VOID IF UNIT IS OPERATED OUT OF IT’S SPECIFICATIONS!

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4. Board Overview

4.1 Features IP 360

Board Format: single eurocard format

Main Processor: MC68360, (QU)ad (I)ntegrated (C)ommunication (C)ontroller
CPU32+ processor core
background debug mode
fixed clock rate up to 33MHz
programmable memory controller functions
four general purpose timers
two independent DMA channels
bus monitor
software watchdog
centronics interface support
RISC controller for communication support
two (S)erial (M)anagement (C)ontrollers
four (S)erial (C)ommunication (C)ontrollers
four baud rate generators
time slot assignor
(T)ime (D)ivision (M)ultiplexed channel support

Dynamic RAM: 4/8MByte ram area with 32 bit data bus
one or two banks of fast page DRAM
each bank with 4MByte capacity

Static RAM: two 8 bit organized SO devices
max. 1 MByte capacity
16 bit data bus width
sharable with other VMEbus masters
optional data backup with onboard supply

Flash Memory: four 8 bit organized TSOP devices
max. 8 MByte capacity
32 bit data bus width
single 5 volt programmable devices

EPROM area: one 32 pin socket according to JEDEC standard
max. 1 MByte capacity
device type selection by soldering links
8 bit data bus width
ROM, PROM, EPROM, EEPROM, FLASH support

EEPROM: 2KByte I2C serial access device

IP-Module: two 16 bit slots for industry pack modules
8/16 bit data memory cycle support
8/16 bit data I/O cycle support
8/16 bit data memory-DMA cycle support
8/16 bit data I/O-DMA cycle support
32 Byte ID read cycle support
two level interrupt support
single channel DMA support
exchangeable front end for I/O connector configuration

Real Time Clock: RTC-72423 with time & date function
backup function with onboard supply

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Data backup:	short time backup via service free gold cap rechargeable NiCd battery support for extended backup long time backup via lithium cell external backup via VMEbus standby line
Front panel Leds:	one user programmable led power status and processor HALT state led
Front panel Keys:	RESET key for complete hardware reset
Interrupt handler:	7 level onboard interrupt handler 7 level VMEbus interrupt handler software programmable VMEbus interrupt mask
System controller:	full VMEbus slot 1 functions single level arbiter single jumper function enable
VMEbus interface:	according to ANSI/IEEE STD1014-1987
VMEbus master:	DTB A16/A24 -D8/D16 VMEbus address modifier support standard and short I/O addressing dynamic bus sizing feature
VMEbus slave:	DTB A24 -D8/D16 programmable VMEbus shared access base address programmable VMEbus shared access window size
VMEbus mailbox:	memory mapped 1KByte range of the SRAM area autovector controlled local interrupt mode
VMEbus arbiter:	single level arbiter on level 3
VMEbus requester:	single level 2:1 pass requester release when done or 4 level release on request modes
VMEbus interrupter:	7 level & vector programmable interrupter

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4.2 Addressmap IP 360

Type	Base	End	Data Lane	Select	Size	DSACK
Boot ROM	$0000 0000	$0007 FFFF	D31-D24	CS0	Byte	internal
68360 internal RAM	$0008 0000	$0008 1FFF	D31-D0	---	LWRD	internal
DRAM Bank A	$0040 0000	$007F FFFF	D31-D0	CS1	LWRD	internal
SRAM	$0F00 0000	$0F13 FFFF	D31-D16	CS3	Word	internal
Flash Memory	$0100 0000	$017F FFFF	D31-D0	CS2	LWRD	internal
IP-Slot A, I/O-Select	$FC00 0000	$FC00 007F	D31-D16	CS5	Word	external
IP-Slot A, ID-Select	$FC00 0080	$FC00 00FF	D31-D16	CS5	Word	external
IP-Slot A, Memory Select	$FC80 0000	$FCFF FFFF	D31-D16	CS5	Word	external
IP-Slot B, I/O-Select	$FD00 0000	$FD00 007F	D31-D16	CS5	Word	external
IP-Slot B, ID-Select	$FD00 0080	$FD00 00FF	D31-D16	CS5	Word	external
IP-Slot B, Memory Select	$FD80 0000	$FDFF FFFF	D31-D16	CS5	Word	external
VMEbus Std.Access	$FE00 0000	$FEFF FFFF	D31-D16	CS6	Word	external
Board Control Register	$FFF0 0000	$FFF0 0001	D31-D24	CS7	Word	external
Interrupter Vector Register	$FFF0 0002	$FFF0 0003	D31-D24	CS7	Word	external
Clear R/W FIFO	$FFF0 0080	$FFF0 0081	---	CS7	Word	external
Status IRQ1 Mask	$FFF0 0080	$FFF0 0081	D31	CS7	Word	external
Status IRQ Mailbox	$FFF0 0082	$FFF0 0083	D31	CS7	Word	external
Clock R/W FIFO	$FFF0 0084	$FFF0 0085	D31	CS7	Word	external
Status IRQ7 Mask	$FFF0 0086	$FFF0 0087	D31	CS7	Word	external
Interrupt Pending	$FFF0 0088	$FFF0 0089	D31	CS7	Word	external
Enable IRQ Mailbox	$FFF0 008A	$FFF0 008B	D31	CS7	Word	external
EEPROM Data	$FFF0 008C	$FFF0 008D	D31	CS7	Word	external
EEPROM Clock	$FFF0 008E	$FFF0 008F	D31	CS7	Word	external
VMEbus Short I/O	$FFF4 0000	$FFF7 FFFF	D31-D16	CS7	Word	external
Real Time Clock	$FFF8 0000	$FFF8 07FF	D27-D24	CS7	Word	external

For compatibility reasons to IP360 Rev.1 and Rev.2 boards, the RTC, usually handled with the CS7 select line, can also be handled with the CS4 select line. In this case, the second DRAM will not be supported on Rev.3 board versions.

optional Real Time lock	$FFF8 0000	$FFF8 07FF	D27-24	CS4	Byte	internal
or DRAM Bank B	$0080 0000	$00BF FFFF	D31-D0	CS4	LWRD	internal

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The given values refer to the MicroSys factory initialization of the MC68360. Base address variations can be easily done by modifying the according CS registers of the MC68360. All subdecoded values cannot be changed by the user.

Select Line:	Start:	End:	DSACK	Purpose:
CS0 decoding range	$0000 0000	$0007 FFFF	internal	Boot ROM
CS1 decoding range	$0040 0000	$007F FFFF	internal	DRAM Bank A
CS2 decoding range	$0100 0000	$017F FFFF	internal	Flash Memory
CS3 decoding range	$0F00 0000	$0F13 FFFF	external	Shared SRAM
CS4 decoding range	$0080 0000 $FFF8 0000	$00BF FFFF $FFF8 07FF	internal internal	either DRAM Bank B or Real Time Clock
CS5 decoding range	$FC00 0000	$FDFF FFFF	external	IP-Slot A & B
CS6 decoding range	$FE00 0000	$FEFF FFFF	external	VME Std.Access
CS7 decoding range	$FFF0 0000	$FFFF FFFF	external	VME Short Access, Board Registers

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5. The MC68360 QUICC

The IP 360 is controlled by the communication processor MC68360 from Motorola. The processor is comprised of three modules. The 32 bit CPU core, the system integration block and the communications processor. The external bus is supported with the dynamic bus sizing feature for 8 and 16 bit devices. For detailed information about the QUICC, please refer to the MC68360 user's manual.

The following signals are supplied and controlled by the QUICC and must be correctly programmed to ensure proper operation of the board.

1.) Boot EPROM:
chip select via CS0 as SRAM bank
8 bit port size on data lines D24 to D31
decoding range max. 1MByte
200ns access time, i.e. 4 waitstates at 25MHz
QUICC internal DSACK generation

2.) DRAM Bank A:
RAS0 via CS1 as a DRAM bank
byte wide CAS lines via CAS0 to CAS3
QUICC internal address multiplex mode
32 bit port size on data lines D0 to D31
decoding range max. 4MByte, A31-A22
two 1Mx16 DRAMs, no parity
60ns t(RAS) access time
1024 refresh cycles within 16msec.
QUICC internal DSACK generation

3.) FLASH Memory:
chip select via CS2 as a SRAM bank
32 bit port size on data lines D0 to D31
decoding range for 2MByte, A31-A21
decoding range for 8MByte, A31-A23
100ns access time, i.e. 2 waitstates at 25MHz
QUICC internal DSACK generation

4.) SRAM Area:
chip select via CS3 as a SRAM bank
16 bit port size on data lines D16 to D31
decoding range max. 1MByte, A31-A20
100ns access time, i.e. 2 waitstates at 25MHz
QUICC internal DSACK generation
shared access via VMEbus
QUICC internal match of shared access address
set GMR to synchronous mode

5a.) Real Time Clock:
chip select via CS4 as a SRAM bank
8 bit port size on data lines D24 to D31
decoding range min. 16Byte, A31-A11
120ns access time, i.e. 2 waitstates at 25MHz
ALE input tied to high
QUICC internal DSACK generation

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5b.) DRAM Bank B:
RAS1 via CS4 as a DRAM bank
byte wide CAS lines via CAS0 to CAS3
QUICC internal address multiplex mode
32 bit port size on data lines D0 to D31
decoding range max. 4MByte, A31-A22
two 1Mx16 DRAMs, no parity
60ns t(RAS) access time
1024 refresh cycles within 16msec.
QUICC internal DSACK generation

6.) IP Modules:
chip select via CS5 as a SRAM bank
16 bit port size on data lines D16 to D31
decoding range 32MByte, A31-A25
QUICC external DSACK generation

7.) VME Std.Access:
chip select via CS6 as a SRAM bank
bit port size on data lines D16 to D31
decoding range 16MByte, A31-A24
QUICC external DSACK generation

8.) Board Control Register:
chip select via CS7 as a SRAM bank
8 bit port size on data lines D24 to D31
decoding range min.512KByte, A31-A19
QUICC internal DSACK generation
zero waitstate read/write access

9.) QUICC Module Base Address Register at $003FF00

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10.) QUICC clock support via external 25 or 32 MHz crystal oscillator

QUICC PA0 :	- RxD channel 1
QUICC PA1 :	- TxD channel 1
QUICC PA2 :	- RxD channel 2
QUICC PA3 :	- TxD channel 2
QUICC PA4 :	- RxD channel 3
QUICC PA5 :	- TxD channel 3
QUICC PA6 :	- RxD channel 4
QUICC PA7 :	- TxD channel 4
QUICC PA8 :	- TxC on the ethernet application
QUICC PA9 :	- RxC on the ethernet application
QUICC PA10 :	- TPE on the ethernet application
QUICC PA11 :	- LBE on the ethernet application
QUICC PA12 :	- APT on the ethernet application
QUICC PA13 :	- SQL on the ethernet application
QUICC PA14 :	- FDS on the ethernet application
QUICC PA15 :	- APC on the ethernet application
QUICC PB0 :	- centronics BSY line via ST2
QUICC PB1 :	- centronics DIR line via ST2
QUICC PB2 :	- ethernet JABBER control
QUICC PB3 :	- ethernet RESET control
QUICC PB4 :	- DMA request 0 input from IP-Modul A or B
QUICC PB5 :	- DMA acknowledge 0 output to IP-Modul A or B
QUICC PB6 :	- onboard RS232 serial out TxD-0
	- DMA done line 0 to or from IP-Modul A or B
QUICC PB7 :	- onboard RS232 serial in RxD-0
QUICC PB8 :	- centronics data line CD0 via ST2
QUICC PB9 :	- centronics data line CD1 via ST2
QUICC PB10 :	- onboard RS232 serial out TxD-1
	- centronics data line CD2 via ST2
QUICC PB11 :	- onboard RS232 serial in RxD-1
	- centronics data line CD3 via ST2
QUICC PB12 :	- centronics data lines CD4
QUICC PB13 :	- centronics data lines CD5
QUICC PB14 :	- centronics data lines CD6
QUICC PB15 :	- centronics data lines CD7
QUICC PB16 :	- centronics strobe line via ST2
QUICC PB17 :	- centronics acknowledge line via ST2



For detailed chip information see

Technical manual MC68360

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5.1 The Boot ROM Socket

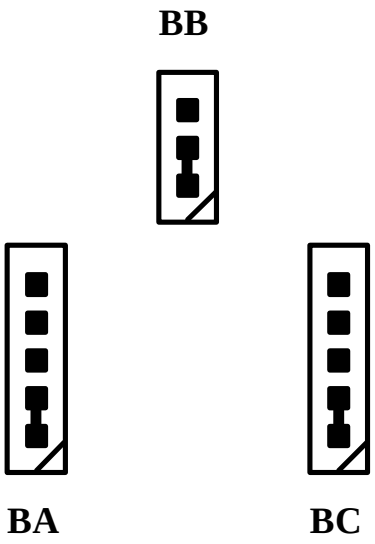
A single 32 pin socket onboard the IP360 is used to carry the firmware ROM. Any types from 512Kbit up to 8Mbit can be mounted into the socket J18. The socket pinout refers to the JEDEC standard for a 600mil, 28 pin or 32 pin, bytewise organized ROM, PROM, EPROM, EEPROM or FLASH devices. The possible Boot-ROM capacity reaches from 128KByte for the small device up to 1MByte. The device specific pinout selection can be made by the soldering links BA, BB and BC on the soldering side of the PCB according to the following table.

Type Selection for Boot-ROM Socket J11

controlled pin:		**pin:1**	**pin:30**	**pin:31**
by link:		**BA**	**BB**	**BC**
ROM:	512Kbit	---	1-2	---
	1Mbit	1-2	---	1-2
	2Mbit	1-2	2-3	1-2
	4Mbit	1-2	2-3	2-3
	8Mbit	2-3	2-3	2-3
EEPROM:	1Mbit	---	---	4-5
Flash:	1Mbit	---	---	4-5
	4Mbit	4-5	2-3	4-5

(--- = don't care)

Default soldering links setting for 512K / 1Mbit types:

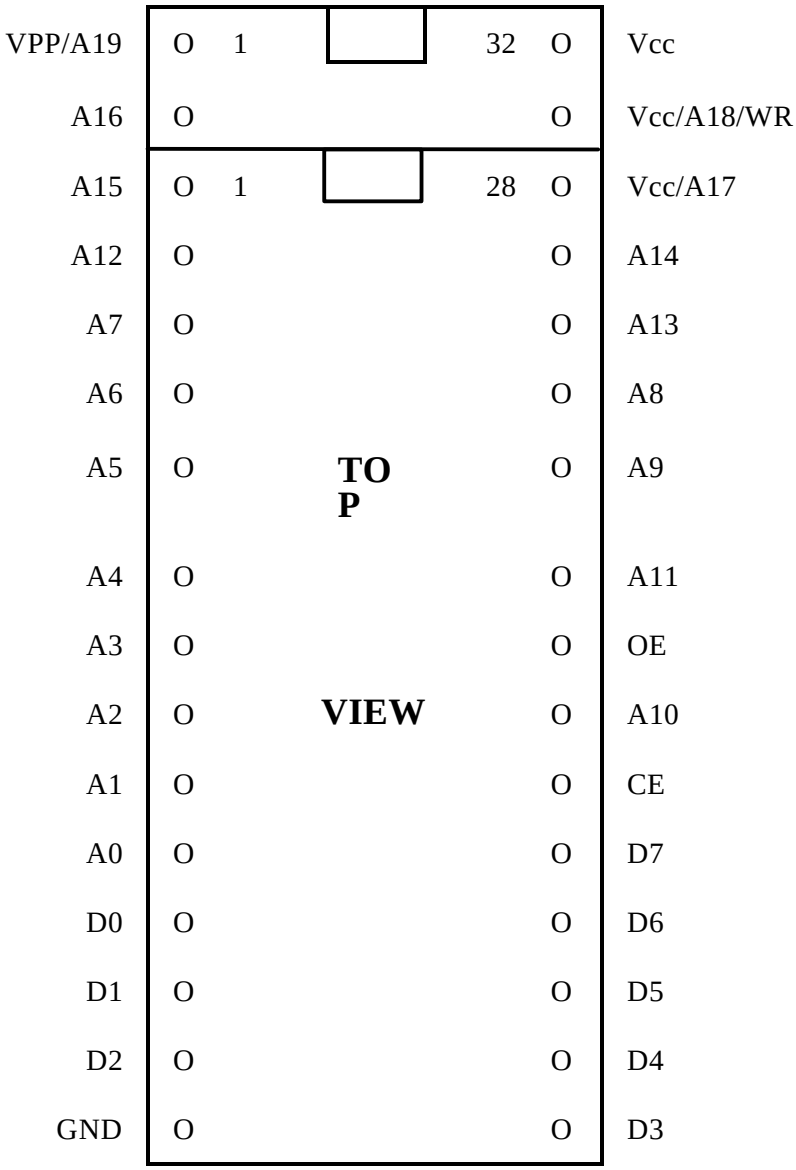


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Please check for correct pin compatibility before mounting any device. 28 pin and 32 pin packages must be inserted into socket as shown below only during power down. Any insertion of other types or not as directed may cause permanent damage to the device and/or the board.

Socket Pinout:



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The data port is 8 bits wide and no parity check is performed. The boot ROM is controlled via the CS0 select line as a SRAM bank. It cannot be shared with other VMEbus masters, because no external data multiplexers are implemented for the 16 bit wide VMEbus access. To avoid an external access, the VMEbus shared access address decoding, contained in the VME-ispLSI, and the onboard boot ROM address decoding must be configured for no possible address match.

After a power up reset, a manual reset or a hardware reset from the VMEbus, the onboard processor requests for the reset vector by driving the CS0 line active. This vector is usually located at the first 8 bytes of the device connected to this select line. During normal operation these address locations depend on the programming of the CS0 line.

Boot-ROM Addressmap:

Address:	$0	MSByte of interrupt stack pointer
	$1	MSByte-1 of interrupt stack pointer
	$2	LSByte+1 of interrupt stack pointer
	$3	LSByte of interrupt stack pointer
	$4	MSByte of program counter
	$5	MSByte-1 of program counter
	$6	LSByte+1 of program counter
	$7	LSByte of program counter
	$8	start of firmware
	|	|
	$X	end of boot rom



For detailed information about the boot ROM chip specif ication, please refer to the according device data sheet.

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5.2 The DRAM Area

The IP360 is able to carry either 4 or 8MByte of dynamic ram in one or two banks. Both banks are directly controlled by MC68360. Each ram block consists of two fast page 1Mx16 DRAM devices with the following characteristics:

KM416C1200AJ-6:	refresh:	1024cycles/16ms
	t(rac):	60ns
	t(cac):	20ns
	t(rcd):	20ns
	t(rp):	40ns
	t(cp):	10ns

The MC68360 controls the first DRAM bank via its CS1 line. The ram data port is 32 bits wide and no parity check is performed. The DRAM area cannot be shared with other VMEbus masters, because no external address multiplexers and data multiplexers are implemented. To avoid an external access, the VMEbus shared access address decoding, contained in the VME-ispLSI, and the onboard DRAM address decoding must be configured for no possible address match.

As a standard configuration the following values have been used:

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0



For detailed information about the DRAM chip specific ation, please refer to the according DRAM data sheet.

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5.3 The Flash Memory

The flash memory area of the IP360 consists of four 5 volt programmable TSOP devices. They may have either a total capacity of 2, 4 or 8MByte. The data bus is 32 bits wide to allow for a fast data transfer. There are no byte write lines leading to the four memories. Any write access will cause the write line of all four devices to be activated. The write cycle sequence is under full software/chip control and depends on the used chip types. The FLASH devices have got the
following characteristics:

AM29F040-90	
Read Cycle Time	90ns
Write Cycle Time	90ns
Write Pulse Width	45ns
Vcc Setup Time	50µs
Byte Programming Time	1ms
Chip Programming Time	25s
Sector Erase Operation	30s
Chip Erase Operation	120s

AM29F080-90	
Read Cycle Time	90ns
Write Cycle Time	90ns
Write Pulse Width	45ns
Vcc Setup Time	50µs
Byte Programming Time	1ms
Chip Programming Time	50s
Sector Erase Operation	15s
Chip Erase Operation	240s

AM29F016-90/95	
Read Cycle Time	90ns
Write Cycle Time	90ns
Write Pulse Width	45ns
Vcc Setup Time	50µs
Byte Programming Time	1ms
Chip Programming Time	100s
Sector Erase Operation	15s
Chip Erase Operation	480s

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The data port is 32 bits wide and no parity check is performed. The FLASH area is controlled via the CS2 select line as a SRAM bank. The FLASH area cannot be shared with other VME-bus masters, because no external data multiplexers are implemented for the 16 bit wide VME-bus access. To avoid an external access, the VMEbus shared access address decoding, contained in the VME-ispLSI, and the onboard FLASH address decoding must be configured for no possible address match.

As a standard configuration the following values have been used:

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0



For detailed chip information see
Technical manual of flash memory products.

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5.4 The Static RAM Area

The IP360 is equipped with two SMD SRAM devices with either 128Kx8 or 512Kx8 capacity. This allows for a total SRAM capacity of 256KByte or 1MByte at a 16 bit wide data bus. If the smaller devices are installed, the default link BD on the soldering side must be in position 1-2. The contents of the SRAM area is protected against data loss by a backup circuitry. The backup power can be either supplied from various onboard sources. Short time backup can be managed by a servicefree gold capacitor. An extended backup time can be reached by using the rechargeable NiCd battery option. For long time applications, a lithium cell can be mounted onboard the IP360. In addition, the VMEbus standby line on ST1B pin 31 can also be used to supply the necessary backup power. In any case, the backup time mainly depends on the used SRAM devices and their standby power consumption. The backup feature of the IP360 can be disabled at all by changing the setting of jumper CA to position 1-2. In position 2-3, the backup power is supplied to the SRAM area as well as to the onboard real time clock.

The implemented SRAM devices have got the following characteristics:

KM681000AL-5L	
Read Cycle Time	55ns
Write Cycle Time	55ns
Write Pulse Width	40ns

KM684000ALG-5L	
Read Cycle Time	55ns
Write Cycle Time	55ns
Write Pulse Width	40ns

The data port is 16 bits wide and no parity check is performed. The SRAM area is controlled via the CS3 select line as a SRAM bank. It can be shared with other VMEbus masters. Therefore the onboard address decoding must match partly or totally with the address decoding, configured within the VME-ispLSI for the VMEbus shared access address. The MC68360 address lines from A28 to A31 are not used and must be configured as byte write lines. The address lines from A24 to A27 are tied to a logical high level. All other address lines are driven by the external VMEbus master during a shared access. The DSACK generation for the SRAM bank is not performed external and must be set to at least two waitstates. The SYNC bit within the GMR of the QUICC should be set to synchronous mode.

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As a standard configuration the following values have been used:

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0



For detailed information about the SRAM chip specific ation, please refer to the according SRAM data sheet.

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5.5 The VMEbus Shared RAM Decoding:

The whole SRAM area can be shared with other VMEbus masters. The necessary VMEbus address decoding and the decoding size are software programmable. The access address from the VMEbus side from A18 to A24 are compared by internal registers of the VME-ispLSI. They areprogrammed in a serial mode via the data line D31 by the VMEbus address register located at an offset of $xxxx xx80 and $xxxx xx84 of the CS7 specified system buffer select area.

The programming of the VMEbus address register is performed in the following manner.

1.) set the EEPROM clock line to a low level by writing a zero to the address offset $xxxx xx8E.

2.) clear the shared access address register by any write access to the address offset $xxxx xx80.

3.) shift in two onboard interrupt mask bits via data line D31 by a two write accesses to the address offset $xxxx xx84. A logical one effects the according interrupt source to activated. The first transfer refers to the mailbox interrupt, the second to the optional ABORT key.

4.) shift in the seven interrupt mask bits via data line D31 by seven write accesses to the address offset $xxxx xx84. A logical one effects the according interrupt line to be active. The first data transferred, refers to the VMEbus interrupt level 7, the last to level 1.

5.) shift in one VMEbus interrupter mask bit via data line D31 by a single write access to the address offset $xxxx xx84. A logical one effects the programmed VMEbus interrupter level not to be masked out automatically.

6.) shift in the two address mask bits via data line D31 by four write accesses to the address offset $xxxx xx84. A logical one effects the according address line to be ignored. The first data transferred, refers to the address mask bit for the VMEbus address line A19, the second to line A18.

7.) shift in the four address compare bits via data line D31 by six write accesses to the address offset $xxxx xx84. The first data transferred refers to the address compare bit for the VMEbus address line A23, the last to line A18. The state match of all non masked compare bits and the according address lines causes a valid address decoding.

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register table at the offset $xxxx xx84, write only:

1.access:	interrupt mask bit for the onboard level 1	1 = enable
2.access:	interrupt mask bit for the onboard level 7	1 = enable
3.access:	interrupt mask bit 7 for level 7	1 = enable
4.access:	interrupt mask bit 6 for level 6	1 = enable
5.access:	interrupt mask bit 5 for level 5	1 = enable
6.access:	interrupt mask bit 4 for level 4	1 = enable
7.access:	interrupt mask bit 3 for level 3	1 = enable
8.access:	interrupt mask bit 2 for level 2	1 = enable
9.access:	interrupt mask bit 1 for level 1	1 = enable
10.access:	interrupter mask bit for auto-level-masking	0 = auto mask
11.access:	address mask bit 1 for VMEA19	1 = ignore
12.access:	address mask bit 0 for VMEA18	1 = ignore
13.access:	address compare bit 5 for VMEA23	compare state
14.access:	address compare bit 4 for VMEA22	compare state
15.access:	address compare bit 3 for VMEA21	compare state
16.access:	address compare bit 2 for VMEA20	compare state
17.access:	address compare bit 1 for VMEA19	compare state
18.access	address compare bit 0 for VMEA18	compare state

The serial transferred data can be read back in a serial mode for verification in the following manner.

1.) set the shift out register position to zero by a read access from the address offset $xxxx xx80.

2.) read out the six address compare bits via data line D31 by four read accesses from the address offset $xxxx xx84. The first data bit transferred refers to the address compare bit for the VMEbus address line A18, the last to line A23.

3.) continue to read out the two address mask bits via data line D31 by two read accesses from the address offset $xxxx xx84. The first data bit transferred refers to the address mask bit for the VMEbus address line A18, the second to line A19.

4.) you may continue to read out the VMEbus interrupter mask bit via data line D31 by a single read access from the address offset $xxxx xx84. This data bit refers to the auto-mask function of the programmable VMEbus interrupter level.

5.) you may continue to read out the seven VMEbus interrupt mask bits via data line D31 by seven read accesses from the address offset $xxxx xx84. The first data bit transferred refers to the VMEbus level 1, the last to level 7.

After 16 read accesses have been performed on the VMEbus address register, the shift register points to location zero again. A reset to zero can be performed at any time. A clear VMEbus address register command will clear the address mask register, the address compare register and the interrupt mask register. The read shift register pointer will not be affected by the this command. It should be performed only once before programming the VMEbus shared access address and the VMEbus interrupt mask.

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register table at the offset $xxxx xx84, read only:

1.access:	address compare bit 0 for VMEA18	compare state
2.access:	address compare bit 1 for VMEA19	compare state
3.access:	address compare bit 2 for VMEA20	compare state
4.access:	address compare bit 3 for VMEA21	compare state
5.access:	address compare bit 3 for VMEA22	compare state
6.access:	address compare bit 3 for VMEA23	compare state
7.access:	address mask bit 0 for VMEA18	1 = ignore
8.access:	address mask bit 1 for VMEA19	1 = ignore
9.access:	interrupter mask bit for auto-level-masking	0 = auto mask
10.access:	interrupt mask bit 1 for level 1	1 = enable
11.access:	interrupt mask bit 2 for level 2	1 = enable
12.access:	interrupt mask bit 3 for level 3	1 = enable
13.access:	interrupt mask bit 4 for level 4	1 = enable
14.access:	interrupt mask bit 5 for level 5	1 = enable
15.access:	interrupt mask bit 6 for level 6	1 = enable
16.access:	interrupt mask bit 7 for level 7	1 = enable

The remaining onboard interrupt mask bits for the onboard level 1 and 7 cannot be read out within this register.

Any shared ram access from the VMEbus side must be performed with the proper address modifier combination for a standard access. The VMEbus address decoding must always be programmed according to the onboard decoded SRAM size via the CS3 line of the MC68360, i.e. the VMEbus base address must match with the onboard programmed base address. Otherwise a partial or double decoding of the shared ram area or no shared access at all might be caused.

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6. The Real Time Clock

The IP360 is equipped with the RTC-72423, which features time and date. The RTC is protected against data loss by a backup circuitry. The backup feature supplied from various onboard sources can be disabled by jumper CA in position 1-2. Position 2-3 enables the backup feature of the IP360 for the RTC as well as for the SRAM area. A short time backup can be managed by using a servicefree gold capacitor. If an extended backup time is desired, a rechargeable NiCd battery or, for long time applications, a lithium cell can be mounted onboard the IP360. In addition, the VMEbus standby line on ST1B pin 31 can also be used to supply the necessary backup power.

The RTC-72423 can be either accessed with the CS4 select line as a SRAM bank on the data line D24 to D27 as a byte device or, if two DRAM banks are implemented onboard the IP360 via the CS7 line as a word device at the address offset location $xxx8 0000. The dynamic bus sizing feature of the MC68360 allows byte, word or longword read or write accesses according to the device size, however only 4 bits of each data byte or data word are valid.

RTC-72423 has got the following timing specifications:

Read Cycle Time	120ns
Read Recovery Time	200ns
Write Cycle Time	120ns
Write Pulse Width	120ns
Write Recovery Time	200ns



For detailed programming information and chip descri ption, please refer to RTC-72423 User's Manual !

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6.1 The RTC-72423 Address Map

Byte/Word	Register	Data Lines				Count	Remarks
Address	Name	D27	D26	D25	D24	Value	
$00/$00	S1	s8	s4	s2	s1	0 - 9	1 second digit
$01/$02	S10	--	s40	s20	s10	0 - 5	10 second digit
$02/$04	Mi1	mi8	mi4	mi2	mi1	0 - 9	1 minute digit
$03/$06	Mi1	--	mi40	mi20	mi10	0 - 5	10 minute digit
$04/$08	H1	h8	h4	h2	h1	0 - 9	1 hour digit
$05/$0A	H10	--	PM/AM	h20	h10	0 - 2	10 hour digit,
$06/$0C	D1	d8	d4	d2	d1	0 - 9	1 day digit
$07/$0E	D10	--	--	d20	d10	0 - 3	10 day digit
$08/$10	Mo1	mo8	mo4	mo2	mo1	0 - 9	1 month digit
$09/$12	Mo1	--	--	--	m10	0 - 3	10 month digit
$0A/$14	Y1	y8	y4	y2	y1	0 - 9	1 year digit
$0B/$16	Y10	y80	y40	y20	y10	0 - 3	10 year digit
$0C/$18	W	--	w4	w2	w1	0 - 6	week day digit
$0D/$1A	CD	30sec Adjust	IRQ Flag	BUSY	HOLD	----	ControlRegister D
$0E/$1C	CE	t1	t0	ITRPT /STND	MASK	----	ControlRegister E
$0F/$1E	CF	TEST	24/12	STOP	RESET	----	ControlRegister F

As a standard configuration the following values have been used:

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register:																
Dx	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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7. The serial EEPROM

The IP360 offers a 2KByte EEPROM for storing system or board parameters. The device is handled in a serial mode via a two wire interface. The clock line of the EEPROM is controlled via the state of the data line D31 at the address offset $xxxx xx8E of the CS7 specified system buffer select area. The data transfer is performed by read or write accesses via data line D31 at the
address offset $xxxx xx8C of CS7. The EEPROM data or clock line is set to a low level by writing a zero to the according access address. A read access of both, the data and the clock line, will reflect their current state. After power up or a manual reset, the data line is set to a high state while the clock line is forced to a low state. The clock line of the EEPROM is shared with the shift signal of the VMEbus address register. Therefore, this clock line must be set to a low state, prior to any data transfer to the VMEbus address shift register located at the address offset $xxxx xx84 of the CS7 select line. The necessary EEPROM access cycle timing is not controlled by hardware and must be handled by software according to the specifications contained in the X24C16 data sheet. The EEPROM responds as a word device with external DSACK generation.



For detailed programming information and chip descri ption, please refer to Data Sheet XICOR X24C16 !

8. The Board Reset Function

During power up or power down sequences, the MAX-691A activates the board reset line and holds the IP360 in a defined state. The reset line will be low for at least 200ms if the supply voltage reaches 4.65 volts. Below that voltage, the reset line will be continuously low. If the board reset key is pressed, an additional circuit will be used for switch debounce and reset time generation. The key reset time is configured for approximately 1.3sec.

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9. The Backup Feature

The backup feature of the IP360 is used to protect the **RTC** as well as the **SRAM** area. Both devices are connected to the MAX-691A, which controls the backup supply and the power up and down sequences to avoid unintended write pulses. The backup power can be supplied by different onboard sources. The RTC as well as the SRAM area can be disconnected from the backup power by the jumper CA in position 1-2. This link does also disconnect any external power, supplied via the 5 volt standby line of the VMEbus.

There are three different onboard backup options available, however only one can be installed at a time.

The **gold capacitor** option allows for a service free short time backup without any battery or other time or temperature degrading parts. If the backup time should be extended from hours to several days, a rechargeable **NiCd** battery can be installed. This solution guarantees a backup time up to a month, but it is not suitable for harsh environmental temperature conditions. An extended temperature and long time application can be arranged by using a **lithium cell**, which has got about a 10 times higher capacity than a package equivalent NiCd type.

A maximum time backup can be arranged, if the backup power is supplied via the VMEbus standby line on connector ST1A, pin 31. The external supply voltage should not exceed 5,25 volts and not fall below 2.5 volts to ensure correct data retention.

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10. Front Panel Description

10.1 Front Panel Layout

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10.2 Front Panel Leds

Led1: WATCHDOG

This led is activated, if D28 within the board control register at the address offset location $xxxx xx00 of CS7 is set to low. The contents of the BCR is not defined after power up and may have any state.

Led2: POWER

This led is activated, if the IP360 board is supplied with power. If the reset key is pressed the power indicator led will be switched off.

Led3: HALT

This led indicates that the MC68360 is in the halted state.

10.3 Front Panel Switches

Pushbutton: RESET:

The reset key performs a hardware reset for the whole board, and if the board is the system controller, for the whole VMEbus system. The contents of the cpu registers is not affected by this reset, but the supervisor stack pointer is loaded with the contents of address location $00000000 and the program counter with the contents of location $00000004. All onboard devices and logic are reset to allow for a defined program start.

10.4 Front Panel Connectors

The IPA03 front end of the IP360 is fitted out with four RJ45 connectors marked with 1:SCC1, 2:SMC1, 3:SMC2 and 4:SCC3. Location 2 and 3 contain the two onboard SMC communication channels of the MC68360. The connectors 1 and 4 require the use of the IE363 I/O-Piggyback. Thereon, the MC68360 SCC1 and SCC3 channels are conditioned for any desired EIA standard and linked to these two RJ45 connectors. Because of pinout differences between the EIA standards, the jumper links YA, YB, YC and YD must be set according to the following tables.

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Pin assignment of the RJ45 connector, marking 1:SCC1

Pin:	RS232 Type:	RS422 Type:	RS485 Type	Twisted Pair:
1		RST+	CLK+	TxD+
2	RTS	RTS-	CLK-	TxD-
3	GND	GND	GND	RxD+
4	TxD	TxD-	TxD-	
5	RxD	RxD-	I/O-	
6	DCD	RxD+	I/O+	RxD-
7	CTS			
8		TxD+	TxD+	
link YA	1-2, 5-6, 7-8, 9-10	1-2, 4-5, 7-8, 9-10	1-2, 4-5, 7-8, 9-10	2-3, 6-7, 8-9
link YB	1-2, 3-4	1-2, 3-4	1-2, 3-4	2-3

Pin assignment of the RJ45 connector, marking 4:SCC3

Pin:	RS232 Type:	RS422 Type:	RS485 Type
1		RST+	CLK+
2	RTS	RTS-	CLK-
3	GND	GND	GND
4	TxD	TxD-	TxD-
5	RxD	RxD-	I/O-
6	DCD	RxD+	I/O+
7	CTS		
8		TxD+	TxD+
link YC	2-3	1-2	1-2

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Pin assignment of the RJ45 connector, marking 2:SMC1

Pin:	RS232 Type:
1	
2	
3	GND
4	TxD
5	RxD
6	
7	
8	

Pin assignment of the RJ45 connector, marking 3:SMC2

Pin:	RS232 Type:
1	
2	
3	GND
4	TxD
5	RxD
6	
7	
8	

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Pin assignment of the molex connector ST15:

Pin:	Signal:	Description:	
1	RSTK*	low active reset key input	180R pull-up resistor
2	LED	anode of user led output	180R pull-up resistor
3	GND	ground	
4	not connected		
5	HLT*	anode of HALT led output	180R pull-up resistor
6	ABO*	low active abort key input	10K pull-up resistor

In case, external leds or switches are added to the IP360 board, the following restrictions must be observed to guarantee proper operation:

- All leds must be connected to ground
- All switches must be connected to ground
- The abort key input requires a debounced low active switch
- The reset key input can be simply realized as a closing switch
- Do not source external voltages above Vcc or below GND

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11. Interrupt Structure

11.1 The Interrupt Handler

The IP360 offers a bit maskable 7 level VMEbus and a 7 level onboard interrupt handler, however only 4 levels are used onboard. The 7 VMEbus interrupt levels work in vector controlled mode only. Onboard interrupt sources on the same level as VMEbus interrupt sources are processed with higher priority.

11.2 The VMEbus Interrupt Handler

Each VMEbus interrupt level can be enabled or disabled by software via the interrupt mask shift register, which is a part of the VMEbus address register. After a hardware reset all bits of this shift register are set to zero and all VMEbus interrupt levels are disabled. **To enable** a VMEbus interrupt level the according bit must be **set to high**. These enable bits are programmed in a serial mode via the data line D31 by the VMEbus address register located at an offset of $xxxx xx80 of the CS7 specified system buffer select area. The programming of this register is performed in the following manner.

1.) set the EEPROM clock line to a low level by writing a zero to the address offset $xxxx xx8E.

2.) clear the shared access address register by any write access to the address offset $xxxx xx80.

3.) shift in two onboard interrupt mask bits via data line D31 by a two write accesses to the address offset $xxxx xx84. A logical one effects the according interrupt source to activated. The first transfer refers to the mailbox interrupt, the second to the optional ABORT key.

4.) shift in the seven interrupt mask bits via data line D31 by seven write accesses to the address offset $xxxx xx84. A logical one effects the according interrupt line to be active. The first data transferred, refers to the VMEbus interrupt level 7, the last to level 1.

5.) shift in one VMEbus interrupter mask bit via data line D31 by a single write access to the address offset $xxxx xx84. A logical one effects the programmed VMEbus interrupter level not to be masked out automatically.

6.) shift in the two address mask bits via data line D31 by four write accesses to the address offset $xxxx xx84. A logical one effects the according address line to be ignored. The first data transferred, refers to the address mask bit for the VMEbus address line A19, the second to line A18.

7.) shift in the four address compare bits via data line D31 by six write accesses to the address offset $xxxx xx84. The first data transferred refers to the address compare bit for the VMEbus address line A23, the last to line A18. The state match of all non masked compare bits and the according address lines causes a valid address decoding.

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register table at the offset $xxxx xx84, write only:

1.access:	interrupt mask bit for the onboard level 1	1 = enable
2.access:	interrupt mask bit for the onboard level 7	1 = enable
3.access:	interrupt mask bit 7 for level 7	1 = enable
4.access:	interrupt mask bit 6 for level 6	1 = enable
5.access:	interrupt mask bit 5 for level 5	1 = enable
6.access:	interrupt mask bit 4 for level 4	1 = enable
7.access:	interrupt mask bit 3 for level 3	1 = enable
8.access:	interrupt mask bit 2 for level 2	1 = enable
9.access:	interrupt mask bit 1 for level 1	1 = enable
10.access:	interrupter mask bit for auto-level-masking	1 = auto mask
11.access:	address mask bit 1 for VMEA19	1 = ignore
12.access:	address mask bit 0 for VMEA18	1 = ignore
13.access:	address compare bit 5 for VMEA23	compare state
14.access:	address compare bit 4 for VMEA22	compare state
15.access:	address compare bit 3 for VMEA21	compare state
16.access:	address compare bit 2 for VMEA20	compare state
17.access:	address compare bit 1 for VMEA19	compare state
18.access	address compare bit 0 for VMEA18	compare state

The serial transferred data can be read back in a serial mode for verification in the following manner.

1.) set the shift out register position to zero by a read access from the address offset $xxxx xx80.

2.) read out the six address compare bits via data line D31 by four read accesses from the address offset $xxxx xx84. The first data bit transferred refers to the address compare bit for the VMEbus address line A18, the last to line A23.

3.) continue to read out the two address mask bits via data line D31 by two read accesses from the address offset $xxxx xx84. The first data bit transferred refers to the address mask bit for the VMEbus address line A18, the second to line A19.

4.) continue to read out the VMEbus interrupter mask bit via data line D31 by a single read access from the address offset $xxxx xx84. This data bit refers to the auto-mask function of the programmable VMEbus interrupter level.

5.) continue to read out the seven VMEbus interrupt mask bits via data line D31 by seven read accesses from the address offset $xxxx xx84. The first data bit transferred refers to the VMEbus level 1, the last to level 7.

After 16 read accesses have been performed on the VMEbus address register, the shift register points to location zero again. A reset to zero can be performed at any time. A clear VMEbus address register command will clear the address mask register, the address compare register and the interrupt mask register. The read shift register pointer will not be affected by the this command. It should be performed only once before programming the VMEbus shared access address and the VMEbus interrupt mask.

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register table at the offset $xxxx xx84, read only:

1.access:	address compare bit 0 for VMEA18	compare state
2.access:	address compare bit 1 for VMEA19	compare state
3.access:	address compare bit 2 for VMEA20	compare state
4.access:	address compare bit 3 for VMEA21	compare state
5.access:	address compare bit 3 for VMEA22	compare state
6.access:	address compare bit 3 for VMEA23	compare state
7.access:	address mask bit 0 for VMEA18	1 = ignore
8.access:	address mask bit 1 for VMEA19	1 = ignore
9.access:	interrupter mask bit for auto-level-masking	1 = auto mask
10.access:	interrupt mask bit 1 for level 1	1 = enable
11.access:	interrupt mask bit 2 for level 2	1 = enable
12.access:	interrupt mask bit 3 for level 3	1 = enable
13.access:	interrupt mask bit 4 for level 4	1 = enable
14.access:	interrupt mask bit 5 for level 5	1 = enable
15.access:	interrupt mask bit 6 for level 6	1 = enable
16.access:	interrupt mask bit 7 for level 7	1 = enable

The remaining onboard interrupt mask bits for the onboard level 1 and 7 cannot be read out within this register.

11.3 The Onboard Interrupt Handler

There are four sources onboard the IP360 for causing interrupts on four different levels. The remaining 3 levels are not used. All onboard interrupt sources are handled in vector or autovector mode. The following table shows the onboard interrupt structure of the IP360.

Level:	Source:	enable:	active:	Mode:
1:	VME-Mailbox	IEMB	high	autovector
2:	IP-Modul low	IP-specific	low	vector
3:	IP-Modul high	IP-specific	low	vector
4:	not used	---	---	---
5:	not used	---	---	---
6:	not used	---	---	---
7:	ABORT-Key	IMRG8	low	autovector

This level distribution can be modified on request according to the user demand within the VME-isPLSI.

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11.4 The VMEbus Interrupter

The IP360 supports an interrupt generation on all 7 VMEbus interrupt levels. The desired level and vector can be programmed within the BCR at offset $xxxx xx00 of the CS7 select line according to the following table. The BCR responds as a word device and it can be read back for verification. The interrupt sequence is started by a state change from high to low of the STVI signal within the BCR. Only if the STVI line is set to low the current state of the interrupt sequence can be checked on data line D31 at the offset $xxx xx80 of the CS7 select line. If this bit is read low, the VMEbus interrupt is still pending and it has not been acknowledged by a VMEbus interrupt handler. The pending bit is forced immediately to low if the STVI line is released to a high state. A new interrupt sequence can only be started by a new transition of the STVI line from high to low. A contiguous low level of the STVI line will not cause several interrupts to be emitted. If level 0 is selected within the BCR, the complete sequence can be processed without any active VMEbus interrupt. This might be of advantage for selftest purposes or to initialize the pending bit to a desired state.

Bit map of the (B)oard (C)ontrol (R)egister:

CS7+$00	D31	D30	D29	D28	D27	D26	D25	D24
read/write	STRBA	STRBB	DMAB	LED	STVI	IL3	IL2	IL1

Bit map of the VMEbus interrupter level:

BCR	**D26**	**D25**	**D24**
disable:	0	0	0
Level 1:	0	0	1
Level 2:	0	1	0
Level 3:	0	1	1
Level 4:	1	0	0
Level 5:	1	0	1
Level 6:	1	1	0
Level 7:	1	1	1

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12. The Board Control Register

The (B)oard (C)ontrol (R)egister of the IP360 consists of an 8 bit wide read/write register for board maintenance. It responds as a word device at the address offset $xxxx xx00 of the CS7 select line. Write operations to the BCR should only be made on aligned word boundaries. Read accesses are allowed with any size on any address boundary.

Bit map of the (B)oard (C)ontrol (R)egister:

CS7+$00	D31	D30	D29	D28	D27	D26	D25	D24
read/write	STRBA	STRBB	DMAB	LED	STVI	IL3	IL2	IL1

Signal	Description	Function
STRBA	IP Module A Strobe Line	IP specific
STRBB	IP Module B Strobe Line	IP specific
DMAB	IP DMA Channel Select	low = IP-A / high = IP-B
LED	Front Panel User Led	low = active
STVI	Start VMEbus Interrupter	transition high/low
IL3	VMEbus-Interrupter-Level bit 3	MSB
IL2	VMEbus-Interrupter-Level bit 2	|
IL1	VMEbus-Interrupter-Level bit 1	LSB

The contents of the BCR is not defined after a power up reset and may have any state !

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13. The VMEbus Mailbox Feature

The IP360 offers a 1KByte range located on top of the onboard shared SRAM area as VMEbus communication block. This area might be used for purposes, like process communication and synchronization in multiprocessor applications. Therefore, the individual interrupt generation on each VMEbus board without using the limited VMEbus interrupt lines is a basic feature for an effective system structure. The VMEbus mailbox feature is able to generate an **autovector** controlled interrupt on **level 1** if the according enable bit is set and a write occurs from the VMEbus side within the last 1KByte of the shared SRAM area.

The interrupt enable bit for the mailbox is controlled via data bit D31 at the address offset $xxxx xx8A of the CS7 select line. After a hardware reset, the enable bit is set to zero and the mailbox interrupt is disabled. The state of this interrupt enable bit can be read back for verification. The actual state of the mailbox interrupt line is reflected on data D31 at the address offset $xxxx xx82 of the CS7 select line. A logical high indicates an active mailbox interrupt.

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14. The IndustryPack Option

The IP360 offers two (I)ndustry(P)ack module slots according to the Green Spring Logic Interface Specification Revision 0.7.1 for IP modules. The front end of the IP module slots is connected to two 50 pin DIN 41651 connectors. The IP360 supports all kind of single or double IP modules with an 8 or 16 bit wide data bus and a module clock rate of 8 MHz. IO- and Memory-Cycles are supported with or without DMA mode. All interrupt sources of each module slot are processed by an interrupter with a round robin scheduler. The strobe function of each slot can be controlled by the BCR. The error report line of both slots cannot be handled and are tied to high. All slot lines, which are not used or work as input to the IP360, are tied to a high level by 10K pull-up resistor networks. The module using the connectors ST3, ST5 and ST7 will have the extension A in the following description. The IP module with the extension 'B' uses the connectors ST4, ST6 and ST8. The DSUB connectors ST5 and ST6, which contain the I/O interface signals are located on an IPAxx adapter board, which allows for different I/O connection facilities. The Rev.6 standard IPA03 board connects 66 out of the 100 module lines to a 30 pin and a 36 pin stack connector, which are used by the AL001 extension board. Additionally, the IPA03 offers a reset switch, three leds and four RJ45 connectors. These RJ45 connectors contain the signal conditioned SCC1, the SCC3, the SMC1 and the SMC2 port lines of the MC68360. The signal conditioning is performed on a communication piggyback board out of the IE36x series.

The component mounting height underneath IP module area is realized below 3mm (0.11inch) to allow for a good air flow between the carrier board and the I-Packs.

Each slot is supplied with ID-, I/O- and memory select lines, controlled by the CS5 select line of the MC68360 as a SRAM bank with external DSACK generation according to following table.

Address map of IP-Module-A:

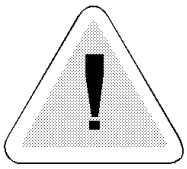
Select Line	Startaddress	Endaddress	Data Lines	Address Lines	Function
I/O	$00000000	$0000007F	D0-D15	A1-A6	read/write
ID	$00000080	$000000FF	D0-D7	A1-A5	read only
Memory	$00800000	$00FFFFFF	D0-D15	A1-A22	read/write

Address map of IP-Module-B:

Select Line	Startaddress	Endaddress	Data Lines	Address Lines	Function
I/O	$01000000	$0100007F	D0-D15	A1-A6	read/write
ID	$01000080	$010000FF	D0-D7	A1-A5	read only
Memory	$01800000	$01FFFFFF	D0-D15	A1-A22	read/write

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Attention!

The given address areas represent offset ranges,
which must be added to the CS5 specified base address !

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The MC68360 internal decoding must be programmed within the CS5 select registers according to the following addressing limitations:

- The address lines A31 to A25 must be programmed as base address
- IP-Module A is selected, if the address line A24 is decoded low.
- IP-Module B is selected, if the address line A24 is decoded high.
- Both Memory-Select ranges decode the address line A23 always as high.
- Both I/O- & ID-Select ranges decode the address line A23 always as low.
- Both I/O-Select ranges decode the address line A7 always as low.
- Both ID-Select ranges decode the address line A7 always as high.

All signals concerning the DMA controlled cycles are supported by the one IDMA channel of the MC68360. Depending on the state of the 'DMAB' bit of the BCR, IP-Slot A or IP-Slot B can be supported with the DMA feature. If the DMAB bit on data line D29 of the BCR is set to zero, IP-Slot A is able to initiate a DMA transfer on its DRQA0* line, otherwise IP-Slot B is supported by this function. The MC68360 IDMA channel 0 on the its port pins P4 to P6 handles incoming requests from the DRQA0* or DRQB0* lines. The DRQA1* and DRQB1* lines are not used. The DREQ lines are always inputs, the DACK lines are always outputs to the MC68360. The DONE lines work bi-directional between the to IP-Slots and the MC68360.

The reserved pins of slot A and slot B are connected to pull-up resistors. The strobe lines of slot A and slot B, STRA and STRB, can be controlled via the BCR, accessible by the CS7 select line. The value of the data line D31 will cause the state of the STRBA line, data line D30, that of the STRBB line. The state of the slot A & B error lines, PERRA* & PERRB*, cannot be detected. For more information about the BCR, please refer to the description of the (B)oard (C)ontrol (R)egister.

Bit map of the (B)oard (C)ontrol (R)egister:

CS7+$00	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**
read/write	STRBA	STRBB	DMAB	LED	STVI	IL3	IL2	IL1

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14.1 IP Slot Specific Parameters:

The data lanes of the IP slots are handled via both data strobes according to following table:

IP data lanes	IP data strobe	IP A1	CPU A1	CPU A0	CPU Address	CPU data lanes
D8-D15	LDS	0	0	0	$0	D24-D31
D0-D7	UDS	0	0	1	$1	D16-D23
D8-D15	LDS	1	1	0	$2	D24-D31
D0-D7	UDS	1	1	1	$3	D16-D23

As a standard access timing for the any cycle type, the 2 clock sequence is implemented within the on board IPC ispLSI. The slow 3 clock sequence, which might be necessary for some older modules is available on request for one or both IP slots.

The 3 clock access timing:

1.)	clock speed:	8MHz / 125ns	
2.)	select phase:	activated signals:	select line
			address lines A1-A22
			byte select lines
			read/write line
			data on write cycles
3.)	hold phase:	deactivated signals:	address lines A7-A22
		check and wait for:	acknowledge line active
4.)	terminate phase:	deactivated signals:	select line
			address lines A1 - A6
			byte select lines
			read/write line
			data on write cycles

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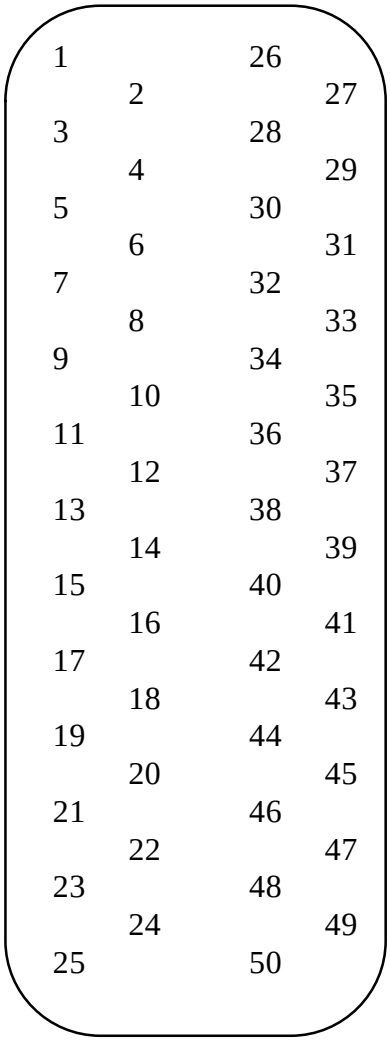
The 2 clock access timing:

1.)	clock speed:	8MHz / 125ns	
2.)	select phase:	activated signals:	select line
			address lines A1-A22
			byte select lines
			read/write line
			data on write cycles
3.)	terminate phase:	deactivated signals:	select line
			address lines A7-A22
		check and wait for:	acknowledge line active
		then deactivate	address lines A1 - A6
			byte select lines
			read/write line
			data on write cycles

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14.2 Pin assignment of logical interface ST12 and ST13



DSUB Connector Pin:	Signal Name:		
1	Ground	26	Ground
2	Clock	27	+5V/1A
3	Reset	28	R/W*
4	D0	29	ID-Select*
5	D1	30	DMA-Request0*
6	D2	31	Memory-Select*
7	D3	32	(DMA-Request1*)
8	D4	33	Int.-Select*
9	D5	34	DMA-Acknowledge*
10	D6	35	I/O-Select*
11	D7	36	(reserved 0)
12	D8	37	A1
13	D9	38	DMA-End*
14	D10	39	A2
15	D11	40	(Error*)
16	D12	41	A3
17	D13	42	IRQ0*
18	D14	43	A4
19	D15	44	IRQ1*
20	LDS*	45	A5
21	UDS*	46	Strobe
22	-12V	47	A6
23	+12V	48	Acknowledge*
24	+5V/1A	49	(reserved 1)
25	Ground	50	Ground

Signals within brackets are not used and tied to high!
An '*' indicates a low active signal.

The layout of the pin numbers within this table corresponds with the physical placement of the pins on the 50 pin IP connectors.

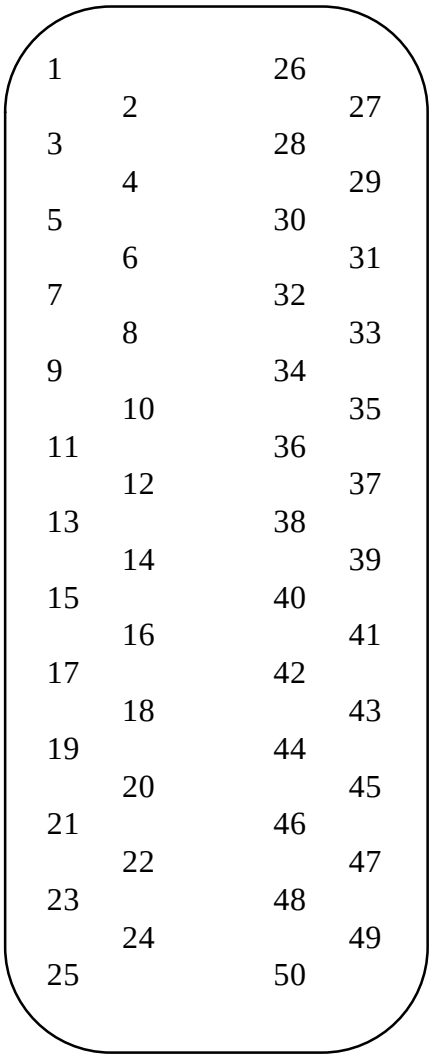
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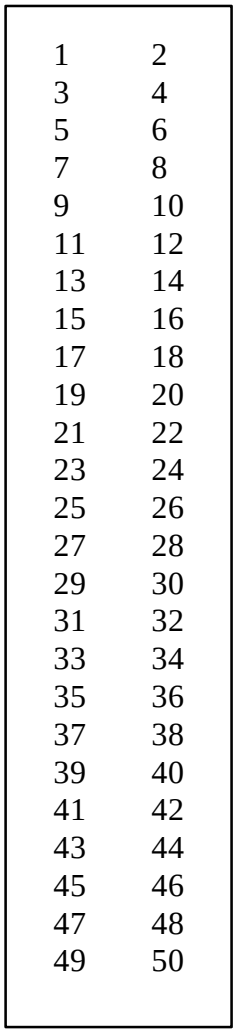
14.3 Pin assignment of I/O connectors ST5/ST7 to ST6/ST8

The 50 pin DSUB I/O connectors ST5 and ST6 of both modules are connected one to one to the 50 DIN 41651 connectors ST7 and ST8, i.e. DSUB pin 1 connects wrap connector pin 1 and DSUB pin 50 connects wrap connector pin 50.

Physical Layout of DSUB Connector ST5/ST6



Physical Layout of Flatcable connector ST7/ST8



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14.4 The I/O-Extension Connector

The IP360 offers a 50 pin DSUB connector for I/O-Extension purposes. The connector contains all necessary signals to support external I/O interface modules, like RS232, RS422, RS485 or an Ethernet serial interface adapter. The IE36x extension module series uses the upper IPack slot A and offers the user a variety of different I/O standards. The lower IPack slot B is not affected by the use of an I/O-Extension module.

Physical Layout of DSUB Connector ST2		**CPU Signal Description**	
1	26	GND	GND
2	27	Vcc	Vcc
3	28	RxD1	RxD3
4	29	TxD1	TxD3
5	30	CTS1*	CTS3*
6	31	RTS1*	RTS3*
7	32	DCD1*	DCD3*
8	33	RxD2	RxD4
9	34	TxD2	TxD4
10	35	CTS2*	CTS4*
11	36	RTS2*	RTS4*
12	37	DCD2*	DCD4*
13	38	PB0	PA8
14	39	PB1	PA9
15	40	PB2	PA10
16	41	PB3	PA11
17	42	PB12	PA12
18	43	PB13	PA13
19	44	PB14	PA14
20	45	PB15	PA15
21	46	PB16	CD3
22	47	PB17	SMTXD
23	48	-12V	DACK1*
24	49	+12V	DREQ1*
25	50	GND	GND

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15. The VMEbus Interface

The bus interface of the IP360 is designed according to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The VMEbus connector ST1 rows A, B and C contain all standard VMEbus lines, necessary for A16/A24, D8/D16 master/slave boards. All unused daisy chain lines are linked through, i.e. no external bypass links are necessary. The address modifier signals AM0 to AM5 are a part of the VMEbus specifications and serve to differentiate between certain memory areas. All address modifier lines are necessary for the shared access decoding logic. The IP360 accepts only slave data accesses within the VMEbus standard access area.

The following AM-Codes are accepted by the IP360:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)

L = logical low H = logical high

The following AM-Codes are generated by the IP360:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	H	L	Standard Supervisory Prog.	(3E)
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	H	L	Standard User Prog.	(3A)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low H = logical high

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15.1 Pin Assignment of the VMEbus Connector ST1

Pin	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	UDS*	BR0*	SYSRESET*
13	LDS*	BR1*	LWORD*
14	RW*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	not connected	A17
22	IACKOUT*	not connected	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	5VSTB	+12V
32	+5V	+5V	+5V

(signals enclosed in brackets are not used and left open)

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16. The VMEbus Requester

The IP360 contains a single level 2:1 pass requester with (**R)**elease (**W)**hen (**D)**one or a four level (**R)**elease (**O)**n (**R)**equest mode. The RWD requester releases the VMEbus mastership after the completion of each bus cycle and it has to request for it for every following VMEbus cycle. The ROR method releases the VMEbus only, if the current VMEbus cycle have been completed and any other device in the VMEbus system requests for the busmastership. If there are no other requests, the ROR requester remains being busmaster even if it does not access the VMEbus.

The **RWD** method is enabled if jumper EC 1-2 is installed.

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17. The VMEbus Arbiter

The IP360 is equipped with a single level VMEbus on request level 3. This allows the board to work as VMEbus controller as well as a bus slave in any combination.

The VMEbus arbiter function can be enabled, if jumper EB is installed. This link enables also all other system controller functions according to following table.

VMEbus Signal	Slot 1 Function	Driver Type	not Slot 1 Function
System Clock	Output	Totem Pole	Tristate
System Reset	Input/Output	Open Drain	Input
Bus Grant In 3	Input/Output	Totem Pole	Input

Please make sure, that only **one** system controller is enabled within a VMEbus system at a time, usually located in the leftmost slot. The use of more that one system controller will lead to improper operation and may cause permanent damage.

17.1 Preparations for VMEbus Multiprocessing

In case a VMEbus system should be configured for more than one VMEbus master, the user must verify, that only **one** system controller is enabled in the whole system. The system controller is usually located in the leftmost slot and drives the bus grant in lines of slot 1. It supplies the system with the system clock, the system reset, and optionally the bus error and the bus clear information. All these lines, with the exception of the system reset and the bus error signal, are totem pole outputs and **must** be controlled **only** by the system controller within the VMEbus system. The system reset and the bus error lines are driven by open collector circuits and might be driven by more than one board.

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17.2 The Boundary Scan Port

The JTAG port of the IP360 is accessible via the 6 pin molex connector AA. The boundary scan feature is only supported by the onboard MC68360 processor. There are not other boundary scan devices onboard the IP360.

The pin assignment of the JTAG port is shown in the following table:

Pin:	Signal:	Description:
1	TCK	Clock Input
2	GND	Ground
3	TRST*	Reset Input
4	TDI	Data Input
5	TDO	Data Output
6	TMS	Mode Select Input

17.3 The Background Debug Port

The MC68360 offers a microcode implemented background debugger, which is accessible via the 15 pin molex connector EA. Besides the BDM signals, this connector also contains the isPLSI programming interface for the onboard logic devices.

No connection **MUST** be made by the user to these programming signals. Otherwise a non user recoverable malfunction or permanent damage might be caused. The programming port can only be used together with a special isPLSI programming interface.

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Pin assignment of the BDM & isPLSI programming port EA:

Pin:	Signal:	Description:
1	IPIPE0*	BDM serial data output
2	Vcc	5V
3	IFETCH*	BDM serial data input
4	KRST*	O.C. reset input/output
5	FREEZE	BDM mode indicator
6	GND	ground
7	BKPT*	BDM serial clock
8	GND	ground
9	BERR*	CPU bus error line
10	DS*	CPU data stobe line
11	PLENP*	ispLSI program enable
12	ABO*	ispLSI data output
13	ARBE*	ispLSI data input
14	A18	ispLSI mode input
15	RMC*	ispLSI clock input

input:	defines an input to the IP360 board
output:	defines an output from the IP360 board

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18. Summary of Jumper & Switches

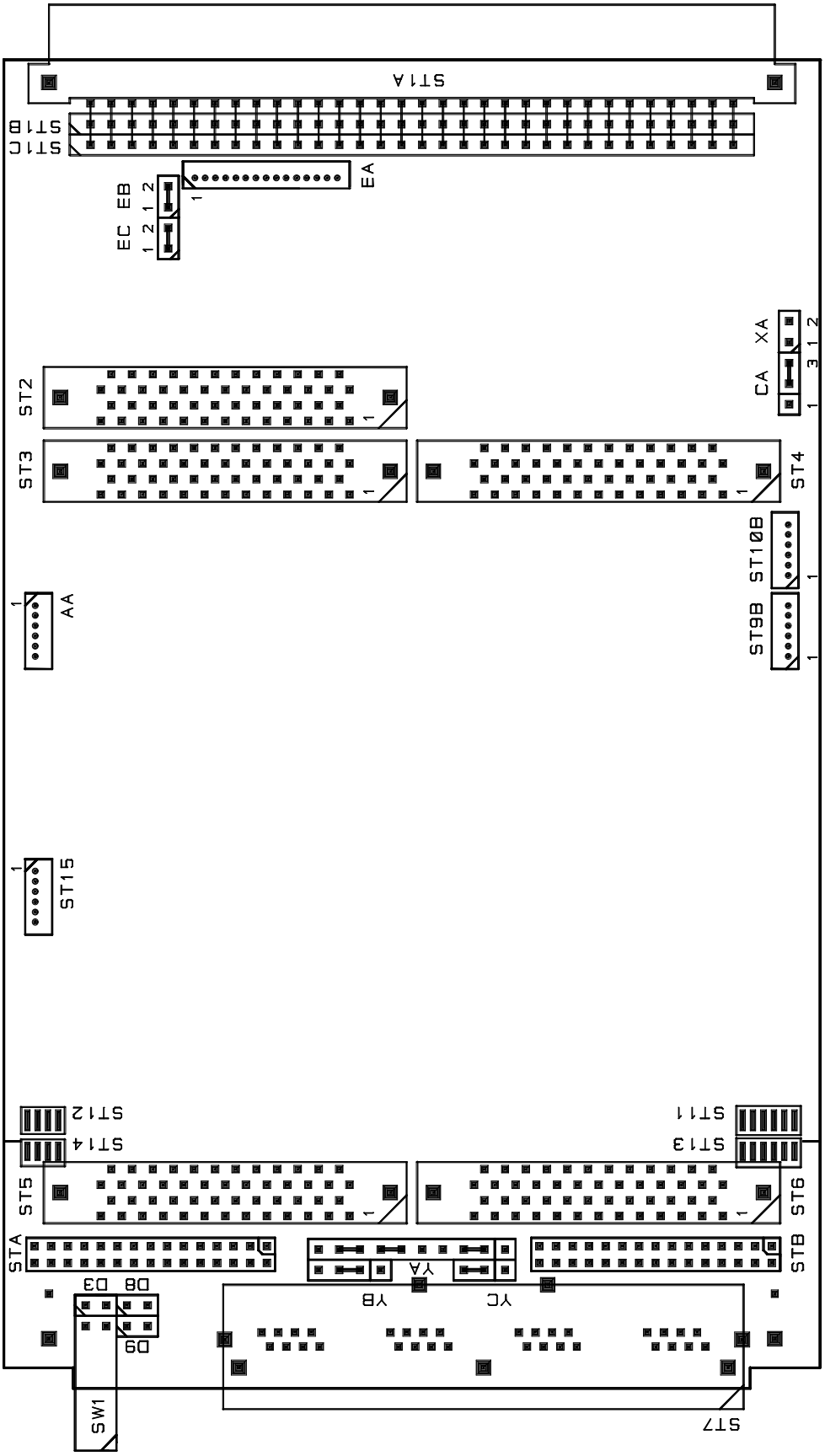
Described function is valid, when jumper is set or link is int act !

Size:	Name:	Default	Position:	Function:
1x3	AB	#	1-2	SMRXD connected to RS232
			2-3	SMRXD connected to Centronics
1x4	AC	#	1-2	PB7 connected to RS232
		#	3-4	fixed factory made connection
			2-3	do not use !
1x5	BA	#	1-2	ROM Pin 1 on Vcc
			2-3	ROM Pin 1 on A19
			4-5	ROM Pin 1 on A18
1x3	BB		1-2	ROM Pin 30 on Vcc
		#	2-3	ROM Pin 30 on A17
1x5	BC	#	1-2	ROM Pin 31 on Vcc
			2-3	ROM Pin 31 on A18
			4-5	ROM Pin 31 on RW
1x3	BD		1-2	SRAM Pin 30 on Vcc
			2-3	SRAM Pin 30 on A18
1x3	CA		1-2	Batterybackup disable
		#	2-3	Batterybackup enable
1x2	CB		1-2	MAX691A OSC IN on GND
		#	---	MAX691A OSC IN open
1x2	CC		1-2	MAX691A OSC SEL on GND
		#	---	MAX691A OSC SEL open
1x2	EB	#	1-2	System Controller Function Enable
			---	System Controller Function Disable
1x2	EC	#	1-2	Release When Done Enable
			---	Release On Request
1x2	XA		1-2	IPC ispLSI Reset activ
		#	---	IPC ispLSI Reset inactiv
1x3	XC		1-2	Board Clock Source = CLKO1
		#	2-3	Board Clock Source = OSC2
1x2	XD	#	1-2	MODCK1 = low
			---	MODCK1 = high

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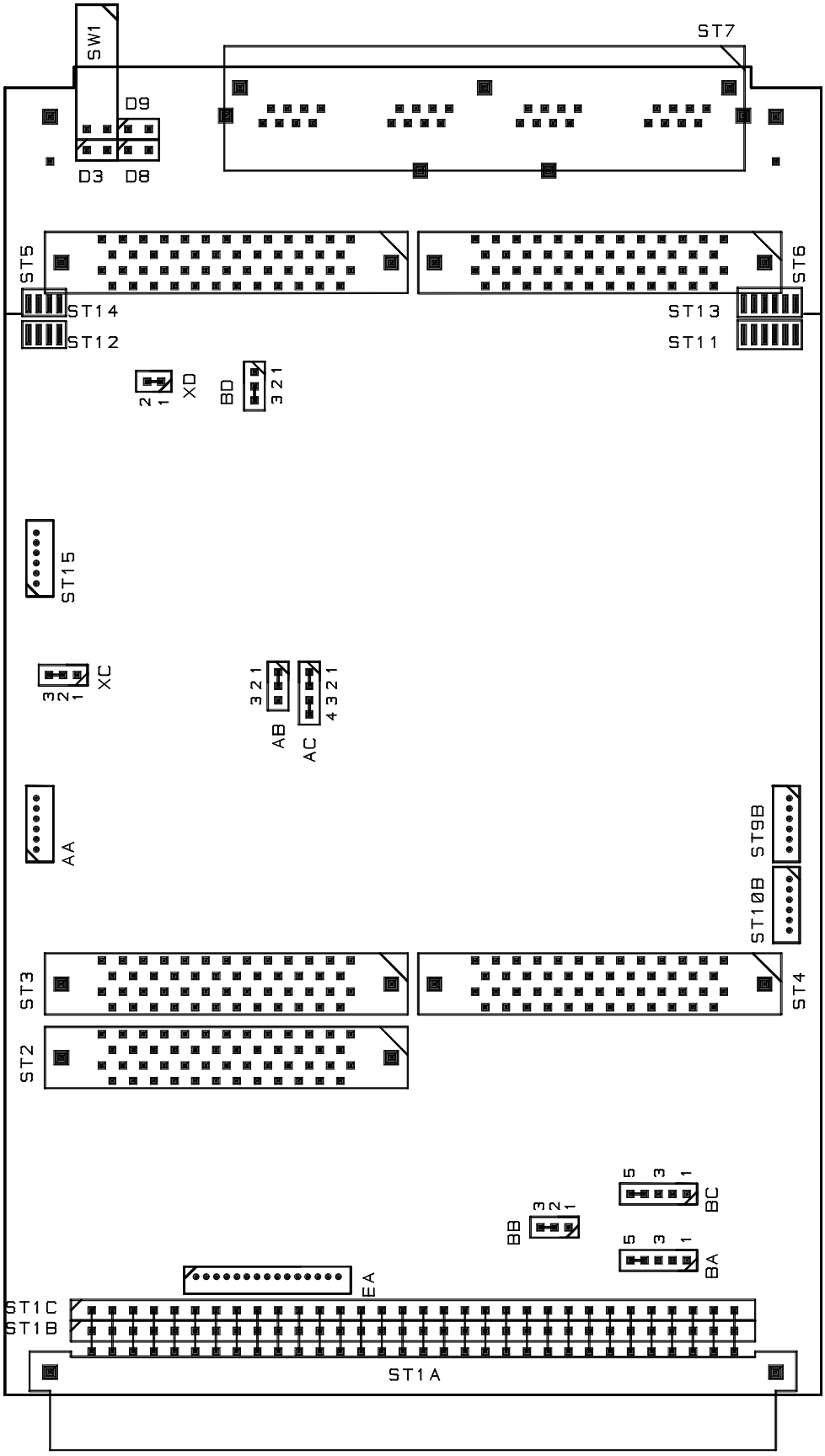
18.1 Jumpers Component Side



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18.2 Jumpers Solder Side



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Appendices

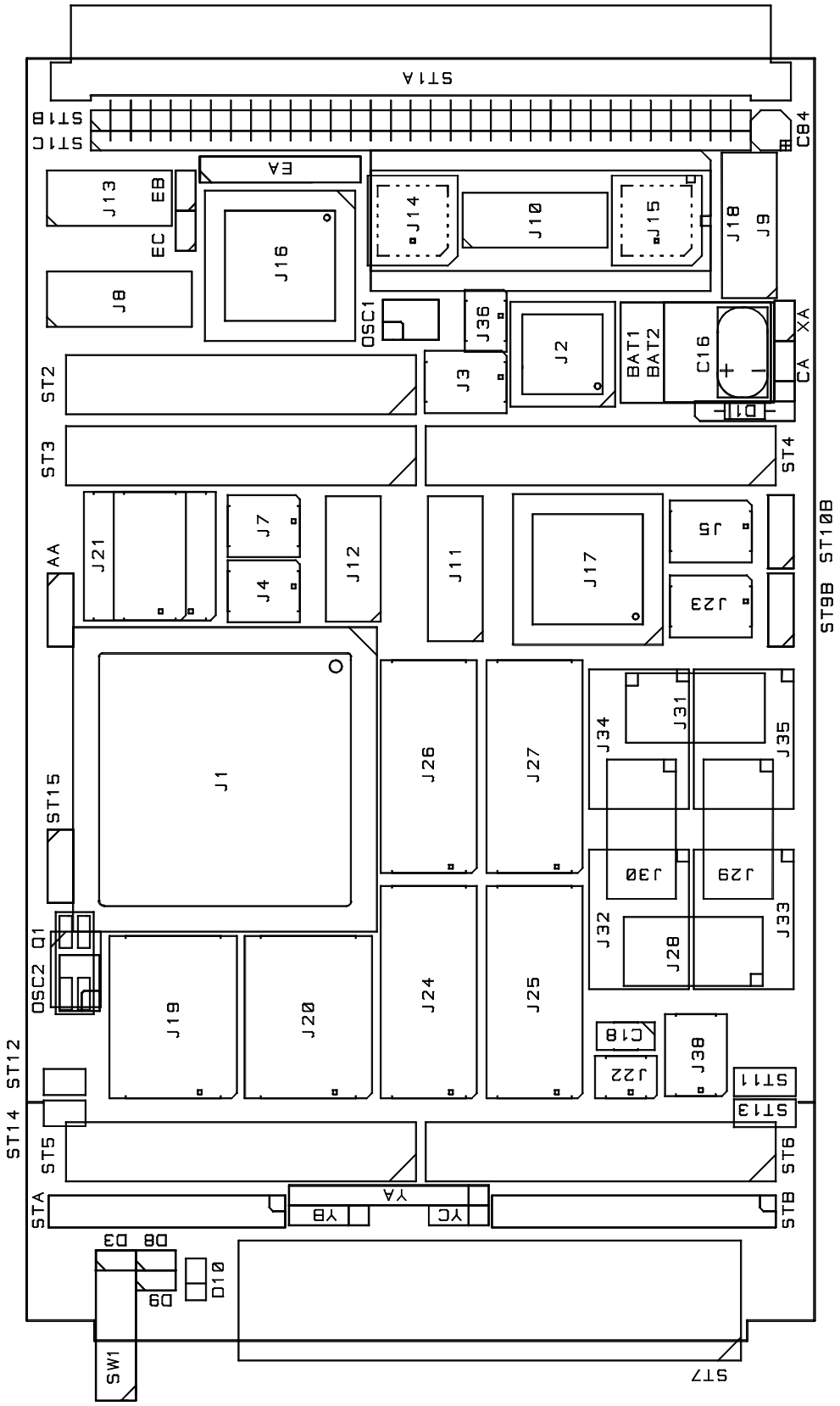
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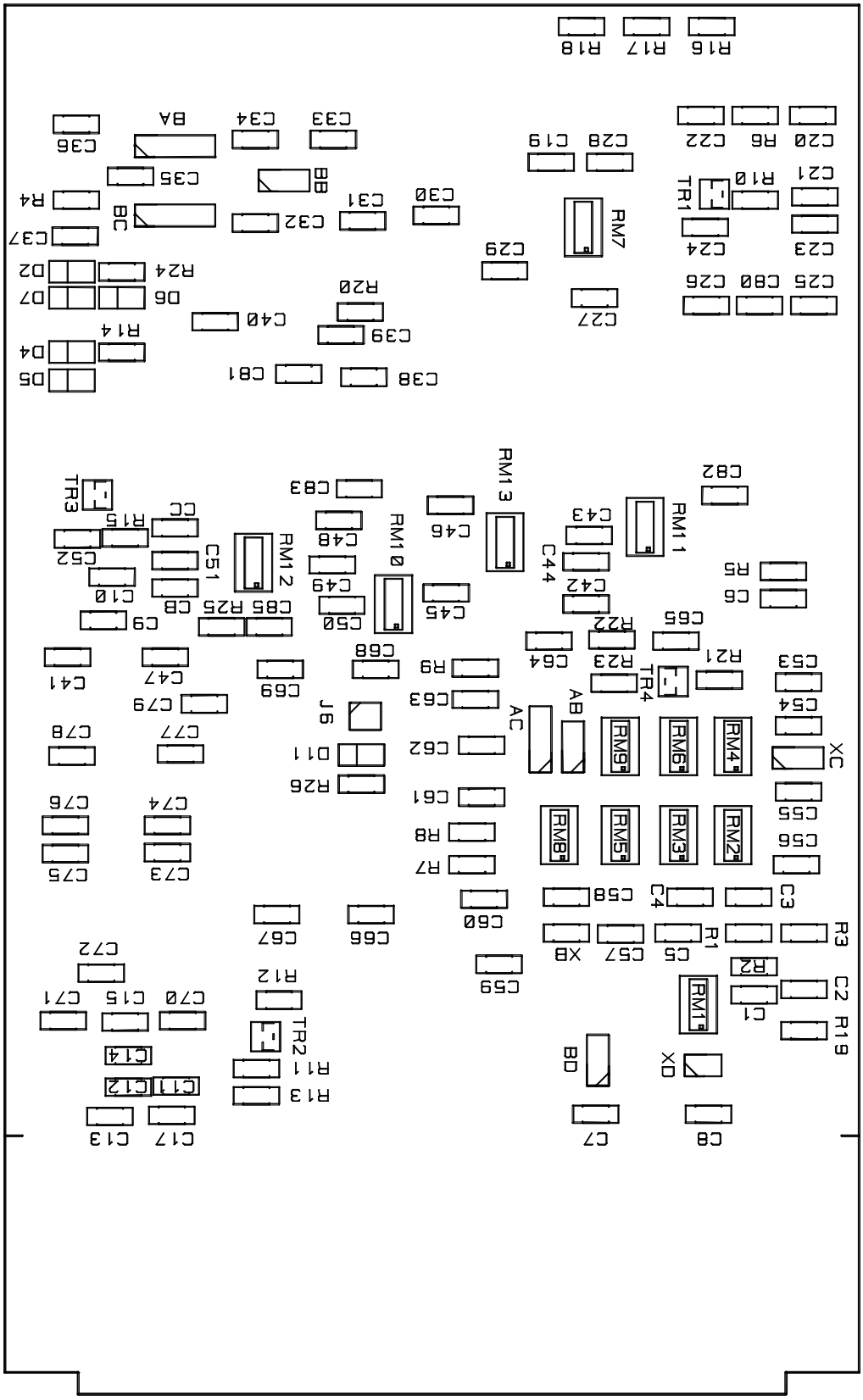
Appendix A: Layout Component Side



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Appendix B: Layout Solder Side



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Appendix C: Schematics

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Appendix D: Example Program for VME Interrupter

```
*****************************************************
*               EXAMPLE PROGRAMM                    *
*               for Interrupter and                 *
*               Dual Port Initialization            *
*****************************************************
*
RBASE       EQU     $FFF00000       ; CS7
RGWCL       EQU     $80             ; write clears fifo
RGWDT       EQU     $84             ; write data to fifo
RGRCL       EQU     $80             ; read sets fifo to position null
RGRDT       EQU     $84             ; read fifo data
IPNDB       EQU     $88             ; interrupt pending bit
CHAROUT     EQU     $FFC0000C       ;character output  routine in Micromon
*
*
*   clear address compare shift register
*
        MOVEA.L     #RBASE,A0
        MOVE.B      #$0,RGWCL(A0)       ; write = clear command
        MOVE.B      #$80, RGWDT (A0)    ; enable onboard level 1
        MOVE.B      #$80, RGWDT (A0)    ; enable onboard level 7
*
*   set VMEbus interrupt mask via D31, 1 = on, 0 = off
*
        MOVE.B      #$00,RGWDT(A0)      ; disable int. level 7
        MOVE.B      #$00,RGWDT(A0)      ; disable int. level 6
        MOVE.B      #$00,RGWDT(A0)      ; disable int. level 5
        MOVE.B      #$00,RGWDT(A0)      ; disable int. level 4
        MOVE.B      #$00,RGWDT(A0)      ; disable int. level 3
        MOVE.B      #$00,RGWDT(A0)      ; disable int. level 2
        MOVE.B      #$80,RGWDT(A0)      ; enable int. level 1
*
*   set auto mask for interrupter level  via D31
*
        MOVE.B      #$80,RGWDT(A0)      ; do not mask interrupter level
*
*   mask address lines A18 and A19 for 256 KByte decoding
*
        MOVE.B      #$80,RGWDT(A0)      ; ignore A19
        MOVE.B      #$80,RGWDT(A0)      ; ignore A18
```


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```
*
*   set std.access address to $xx000000  via D31
*
        MOVE.B      #$00,RGWDT(A0)          ; compare to A23
        MOVE.B      #$00,RGWDT(A0)          ; compare to A22
        MOVE.B      #$00,RGWDT(A0)          ; compare to A21
        MOVE.B      #$00,RGWDT(A0)          ; compare to A20
        MOVE.B      #$00,RGWDT(A0)          ; compare to A19
        MOVE.B      #$00,RGWDT(A0)          ; compare to A18
*
*   read back the stuff
*
        MOVE.B      RGRCL(A0),D0            ; read = clear command
*
        MOVEA.L     #$F002000,A1            ; use as buffer
        MOVE.L      #$F,D0                  ; 16 values
LP0     MOVE.B      RGRDT(A0),(A1)+         ; read fifo
        DBRA        D0,LP0
*
*   emit some interrupts
*
        LEA.L       ISRV(PC),A0             ; get service address
        MOVE.L      A0,$400180              ; store in table
*
*   Bord Control Register Bit Map
*
*   D31     = Strobe IP-Module A
*   D30     = Strobe IP-Module B
*   D29     = DMA for IP-A = 0 / for IP-B = 1
*   D28     = LED on = 0 / off = 1
*   D27     = Start VMEbus Interrupt on 1 -> 0 change
*   D26     = IL3 \
*   D25     = IL2 - high active binary coded interrupt level
*   D24     = IL1 /
```


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```
*
LP2         MOVEA.L   #RBASE,A0          ; get system buffer
            MOVE.B    #$19,(A0)          ; set led off, level 1, STVI high
            MOVE.B    #$60,2(A0)         ; load vector $60 = $180
            MOVE.B    #$09,(A0)          ; set led on, level 1, STVI high
            MOVE.B    #$01,(A0)          ; emit interrupt, set STVI low
LP1         MOVE.B    IPNDB(A0),D0       ; get interrupt pending bit
            BTST      #$7,D0             ; set to one = done
            BEQ       LP1                ; still pending
            MOVE.B    #$19,(A0)          ; set led off, level 1, STVI high
            BRA       LP2                ; do it again
*
*      interrupt service
*
ISRV        MOVE.B    #'>',D0            ; lets see something
            JSR       CHAROUT            ; on screen
            RTE                          ; ...and get back
*
            END
```


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Appendix E: Pin Assignment of Connector AA

This connector contains all signals necessary for boundary scan interface of the 68360.
Used connector: 53047-0610 (MOLEX)
Mating connector: 51021-0600 (MOLEX)

Pin	Signal
1	TCK
2	GND
3	TRST*
4	TDI
5	TDO
6	TMS

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Appendix F: Pin Assignment of Connector EA

This connector contains all signals necessary for BDM interface and the programming interface for the ispLSI devices.

Used connector: 53048-1510 (MOLEX)
Mating connector: 51021-1500 (MOLEX)

Pin	Signal	BDM Signal	
1	IPIPE*	IPIPE / DSI	
2	+ 5V	Vdd	
3	IFETCH*	IFETCH / DSO	
4	PLRST*	RESET	
5	FREEZE	FREEZE	
6	GND	GND	
7	BKPT*	BKPT / DSCLK	
8	GND	GND	
9	BERR*	BERR	
10	DS*	DS	
11	PLENP*		
12	PLSDO		
13	PLSDI		ispLSI programming interface
14	PLMODE		
15	PLSCLK		



NOTE !

Do not use any of the ispLSI interface signals. Wrong handling may d estroy ispLSI devices or their contents and/or the complete IP360 board.

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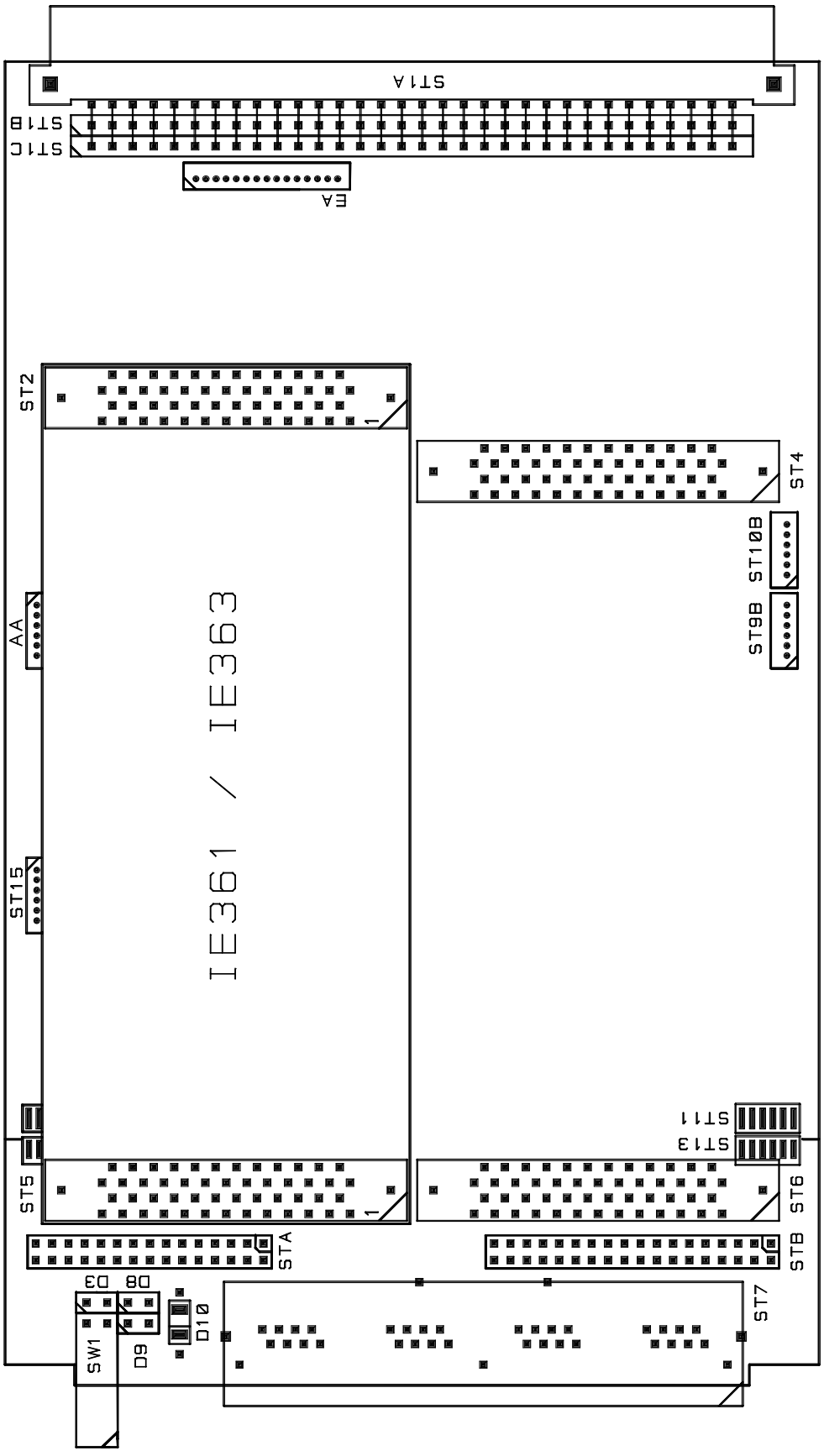
Appendix G: The IE361/IE363 Extension Boards

The IP360 supports a lot of port signals for the SCC, Ethernet and parallel ports which are available on connector ST2. The special interface boards IE36X are designed to buffer these signals and connect them to the output connectors ST5 and ST7. These adapter boards can be mounted on the second IP slot on IP360.
The IE361 piggyback offers 4 sockets for MicroSys I/O modules to buffer the 4 SCC channels of the 68360 processor with various serial line drivers (e.g. RS232, RS422 or RS485) and a centronics compatible interface.
The IE363 is similar to the IE361 piggyback, but has a built in Ethernet AUI interface for the SCC1. A version for twisted pair Ethernet instead of AUI is available on request. The centronics interface and the I/O module connectors for the serial channels SCC2 to SCC4 are the same as on IE361.

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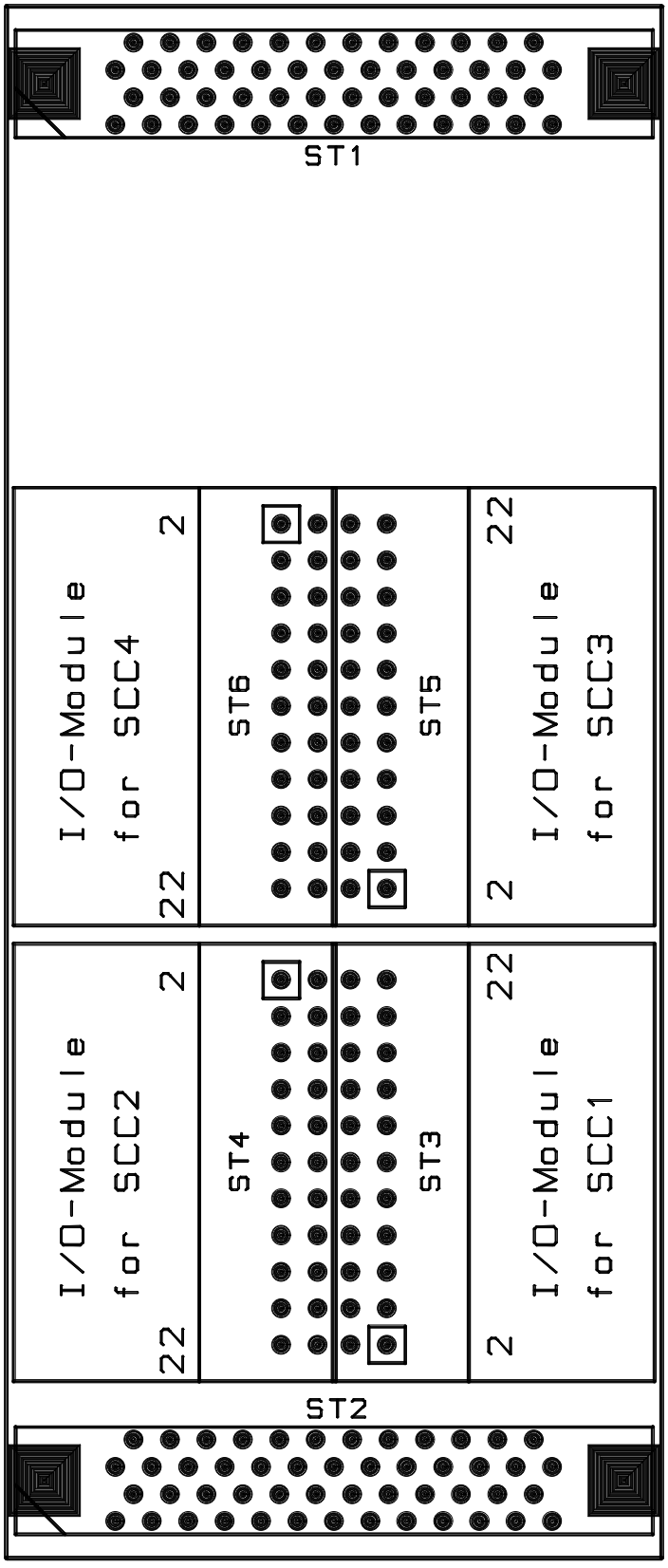
Mounting IE36X on IP360



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Mounting I/O Modules on IE36X



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Pin Configuration of ST7 with IE361

Pin	Signal	Signal	Pin	
1	Strobe	D0	2	
3	D1	D2	4	
5	D3	D4	6	**Centronics**
7	D5	D6	8	
9	D7	ACK	10	
11	Busy	GND	12	
13	GND		14	
15		CTS4	16	**SCC4** (RS232)
17	TxD4	RTS4	18	
19	RxD4		20	
21	DCD4	GND	22	
23			24	
25	CTS3	TxD3	26	**SCC3** (RS232)
27	RTS3	RxD3	28	
29		DCD3	30	
31	GND		32	
33		CTS2	34	**SCC2** (RS232)
35	TxD2	RTS2	36	
37	RxD2		38	
39	DCD2	GND	40	
41			42	
43	CTS1	TxD1	44	**SCC1** (RS232)
45	RTS1	RxD1	46	
47		DCD1	48	
49	+12V	GND	50	not used

Example for RS422 pin configuration (also for IE363)

13	GND	CTS4+	14	
15	TxD4+	CTS4-	16	**SCC4** (RS422)
17	TxD4-	RTS4-	18	
19	RxD4-	RTS4+	20	
21	RxD4+	GND	22	
23	CTS3+	TxD3+	24	
25	CTS3-	TxD3-	26	**SCC3** (RS422)
27	RTS3-	RxD3-	28	
29	RTS2+	RxD3+	30	

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Pin Configuration of ST7 with IE363 (AUI-Interface)

Pin	Signal	Signal	Pin	
1	Strobe	D0	2	
3	D1	D2	4	
5	D3	D4	6	**Centronics**
7	D5	D6	8	
9	D7	ACK	10	
11	Busy	GND	12	
13	GND		14	
15		CTS4	16	**SCC4**
17	TxD4	RTS4	18	
19	RxD4		20	
21	DCD4	GND	22	
23			24	
25	CTS3	TxD3	26	**SCC3**
27	RTS3	RxD3	28	
29		DCD3	30	
31	GND		32	
33		CTS2	34	**SCC2**
35	TxD2	RTS2	36	
37	RxD2		38	
39	DCD2	GND	40	(Pin 40 = Pin 1 of 15pin DSUB)
41	COL-	COL+	42	
43	TxD-	TxD+	44	**AUI-Interface**
45	GND	GND	46	
47	RxD-	RxD+	48	
49	+12V	GND	50	

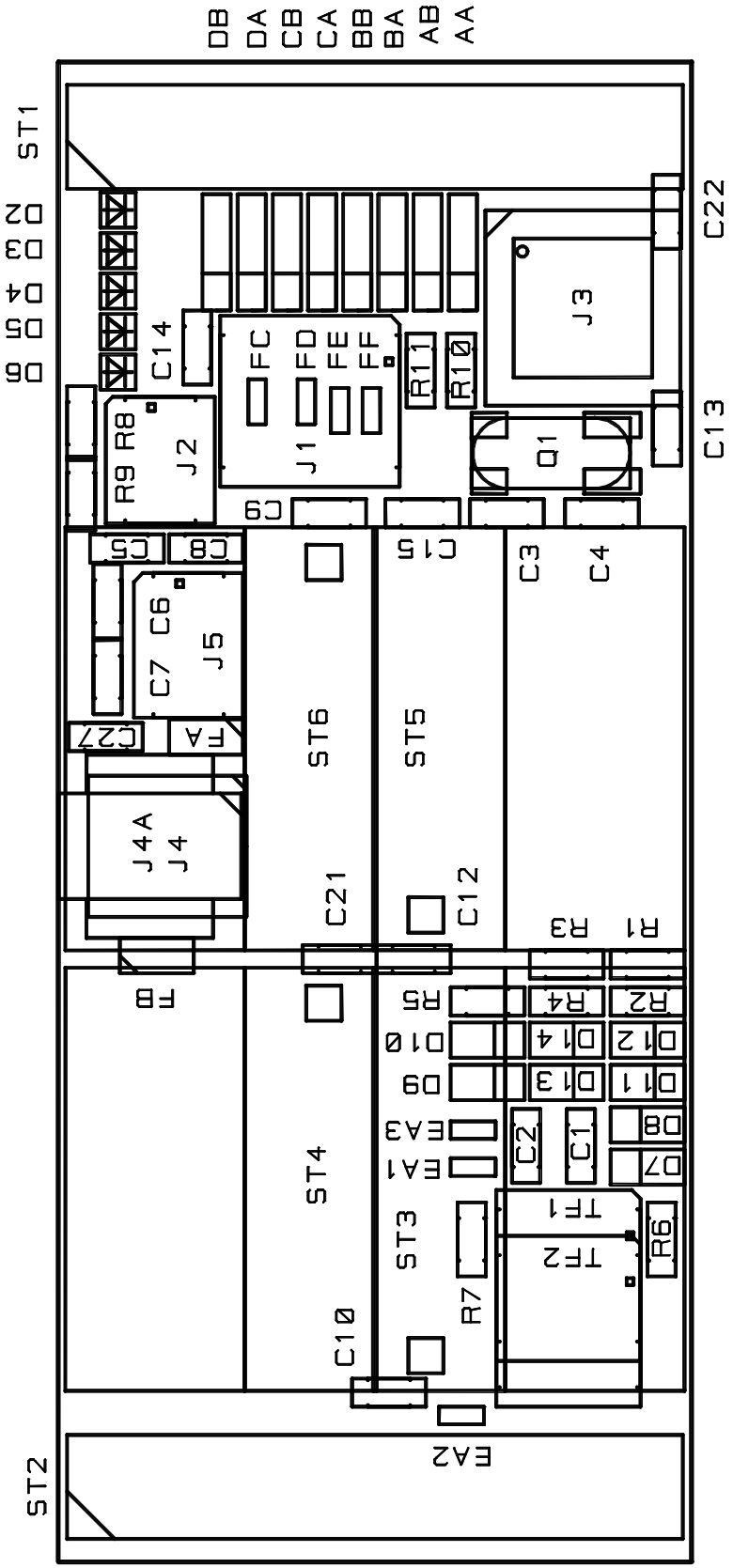
Pin Configuration of ST7 with IE363 (TP-Interface)

		----	40	
41	----	----	42	
43	TxD-	TxD+	44	**TP-Interface**
45	----	----	46	
47	RxD-	RxD+	48	
49	+12V	----	50	

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Layout IE363 Componentside



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Jumpers and LEDs on IE36X

Size	Jumper	Position		Function	
1x3	AA	1-2		RxC connected to SCC1 I/O module pin 10	IE361 only
	AA	2-3	*	CTS connected to SCC1 I/O module pin 10	
1x3	AB	1-2		TxC connected to SCC1 I/O module pin 14	
	AB	2-3	*	RTS connected to SCC1 I/O module pin 14	
1x3	BA	1-2		RxC connected to SCC2 I/O module pin 10	
	BA	2-3	*	CTS connected to SCC2 I/O module pin 10	
1x3	BB	1-2		TxC connected to SCC2 I/O module pin 14	
	BB	2-3	*	RTS connected to SCC2 I/O module pin 14	
1x3	CA	1-2		RxC connected to SCC3 I/O module pin 10	
	CA	2-3	*	CTS connected to SCC3 I/O module pin 10	
1x3	CB	1-2		TxC connected to SCC3 I/O module pin 14	
	CB	2-3	*	RTS connected to SCC3 I/O module pin 14	
1x3	DA	1-2		RxC connected to SCC4 I/O module pin 10	
	DA	2-3	*	CTS connected to SCC4 I/O module pin 10	
1x3	DB	1-2		TxC connected to SCC4 I/O module pin 14	
	DB	2-3	*	RTS connected to SCC4 I/O module pin 14	
1x2	EA1	1-2		connects GND to AUI	*)
1x2	EA2	1-2		connects GND to AUI	*)
1x2	EA3	1-2		connects GND to AUI	*)

*) installed on AUI Version
*) not installed on Twisted Pair Version

LEDs:

D2	LED red	Twisted pair link polarity	IE363 only
D3	LED green	Twisted pair link integrity	
D4	LED red	Collision	
D5	LED green	Receive data	
D6	LED yellow	Transmit data	

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Schematics IE363

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