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MicroSys

User's Manual

PM001

2nd edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
D-82054 Sauerlach
Germany

declare that the product

PM 001

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date: 19.03.1997

Signature:

Position: General Manager

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1. Introduction

1.1 Short Description

The **PM001** is another excellent product out of the MicroSys' **Single Euro** VME line. The board offers two **PCMCIA** slots according to the **PC Card Standard Release 2**. Both slots allow the use **memory cards** as well as **I/O cards**. The necessary programming voltage for FLASH memory cards is supplied by a separate **DC/DC converter** for each slot. The access time can be individually changed for each slot in **50ns steps** by software. The address base and range for memory cards can be programmed in **1MByte steps** within the VMEbus standard access area. Memory cards are also supported within the VMEbus short I/O access area by an address load and **autoincrement** feature of the **PM001**. The complete board is implemented in **CMOS technology**. This allows for a power consumption **as low as** : 5V / xxW.

1.2 Specifications

The power requirements for the PM001 board without an inserted PC card are shown in the following table. The given values are valid for PM001 with inactive DC/DC converters for FLASH programming. The maximum values of each of these converters is shown separately. The power consumption of the inserted PC cards must be added to the given values.

Power Requirements:	typ.	max.	min.	typ.current + PC cards
PM001 board logic	+5V	+0.60V	-0.36V	600mA
PM001 DC/DC converter A	+5V	+0.60V	-0.36V	5mA, no load
PM001 DC/DC converter B	+5V	+0.60V	-0.36V	5mA, no load

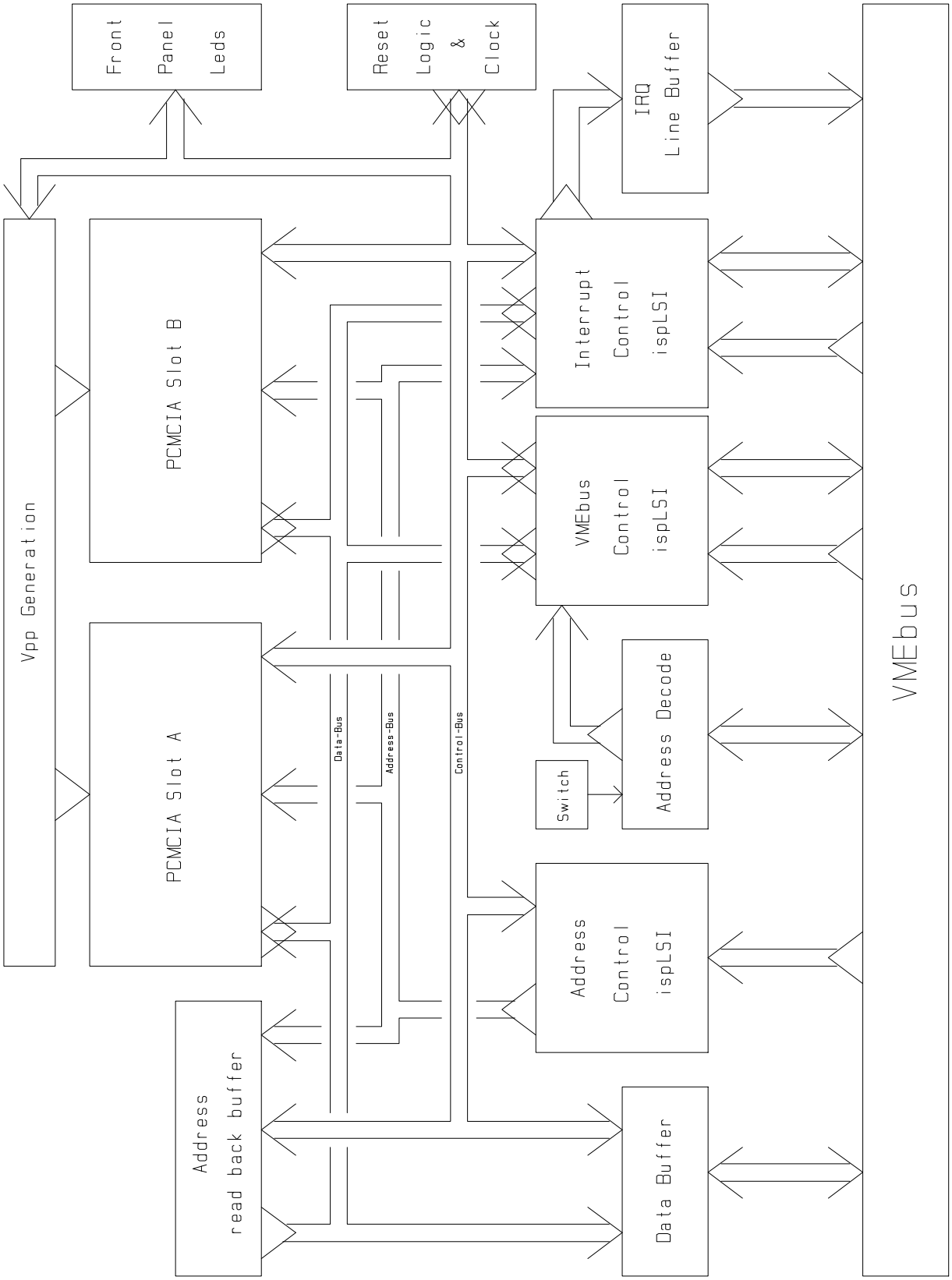
1.3 Related Documentation

The following manuals are applicable to the PM001:

- VMEbus Specification Manual ANSI/IEEE STD1014-1987
- PCMCIA PC Card Standard - Release 2.0

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1.4 Block Diagram



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2. Delivery

2.1 Items shipped with this unit

- User's Manual PM001 Hardware
- MicroSys shipping carton



ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys Shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

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3. Installation

3.1 Items required for PM001installation

For the installation of the PM001, the following items are required:

- Card Cage or housing
- VMEbus Motherboard
- Adequate rated power supply

3.2 Points to be observed

Before the unit is inserted into the card cage, the following points should be observed:

- Unit requires +5V (+5/-2.5%)
- Be sure voltage is of correct polarity
- Unit should only be inserted into, and removed from card cage when power is off
- The card cage should be well ventilated. The operating temperature should never exceed it's specified range
- Check default jumper setting



GUARANTEE IS VOID IF UNIT IS OPERATED

OUT OF IT'S SPECIFICATIONS!

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4. Board Overview

4.1 Features PM001

format:	single euro
PCMCIA:	two independent 16Bit slots
interface:	memory and I/O card support
card types:	2 x type I or 2 x type II or 1 x type III
memory decoding:	memory card support upto 64MByte
access time:	programmable in 50ns steps from 150ns to 300ns
FLASH support:	VPP generation via two separate DC/DC converters
I/O card support:	onboard piezoelectric sounder for speaker support
front panel leds:	VPP enable card detect busy
addressing:	VMEbus standard access VMEbus short I/O access
VMEbus base address:	programmable in 1 MByte address steps
VMEbus address range:	programmable in 1 MByte address steps
VMEbus short I/O feature:	4KByte address range I/O card support memory card base address register memory card autoincrement address feature
VMEbus interrupter:	**7** level & vector programmable interrupter
VMEbus interface:	according to ANSI/IEEE STD1014-1987
VMEbus slave:	DTB A16/A24 -D8/D16

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4.2 Addressmap PM001

Register Name	Abbreviation	Address	Direction	Data Path
Board Select Register	BSR	$0001	read/write	D0-D7
Mode Register	MOD	$0003	read/write	D0-D7
Interrupt Level Register	ILR	$0005	read/write	D0-D7
Interrupt Enable Register	IER	$0007	read only	D0-D7
Card Bank Switch Register A	CBSA	$0009	read only	D0-D7
Card VPP Register A	CVPA	$000B	read & write	D0-D7
Card Bank Switch Register B	CBSB	$000D	read only	D0-D7
Card VPP Register B	CVPB	$000F	read & write	D0-D7
Address Register A 1	ADA1	$0010	read only	D8-D15
Address Register A 0	ADA0	$0011	read/write	D1-D7
Address Register B 1	ADB1	$0012	read only	D8-D15
Address Register B 0	ADB0	$0013	read/write	D1-D7
Address Register A 2	ADA2	$0015	read/write	D0-D3
Address Register B 2	ADB2	$0017	read/write	D0-D3
Address Register A 3	ADA3	$0019	read & write	D0-D5
Address Register B 3	ADB3	$001B	read & write	D0-D5
Address Register A 4	ADA4	$001D	write only	D0-D7
Address Register B 4	ADB4	$001F	write only	D0-D7
Interrupt Vector Register A	IVRA	$0021	read/write	D0-D7
Interrupt Vector Register B	IVRB	$0023	read/write	D0-D7
Interrupt Enable Register	IER	$0025	write only	D0-D7
Address Function Register	AFR	$0031	read/write	D0-D3
Autoincrement Access Slot A	AIAIO	$0080	read/write	D0-D15
Fixed Address Access Slot A	FAAIO	$0082	read/write	D0-D15
Autoincrement Access Slot B	AIBIO	$0180	read/write	D0-D15
Fixed Address Access Slot B	FABIO	$0182	read/write	D0-D15
Autoincrement Access Slot A	AIAM	$0280	read/write	D0-D15
Fixed Address Access Slot A	FAAM	$0282	read/write	D0-D15
Autoincrement Access Slot B	AIBM	$0380	read/write	D0-D15
Fixed Address Access Slot B	FABM	$0382	read/write	D0-D15
I/O Data Access Range Slot A	IODA	$0400-$04FF	read/write	D0-D15
I/O REG Access Range Slot A	REGA	$0500-$05FF	read/write	D0-D15
I/O Data Access Range Slot B	IODB	$0600-$06FF	read/write	D0-D15
I/O REG Access Range Slot B	REGB	$0700-$07FF	read/write	D0-D15

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5. The Memory and I/O Card Interface

The **PM001** contains **two independent PCMCIA** slots for the use of **memory** or **I/O cards**. Is automatically configured after power up or manual reset as memory interface on both slots. The initial access time is set to 300ns. The I/O interface standard is only available if the card and the socket have been configured to their dedicated function by software. The interface pinout of both 68 pin PCMCIA connectors is shown in following table.

Memory Card Interface				I/O & Memory Card Interface		
Signal	**I/O**	**Function**	**Pin**	**Function**	**I/O**	**Signal**
GND	**O**	**ground**	**1**	**ground**	**O**	**GND**
D3	**I/O**	**data line 3**	**2**	**data line 3**	**I/O**	**D3**
D4	**I/O**	**data line 4**	**3**	**data line 4**	**I/O**	**D4**
D5	**I/O**	**data line 5**	**4**	**data line 5**	**I/O**	**D5**
D6	**I/O**	**data line 6**	**5**	**data line 6**	**I/O**	**D6**
D7	**I/O**	**data line 7**	**6**	**data line 7**	**I/O**	**D7**
CE1-A/B	**O**	**card enable**	**7**	**card enable**	**O**	**CE1-A/B**
A10	**O**	**address line 10**	**8**	**address line 10**	**O**	**A10**
OE-A/B	**O**	**output enable**	**9**	**output enable**	**O**	**OE-A/B**
A11	**O**	**address line 11**	**10**	**address line 11**	**O**	**A11**
A9	**O**	**address line 9**	**11**	**address line 9**	**O**	**A9**
A8	**O**	**address line 8**	**12**	**address line 8**	**O**	**A8**
A13	**O**	**address line 13**	**13**	**address line 13**	**O**	**A13**
A14	**O**	**address line 14**	**14**	**address line 14**	**O**	**A14**
WE/PRGM-A/B	**O**	**write enable**	**15**	**write enable**	**O**	**WE/PRGM-A/B**
RDY/BSY-A/B	**I**	**ready/busy**	**16**	**interrupt request**	**I**	**RDY/BSY-A/B**
Vcc	**O**	**5 volts**	**17**	**5 volts**	**O**	**Vcc**
Vpp-A/B	**O**	**programming voltage**	**18**	**programming voltage**	**O**	**Vpp-A/B**
A16	**O**	**address line 16**	**19**	**address line 16**	**O**	**A16**
A15	**O**	**address line 15**	**20**	**address line 15**	**O**	**A15**
A12	**O**	**address line 12**	**21**	**address line 12**	**O**	**A12**
A7	**O**	**address line 7**	**22**	**address line 7**	**O**	**A7**
A6	**O**	**address line 6**	**23**	**address line 6**	**O**	**A6**
A5	**O**	**address line 5**	**24**	**address line 5**	**O**	**A5**
A4	**O**	**address line 4**	**25**	**address line 4**	**O**	**A4**
A3	**O**	**address line 3**	**26**	**address line 3**	**O**	**A3**
A2	**O**	**address line 2**	**27**	**address line 2**	**O**	**A2**
A1	**O**	**address line 1**	**28**	**address line 1**	**O**	**A1**
A0	**O**	**address line 0**	**29**	**address line 0**	**O**	**A0**
D0	**I/O**	**data line 0**	**30**	**data line 0**	**I/O**	**D0**
D1	**I/O**	**data line 1**	**31**	**data line 1**	**I/O**	**D1**
D2	**I/O**	**data line 2**	**32**	**data line 2**	**I/O**	**D2**
WP-A/B	**I**	**write protect**	**33**	**IO port is 16 bit**	**I**	**WP-A/B**
GND		**ground**	**34**	**ground**		**GND**

I = input to PM001	O = output from PM001	I/O = bidirectional

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Memory Card Interface				I/O & Memory Card Interface		
Signal	**I/O**	**Function**	**Pin**	**Function**	**I/O**	**Signal**
GND	**O**	**ground**	**35**	**ground**	**O**	**GND**
CD1-A/B	**I**	**card detect**	**36**	**card detect**	**I**	**CD1-A/B**
D11	**I/O**	**data line 11**	**37**	**data line 11**	**I/O**	**D11**
D12	**I/O**	**data line 12**	**38**	**data line 12**	**I/O**	**D12**
D13	**I/O**	**data line 13**	**39**	**data line 13**	**I/O**	**D13**
D14	**I/O**	**data line 14**	**40**	**data line 14**	**I/O**	**D14**
D15	**O**	**data line 15**	**41**	**data line 15**	**O**	**D15**
CE2-A/B	**O**	**card enable**	**42**	**card enable**	**O**	**CE2-A/B**
RFS	**O**	**(refresh)**	**43**	**(refresh)**	**O**	**RFS**
RFU	**O**	**reserved**	**44**	**IO read**	**O**	**IORD**
RFU	**O**	**reserved**	**45**	**IO write**	**O**	**IOWR**
A17	**O**	**address line 17**	**46**	**address line 17**	**O**	**A17**
A18	**O**	**address line 18**	**47**	**address line 18**	**O**	**A18**
A19	**O**	**address line 19**	**48**	**address line 19**	**O**	**A19**
A20	**O**	**address line 20**	**49**	**address line 20**	**O**	**A20**
A21	**O**	**address line 21**	**50**	**address line 21**	**O**	**A21**
Vcc	**O**	**5 volts**	**51**	**5 volts**	**O**	**Vcc**
Vpp-A/B	**O**	**programming voltage**	**52**	**programming voltage**	**O**	**Vpp-A/B**
A22	**O**	**address line 22**	**53**	**address line 22**	**O**	**A22**
A23	**O**	**address line 23**	**54**	**address line 23**	**O**	**A23**
A24	**O**	**address line 24**	**55**	**address line 24**	**O**	**A24**
A25	**O**	**address line 25**	**56**	**address line 25**	**O**	**A25**
RFU		**reserved**	**57**	**reserved**		**RFU**
RESET	**O**	**card reset**	**58**	**card reset**	**O**	**RESET**
WAIT-A/B	**I**	**extended bus cycle**	**59**	**extended bus cycle**	**I**	**WAIT-A/B**
RFU	**I**	**reserved**	**60**	**input port acknowledge**	**I**	**INPACK-A/B**
REG-A/B	**O**	**register select**	**61**	**register select / IO enable**	**O**	**REG-A/B**
BVD2-A/B	**I**	**battery voltage detect 2**	**62**	**audio digital waveform**	**I**	**SPKR-A/B**
BVD1-A/B	**I**	**battery voltage detect 1**	**63**	**card status changed**	**I**	**STSCHG-A/B**
D8	**I/O**	**data line 8**	**64**	**data line 8**	**I/O**	**D8**
D9	**I/O**	**data line 9**	**65**	**data line 9**	**I/O**	**D9**
D10	**I/O**	**data line 10**	**66**	**data line 10**	**I/O**	**D10**
CD2-A/B	**I**	**card detect**	**67**	**card detect**	**I**	**CD2-A/B**
GND	**O**	**ground**	**68**	**ground**	**O**	**GND**

I = input to PM001	O = output from PM001	I/O = bidirectional

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6. The VMEbus Short I/O Addressing

The **PM001** is equipped either with a **4 bit hex switch** or a **5 bit jumper** area to select the desired base address within the VMEbus short I/O access range. All control and function registers of the PM001 are located within this VMEbus short I/O address range. The decoding is performed according to the following table. If the code switch is used, the VMEbus address line A11 is always decoded to a logical one. The given address map of the PM001 contains offset values in respect to the base of the show address range.

Code Switch SW1	Address Range:	Jumper Area AA				
	Base:	9-10	7-8	5-6	3-4	1-2
Position 0	$0000 - $07FF	0	0	0	0	0
	$0800 - $0FFF	0	0	0	0	1
Position 1	$1000 - $17FF	0	0	0	1	0
	$1800 - $1FFF	0	0	0	1	1
Position 2	$2000 - $27FF	0	0	1	0	0
	$2800 - $2FFF	0	0	1	0	1
Position 3	$3000 - $37FF	0	0	1	1	0
	$3800 - $3FFF	0	0	1	1	1
Position 4	$4000 - $47FF	0	1	0	0	0
	$4800 - $4FFF	0	1	0	0	1
Position 5	$5000 - $57FF	0	1	0	1	0
	$5800 - $5FFF	0	1	0	1	1
Position 6	$6000 - $67FF	0	1	1	0	0
	$6800 - $6FFF	0	1	1	0	1
Position 7	$7000 - $77FF	0	1	1	1	0
	$7800 - $7FFF	0	1	1	1	1
Position 8	$8000 - $87FF	1	0	0	0	0
	$8800 - $8FFF	1	0	0	0	1
Position 9	$9000 - $97FF	1	0	0	1	0
	$9800 - $9FFF	1	0	0	1	1
Position 10	$A000 - $A7FF	1	0	1	0	0
	$A800 - $AFFF	1	0	1	0	1
Position 11	$B000 - $B7FF	1	0	1	1	0
	$B800 - $BFFF	1	0	1	1	1
Position 12	$C000 - $C7FF	1	1	0	0	0
	$C800 - $CFFF	1	1	0	0	1
Position 13	$D000 - $D7FF	1	1	0	1	0
	$D800 - $DFFF	1	1	0	1	1
Position 14	$E000 - $E7FF	1	1	1	0	0
	$E800 - $EFFF	1	1	1	0	1
Position 15	$F000 - $F7FF	1	1	1	1	0
	$F800 - $FFFF	1	1	1	1	1

0 = jumper inserted	1 = jumper removed

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The following VMEbus AM-Codes are necessary for the short I/O addressing:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	hex. Value
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low H = logical high

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7. The PM001 Board Registers

7.1 The Board Select Register

The **BSR** of the PM001 is located at the offset address **$0001** and contains **8 data bits** which can be **read back** for verification. It is used to set the desired base address and decoding size within the VMEbus standard access range. Data bit D5 disables the VMEbus standard access at all, if set to zero. The reset line of both PCMCIA slots is controlled via data bit D4.

BSR	D7	D6	D5	D4	D3	D2	D1	D0
read:	BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
write:	BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
function:	size	size	enable	reset	function	compare	compare	compare
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	high	high	---	---	---	---

function	D7	D6	D5	D4	D3	D2	D1	D0
compare state to VMEbus address	---	---	---	---	---	A23	A22	A21
decoding size 1MByte for each slot	0	0	---	---	---	---	---	---
decoding size 2MByte for each slot	0	1	---	---	---	---	---	---
decoding size 4MByte for each slot	1	0	---	---	---	---	---	---
decoding size 8MByte for each slot	1	1	---	---	---	---	---	---
activate reset line of slot A	---	---	---	0	---	---	---	---
enable VMEbus standard access	---	---	1	---	---	---	---	---
MOD2=0: activate reset line of slot B	---	---	---	---	1	---	---	---
MOD2=1: compare state to VMEA20	---	---	---	---	A20	---	---	---

If the MOD2 bit of the mode register is set to high, the reset control bit D4 of the board select register activates the reset line of both slots. In this case, the memory select range within the standard VMEbus access decoding is limited to 1MByte. Depending on the decoding, only slot A, if D3 is set to low, or only slot B, if D3 is set to high, can be accessed within the defined memory access range.

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7.2 The Mode Register

The **MOD** of the PM001 is located at the offset address **$0003** and contains **4 bit of read only** information and **4 data bits** which can be **written and read** back for verification. The read only part reflects the state of two onboard jumper links and the INPACK lines of both PCMCIA slots. The remaining read/write part is used to the control the **REG** lines of the PCMCIA slots and the VMEbus short I/O user/supervisor access. The function of data bit D2 is not defined yet.

MOD register overview at address location $0003:

MOD	D7	D6	D5	D4	D3	D2	D1	D0
read:	JP7	JP7	MOD5	INPACK-A	INPACK-B	MOD2	MOD1	MOD0
write:	---	---	MOD5	---	---	MOD2	MOD1	MOD0
function:	user def.	user def.	enable	slot input	slot input	function	slot output	slot output
reset state:	---	---	0	1	1	0	0	0
active state:	---	---	---	0	0	---	1	1

function	D7	D6	D5	D4	D3	D2	D1	D0
PCMCIA slot-A REG line active	---	---	---	---	---	---	---	1
PCMCIA slot-B REG line active	---	---	---	---	---	---	1	---
PCMCIA slot-A INPACK line	---	---	---	state	---	---	---	---
PCMCIA slot-B INPACK line	---	---	---	---	state	---	---	---
VMEbus short I/O supervisor only	---	---	1	---	---	---	---	---
Jumper PP 9-10 inserted	---	0	---	---	---	---	---	---
Jumper PP 11-12 inserted	0	---	---	---	---	---	---	---
BSR3 reset function of slot B	---	---	---	---	---	0	---	---
BSR3 compare function of VMEA20	---	---	---	---	---	1	---	---

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7.3 The Interrupt Level Register

The **ILR** of the PM001 is located at the offset address **$0005**. It is **5 bits wide** and any written data can be **read back** for verification. Two bits of the ILR are used for **interrupt enable functions** and three bits define the binary coded **interrupt level**, which is used by the VMEbus interrupter. An **audio control bit**, which must be toggled with the desired frequency to activated the onboard piezo speaker. This bit should be set to zero, if the speaker is used by the audio line of an inserted PCMCIA card. A logical one will disable the audio out function at all. The remaining 2 bits of the data byte will always reflect a logical zero during read cycles.

ILR register overview at address location $0005:

ILR	D7	D6	D5	D4	D3	D2	D1	D0
read:	IE9	IE8	0	0	SPKR	IL3	IL2	IL1
write:	IE9	IE8	---	---	SPKR	IL3	IL2	IL1
function:	enable	enable	non	non	sound	binary coded level		
reset state:	0	0	0	0	0	0	0	0
active state:	1	1	---	---	---	---	---	---

function	D7	D6	D5	D4	D3	D2	D1	D0
IRQ enable for BVD2 on slot B	1	---	---	---	---	---	---	---
IRQ enable for BVD2 on slot A	---	1	---	---	---	---	---	---
reflect always zero	---	---	0	0	---	---	---	---
PCMCIA audio line enable	---	---	---	---	0	---	---	---
PCMCIA audio line disable	---	---	---	---	1	---	---	---
Frequency output to speaker	---	---	---	---	toggle	---	---	---
VMEbus interrupter off	---	---	---	---	---	0	0	0
VMEbus interrupter level 1	---	---	---	---	---	0	0	1
VMEbus interrupter level 2	---	---	---	---	---	0	1	0
VMEbus interrupter level 3	---	---	---	---	---	0	1	1
VMEbus interrupter level 4	---	---	---	---	---	1	0	0
VMEbus interrupter level 5	---	---	---	---	---	1	0	1
VMEbus interrupter level 6	---	---	---	---	---	1	1	0
VMEbus interrupter level 7	---	---	---	---	---	1	1	1

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7.4 The Interrupt Enable Register

The **8 bit** wide **IER** of the PM001 is split into **different read and write** address locations. Any write access must be performed at the address offset **$0025**, while the written data can be read back for verification at the address offset location **$0007**. All eight bits of the ILR are used for **interrupt enable** functions of both PCMCIA slots.

IER register overview at address location $0007 & $0025:

IER	D7	D6	D5	D4	D3	D2	D1	D0
read at $07:	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
write at $25:	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
function:	enable	enable	enable	enable	enable	enable	enable	enable
reset state:	0	0	0	0	0	0	0	0
active state:	1	1	1	1	1	1	1	1

function	D7	D6	D5	D4	D3	D2	D1	D0
IRQ enable for BVD1 on slot B	1	---	---	---	---	---	---	---
IRQ enable for rising edge of RDY/BSY on slot B	---	1	1	---	---	---	---	---
IRQ enable for falling edge of RDY/BSY on slot B	---	1	0	---	---	---	---	---
IRQ enable for CD1/CD2 on slot B	---	---	---	1	---	---	---	---
IRQ enable for BVD1 on slot A	---	---	---	---	1	---	---	---
IRQ enable for rising edge of RDY/BSY on slot A	---	---	---	---	---	1	1	---
IRQ enable for falling edge of RDY/BSY on slot A	---	---	---	---	---	1	0	---
IRQ enable for CD1/CD2 on slot A	---	---	---	---	---	---	---	1

The described interrupt sources are either issued on a state change or level sensitive according to following table:

Interrupt Source	high to low	low to high	low active
CD1/CD2 on slot A	X	X	
BVD1 on slot A			X
BVD2 on slot A (*)			X
RDY/BSY on slot A	X	X	
CD1/CD2 on slot B	X	X	
BVD1 on slot B			X
BVD2 on slot B (*)			X
RDY/BSY on slot B	X	X	

(*) signal refers to enable function bits within interrupt level register

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7.5 The Card Bank Switch Register A

For compatibility reasons to the FM001 FLASH-Memory board, the **CBSA** of the PM001 can be accessed on two different address locations. The card bank switch register of slot A can be accessed at the address location **$0009**. The **ADA3** register at the address location **$0019** is **identical with the CBSA** register. The register contains two card dependent status bits and a 6 bit wide extension address for memory cards in slot A, which allows for upto 64MByte address range.

CBSA register overview at address location $0009:

CBSA	D7	D6	D5	D4	D3	D2	D1	D0
read:	BSY-A	WP-A	A25-A	A24-A	A23-A	A22-A	A21-A	A20-A
write:	---	---	A25-A	A24-A	A23-A	A22-A	A21-A	A20-A
function:	status	status	base address for memory cards in slot A					
reset state:	---	---	0	0	0	0	0	0
active state:	0	1	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
BUSY status active of slot A	0	---	---	---	---	---	---	---
READY status active of slot A	1	---	---	---	---	---	---	---
write protect status inactive of slot A	---	0	---	---	---	---	---	---
write protect status active of slot A	---	1	---	---	---	---	---	---
set state of base address of slot A	---	---	A25-A	A24-A	A23-A	A22-A	A21-A	A20-A

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7.6 The Card VPP Register A

The **CVPA** of the PM001 is located at the address offset **$000B**. It is **8 bits wide** and contains four status bits and two enable signals for the control of the **FLASH memory programming** voltage and two **access time selection** bits. The status lines are read only, while the data written to the enable bits can be read back for verification.

CVPA register overview at address location $000B:

CVPA	D7	D6	D5	D4	D3	D2	D1	D0
read:	CD2-A	CD1-A	BVD2-A	BVD1-A	AC1-A	AC0-A	VP1-A	VP0-A
write:	---	---	---	---	AC1-A	AC0-A	VP1-A	VP0-A
function:	status	status	status	status	timing	timing	enable	enable
reset state:	---	---	---	---	0	0	0	0
active state:	0	0	---	---	---	---	1	1

function	D7	D6	D5	D4	D3	D2	D1	D0
PCMCIA slot-A CD2 line active	0	---	---	---	---	---	---	---
PCMCIA slot-A CD1 line active	---	0	---	---	---	---	---	---
PCMCIA slot-A battery o.k.	---	---	1	1	---	---	---	---
PCMCIA slot-A battery weak	---	---	0	1	---	---	---	---
PCMCIA slot-A battery low	---	---	1	0	---	---	---	---
PCMCIA slot-A battery low	---	---	0	0	---	---	---	---
PCMCIA slot-A 150ns access time	---	---	---	---	1	1	---	---
PCMCIA slot-A 200ns access time	---	---	---	---	1	0	---	---
PCMCIA slot-A 250ns access time	---	---	---	---	0	1	---	---
PCMCIA slot-A 300ns access time	---	---	---	---	0	0	---	---
PCMCIA slot-A VPP enable	---	---	---	---	---	---	1	1
PCMCIA slot-A VPP enable	---	---	---	---	---	---	0	1
PCMCIA slot-A VPP enable	---	---	---	---	---	---	1	0
PCMCIA slot-A VPP disable	---	---	---	---	---	---	0	0

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7.7 The Card Bank Switch Register B

The **CBSB** of the PM001, like the CSBA, can be accessed on two different address locations. The card bank switch register of slot B can be accessed at the address location **$000D** as well as the **identical ADB3** register at location **$001B**. The register contains two card dependent status bits and a 6 bit wide extension address for memory cards in slot B, which allows for upto 64MByte address range.

CBSB register overview at address location $000D:

CBSB	D7	D6	D5	D4	D3	D2	D1	D0
read:	BSY-B	WP-B	A25-B	A24-B	A23-B	A22-B	A21-B	A20-B
write:	---	---	A25-B	A24-B	A23-B	A22-B	A21-B	A20-B
function:	status	status	base address for memory cards in slot B					
reset state:	---	---	0	0	0	0	0	0
active state:	0	1	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
BUSY status active of slot B	0	---	---	---	---	---	---	---
READY status active of slot B	1	---	---	---	---	---	---	---
write protect status inactive of slot B	---	0	---	---	---	---	---	---
write protect status active of slot B	---	1	---	---	---	---	---	---
set state of base address of slot B	---	---	A25-B	A24-B	A23-B	A22-B	A21-B	A20-B

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7.8 The Card VPP Register B

The **CVPB** of the PM001 is located at the address offset **$000F**. It is **8 bits wide** and contains four status bits and two enable signals for the control of the **FLASH memory programming** voltage and two **access time selection** bits. The status lines are read only, while the data written to the enable bits can be read back for verification.

CVPB register overview at address location $000F:

CVPB	D7	D6	D5	D4	D3	D2	D1	D0
read:	CD2-B	CD1-B	BVD2-B	BVD1-B	AC1-B	AC0-B	VP1-B	VP0-B
write:	---	---	---	---	AC1-B	AC0-B	VP1-B	VP0-B
function:	status	status	status	status	timing	timing	enable	enable
reset state:	---	---	---	---	0	0	0	0
active state:	0	0	---	---	---	---	1	1

function	D7	D6	D5	D4	D3	D2	D1	D0
PCMCIA slot-B CD2 line active	0	---	---	---	---	---	---	---
PCMCIA slot-B CD1 line active	---	0	---	---	---	---	---	---
PCMCIA slot-B battery o.k.	---	---	1	1	---	---	---	---
PCMCIA slot-B battery weak	---	---	0	1	---	---	---	---
PCMCIA slot-B battery low	---	---	1	0	---	---	---	---
PCMCIA slot-B battery low	---	---	0	0	---	---	---	---
PCMCIA slot-B 150ns access time	---	---	---	---	1	1	---	---
PCMCIA slot-B 200ns access time	---	---	---	---	1	0	---	---
PCMCIA slot-B 250ns access time	---	---	---	---	0	1	---	---
PCMCIA slot-B 300ns access time	---	---	---	---	0	0	---	---
PCMCIA slot-B VPP enable	---	---	---	---	---	---	1	1
PCMCIA slot-B VPP enable	---	---	---	---	---	---	0	1
PCMCIA slot-B VPP enable	---	---	---	---	---	---	1	0
PCMCIA slot-B VPP disable	---	---	---	---	---	---	0	0

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7.9 The Address Registers ADA-0 to ADA-4

The PM001 offers a **24bit** wide access address register for **each PCMCIA** slot. This is useful in case a memory card should be accessed within the address space limited VMEbus short I/O range. Previous to any memory data access, the according access address within the 64MByte wide address range must be loaded into the address registers **ADA-0** to **ADA-4**. After any access to the PCMCIA **memory autoincrement** address location the access address is **automatically incremented** upto the limit of the next 16MByte boundary. The five address registers for slot A can be accessed according to following table.

ADA0 register overview at address location $0011:

ADA0	D7	D6	D5	D4	D3	D2	D1	D0
read:	A7-A	A6-A	A5-A	A4-A	A3-A	A2-A	A1-A	0
write:	A7-A	A6-A	A5-A	A4-A	A3-A	A2-A	A1-A	---
function:	state	state	state	state	state	state	state	fixed
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot A	A7-A	A6-A	A5-A	A4-A	A3-A	A2-A	A1-A	---
fixed state of address bit of slot A	---	---	---	---	---	---	---	0

ADA1 read only register overview at address location $0010:

ADA1	D15	D14	D13	D12	D11	D10	D9	D8
read:	A15-A	A14-A	A13-A	A12-A	A11-A	A10-A	A9-A	A8-A
write:	---	---	---	---	---	---	---	---
function:	state	state	state	state	state	state	state	state
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D15	D14	D13	D12	D11	D10	D9	D8
read current state of base address	A15-A	A14-A	A13-A	A12-A	A11-A	A10-A	A9-A	A8-A

The write function of the ADA1 address bits from A8-A to A15-A is performed via the ADA4 register.

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ADA2 register overview at address location $0015:

ADA2	D7	D6	D5	D4	D3	D2	D1	D0
read:	the data lines are not driven				A19-A	A18-A	A17-A	A16-A
write:	---	---	---	---	A19-A	A18-A	A17-A	A16-A
function:	---	---	---	---	state	state	state	state
reset state:	---	---	---	---	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot A	---	---	---	---	A19-A	A18-A	A17-A	A16-A

ADA3 register overview at address location $0019:

ADA3	D7	D6	D5	D4	D3	D2	D1	D0
read:	0	0	A25-A	A24-A	A23-A	A22-A	A21-A	A20-A
write:	---	---	A25-A	A24-A	A23-A	A22-A	A21-A	A20-A
function:	---	---	state	state	state	state	state	fixed
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot A	---	---	A25-A	A24-A	A23-A	A22-A	A21-A	A20-A

The ADA3 register is fully function compatible to the CBSA register.

ADA4 register overview at address location $001D:

ADA4	D7	D6	D5	D4	D3	D2	D1	D0
read:	0	0	0	0	0	0	0	0
write:	A15-A	A14-A	A13-A	A12-A	A11-A	A10-A	A9-A	A8-A
wr function:	state	state	state	state	state	state	state	state
reset state:	0	0	0	0	0	0	0	0

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot A	A15-A	A14-A	A13-A	A12-A	A11-A	A10-A	A9-A	A8-A

The read function of the ADA4 address bits from A8-A to A15-A is performed via the ADA1 register.

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7.10 The Address Registers B-0 to B-3

The PCMCIA slot B uses the second **24bit** address register set to perform the same features than slot A. The **auto-increment** function works **independent** between both slots and any **alternate accesses** does **not influence** each other. The five address registers for slot B can be accessed according to following table.

ADB0 register overview at address location $0013:

ADB0	D7	D6	D5	D4	D3	D2	D1	D0
read:	A7-B	A6-B	A5-B	A4-B	A3-B	A2-B	A1-B	0
write:	A7-B	A6-B	A5-B	A4-B	A3-B	A2-B	A1-B	---
function:	state	state	state	state	state	state	state	fixed
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot A	A7-B	A6-B	A5-B	A4-B	A3-B	A2-B	A1-B	---
fixed state of address bit of slot A	---	---	---	---	---	---	---	0

ADB1 read only register overview at address location $0012:

ADB1	D15	D14	D13	D12	D11	D10	D9	D8
read:	A15-B	A14-B	A13-B	A12-B	A11-B	A10-B	A9-B	A8-B
write:	---	---	---	---	---	---	---	---
function:	state	state	state	state	state	state	state	state
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D15	D14	D13	D12	D11	D10	D9	D8
read current state of base address	A15-B	A14-B	A13-B	A12-B	A11-B	A10-B	A9-B	A8-B

The write function of the ADB1 address bits from A8-B to A15-B is performed via the ADB4 register.

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ADB2 register overview at address location $0015:

ADB2	D7	D6	D5	D4	D3	D2	D1	D0
read:	the data lines are not driven				A19-B	A18-B	A17-B	A16-B
write:	---	---	---	---	A19-B	A18-B	A17-B	A16-B
function:	---	---	---	---	state	state	state	state
reset state:	---	---	---	---	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot B	---	---	---	---	A19-B	A18-B	A17-B	A16-B

ADB3 register overview at address location $001B:

ADB3	D7	D6	D5	D4	D3	D2	D1	D0
read:	0	0	A25-B	A24-B	A23-B	A22-B	A21-B	A20-B
write:	---	---	A25-B	A24-B	A23-B	A22-B	A21-B	A20-B
function:	---	---	state	state	state	state	state	fixed
reset state:	---	---	0	0	0	0	0	0
active state:	---	---	---	---	---	---	---	---

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot B	---	---	A25-B	A24-B	A23-B	A22-B	A21-B	A20-B

The ADA3 register is identical to the CBSA register at address location $0009.

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ADB4 register overview at address location $001F:

ADB4	D7	D6	D5	D4	D3	D2	D1	D0
read:	0	0	0	0	0	0	0	0
write:	A15-B	A14-B	A13-B	A12-B	A11-B	A10-B	A9-B	A8-B
wr function:	state	state	state	state	state	state	state	state
reset state:	0	0	0	0	0	0	0	0

Attention ! The reset state refers to the power up reset only, a VMEbus reset will not affect the register contents !

function	D7	D6	D5	D4	D3	D2	D1	D0
set state of base address of slot B	A15-B	A14-B	A13-B	A12-B	A11-B	A10-B	A9-B	A8-B

The read function of the ADB4 address bits from A8-B to A15-B is performed via the ADB1 register.

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7.11 The Interrupt Vector Register A & B

The PM001 contains an **8 bit** interrupt vector register for **each PCMCIA** slot to provide the necessary vector during VMEbus interrupt acknowledge cycles. The access address location for slot A is set to **$0021**, for slot B **$0023**. The written data of both registers can be **read back** for verification.

IVRA register overview at address location $0021:

IVRA	D7	D6	D5	D4	D3	D2	D1	D0
read:	IV7-A	IV6-A	IV5-A	IV4-A	IV3-A	IV2-A	IV1-A	IV0-A
write:	IV7-A	IV6-A	IV5-A	IV4-A	IV3-A	IV2-A	IV1-A	IV0-A
function:	user defined interrupt vector							
reset state:	0	0	0	0	0	0	0	0

IVRB register overview at address location $0023:

IVRB	D7	D6	D5	D4	D3	D2	D1	D0
read:	IV7-B	IV6-B	IV5-B	IV4-B	IV3-B	IV2-B	IV1-B	IV0-B
write:	IV7-B	IV6-B	IV5-B	IV4-B	IV3-B	IV2-B	IV1-B	IV0-B
function:	user defined interrupt vector							
reset state:	0	0	0	0	0	0	0	0

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7.12 The Address Function Register

The address function register of the PM001 is used to declare the source of the upper slot address lines from A20 to A23 for memory cards during a standard VMEbus access. The register is 4 **bits** wide and can be read back for verification. It is located at the address **$0031**. A logical one connects the according VMEbus address line to **both PCMCIA** slots. After a reset all function bits are set to zero, i.e. the address lines are sourced from the slot specific address registers ADA4 and ADB4.

AFRG register overview at address location $0031:

AFRG	D7	D6	D5	D4	D3	D2	D1	D0
read:	0	0	0	0	AFR3	AFR2	AFR1	AFR0
write:	---	---	---	---	AFR3	AFR2	AFR1	AFR0
function:	---	---	---	---	select	select	select	select
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	---	---	1	1	1	1

function	D7	D6	D5	D4	D3	D2	D1	D0
ADA4/ADB4 is slot-A20 source	---	---	---	---	---	---	---	0
ADA4/ADB4 is slot-A21 source	---	---	---	---	---	---	0	---
ADA4/ADB4 is slot-A22 source	---	---	---	---	---	0	---	---
ADA4/ADB4 is slot-A23 source	---	---	---	---	0	---	---	---
VMEA20 is slot-A20 source	---	---	---	---	---	---	---	1
VMEA21 is slot-A21 source	---	---	---	---	---	---	1	---
VMEA22 is slot-A22 source	---	---	---	---	---	1	---	---
VMEA23 is slot-A23 source	---	---	---	---	1	---	---	---

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7.13 The I/O Data Access Range

The PCMCIA I/O data access area is contained within the VMEbus short I/O range. It starts at the offset address **$0400** for slot A and reaches upto **$04FF**. Slot B uses the address range from **$0600** to **$06FF**. Within this address space, the **REG** line of both slots is in an **inactive** state. The necessary access address for each PCMCIA card must be loaded by a previous access into its 24 bit wide address register. The slot address line A0 is set to low level for both slots at any time. The addresses from A1 to A7 are directly sourced from the according VMEbus address lines. The address registers lines from A8 to A25 are used for the upper address lines. The address registers lines from A1 to A7 do not affect the I/O data access. The data bus is **16 bits wide** and the slot byte D0 to D7 is connected to the VMEbus data lines D0 to D7. The wiring for the data lines D8 to D15 is made respectively.

7.14 The I/O Register Access Range

The PCMCIA I/O register access area is also decoded within the VMEbus short I/O range. It starts at the offset address **$0500** for slot A and reaches upto **$05FF**. Slot B uses the address range from **$0700** to **$07FF**. Within this address space, the **REG** line of both slots is in an **active** state. The necessary access address for each PCMCIA card must be loaded by a previous access into its 24 bit wide address register. All other slot specific parameters are identical to the I/O data access range.

7.15 The Standard Data Access Range

The PCMCIA standard data access area for memory cards uses, if enabled, the VMEbus standard access range. The VMEbus decoding is handled via the contents of the **BSR**, located at the address offset **$0001**. The decoding range reaches from $000000 upto $F00000 in **1MByte address steps**. The VMEbus decoding size can be programmed for **1, 2, 4 or 8MByte**. After power up or a manual reset, the standard access is disabled at all. If required, the standard access can be dynamically enabled or disabled by the state of bit BSR5. The BSR is common for both PCMCIA slots.

BSR register overview at address location $0023:

BSR	D7	D6	D5	D4	D3	D2	D1	D0
read:	BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
write:	BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
function:	size	size	enable	reset	function	compare	compare	compare
reset state:	0	0	0	0	0	0	0	0
active state:	---	---	high	high	---	---	---	---

function	D7	D6	D5	D4	D3	D2	D1	D0
compare state to VMEbus address	---	---	---	---	---	A23	A22	A21
decoding size 1MByte for each slot	0	0	---	---	---	---	---	---
decoding size 2MByte for each slot	0	1	---	---	---	---	---	---
decoding size 4MByte for each slot	1	0	---	---	---	---	---	---
decoding size 8MByte for each slot	1	1	---	---	---	---	---	---
activate reset line of slot A	---	---	---	1	---	---	---	---
enable VMEbus standard access	---	---	1	---	---	---	---	---
MOD2=0: activate reset line of slot B	---	---	---	---	1	---	---	---
MOD2=1: compare state to VMEA20	---	---	---	---	A20	---	---	---

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8. The VMEbus Short I/O Access Ports

8.1 The I/O & Memory Autoincrement Access Port

The PM001 offers the use of I/O & memory cards within the address limited VMEbus short I/O access range. The complete 64MByte card address range is managed by a single access address with an autoincrement feature. A 24 bit wide address register must be previous loaded with the desired access address. **Each PCMCIA** slot uses its own address register which allows for alternate accesses between both slots. The current address register contents can be read back or modified at any time. It is automatically incremented after each access to the I/O port access address $0080 or the memory port access address $0280 for slot A and respectively $0180 or $0380 for slot B. Both address counters are limited to the next 16MByte boundary. Because there is only one address counter for each slot, any access to the given locations of the I/O or memory port will increment the access address. The address lines A24 and A25 are directly sourced from the address register and are not affected by the autoincrement function. The state of the according REG line during the port access depends on the contents of the mode register.

8.2 The I/O & Memory Fixed Address Access Port

In case a PC card should be accessed with a fixed, non autoincrementing address, the two 24 bit wide address registers will source their current contents to both PCMCIA slots without the previous described autoincrement feature at the access address $0082 or $0282 for slot A and $0182 or $0382 for slot B. The desired access address must be loaded into the ADA0-4 and the ADB0-4 address registers.

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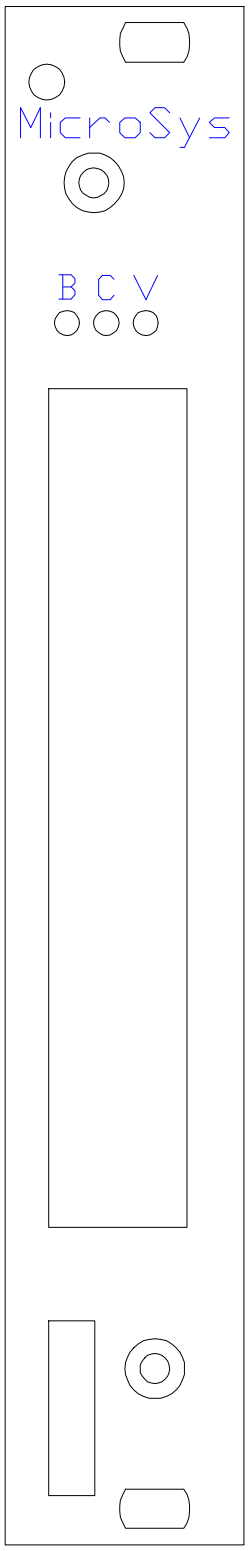
9. The Board Reset Function

During power up or power down sequences, the TL7705 activates the board reset line and holds the PM001 in a defined state. The reset line will be low for approximately **1.3sec** if the supply voltage reaches **4.65 volts**. Below that voltage, the reset line will be continuously low. The function of VMEbus reset line does not influence the onboard reset generator.

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10. Front Panel Description

10.1 Front Panel Layout



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10.2 Front Panel Leds

Led1: VP

This led indicates one or both onboard programming voltage generators for FLASH devices to be active

Led2: CD

This led is switched on if one or more out of the four card detect lines are active.

Led3: BS

This led is activated, if the PM001 is selected either in the VMEbus standard or short I/O access range

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11. The VMEbus Interrupter

The PM001 supports an interrupt generation on all **7 VMEbus interrupt levels**. The desired level can be programmed within the **ILR** at location **$0005** according to the following table. Each PCMCIA slot uses its own interrupt **vector register** located at **$0021** for slot A and **$0025** for slot B. The contents of the level register as well as of both vector registers can be read back for verification. Each interrupt source out of the four possible for each slot can be enabled or disabled via the **IER** at location **$0007**.

ILR register overview at address location $0005:

ILR	D7	D6	D5	D4	D3	D2	D1	D0
read:	IE9	IE8	0	0	0	IL3	IL2	IL1
write:	IE9	IE8	---	---	---	IL3	IL2	IL1
function:	enable	enable	non	non	non	binary coded level		
reset state:	0	0	0	0	0	0	0	0
active state:	1	1	---	---	---	---	---	---

function	D7	D6	D5	D4	D3	D2	D1	D0
IRQ enable for BVD2 on slot B	1	---	---	---	---	---	---	---
IRQ enable for BVD2 on slot A	---	1	---	---	---	---	---	---
reflect always zero	---	---	0	0	0	---	---	---
PCMCIA slot-B INPACK line	---	---	---	---	state	---	---	---
VMEbus interrupter off	---	---	---	---	---	0	0	0
VMEbus interrupter level 1	---	---	---	---	---	0	0	1
VMEbus interrupter level 2	---	---	---	---	---	0	1	0
VMEbus interrupter level 3	---	---	---	---	---	0	1	1
VMEbus interrupter level 4	---	---	---	---	---	1	0	0
VMEbus interrupter level 5	---	---	---	---	---	1	0	1
VMEbus interrupter level 6	---	---	---	---	---	1	1	0
VMEbus interrupter level 7	---	---	---	---	---	1	1	1

IVRA register overview at address location $0021:

IVRA	D7	D6	D5	D4	D3	D2	D1	D0
read:	IV7-A	IV6-A	IV5-A	IV4-A	IV3-A	IV2-A	IV1-A	IV0-A
write:	IV7-A	IV6-A	IV5-A	IV4-A	IV3-A	IV2-A	IV1-A	IV0-A
function:	user defined interrupt vector							
reset state:	0	0	0	0	0	0	0	0

IVRB register overview at address location $0023:

IVRB	D7	D6	D5	D4	D3	D2	D1	D0
read:	IV7-B	IV6-B	IV5-B	IV4-B	IV3-B	IV2-B	IV1-B	IV0-B
write:	IV7-B	IV6-B	IV5-B	IV4-B	IV3-B	IV2-B	IV1-B	IV0-B
function:	user defined interrupt vector							
reset state:	0	0	0	0	0	0	0	0

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IER register overview at address location $0007 & $0025:

IER	D7	D6	D5	D4	D3	D2	D1	D0
read at $07:	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
write at $25:	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
function:	enable	enable	enable	enable	enable	enable	enable	enable
reset state:	0	0	0	0	0	0	0	0
active state:	1	1	1	1	1	1	1	1

function	D7	D6	D5	D4	D3	D2	D1	D0
IRQ enable for BVD1 on slot B	1	---	---	---	---	---	---	---
IRQ enable for rising edge of RDY/BSY on slot B	---	1	1	---	---	---	---	---
IRQ enable for falling edge of RDY/BSY on slot B	---	1	0	---	---	---	---	---
IRQ enable for CD1/CD2 on slot B	---	---	---	1	---	---	---	---
IRQ enable for BVD1 on slot A	---	---	---	---	1	---	---	---
IRQ enable for rising edge of RDY/BSY on slot A	---	---	---	---	---	1	1	---
IRQ enable for falling edge of RDY/BSY on slot A	---	---	---	---	---	1	0	---
IRQ enable for CD1/CD2 on slot A	---	---	---	---	---	---	---	1

The described interrupt sources are either issued on a state change or level sensitive according to following table:

Interrupt Source	high to low	low to high	low active
CD1/CD2 on slot A	X	X	
BVD1 on slot A			X
BVD2 on slot A (*)			X
RDY/BSY on slot A	X	X	
CD1/CD2 on slot B	X	X	
BVD1 on slot B			X
BVD2 on slot B (*)			X
RDY/BSY on slot B	X	X	

The interrupt sequence is started by the event of one or more of the given sources. The according interrupt line of the VMEbus stays active until the level sensitive interrupt source is inactive or the according enable bit is cleared.

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12. The VMEbus Interface

The bus interface of the **PM001** is designed according to the VMEbus specification **ANSI/IEEE STD1014-1987, IEC 821 & 297**. The VMEbus connector ST1 row A, B and C contain all standard VMEbus lines, necessary for A16/A24, D8/D16 slave boards. All unused daisy chain lines are linked through, i.e. no external bypass links are necessary. The address modifier signals **AM0 to AM5** are a part of the VMEbus specifications and serve to differentiate between certain memory areas. **All** address modifier lines are **necessary** for any access to the PM001. The PM001 accepts only slave data or program accesses within the VMEbus short I/O range and the VMEbus standard access area.

The following AM-Codes are accepted by the PM001:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low H = logical high

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12.1 Pin Assignment of the VMEbus Connector ST1

Pin	Row A	Row B	Row C
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	(SYSCLK)	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	UDS*	(BR0*)	SYSRESET*
13	LDS*	(BR1*)	LWORD*
14	RW*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	not connected	A17
22	IACKOUT*	not connected	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	(-12V)	(5VSTB)	(+12V)
32	+5V	+5V	+5V

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13. The ispLSI programming port:

The 12 pin connector PP of the **PM001** is partly factory used for programming the onboard ispLSI device. This port can only be used for programming purposes with a special interface. In respect to the FM001 board, two jumper links can be installed into location **PP 9-10** and **PP 11-12**. Any other connections made to this port may cause permanent damage or not user recoverable malfunctions. The connector contains 5 volts and ground pins, which may lead to a short circuit, in case other pins than the shown are connected.

Pin assignment of connector PP:

1	3	5	7	9	11
2	4	6	8	10	12
do not make any connections				JP6	JP7



ATTENTION: DO NOT MAKE ANY CONNECTIONS TO

CONNECTOR PP 1-8 !

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14. Summary of Jumper & Switches

Size:	Name:	Default	Position:	Function:	
2x5	AA	#	1-2	VMEbus Address Decode Line A11	
			3-4	VMEbus Address Decode Line A12	
			5-6	VMEbus Address Decode Line A13	
			7-8	VMEbus Address Decode Line A14	
			9-10	VMEbus Address Decode Line A15	
2x6	PP		1-2	do NOT make any connections	
			3-4	do NOT make any connections	
			5-6	do NOT make any connections	
			7-8	do NOT make any connections	
			9-10	JP-6, FM001 compatible jumper	
			11-12	JP-7, FM001 compatible jumper	

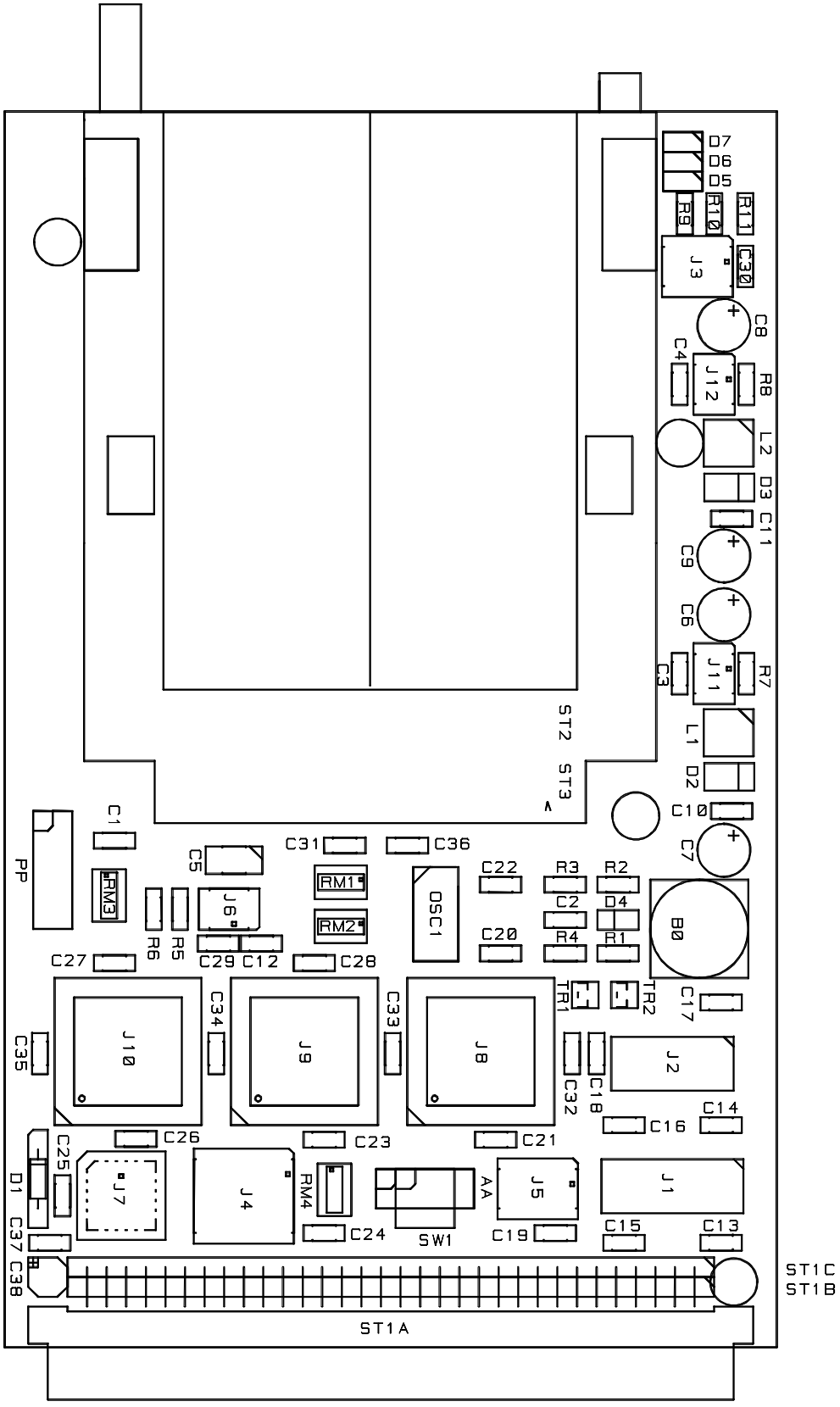
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Appendices

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Appendix A: Layout Component side



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Appendix B: Schematics

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