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MITSUBISHI

PROGRAMMABLE CONTROLLER

# MELSEC-A

User's Manual

# Computer link module type AJ71C24-S3

MITSUBISHI ELECTRIC

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# INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.



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5. SETTING TRANSMISSION CONTROL DATA
6. COMPUTER COMMUNICATION USING THE DEDICATED PROTOCOLS
7. COMMUNICATIONS IN THE NO-PROTOCOL MODE
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## 1. GENERAL DESCRIPTION

This User's Manual describes the specification, handling and transmission control protocols of the AJ71C24-S3 computer link module.

The AJ71C24-S3 computer link module has improved functions to those of the conventional AJ71C24 computer link module (AJ71C24-S3 is hereinafter referred to as "AJ71C24"). Compatibility and function comparisons between the two models are shown in Appendices 1 and 2. Be sure to read these appendices before using any existing program with the new module.

The AJ71C24 has one RS-232C port and one RS-422 port. It acts as the interface between the programmable controller CPU and external equipment (such as a computer, printer) or to the CPU of another programmable controller station. ("Programmable controller" is hereinafter referred to as "PC").

Dedicated transmission protocols 1 to 4 are used as transmission control procedures on the AJ71C24 and a no-protocol mode is also available. The user can select and set these independently for the RS-232C and RS-422 ports.
When using a dedicated transmission protocol or the no-protocol mode, data is transmitted using the codes below.

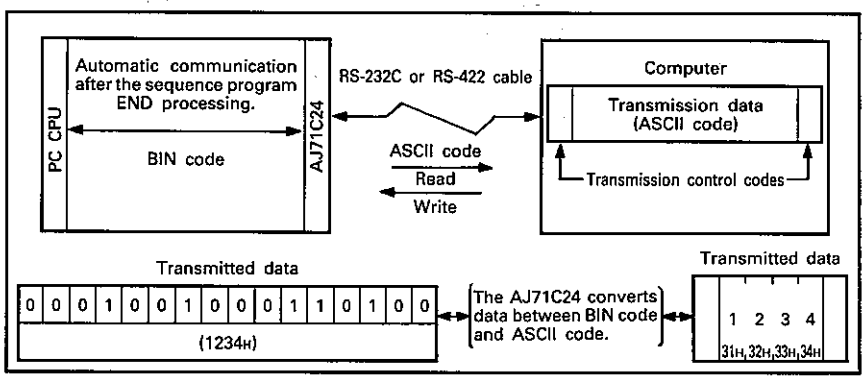



**Fig. 1.1 Data Transmission with Dedicated Protocol**

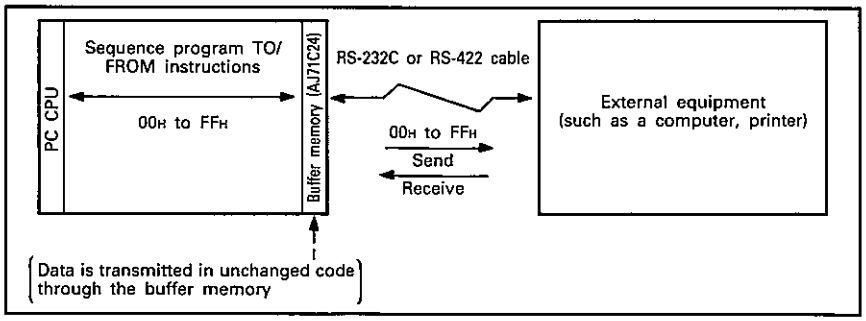



**Fig. 1.2 Data Transmission in No-Protocol Mode**

In this manual, "PC CPU" is used as a general term to cover the following PC CPU's:

| | | |
|---|---|---|
| A1NCPU(P21/R21) | A1CPU(P21/R21) | A1ECPU(P21/R21) |
| A2NCPU(P21/R21) | A2CPU(P21/R21) | A2ECPU(P21/R21) |
| A3NCPU(P21/R21) | A3CPU(P21/R21) | A3ECPU(P21/R21) |
| A3HCPU(P21/R21) | | |



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## 1.1 Features

The main features of the AJ71C24 are described below.

(1) Functions and system configuration using the dedicated protocols

(a) Read and write possible to and from all PC CPU devices
Data can be read from all PC CPU devices. This permits observation and monitoring of all operations, and the collection and analysis of data. Data can be written to all PC CPU devices. This permits production control and production directives to be carried out.

(b) The AJ71C24 can upload and download programs from PC CPU. PC CPU programs (main sequence and subsequence control programs and microcomputer programs), parameter data and comment data is read by the computer and stored. When required it can be written to the PC CPU to change the program.

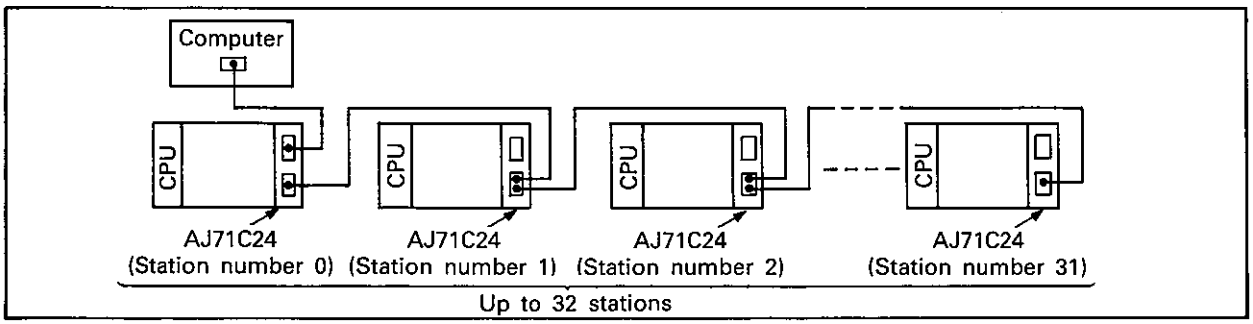
(c) Sequence programs not required for data transfer
Data communication is always initiated by the computer. It is not necessary to create and change special sequence programs in order to use the AJ71C24.

(d) Remote RUN and STOP of the PC CPU
The PC CPU can be remote-controlled by means of RUN and STOP instructions from the computer.

(e) On-demand function
This function is used when emergency data has to be sent from the PC CPU to the computer. The PC CPU sends a transmission request to the computer which is processed as an interrupt. This function is available only when a single PC is linked to a computer.

(f) The system configuration required to carry out functions (a) to (d) above can be a single computer and PC CPU (1:1) system, or any of the systems described below.

1) One computer and multiple PC CPU (1:n) system
This is a method whereby data communication is carried out between a single computer and multiple PC CPU's (up to 32 stations). In this system the station that is to communicate with the computer is specified and a request for data communication is sent. At the necessary time, data communication is carried out with the necessary PC CPU. This type of system is referred to as a "multidrop link system."

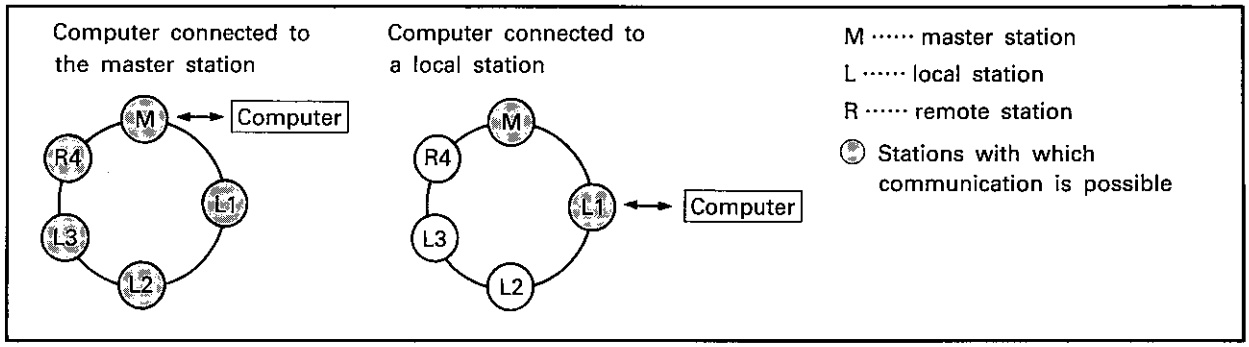





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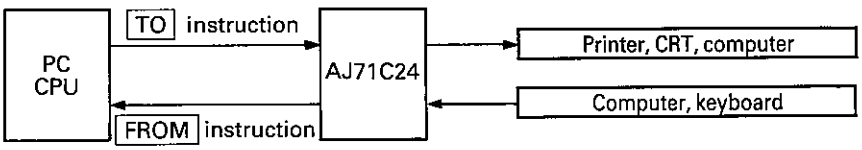
2) Link with a computer through MELSECNET
In a system connected through MELSECNET, if the system contains a PC CPU connected to the computer via the AJ71C24, data communication is possible between the computer and a PC CPU not equipped with the AJ71C24.
However, communication is not possible with A0J2CPUP23/R23 or A0J2CPUP25/R25 modules.

MELSECNET master and local stations: { communication of all data (device memory, programs) is possible }
MELSECNET remote stations: { communication only possible for data from special-function module buffer memory }




(2) Functions in the no-protocol mode

(a) Data communication can be initiated by PC CPU's
Data communication can be initiated by the computer or any PC CPU. Data can be sent from a PC CPU to an external device by using the TO instruction in the sequence program to write data to the buffer memory.
Data sent from an external device can be read by a PC CPU using the FROM instruction in the sequence program.
Taking the example of a system with a printer, CRT and keyboard terminal connected in a 1:1 ratio. Data can be output from the buffer memory to the printer on CRT display using the TO instruction from the PC CPU. Data input from the keyboard to the buffer memory can be read using a FROM instruction from the PC CPU.




(b) Selection between data receive using a completion code or fixed-length format
The user can select between using a receive-complete code or fixed-length format to determine the amount of data received, to match the specification of the external equipment (such as a computer, keyboard).

(c) Variable communication memory area
The user can allocate the user memory area to suit the purpose and application of the data transmission.



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# 2. SYSTEM CONFIGURATION

This chapter describes system configurations which may be combined with the AJ71C24.

## 2.1 Overall Configuration

Fig. 2.1 shows the overall configuration of A series system which is loaded with the AJ71C24.

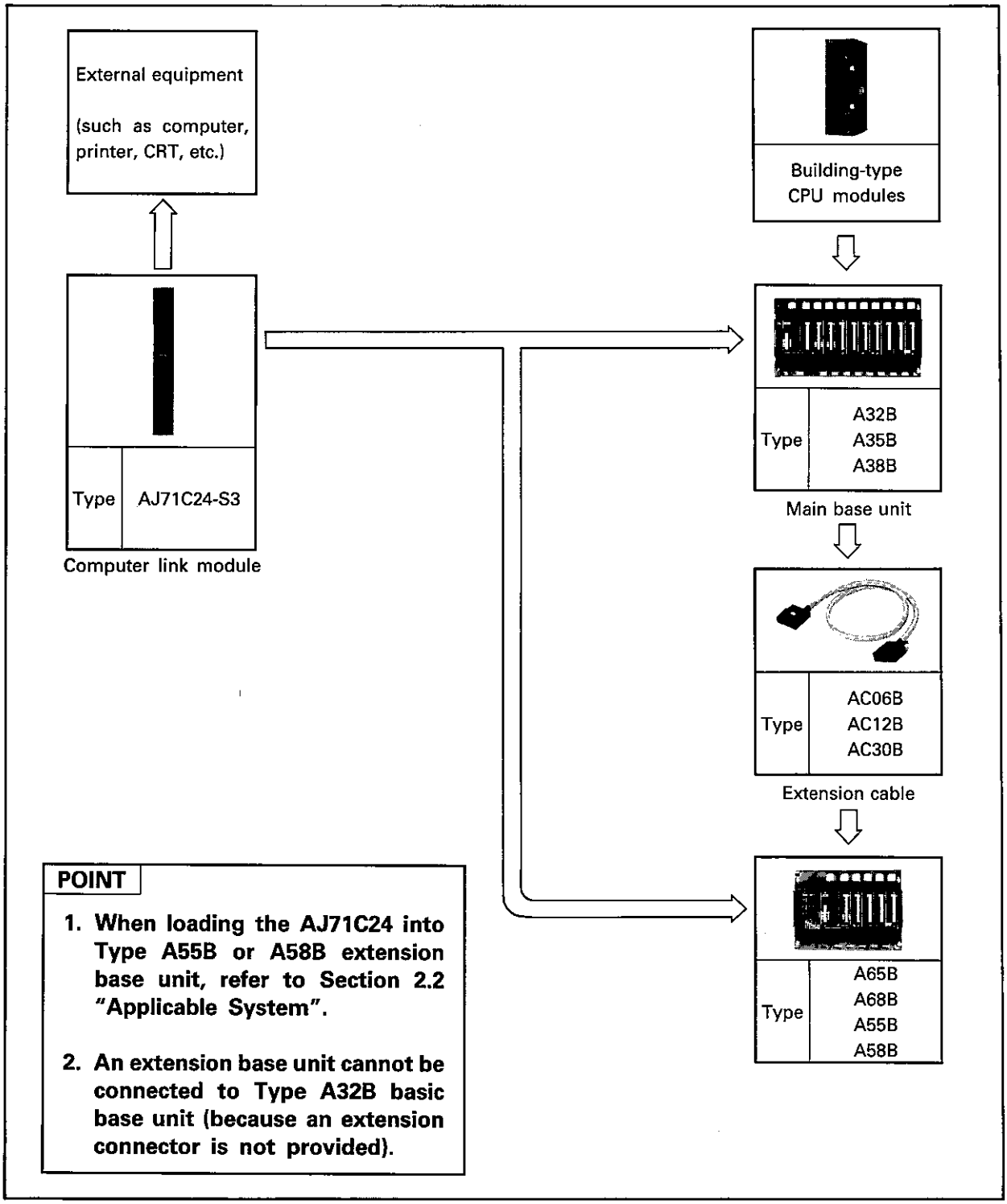



**Fig. 2.1 Overall Configuration**



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## 2.2 Applicable Systems

The AJ71C24 can be used in the systems described below only. It cannot be used in other systems.

(1) Applicable CPU modules
The AJ71C24 can be used in the following CPU modules. It cannot be used in the A0J2CPU.

| | | |
|---|---|---|
| Applicable CPU modules | A1NCPU<br>A2NCPU<br>A3NCPU<br>A3HCPU | A1(E)CPU<br>A2(E)CPU<br>A3(E)CPU |

(2) Up to two AJ71C24 modules can be used per sequencer CPU module. When the sequencer CPU module is used in combination with the following modules, up to two AJ71C24 modules can be used for each combination.
- AD51 intelligent communication module
- AJ71C22 multi-drop link system module

(3) The AJ71C24 can be inserted into any slot of a main base module or extension base module, except in the cases listed below.
(a) The power supply capacity may be insufficient to load the AJ71C24 into an extension base module with no built-in power supply (A55B or A58B). Wherever possible, avoid loading an AJ71C24 module into this type of extension base module. If it is necessary to use an AJ71C24 module in an extension base module with no built-in power supply, it is important to take the power supply capacity of the main base module and the voltage drop along the extension cables into consideration when selecting the extension cables.
(b) The AJ71C24 should not be loaded into the last slot of the A3(E)CPU extension level 7.

(4) The AJ71C24 can be loaded in the following CPU modules at master and local stations of a data link system (MELSECNET system). The AJ71C24 cannot be used in a remote I/O station.

| | | |
|---|---|---|
| Applicable CPU modules at master and local stations | A1NCPUP21/R21<br>A2NCPUP21/R21<br>A3NCPUP21/R21<br>A3HCPUP21/R21 | A1(E)CPUP21/R21<br>A2(E)CPUP21/R21<br>A3(E)CPUP21/P21 |

**POINT**

**(1) The AJ71C24 can also be loaded into the A81CPU base module (A78B). Refer to the A81CPU Users Manual for the commands available when the AJ71C24 is loaded.**
**(2) The A0J2C214 can be connected to a multi-drop link system.**



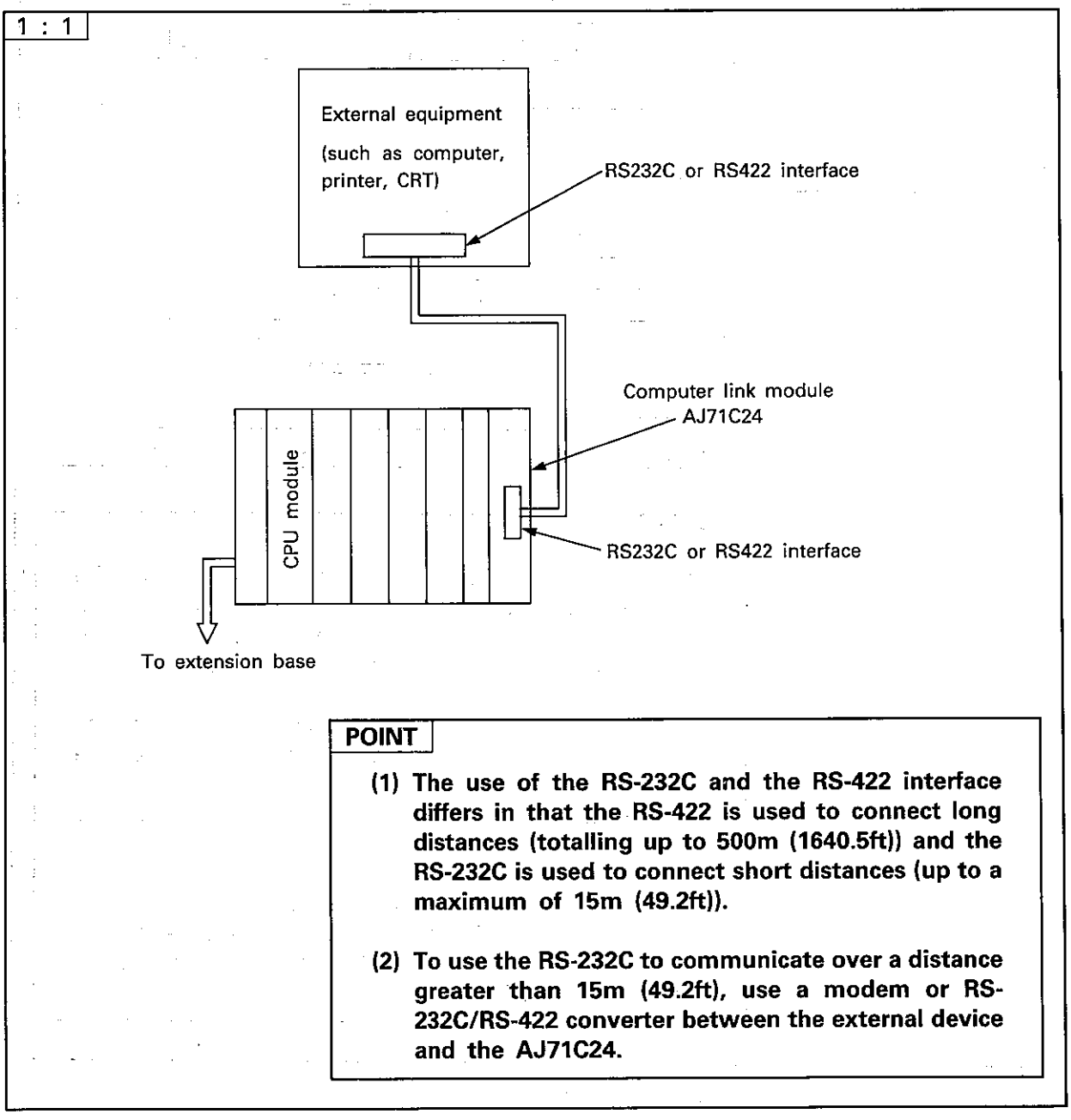
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## 2.3 System Configuration

The AJ71C24 is a link module to provide connection between external equipment (such as a computer) and PC CPU's. The system can comprise of a single external device and from 1 to 32 PC CPU stations (1:1 to 32 ratio system) or two external devices and from 1 to 32 PC CPU stations (2:1 to 32 ratio system). The connection may be made in two ways: using the RS-232C port or the RS-422 port.

### 2.3.1 1:1 ratio of external devices to PC CPU's

The system configuration for a 1:1 ratio of external devices (such as a computer) to PC CPU's is shown in Fig. 2.2 below.




**POINT**

**(1) The use of the RS-232C and the RS-422 interface differs in that the RS-422 is used to connect long distances (totalling up to 500m (1640.5ft)) and the RS-232C is used to connect short distances (up to a maximum of 15m (49.2ft)).**

**(2) To use the RS-232C to communicate over a distance greater than 15m (49.2ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.**

**Fig. 2.2 System Configuration (I)**



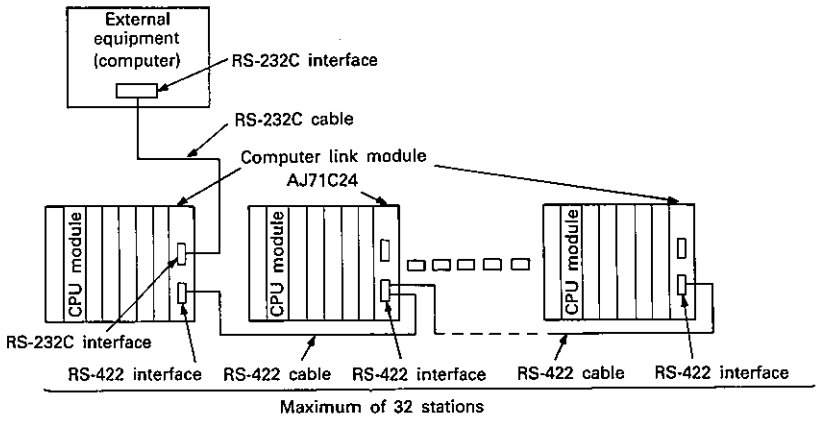
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### 2.3.2 1:n ratio of external devices to PC CPU's

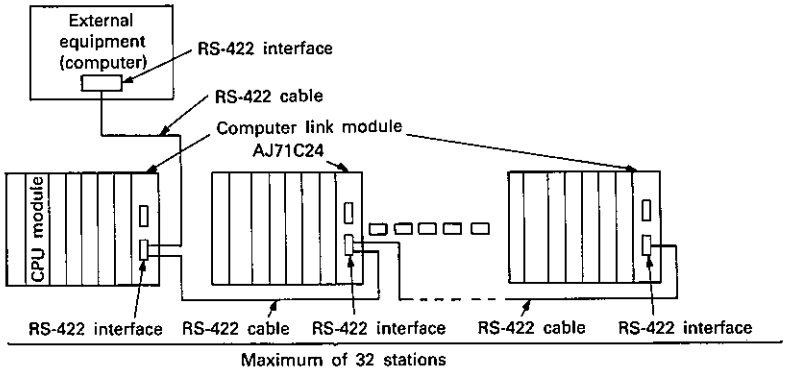
The system configuration for a 1:n ratio (where 'n' is up to 32) of external devices (such as a computer) to PC CPU's is shown in Fig. 2.3 below.

1 : n

System configuration 1




System configuration 2




**POINT**

**(1) The RS-232C interface which is not used in the multidrop link may be connected to communicate with an external device such as a computer, printer or CRT display in the no-protocol mode.**

**(2) The use of the RS-232C and the RS-422 interface differs in that the RS-422 is used to connect long distances (totalling up to 500m (1640.5ft)) and the RS-232C is used to connect short distances (up to a maximum of 15m (49.2ft)).**

**(3) To use the RS-232C to communicate over a distance greater than 15m (49.2ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.**

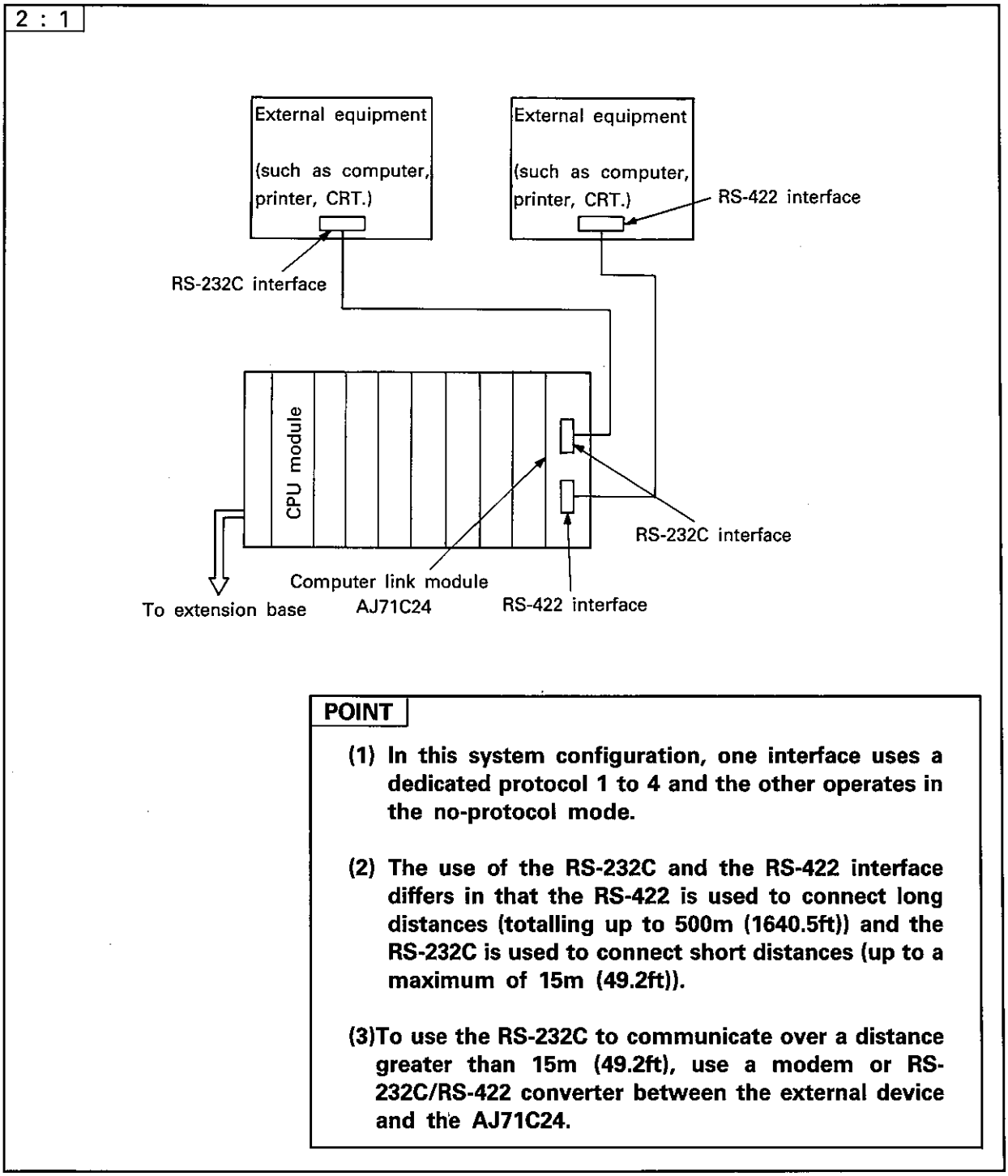
**Fig. 2.3 System Configuration (Ⅱ)**



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### 2.3.3 2:1 ratio of external devices to PC CPU's

The system configuration for a 2:1 ratio of external devices (such as a computer) to PC CPU's is shown in Fig. 2.4 below.
When this configuration is used, the mode setting switch (described in section 4.3.1) must be set in the range 1 to 8.




**POINT**

**(1) In this system configuration, one interface uses a dedicated protocol 1 to 4 and the other operates in the no-protocol mode.**

**(2) The use of the RS-232C and the RS-422 interface differs in that the RS-422 is used to connect long distances (totalling up to 500m (1640.5ft)) and the RS-232C is used to connect short distances (up to a maximum of 15m (49.2ft)).**

**(3)To use the RS-232C to communicate over a distance greater than 15m (49.2ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.**

**Fig. 2.4 System Configuration (Ⅲ)**

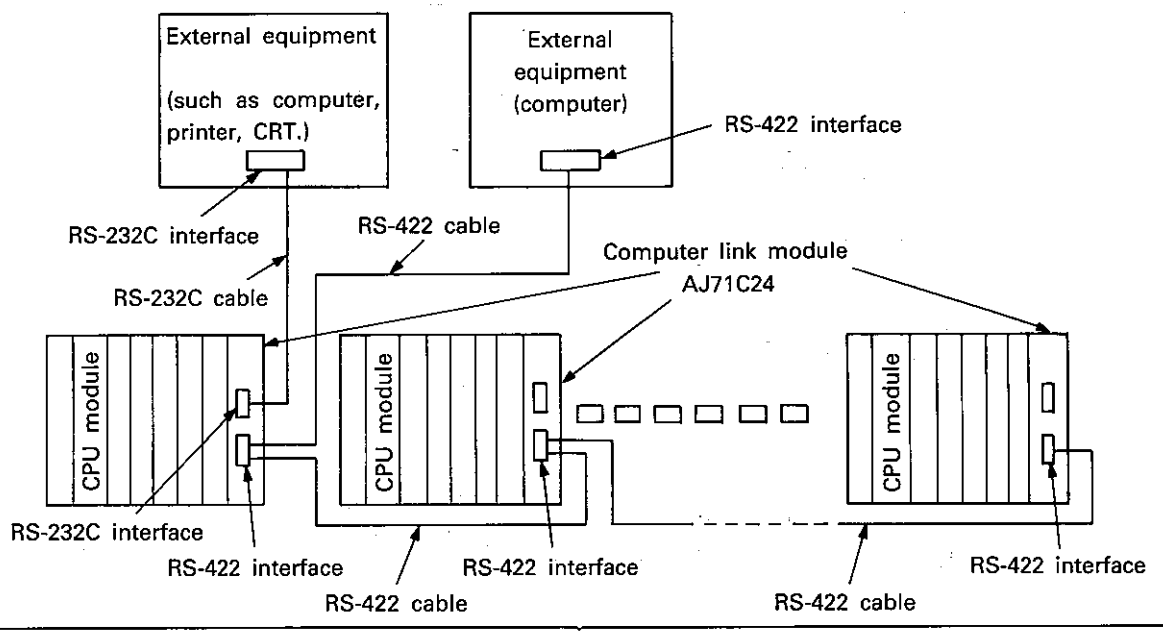


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### 2.3.4 2:1 ratio of external devices to PC CPU's

The system configuration for a 2:n ratio (where 'n' is up to 32) of external devices (such as a computer) to PC CPU's is shown in Fig. 2.5 below.
When this configuration is used, the mode setting switch (described in section 4.3.1) must be set in the range 1 to 8.

2 : 1




Maximum of 32 stations

**POINT**

**(1) The RS-232C interface which is not used in the multidrop link may be connected to communicate with an external device such as a computer, printer or CRT display in the no-protocol mode.**

**(2) The RS-232C interface which is not used in the multidrop link may be connected to communicate with and external device such as a computer, printer or CRT display in the no-protocol mode.**

**(3) To use the RS-232C to communicate over a distance greater than 15m (49.2ft), use a modem or RS-232C/RS-422 converter between the external device and the AJ71C24.**

**Fig. 2.5 System Configuration (IV)**



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### 2.3.5 Link with an external device (such as a computer) through MELSECNET

By installing the AJ71C24 to a PC CPU linked with other PC CPU's on MELSECNET, communication is possible with other PC CPU stations on MELSECNET.
However, communication is not possible with AOJ2CPUP23/R23 or AOJ2CPUP25/R25 modules.

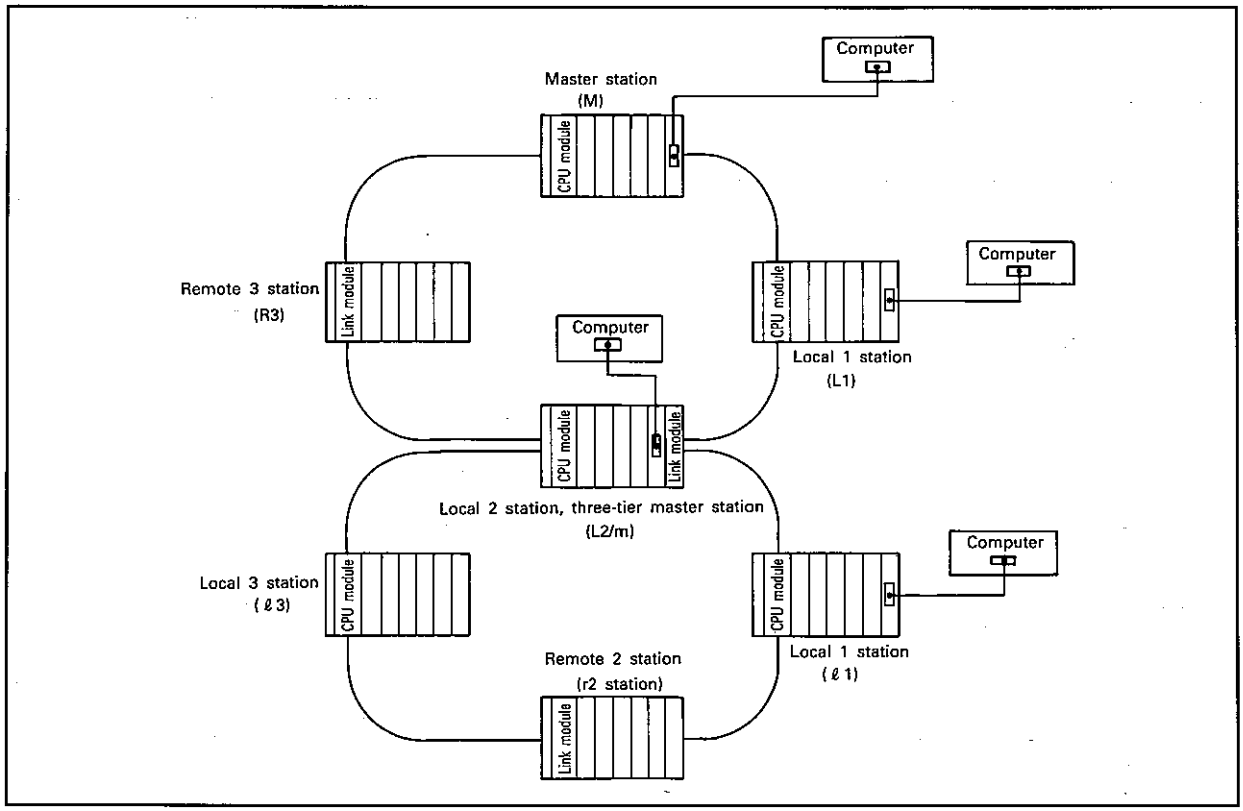



**Fig. 2.6 System Configuration (V)**

Range of PC CPU's for which communication is possible:

| (PC CPU's equipped with AJ71C24) | (MELSECNET stations for which communication is possible) |
|---|---|
| • M station (master station) ····· | (1) Host<br>(2) All second-tier local stations (L1, L2/m)<br>(3) Second-tier remote I/O stations equipped with the special-function module (R3) |
| • L stations (local stations) ····· | (1) Host<br>(2) Second-tier master station (M station) |
| • L/m station (local/third-tier master station) ····· | (1) Host<br>(2) Second-tier master station (M station)<br>(3) All third-tier local stations (ℓ1, ℓ3)<br>(4) Third-tier remote I/O stations equipped with the special-function module (r2) |
| • ℓ station (third-tier local station) ····· | (1) Host<br>(2) Third-tier master station (M station) (L2/m) |





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# 3. SPECIFICATIONS

## 3.1 General Specifications

| Item | Specifications | | | | |
|---|---|---|---|---|---|
| Operating ambient temperature | 0 to 55°C | | | | |
| Storage ambient temperature | −20 to 75°C | | | | |
| Operating ambient humidity | 10 to 90%RH, no condensation | | | | |
| Storage ambient humidity | 10 to 90%RH, no condensation | | | | |
| Vibration resistance | Conforms to *JIS C 0911 | **Frequency** | **Acceleration** | **Amplitude** | **Sweep Count** |
| | | 10 to 55Hz | —— | 0.075mm (0.003inch) | 10 times |
| | | 55 to 150Hz | 1g | —— | *(1 octave/minute) |
| Shock resistance | Conforms to JIS C 0912 (10g × 3 times in 3 directions) | | | | |
| Noise durability | By noise simulator 1500Vpp noise voltage, 1 μs noise width and 25 to 60Hz noise frequency | | | | |
| Dielectric withstand voltage | 500V AC for 1 minute across batch of DC external terminals and ground | | | | |
| Insulation resistance | 50MΩ or more with 500V DC insulation resistance tester at the same location as dielectric strength. | | | | |
| Operating ambience | No corrosive gases or dust. | | | | |
| Cooling method | Self-cooling | | | | |

**Table 3.1 General Specifications**

3

**REMARKS**

(1) One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

(2) The noise durability and dielectric withstand voltage values were obtained with the RS-232C and RS-422 interfaces unconnected.

*JIS: Japanese Industrial Standard



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## 3.2 Performance Specifications

### 3.2.1 Transmission specifications

| Item | | Specifications | |
|---|---|---|---|
| Interface | | Conforms to RS-232C. | |
| | | Conforms to RS-422. | |
| Transmission system | | Half-duplex communication system (dedicated protocol) * | |
| | | Full-duplex communication system (no protocol) | |
| Synchronous system | | Asynchronous system | |
| Transmission speed | | 300, 600, 1200, 2400, 4800, 9600, 19200 BPS (Switch selected) | |
| Data format | Start bit | 1 | |
| | Data bit | 7 or 8 | |
| | Parity bit | 1 or none | Selectable |
| | Stop bit | 1 or 2 | |
| Access cycle | | Made at END processing of sequence program. Therefore, access cycle is 1 scan time. | |
| Error detection | | Parity check present (odd/even)/absent | |
| | | Sum check present/absent | |
| DTR/DSR (ER/DR) control | | Present (RS-232C only) | |
| X ON/OFF (DC1/DC3) control | | Absent | |
| Transmission distance | | Up to 15m (49.2ft) for RS-232C | |
| | | Up to 500m (1640.5ft) for RS-422 | |
| Data format | | Start bit (1 bit) + data bit (7 bits or 8 bits) + parity bit (1 bit) + stop bit (1 bit or 2 bits) | |
| Current consumption | | 5V DC, 1.4A | |
| I/O required | | 32 points | |
| Weight | | 630g (1.39lb) | |

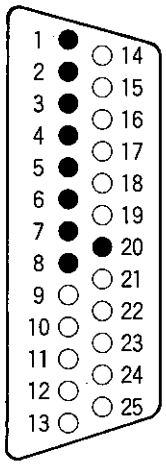
*If the on-demand function is used, only full-duplex communication is available.

**Table 3.2 Transmission Specifications**



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### 3.2.2 RS232C connector specifications




| Pin Number | Name | Signal Abbreviation | Signal Direction AJ71C24←→Computer |
|---|---|---|---|
| 1 | Frame ground | FG | ⟶ |
| 2 | Send data | SD (TXD) | ⟶ |
| 3 | Receive data | RD (RXD) | ⟵ |
| 4 | Request to send | RS (RTS) | ⟶ |
| 5 | Clear to send | CS (CTS) | ⟵ |
| 6 | Data set ready | DSR (DR) | ⟵ |
| 7 | Signal ground | SG | ⟵ |
| 8 | Receive carrier detection | CD | ⟵ |
| 20 | Data terminal ready | DTR (ER) | ⟶ |

**Fig. 3.1 RS-232C Connector Specifications**

(1) Signals are described below.

FG: Frame ground. Connect the cable screening to pin 1 of the AJ71C24. If both the computer and the AJ71C24 have a FG pin, connect the cable screening to one of the FG pins only.
If the cable screening is connected to both FG pins, the resulting noise may prevent correct data communication.

RS: Turns on when the AJ71C24 hardware is ready. Remains on during data transmission.
When the CD terminal check is not enabled, the AJ71C24 hardware ready signal is permanently ON regardless of the ON/OFF status of the CD terminal.

DSR: Data is only transmitted from the AJ71C24 when this signal is on.

CD: Transmission sequence is initialized when this signal is off. During normal operation, CD should be on.
The AJ71C24 has a function to enable or disable CD terminal checking.

DTR: Turns on when the AJ71C24 is ready to receive data.

(2) ON/OFF definitions are as follows:
ON : 5V to 15V DC
OFF: −5V to −15V DC

(3) Interface connectors
The following type of RS-232C connectors is used. Use a matching connector.
25-pin D-sub (female) screw-fixing type

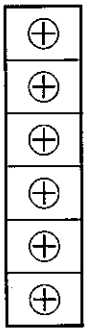


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**POINT**

**In some devices, the FG pin is connected internally to the SG pin. When connecting the AJ71C24 to such an external device, do not connect any wiring to pin 1 of the AJ71C24 RS-232C connector.**

### 3.2.3 RS422 connector specifications




| Signal Abbreviation | Signal Direction AJ71C24 ↔ Computer | Description |
|---|---|---|
| SDA | ⟶ | Send data |
| SDB | ⟶ | Send data |
| RDA | ⟵ | Receive data |
| RDB | ⟵ | Receive data |
| SG | ⟷ | Signal ground |
| FG | ⟷ | Frame ground |

**Fig. 3.2 RS422 Connector Specifications**

### 3.2.4 RS-422 cable specifications

An RS-422 cable is recommended in section 3.2.1. Other types of cables may be used instead, providing that they conform to the specifications listed in the table below.

| Item | Description |
|---|---|
| Cable type | Shielded |
| Number of pins | 3 Pairs |
| Conductor resistance (20°C) | 88.0Ω/km or less |
| Insulation resistance | 10,000MΩ·km or less |
| Dielectric strength | 500V DC, 1 minute |
| Electrostatic capacity (1kHz) | 60nF/km or less on average |
| Characteristic impedance (100kHz) | 110 ± 10Ω |

**Fig. 3.3 RS-422 Cable Specifications** (km=0.621mile)





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## 3.3 Function List

The tables below list the functions available when an external device (such as a computer) and a PC CPU are connected by means of the AJ71C24 interface.

### 3.3.1 Functions available using dedicated protocols

The functions available using a dedicated protocol 1 to 4 are listed in Table 3.3.
These functions are also available when using a 1:n station ratio multidrop link or a computer connection via MELSECNET.

| Function | | | Command: Symbol | Command: ASCII code | Description | No. of Points Processed Per Communication | PC CPU State: During STOP | PC CPU State: During RUN: SW22 ON | PC CPU State: During RUN: SW22 OFF | Reference Section |
|---|---|---|---|---|---|---|---|---|---|---|
| Device memory | Batch read | Bit units | BR | 42H, 52H | Reads bit device (such as X, Y, M) in units of 1 point. | 256 points | ○ | ○ | ○ | 6.6.2 |
| | | Word units | WR | 57H, 52H | Reads bit device (such as X, Y, M) in units of 16 points. | 32 words (512 points) | | | | 6.6.3 |
| | | | | | Reads word device (such as D, R, T, C) in units of 1 point. | 64 points | | | | |
| | Batch write | Bit units | BW | 42H, 57H | Writes bit device (such as X, Y, M) in units of 1 point. | 160 points | ○ | ○ | × | 6.6.4 |
| | | Word units | WW | 57H, 57H | Writes bit device (such as X, Y, M) in units of 16 points. | 10 words (160 points) | | | | 6.6.5 |
| | | | | | Writes word device (such as D, R, T, C) in units of 1 point. | 64 points | | | | |
| | Test (random write) | Bit units | BT | 42H, 54H | Specifies bit device (such as X, Y, M) and device number in units of 1 point at random and sets/resets the device. | 20 points | ○ | ○ | × | 6.6.6 |
| | | Word units | WT | 57H, 54H | Specifies bit device (such as X, Y, M) and device number in units of 16 points at random and sets/resets the device. | 10 words (160 points) | | | | 6.6.7 |
| | | | | | Specifies word device (such as D, R, T) and device number in units of 1 point at random and sets/resets the device. Monitor data entry | 10 points | | | | |
| | Monitor data entry | Bit units | BM | 42H, 4DH | Sets bit device to be monitored (such as X, Y, M) in units of 16 points. | 40 points *1 | ○ | ○ | ○ | 6.6.8 |
| | | Word units | WM | 57H, 4DH | Sets bit device to be monitored (such as X, Y, M) in units of 1 point. | 20 words (320 points) *1 | | | | |
| | | | | | Sets word device to be monitored (such as D, R, T, C) in units of 1 point. | 20 points | | | | |
| | Monitor | Bit units | MB | 4DH, 42H | Reads data from device for which device data entry has been made. | —— | ○ | ○ | ○ | |
| | | Word units | MN | 4DH, 4EH | | | | | | |
| Extension file register | Batch read | | ER | 45H, 52H | Reads extension file register (R) in units of 1 point. | 64 points | ○ | ○ | ○ | 6.7.3 |
| | Batch write | | EW | 45H, 57H | Writes extension file register (R) in units of 1 point. | 64 points | ○ | ○ | × | 6.7.4 |
| | Test (random write) | | ET | 45H, 54H | Specifies the extension file register (R) in units of 1 point using block or device number and makes a random write. | 10 points | ○ | ○ | × | 6.7.5 |
| | Monitor data entry | | EM | 45H, 4DH | Sets the extension file register (R) device numbers to be monitored in units of 1 point. | 20 points | ○ | ○ | ○ | 6.7.6 |
| | Monitor | | ME | 4DH, 45H | Monitors the extension file register after monitor data entry. | —— | ○ | ○ | ○ | |
| Buffer memory | Batch read | | CR | 43H, 52H | Reads data from the AJ71C24 buffer memory. | 64 words (128 bytes) | ○ | ○ | ○ | 6.8.2 |
| | Batch write | | CW | 43H, 57H | Writes data to the AJ71C2 buffer memory. | | | | | 6.8.3 |

**Table 3.3 Function List when using a Dedicated Protocol (Continue)**

*1 For other than A3HCPU, the number of points processed per communication is halved when designated device is 'X' (input)



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| Function | | | | Command: Symbol | Command: ASCII code | Description | No. of Points Processed Per communication | PC CPU State: During STOP | PC CPU State: During RUN: SW22 ON | PC CPU State: During RUN: SW22 OFF | Reference Section |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Special function module | Batch read | | | TR | 54H, 52H | Reads the contents of the special-function module buffer memory. | 64 words (128 bytes) | ○ | ○ | ○ | 6.9.3 |
| | Batch write | | | TW | 54H, 57H | Writes the contents of the special-function module buffer memory. | | ○ | ○ | × | 6.9.4 |
| Sequence Program | Batch read | Main | 1 not T/C set value | MR | 4DH, 52H | Reads main sequence programs | 64 steps | ○ | ○ | ○ | 6.11.4 |
| | | | T/C set value | | | Reads T/C set values used in main sequence programs | 64 points | | | | |
| | | Sub | 1 not T/C set value | SR | 53H, 52H | Reads subsequence programs | 64 steps | ○ | ○ | ○ | |
| | | | T/C set value | | | Reads T/C set values used in subsequence programs | 64 points | | | | |
| | Batch write | Main | 1 not T/C set value | MW | 4DH, 57H | Writes main sequence programs | 64 steps | ○ | ○*2 | × | |
| | | | T/C set value | | | Writes T/C set values used in main sequence programs | 64 points | ○ | ○ | × | |
| | | Sub | 1 not T/C set value | SW | 53H, 57H | Writes subsequence programs | 64 steps | ○ | ○*2 | × | |
| | | | T/C set value | | | Writes T/C set values used in subsequence programs | 64 points | ○ | ○ | × | |
| Micro-computer program | Batch read | Main | | UR | 55H, 52H | Reads main microcomputer programs | 128 bytes | ○ | ○ | ○ | 6.11.5 |
| | | Sub | | VR | 56H, 52H | Reads microcomputer subprograms | | | | | |
| | Batch write | Main | | UW | 55H, 57H | Writes main microcomputer programs | | ○ | ○*2 | × | |
| | | Sub | | VW | 56H, 57H | Writes microcomputer subprograms. | | | | | |
| Comments | Batch read | | | KR | 4BH, 52H | Reads comment data. | 128 bytes | ○ | ○ | ○ | 6.11.6 |
| | Batch write | | | KW | 4BH, 57H | Writes comment data. | | ○ | ○ | × | |
| Parameter | Batch read | | | PR | 50H, 52H | Reads parameters. | 128 bytes | ○ | ○ | ○ | 6.11.3 |
| | Batch write | | | PW | 50H, 57H | Writes parameters. | | ○ | × | × | |
| | Analysis request | | | PS | 50H, 53H | Causes PC CPU to acknowledge and check rewritten parameters. | —— | ○ | × | × | |
| PC CPU | Remote RUN | | | RR | 52H, 52H | Request remote run/stop of PC CPU. | —— | ○ | ○ | ○ | 6.10.2 |
| | Remote STOP | | | RS | 52H, 53H | | | | | | |
| | PC type mode | | | PC | 50H, 43H | Reads the type of the PC CPU: A1, A2, A3, A3H | | ○ | ○ | ○ | 6.10.3 |
| Global | | | | GW | 47H, 57H | Turns on and off the global signal of the AJ71C24's loaded in each PC CPU system. | 1 point | ○ | ○ | ○ | 6.12 |
| On-demand | | | | —— | | Transmission request initiated by a PC CPU. (Available in full-duplex communication with an external device in a 1:1 ratio system.) | Data length specified in the sequence program. (Max. 1760 words) | — | ○ | ○ | 6.13 |
| Loopback test | | | | TT | 54H, 54H | Echoes unchanged characters back to the computer. | 254 characters | ○ | ○ | ○ | 6.14 |

**Table 3.3 Function List when using a Dedicated Protocol**

*2 Writing during a program run may be carried out if all the following conditions are met:

1) The PC CPU is type A3, A3E, A3N or A3H
2) The program is not the currently running program (includes subprograms called by the currently running main program)
3) the PC CPU special relay is in the following status:
   (a) M9050 signal flow exchange contact·····OFF (A3CPU only)
   (b) M9051 (CHG instruction disable)·····ON



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### 3.3.2 Functions available in the no-protocol mode

(1) Functions in the no-protocol mode

| Function | Command | Description | No. of Points Processed Per Communication | PC CPU State | | | Reference Section |
|---|---|---|---|---|---|---|---|
| | | | | During STOP | During RUN | | |
| | | | | | SW22 ON | SW22 OFF | |
| Send (PC → external device) | ——— | The PC CPU uses the TO instruction to output data written to the AJ71C24 buffer memory area in unchanged code to an external device. | 127 words (default value) Can be changed with the buffer area length specification. (Refer to 5.4.4 and 5.4.5) | ○ | ○ | ○ | Section 7 |
| Receive (External device → PC) | ——— | The PC CPU uses the FROM instruction to read data in the AJ71C24 buffer memory which was sent from an external device. | | | | | |

(2) Completing receiving data with the end code or with the fixed data length

The user can select between two methods to complete the data receive when the AJ71C24 is receiving data from an external device.

(a) End code
A predetermined end code is appended to the end of the data. The AJ71C24 stops receiving data when it receives this code.
The user can select any value for the end code

(b) Fixed data length
The AJ71C24 stops receiving data after it has received the preset amount of data. The user can set the length of data that will complete the data receive to any value.



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### 3.3.3 RS-232C CD pin check enable/disable function

When communication is carried out via the RS-232C, the AJ71C24 carries out data communication according to the status of the ON signal sent from the external device to the RS-232C CD pin (receive carrier detection pin).
The AJ71C24 has a function to permit this CD pin check to be enabled or disabled.

If the CD pin check is disabled, data communication is carried out as if the CD pin were ON, regardless of the actual ON/OFF status of the pin. This function permits data communication with external devices that do not have the ability to turn ON the CD pin.
Refer to section 5.2 for details of how to set this function.

### 3.3.4 Transmission error data read function

This function permits the sequence program to read error data when an error LED's on the front panel of the module are lit and permits the sequence program to turn off error LED's which are lit.
Refer to section 5.3 for details about sequence programs.

(1) Reading transmission error data

The status of the error LED display is stored in buffer memory. The sequence program can read this data to permit the PC CPU to carry out error checking and interlocking with data communication sequence programs.

(2) Function to turn off error LED's

This function permits the sequence program to turn off error LED's which are lit without resetting the PC CPU.





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## 3.4 I/O List for Programmable Controller CPU

The I/O signals of the AJ71C24 for PC CPU are listed below. The numbers (n number) appended to X and Y are determined by the installing position of the AJ71C24 and the number of I/O modules up to the AJ71C24. (Example: Xn0 → X0 when the AJ71C24 is loaded in slot 0 of the main base unit)

(1) Input signals (AJ71C24 → PC CPU)
There are 16 input signals: Xn0 to XnF

<table>
<tr><th>Input Signal</th><th>Signal Name</th><th>Description</th><th>Reference Section</th></tr>
<tr><td>Xn0</td><td>Transmission complete</td><td>Turns on upon completion of transmission from AJ71C24 to an external device in no-protocol mode.</td><td>7.2</td></tr>
<tr><td>Xn1</td><td>Receive data read request</td><td>Turns on when AJ71C24 completes receiving data from an external device.</td><td>7.2</td></tr>
<tr><td>Xn2</td><td>Global signal</td><td>Turns on and off in response to global command signals from the computer.</td><td>6.12</td></tr>
<tr><td>Xn3</td><td>On-demand function operating</td><td>Turns on when the PC CPU executes an on-demand request.</td><td>6.13</td></tr>
<tr><td>Xn4 to Xn6</td><td>AJ71C24 state of message sequence</td><td>(1) Shows the communication status between computer and AJ71C24 using a dedicated protocol.<br>(2) Used by a sequence program to check a communication status, etc.
<table>
<tr><th>Value</th><th>Xn6</th><th>Xn5</th><th>Xn4</th><th>State of Message Sequence</th></tr>
<tr><td>0</td><td>OFF</td><td>OFF</td><td>OFF</td><td>AJ71C24 initializing after power on or not using protocol 1 to 4</td></tr>
<tr><td>1</td><td>OFF</td><td>OFF</td><td>ON</td><td>Waiting for ENQ</td></tr>
<tr><td>2</td><td>OFF</td><td>ON</td><td>OFF</td><td>Received ENQ</td></tr>
<tr><td>3</td><td>OFF</td><td>ON</td><td>ON</td><td>Received host station number</td></tr>
<tr><td>4</td><td>ON</td><td>OFF</td><td>OFF</td><td>Waiting for response from PC after receiving all data</td></tr>
<tr><td>5</td><td>ON</td><td>OFF</td><td>ON</td><td>Waiting for message</td></tr>
<tr><td>6</td><td>ON</td><td>ON</td><td>OFF</td><td>Unused</td></tr>
<tr><td>7</td><td>ON</td><td>ON</td><td>ON</td><td>Unused</td></tr>
</table></td><td>——</td></tr>
<tr><td>Xn7</td><td>AJ71C24 READY signal</td><td>(1) Turns on when AJ71C24 is ready after the power is turned on. (This requires several seconds after the power is turned on.)<br>(2) Used as the communication ready signal in the no-protocol mode.</td><td>——</td></tr>
<tr><td>Xn8 to XnC</td><td>——</td><td>Reserved</td><td>——</td></tr>
<tr><td>XnD</td><td>Watchdog timer error</td><td>(1) Turns on when a AJ71C24 watchdog timer error occurs.</td><td>8.2</td></tr>
<tr><td>XnE XnF</td><td>——</td><td>Reserved</td><td>——</td></tr>
</table>

**Table 3.4 Input Signal List**

**POINT**

**Y (Yn0 to YnF) corresponding to Xn0 to XnF may be used as internal relays.**



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(2) Output signals (PC CPU → AJ71C24)
There are 16 output signals: $Y_{(n+1)}0$ to $Y_{(n+1)}F$

| Output Signal | Signal Name | Description | Reference Section |
|---|---|---|---|
| $Y_{(n+1)}0$ | Transmission request | When this is turned on by the sequence program in the no-protocol mode, data written to the buffer memory is transmitted from the AJ71C24 to an external device. | 7.2 |
| $Y_{(n+1)}1$ | Receive data read complete | This turns on in the no-protocol mode when the PC CPU has completed reading the data received from an external device, which is stored in the AJ71C24 buffer memory. | 7.2 |
| $Y_{(n+1)}2$ | ——— | Reserved | —— |

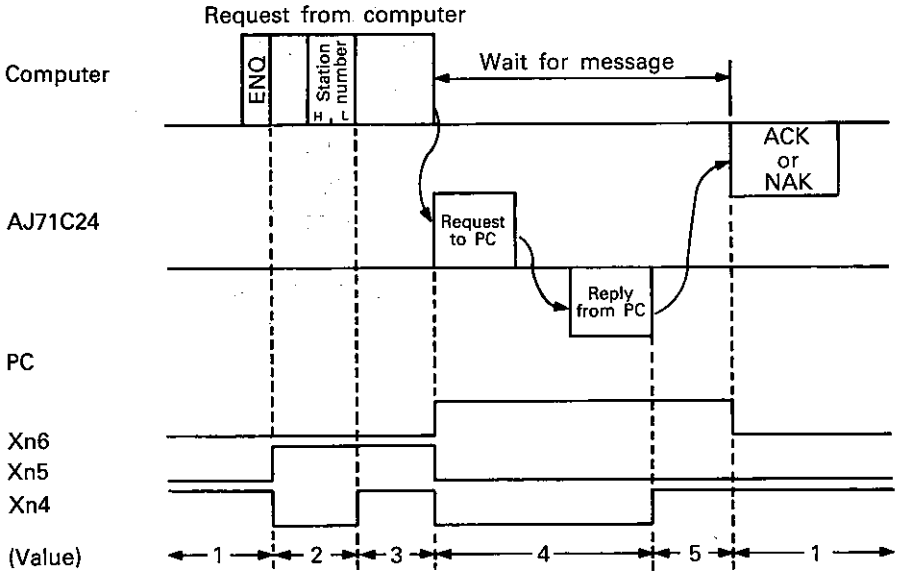
**Table 3.5 Output Signal List**

**IMPORTANT**

**$Y_{(n+1)}$ 2 to $Y_{(n+1)}$ F are reserved for system use and cannot be used by a user. The functions of the AJ71C24 cannot be guaranteed if these signals are turned on or off by a sequence program.**

**REMARKS**

Example: Use of input signals Xn4 to Xn6.






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### 3.5 Buffer Memory

The buffer memory is a memory area of the AJ71C24 used for data communication between an external device (such as a computer) and the PC CPU.

(1) Applications of the buffer memory
There are two types of buffer memory area. One area may be used freely by the user but the other area has a fixed application.

(a) User area
There are four applications of the user area, which can be categorized as follows.
1) Data receive area in no-protocol mode
This area stores data sent from an external device in the no-protocol mode.
2) No-protocol mode data transmission area
This area stores data from the PC CPU to be sent to an external device.
3) On-demand data storage area
This area stores transmission data when using the on-demand function.
4) Area when using buffer memory read/write commands
This area stores data when communication is made using the protocol 1 to 4 buffer memory read/write commands (CR, CW).

(b) Special-application area
The applications of this memory area are fixed. It is used to determine data communication format and to change the allocation of the memory area for section (a) above.
When the power is turned on or the PC CPU is reset, default values are written to this special-application area. It is possible to change the default values to suit the purpose and application of data transmission and the specification of the external device.



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(2) Allocation of buffer memory

The buffer memory comprises of 16-bit addresses. The buffer memory has no battery back-up.

The buffer memory address names and values are listed for each address in the table below.

| Address | Buffer memory address names | | Default value | Reference section |
|---|---|---|---|---|
| 0H<br>1H<br>to<br>7FH<br>80H<br>81H<br>to<br>FFH | User area (256 words) | Default assignment: Area for amount of data transmitted in no-protocol mode<br>No-protocol mode transmission buffer memory area<br>Area for amount of data received in no-protocol mode<br>No-protocol mode receive buffer memory area | 0 | |
| 100H | Area to specify receive-end code in no-protocol mode | | 0D0AH (CR, LF) | 5.4.1 |
| 101H | Error LED display area | | 0 | 5.3.1 |
| 102H | Error LED extinguish request area | | 0 | 5.3.2 |
| 103H | Area to specify word or byte units in no-protocol mode | | 0 (words) | 5.4.3 |
| 104H | Area to specify head address of transmission buffer memory for no-protocol mode | | 0 | 5.4.4 |
| 105H | Area to specify length of transmission buffer memory for no-protocol mode | | 80H | 5.4.4 |
| 106H | Area to specify head address of receive buffer memory for no-protocol mode | | 80H | 5.4.5 |
| 107H | Area to specify length of receive buffer memory for no-protocol mode | | 80H | 5.4.5 |
| 108H | Area to specify amount of data to complete receive in no-protocol mode | | 127 (words) | 5.4.2 |
| 109H | Area to specify head address of on-demand buffer memory | | 0 | 6.13 |
| 10AH | Area to specify length of on-demand buffer memory | | 0 | 6.13 |
| 10BH | Area to specify RS-232C CD pin check | | 0 (check CD pin) | 5.2 |
| 10CH | Storage area for on-demand errors | | 0 | 6.13 |
| 10DH | Receive data clear request area for no-protocol mode | | 0 | 7.4 |
| 10EH<br>to<br>11FH | System area (reserved) | | ——— | |
| 120H<br>to<br>7FFH | User area (1760 words) | | 0 | |

**Table 3.6 Buffer Memory Table**

**IMPORTANT**

**Buffer memory addresses 10EH to 11FH are reserved for system use. The user should not write data to this area as this will prevent correct operation of the AJ71C24.**

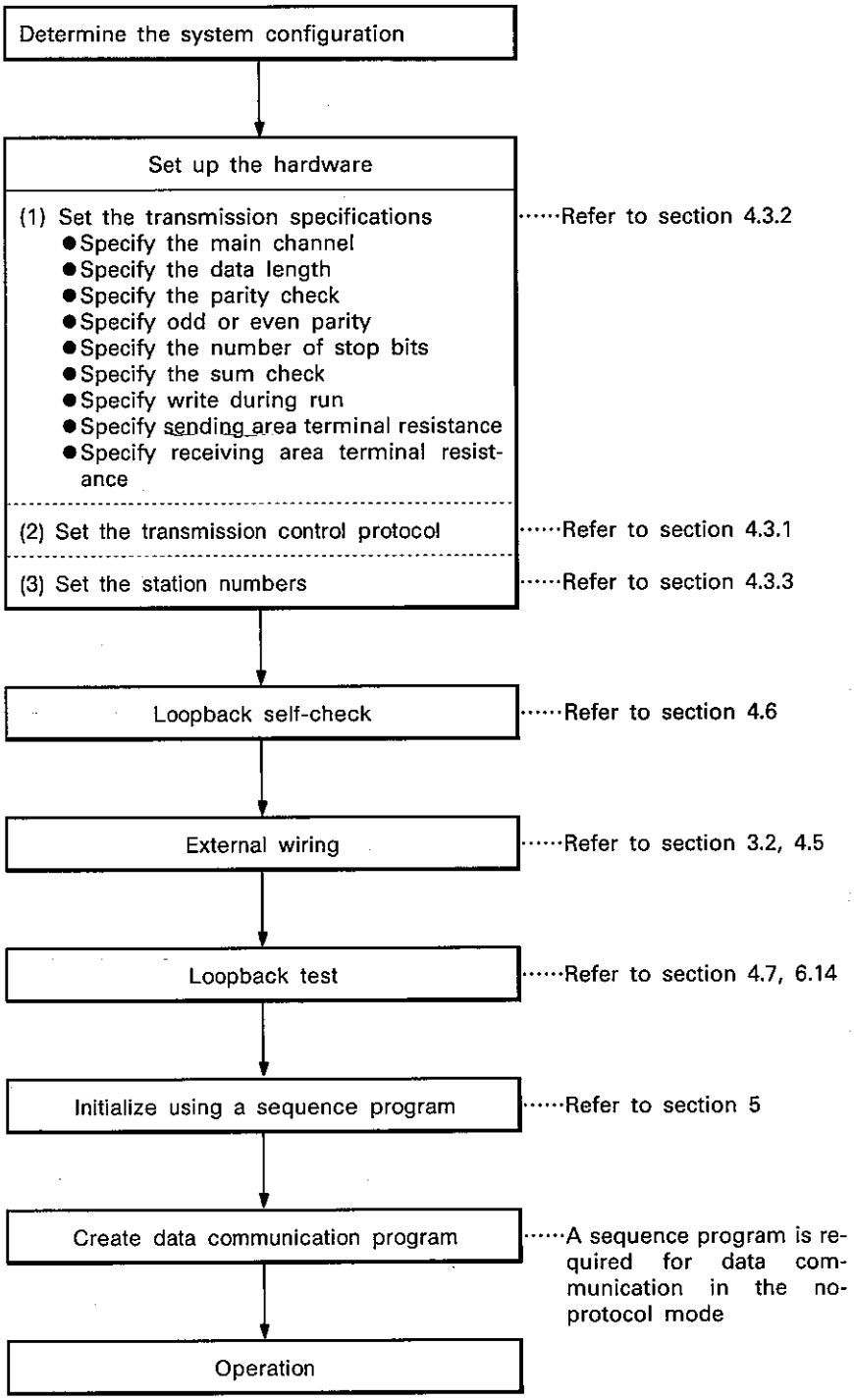


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# 4. SETTINGS AND PROCEDURES BEFORE OPERATION

## 4.1 Settings and Procedures before Operation

The settings and procedures which have to be carried out before a system using the AJ71C24 can be started are described below.

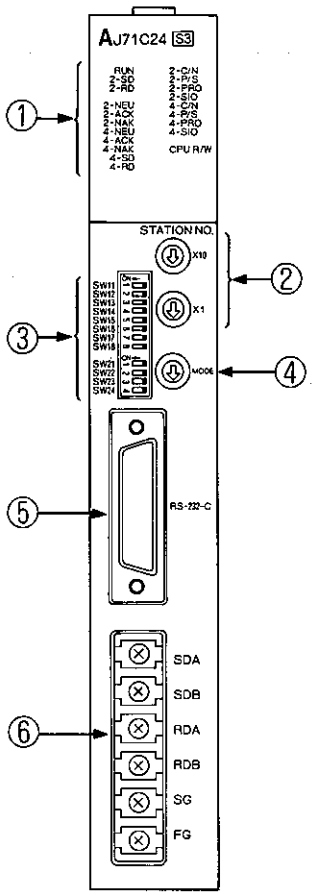





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## 4.2 Nomenclature

### 4.2.1 Nomenclature




| No. | Name | Description |
|---|---|---|
| ① | Indicator LEDs | Display the operating status, computer communication underway and alarms.<br>The meaning of an LED turning on or off differs according to the LED. |
| ② | Station number setting switches | Switch to set the station number in a 1:n ratio computer link system<br>The station number may be set to any value which does not duplicate another station number.<br>Setting range 0 to 31. (Factory-set to 0.) |
| ③ | Transmission specification setting switches | Used to select RS-422/RS-232C, data bit, parity presence/absence, stop bit, sum check, etc. |
| ④ | Mode setting switch | Switch for selecting transmission control protocol format and RS-422/RS-232C control protocol. (Factory-set to 0.) |
| ⑤ | RS-232C connector | RS-232C connector for connecting AJ71C24 with computer. |
| ⑥ | RS-422 terminal block | RS-422 terminal block connectors for connecting AJ71C24 with computer or another AJ71C24.<br>Terminal block screws are M4. |

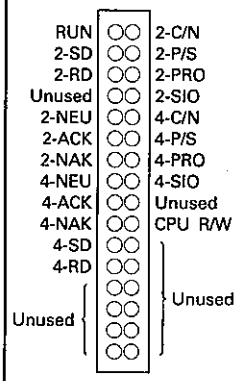






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### 4.2.2 LED signals and displays

| LED Area Details | LED No. | LED | Meaning of LED Display | LED ON | LED OFF | Initial State of LED |
|---|---|---|---|---|---|---|
|  | 0 | RUN | Normal run display | Normal | Error | ON |
| | 1 | 2-SD | RS-232C transmission data level | Flickers during data sending | | OFF |
| | 2 | 2-RD | RS-232C received data level | Flickers during data receiving | | OFF |
| | 4 | 2-NEU | RS-232C's neutral | Transmission sequence initial state (waiting for ENQ) | ENQ received | ON |
| | 5 | 2-ACK | RS-232C's ACK | After sending ACK | After sending NAK | OFF |
| | 6 | 2-NAK | RS-232C's NAK | After sending NAK | After sending ACK | OFF |
| | 7 | 4-NEU | RS-422's neutral | Transmission sequence initial state (waiting for ENQ) | ENQ received | ON |
| | 8 | 4-ACK | RS-422's ACK | After sending ACK | After sending NAK | OFF |
| | 9 | 4-NAK | RS-422's NAK | After sending NAK | After sending ACK | OFF |
| | 10 | 4-SD | RS-422 transmission data level | Flashes during data transmission | | OFF |
| | 11 | 4-RD | RS-422 received data level | Flashes during data receive | | OFF |
| | 16 | 2-C/N | Result of RS-232C and PC CPU communication | Refer to (4) below | Normal | OFF |
| | 17 | 2-P/S | RS-422 parity/sum check | Parity/sum check error | Normal | OFF |
| | 18 | 2-PRO | RS-232C protocol | Communication protocol error | Normal | OFF |
| | 19 | 2-SIO | RS-232C SIO | Overrun, framing error | Normal | OFF |
| | 20 | 4-C/N | Result of RS-232C and PC CPU communication | Refer to (4) below | Normal | OFF |
| | 21 | 4-P/S | RS-422 parity/sum check | Parity/sum check error | Normal | OFF |
| | 22 | 4-PRO | RS-422 protocol | Communications protocol error | Normal | OFF |
| | 23 | 4-SIO | RS-422 SIO | Overrun, framing error | Normal | OFF |
| | 25 | CPU R/W | Communication with PC | Flickers during communication with PC (On at no communication) | | ON |



(1) The LED's 2-C/N - 4-SIO (LED Nos. 16 - 23) above light when an error occurs.
The ON/OFF statuses of the LED Nos. 16 - 23 are stored in the buffer memory at address $101_H$. The statuses can be read using the PC CPU FROM instruction to permit checking by a sequence program.

(2) After any LED's 2-C/N - 4-SIO (LED Nos. 16 - 23) have lit, they remain lit even if the cause of the error is eliminated.
It is necessary to send an extinguish request to address $102_H$ of the buffer memory using the PC CPU TO instruction to turn off the LED's.

(3) The LED's RUN - 4-RD (LED Nos. 0 - 11) and CPUR/W (LED No. 25) above light corresponding to the relevant status.

(4) The LED's 2-C/N and 4-C/N (LED No. 16 and No. 20) above light in the following circumstances.
(a) When the AJ71C24 attempts to make an illegal access while the PC CPU is running (a write during program execution, for example).
(b) During abnormal PC CPU access.

(5) The "initial state" column indicates the status at power-on or CPU reset.



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## 4.3 Settings

This section describes the setting method and explains the settings of the transmission control protocol and communication specifications (data length, sum check, etc.).
After changing the settings, turn the PC CPU power supply off and back on, or reset the PC CPU.

### 4.3.1 Setting a protocol or the no-protocol mode

(1) The method of setting the transmission control protocol and the meaning of the switch settings are described in the table below.

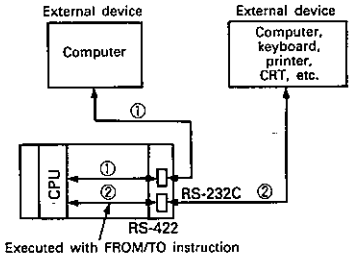
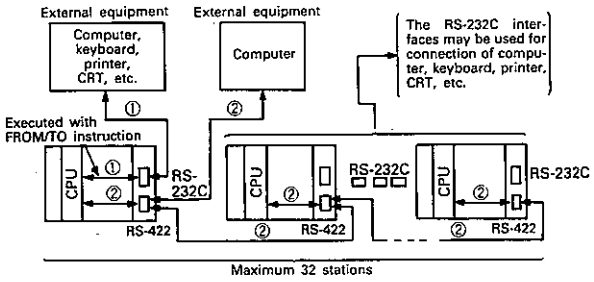
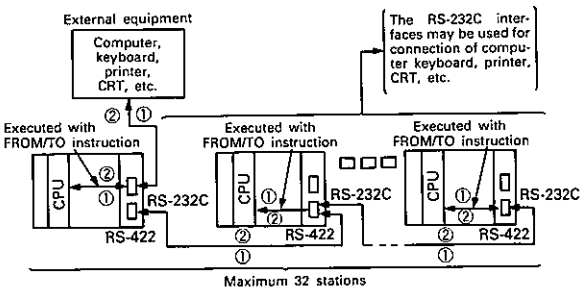
| Mode Setting Switch | Mode Setting Switch Number | Setting | | Remarks |
|---|---|---|---|---|
| | | RS-232C | RS-422 | |
|  MODE | 0 | Unused | | For connection of computers to RS-232C and RS-422 individually or for connection of a printer to the no protocol interface. Both interfaces work independently. |
| | 1 | Format 1 protocol | No protocol | |
| | 2 | Format 2 protocol | No protocol | |
| | 3 | Format 3 protocol | No protocol | |
| | 4 | Format 4 protocol | No protocol | |
| | 5 | No protocol | Format 1 protocol | |
| | 6 | No protocol | Format 2 protocol | |
| | 7 | No protocol | Format 3 protocol | |
| | 8 | No protocol | Format 4 protocol | |
| | 9 | No protocol ←→ | No protocol | Used to write data sent by computer to all stations. |
| | A | Format 1 protocol ←→ | Format 1 protocol | Mode used for computer link of 1 : n stations. RS-232C and RS-422 operate jointly. |
| | B | Format 2 protocol ←→ | Format 2 protocol | |
| | C | Format 3 protocol ←→ | Format 3 protocol | |
| | D | Format 4 protocol ←→ | Format 4 protocol | |
| | E | Unused | | |
| | F | For module test | | RS-232C and RS-422 operate independently. |

The RS-232C and RS-422 transmission specification protocols are identical.



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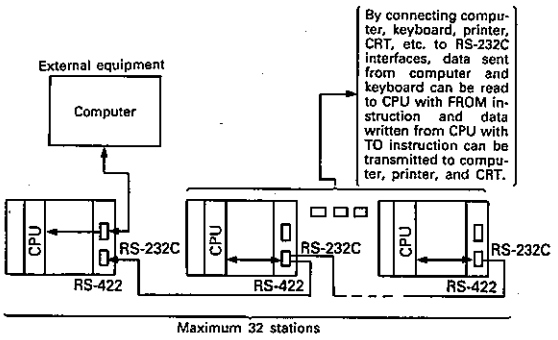
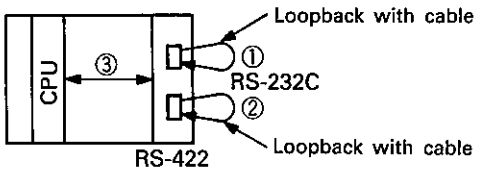
(2) System configurations for control classified by setting modes
This section describes usable system configurations according to the positions of mode setting switch.

| Mode Setting Switch | | Control | System Configuration Example |
|---|---|---|---|
| Station connected to external device | Other stations | | |
| Mode setting switch 1 to 4<br><br>(RS-232C:<br>Format 1 to 4<br>RS-422:<br>No protocol) | ——— | 1) Computer reads/writes data from/to PC CPU.<br>2) Data sent from computer or keyboard to AJ71C24 is read by PC CPU with FROM instruction. Data written from PC CPU to AJ71C24 with TO instruction is transmitted to computer, printer, or CRT. |  |
| Mode setting switch 5 to 8<br><br>(RS-232C:<br>No protocol<br>RS-422:<br>Format 1 to 4) | Mode setting switch 5 to 8<br><br>(RS-232C:<br>No protocol<br>RS-422:<br>Format 1 to 4) | 1) Data sent from computer or keyboard to AJ71C24 is read by PC CPU with FROM instruction. Data written from PC CPU to AJ71C24 with TO instruction is transmitted to computer, printer, or CRT.<br>2) Computer reads/writes data from/to PC CPU. |  |
| Mode setting switch 9<br><br>(RS-232C:<br>Format 1 to 4<br>RS-422:<br>No protocol) | Mode setting switch 1 to 4<br><br>(RS-232C:<br>Format 1 to 4<br>RS-422:<br>No protocol) | 1) Data sent from computer or keyboard to AJ71C24 is read by PC CPU with FROM instruction.<br>2) Data written from PC CPU to AJ71C24 with TO instruction is transmitted to computer, printer, or CRT. |  |



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| Mode Setting Switch | | Control | System Configuration Example |
|---|---|---|---|
| Station connected to external device | Other stations | | |
| Mode setting switch A to D<br><br>(RS-232C:<br>Format 1 to 4<br>RS-422:<br>Format 1 to 4) | Mode setting switch 5 to 8<br><br>(RS-232C:<br>No protocol<br>RS-422:<br>Format 1 to 4) | Computer reads/write data from/to PC CPU at one of 32 stations. |  |
| Mode setting switch F (Unit test) | ——— | 1) Checks RS-232C.<br>2) Checks RS-422.<br>3) Checks communication between AJ71C24 and PC CPU. |  |

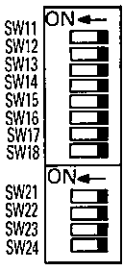
**REMARKS**

Since 2 AJ71C24s may be loaded into each base, combinations of the above control configurations can be built up.



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### 4.3.2 Setting of transmission specifications

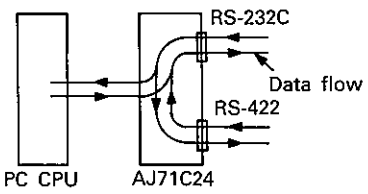
| Setting of Switches | Setting Switches | Setting Item | Position of Setting Switch ON | Position of Setting Switch OFF | Remarks |
|---|---|---|---|---|---|
|  | SW11 | Main channel setting | RS-422 | RS-232C | Valid for modes 9 to D |
| | SW12 | Data length | 8 bits | 7 bits | |
| | SW13 SW14 SW15 | Transmission speed setting | Baud rate: 300 / 600 / 1200 / 2400 / 4800 / 9600 / 19200 / Unused<br>SW13: OFF / ON / OFF / ON / OFF / ON / OFF / ON<br>SW14: OFF / OFF / ON / ON / OFF / OFF / ON / ON<br>SW15: OFF / OFF / OFF / OFF / ON / ON / ON / ON | | |
| | SW16 | Parity check | Yes | No | |
| | SW17 | Parity setting | Even | Odd | Valid only when parity check on is selected |
| | SW18 | Stop bit | 2 bits | 1 bit | |
| | SW21 | Sum check | Yes | No | |
| | SW22 | Write during run | Allowed | Disallowed | |
| | SW23 | Sending area terminal resistance | Present | Absent | |
| | SW24 | Receiving area terminal resistance | Present | Absent | |

**REMARKS**

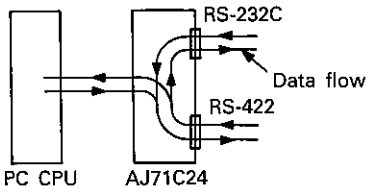
(a) The main channel in the above table refers to the interface to which the computer is connected (unless in no protocol mode). The main channel setting is valid only for modes 9 to D.
In other modes, the setting switch may be in ON or OFF position.

(b) Do not set the "unused" baud rate setting (SW13, 14, and 15 ON).
If these switches are set, the RUN indicator LED (LED No. 0) is turned off and operation is not possible.

(c) Setting the main channel defines data flow as shown below:
Data received by the main channel is automatically sent from the sub channel.
Data received by the sub channel is automatically sent to the main channel.
If data received by the main channel is process commands for the host PC CPU, the commands are processed via the main channel and host PC CPU.



Main channel RS-232C



Main channel RS-422



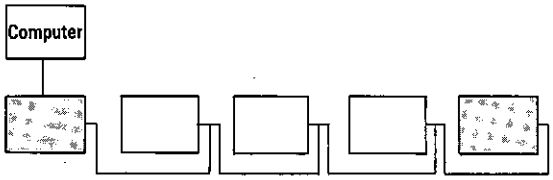
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**POINT**

**In multidrop systems, set terminal resistance "present" at end stations and "absent" for others.**

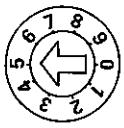
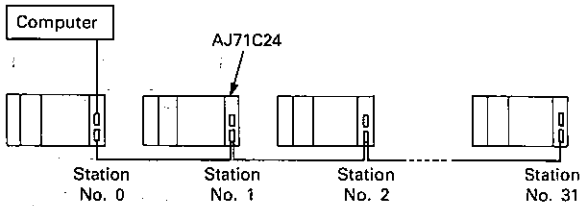
**Example: If the computer is connected to the AJ71C24 through the RS-232C**




**, with terminal resistance. (Set SW23 and 24 to ON position.)**
**, without terminal resistance. (Set SW23 and 24 to OFF position.)**

### 4.3.3 Station number setting

The station number is set on each AJ71C24 so that the computer knows which AJ71C24 to access in a 1:n ratio computer link system.

| Station Number Setting Switch | Description |
|---|---|
|  X10<br> X1 | (1) Set the station number in the range 0 to 31. (Never set a station number to more than 32.)<br>(2) Set the × 10 switch to the number of tens in the station number.<br>(3) Set the × 1 switch to the number of units in the station number.<br>(4) The station number may be set to any value which does not duplicate another station number. It is not necessary to consider the order of connection when viewed from the computer. Station numbers do not have to be sequential and may be skipped.<br>(5) If the switches are set as shown on the left, the station number is 25.<br> |



**POINT**

**Take care not to set a station number which duplicates another station number as this leads to destruction of transmission data and precludes correct data communication.**



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## 4.4 Loading and Installation

### 4.4.1 Handling instructions

(1) Protect the AJ71C24 and its terminal block impact.

(2) Do not touch or remove the printed circuit board from the case.

(3) Do not allow metal particles or wire offcuts to enter the AJ71C24.

(4) Tighten the module mounting and terminal screws as specified below.

| Screw | Tightening Torque kg·cm (lb·inch) |
|---|---|
| RS-422 terminal block installation screws (M4) | 8 (6.93) to 14 (12.13) |
| Module mounting screws (optional) (M4) | 8 (6.93) to 12 (10.39) |

(5) To load the AJ71C24 onto the base, press the AJ71C24 against the base so that the latch is securely locked. To unload the AJ71C24, push the latch, and after the latch is disengaged from the base, pull the AJ71C24 toward you.

### 4.4.2 Installation environment

Never install the System in the following environments:

(1) Locations where ambient temperature is outside the range 0 to 55°C.

(2) Locations where ambient humidity is outside the range of 10 and 90%RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations where there are corrosive gasses and combustible gasses.

(5) Locations where there is a high level of conductive powder such as dust and iron filings, oil mist, salt, and organic solvent.

(6) Locations exposed to the direct rays of the sun.

(7) Locations where strong power and magnetic fields are generated.

(8) Locations where vibration and shock are directly transmitted to the main unit.



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## 4.5 External Wiring

### 4.5.1 Precautions when carrying out wiring

External wiring which is resistant to external noise effects is a prerequisite for reliable AJ71C24 operation to permit full use of all available functions.
Necessary precautions when carrying out external wiring of the AJ71C24 are listed below.

(1) Keep main circuit wiring, high-voltage wiring and other load-carrying wiring outside the PC separate from AJ71C24 wiring and never bundle them together. This is to prevent noise and surge-induction effects.
AJ71C24 external wiring should be at least 100 mm (in.) away from other wiring.
(2) Ground the shield of shielded wires and cables at one point only.
(3) The RS-422 terminal has M4 screw connectors. Fasten suitable-sized crimped terminals to the ends of the cables before connecting the cables to the terminals.

### 4.5.2 Connecting the RS-232C connectors

Standard examples of connections to an RS-232C connector is shown in the diagram below.

(1) Connection to a device which can turn the CD pin ON

| AJ71C24 End | | Cable Connection and Signal Direction | Computer End | |
|---|---|---|---|---|
| Signal name | Pin number | | Pin number | Signal name |
| FG | 1 | | 1 | FG |
| SD (TXD) | 2 | | 2 | SD (TXD) |
| RD (RXD) | 3 | | 3 | RD (RXD) |
| RS | 4 | | 4 | RS |
| CS (CTS) | 5 | | 5 | CS (CTS) |
| DSR (DR) | 6 | | 6 | DSR (DR) |
| SG | 7 | | 7 | SG |
| CD | 8 | | 8 | CD |
| DTR (ER) | 20 | | 20 | DTR (ER) |

(2) Connection to a device which cannot turn the CD pin On
(a) When wired as in step (1) above, disable the RS-232C CD pin check.
(b) If the RS-232C CD pin check function is enabled, wire the connectors as shown below.

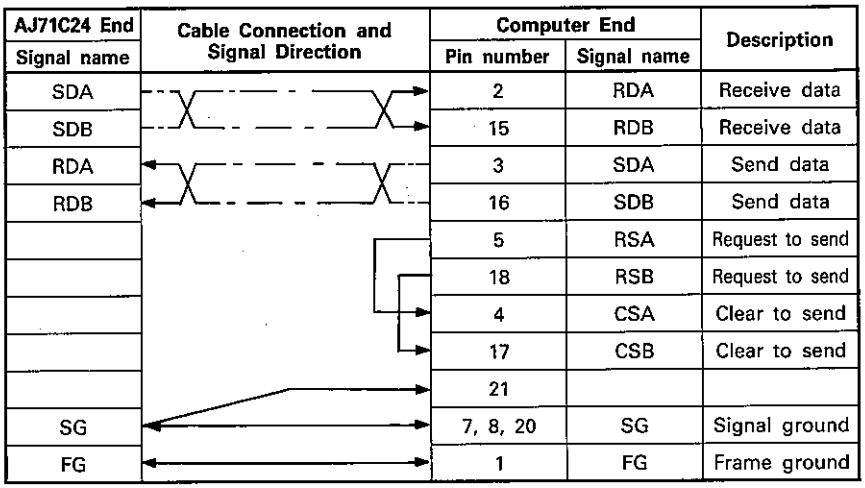
| AJ71C24 End | | Cable Connection and Signal Direction | Computer End | |
|---|---|---|---|---|
| Signal name | Pin number | | Pin number | Signal name |
| FG | 1 | | 1 | FG |
| SD (TXD) | 2 | | 2 | SD (TXD) |
| RD (RXD) | 3 | | 3 | RD (RXD) |
| RS | 4 | | 4 | RS |
| CS (CTS) | 5 | | 5 | CS (CTS) |
| DSR (DR) | 6 | | 6 | DSR (DR) |
| SG | 7 | | 7 | SG |
| CD | 8 | | 8 | CD |
| DTR (ER) | 20 | | 20 | DTR (ER) |



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### 4.5.3 Connecting the RS-422 connectors

Standard examples of connections to an RS-422 connector is shown in the diagram below.



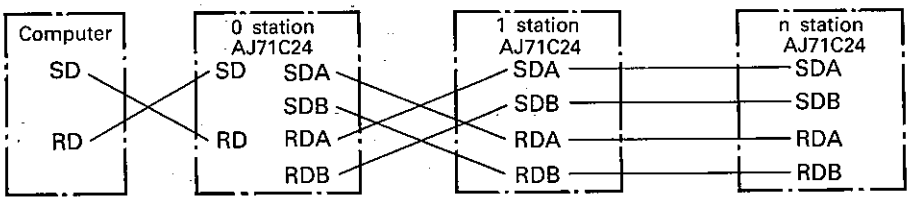
| AJ71C24 End Signal name | Cable Connection and Signal Direction | Computer End Pin number | Computer End Signal name | Description |
|---|---|---|---|---|
| SDA | | 2 | RDA | Receive data |
| SDB | | 15 | RDB | Receive data |
| RDA | | 3 | SDA | Send data |
| RDB | | 16 | SDB | Send data |
| | | 5 | RSA | Request to send |
| | | 18 | RSB | Request to send |
| | | 4 | CSA | Clear to send |
| | | 17 | CSB | Clear to send |
| | | 21 | | |
| SG | | 7, 8, 20 | SG | Signal ground |
| FG | | 1 | FG | Frame ground |

*Connect pin 21 if required by the specification of the external device.

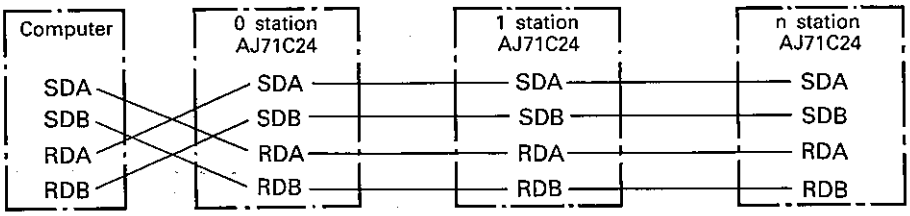
### 4.5.4 Connecting a multidrop link

Methods of connecting a computer and PC CPU's in a 1:n station ratio multidrop link are shown in the diagram below.

(1) The computer and the 0 station PC CPU are connected through the RS-232C port:




(2) The computer and the 0 station PC CPU are connected through the RS-422 port:






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## 4.6 Loopback Self-Check

The loopback self-check function is used when the AJ71C24 is not connected to the computer to check that the AJ71C24 module is operating normally. This function is selected by setting the mode setting switch to "F".

### 4.6.1 Procedure to carry out the loopback self-check

The procedure to carry out the loopback self-check is listed below.

Step 1 Connect the cable

Connect cables to the RS-232C and RS-422 connectors as shown below.

**RS-232C Cable Connections**

| AJ71C24 End | | Cable Connections |
|---|---|---|
| Signal name | Pin number | |
| FG | 1 | |
| SD | 2 | |
| RD | 3 | |
| RS | 4 | |
| CS | 5 | |
| SDR | 6 | |
| SG | 7 | |
| CD | 8 | |
| DTR | 20 | |

**RS-422 Cable Connections**

| AJ71C24 End | Cable Connections |
|---|---|
| Signal name | |
| SDA | |
| SDB | |
| RDA | |
| RDB | |
| SG | |
| FG | |

Step 2 Set the mode setting switch

Set the mode setting switch to "F" to select the loopback self-check. (Refer to section 4.3.1 for details of how to set this switch.)

Step 3 Carry out the loopback self-check

(1) Turn on the PC CPU power supply or reset the PC CPU. The check starts automatically when the AJ71C24 READY signal turns ON. The READY signal turns ON a few seconds after the power supply is turned on or the PC CPU is reset.

(2) Check sequence

Checks are carried out in the following order:

1) PC CPU communication check
2) RS-232C communication check
3) RS-422 communication check.

The checks are then repeated. The checks are completed within one second. The checks are carried out automatically by the AJ71C24.

(3) Check the LED display status, as described in section 4.6.2.

Normal·····checks are complete
Error·····correct the error and repeat the loopback self-check

(4) Operation when checks are complete

1) Turn the power supply off.
2) Disconnect the cables.
3) Change the setting of the mode setting switch.

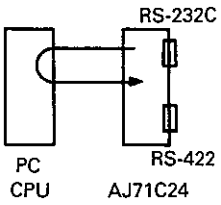
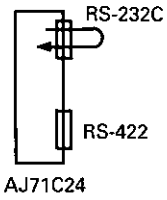
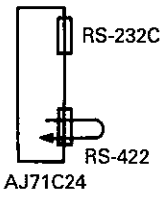
**POINT**

**In cases where two AJ71C24's are mounted in one PC CPU, do not carry out the loopback self-check simultaneously for both modules as this will result in a PC communication check error.**



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### 4.6.2 Self-check operation

| Check Items | Check | Normal Indicator LED | | Error Indicator LED | | Information Flow |
|---|---|---|---|---|---|---|
| PC communication check | After writing data to special data register D9072, the AJ71C24 reads and verifies it. If the data matches, it is changed and the procedure is repeated. If data does not match, an error is indicated. | 2-C/N (LED No. 16) | OFF | 2-C/N (LED No. 16) | ON |   |
| | | CPU R/W (LED No. 25) | Flicker | | | |
| RS-232C communication check | Checks data sent from RS-232C connector. If normal, AJ71C24 changes data and the procedure is repeated. If not normal, an error is indicated. An error is indicated if no cable is connected. | 2-SIO (LED No. 19) | OFF | 2-SIO (LED No. 19) | ON |   |
| | | 2-SD (LED No. 1) | Flicker | | | |
| | | 2-RD (LED No. 2) | | | | |
| RS-422 communication check | Checks data sent from RS-422 connector. If normal, AJ71C24 changes data and the procedure is repeated. If not normal, an error is indicated. An error is indicated if no cable is connected. | 4-SIO (LED No. 23) | OFF | 4-SIO (LED No. 23) | ON |   |
| | | 4-SD (LED No. 10) | Flicker | | | |
| | | 4-RD (LED No. 11) | | | | |

* Checks are carried out in the following order: 1) PC CPU communication check 2) RS-232C communication check 3) RS-422 communication check, and then repeated.



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## 4.7 Loopback Test

The loopback test checks correctness of data communication between the computer and the AJ71C24 using the dedicated protocols 1 to 4.
The procedure to carry out the loopback test is listed below.

(1) Connect the computer and AJ71C24
Connect the cable between the computer and AJ71C24 as described in section 4.5.2.

(2) Execute the loopback test command
1) Create a loopback test command and data at the computer and transmit this to the AJ71C24. (Refer to section 6.14 for details of the commands.)
2) The AJ71C24 echoes the unchanged data back to the computer.

(3) Computer coincidence check
Check at the computer if data sent from the computer to the AJ71C24 coincides with the data echoed back from the AJ71C24 to the computer.
Coincident data indicates that the communication between the computer and AJ71C24 is normal.
If the data sent from the computer to the AJ71C24 and the data echoed back from the AJ71C24 to the computer do not coincide, it is likely that the transmission specification settings do not match or the CD pin is repeatedly turning ON/OFF.
Use the troubleshooting charts in Sections 8.2.5 and 8.2.6 to determine and correct the problem and then repeat the loopback test.

(4) If no data communication is possible
It is likely that the hardware settings or cable connections have not been carried out correctly.
Use the troubleshooting charts in Sections 8.2.2, 8.2.3 and 8.2.4 to determine and correct the problem and then repeat the loopback test.



## 4.8 Inspection and Maintenance

The AJ71C24 module itself requires no particular inspection procedures. However, carry out the inspections listed in the PC CPU User's Manual to ensure optimum system performance.



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# 5. SETTING TRANSMISSION CONTROL DATA

The buffer memory has a special-application area used to set the transmission control data, as shown in section 3.5. Each transmission data item has a default value. However, depending on the purpose and application of data transmission and the specification of the external devices, using the default values can lead to increased complexity of the data communication programs and may even preclude data communication. This chapter describes the settings of all items in the buffer memory special-application area, the method for specifying changes and examples.

**REMARKS**

The contents of this chapter are only required when changing the preset default values. This chapter is not required when carrying out data communication using the default values.

## 5.1 Precautions when Creating a Program

The following precautions are important when using a sequence program to write data to the buffer memory special-application area.

(1) Data can only be written to the special-application area using the sequence program TO instruction. The AJ71C24 will not operate correctly if data is written from the computer. Never write data to the buffer memory special-application area from the computer.

(2) The buffer memory has no battery back-up
When the power supply is turned off and back on or the PC CPU reset, previously written data is lost and all values return to the default values.
Therefore it is necessary to write data settings and changes after turning on the power supply or resetting the PC CPU.

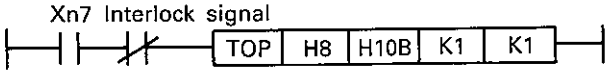
(3) If the buffer memory area allocation is changed when using both the protocols 1 to 4 and the no-protocol mode, the user area buffer memory addresses also change.
If data is erroneously written to the no-protocol mode communication data buffer memory areas with the buffer memory read or write commands (CR, CW) or by the on-demand function, the no-protocol mode communication data will be changed and normal data communication impossible.

(4) When word or byte units are specified for data communication in the no-protocol mode, the on-demand data units become the same as those in the no-protocol mode.

(5) The buffer memory addresses $10E_H$ and $11F_H$ are reserved for system use and must not be used by the user. Never write data to the system area as this precludes normal operation of the AJ71C24.

(6) When setting an item or changing a setting, first turn the power supply off and back on or reset the PC CPU. Carry out the settings on the rising edge of the AJ71C24 READY signal (Xn7) only, as shown in the example below. The AJ71C24 will not operate correctly if the changes are made during data communication between the external device and AJ71C24.

Example: To disable the RS-232C CD pin check function





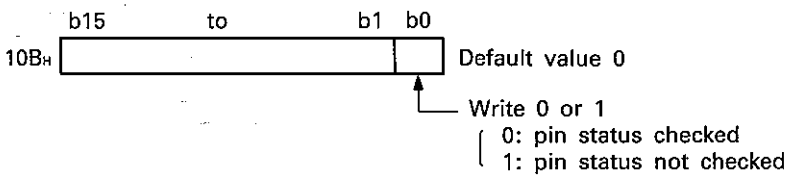

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## 5.2 RS-232C CD Pin Check Enable/Disable Function

The setting of this RS-232C CD pin check function to enable or disable determines whether or not the AJ71C24 checks the ON/OFF status of the CD pin (receive carrier detection pin).

Disabling the RS-232C CD pin (receive carrier detection pin) check function.
If a "1" is written to buffer memory address $10B_H$, the AJ71C24 does not check the ON/OFF status of the CD pin, and operates as if the CD pin were ON.

**How to specify the setting**



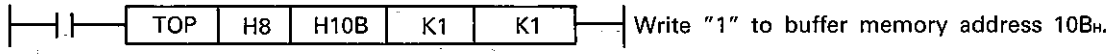

**POINT**

**Bits b1 to b15 of address $10B_H$ may be set either to 0 or 1. They are ignored by the AJ71C24.**

**Example**

To disable the RS-232C CD pin check function (AJ71C24 I/O addresses 80 to 9F).

Sequence program




5



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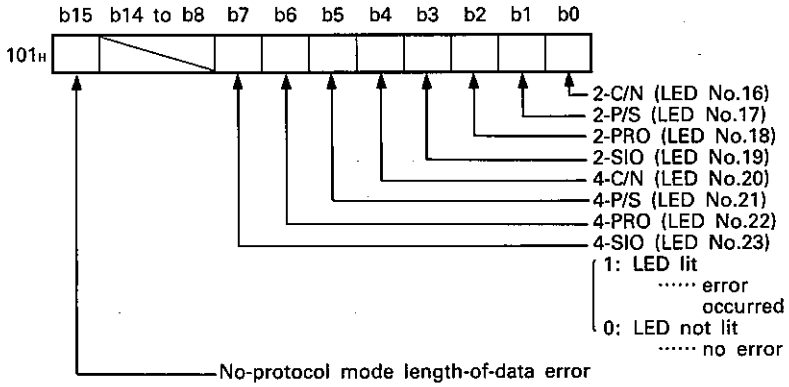
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## 5.3 Transmission Error Data Read Function

This section explains the contents of the buffer memory area storing the ON/OFF statuses of the error LED's and how to turn off LED's which are lit.

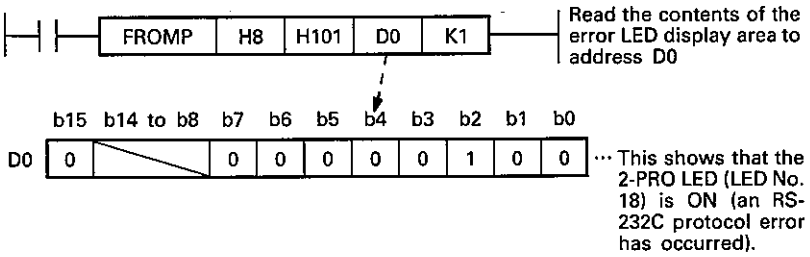
### 5.3.1 Reading the error LED display status

(1) Error LED display area
The ON/OFF statuses of the error LED's are stored in address $101_H$ of the buffer memory as shown below.




(2) Program example to read the error LED display area
This shows an example of a program using the sequence program FROM instruction to read the error LED display ON/OFF statuses stored in buffer memory address $101_H$.

Program example to read the error LED display area (AJ71C24 I/O addresses 80 to 9F)



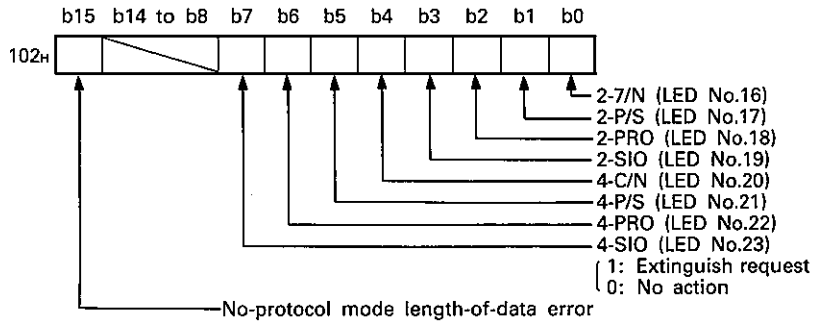



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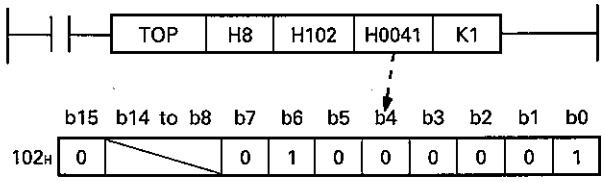
### 5.3.2 Turning off error LED's

When an LED turns on, it remains lit even if the cause of the error is eliminated.
It is necessary to write "1" to the appropriate bit of address $102_H$ of the buffer memory using the PC CPU TO instruction to turn off the LED which is lit.

(1) Error LED extinguish request area




(2) Program example to turn off error LED's
This shows a sequence program example to turn off LED 2-C/N (LED No.16) and LED 4-PRO (LED No.22)




**POINT**

**(1) The LED extinguish request is only valid when it is written.**

**(2) The relevant data in the error LED display area at address $101_H$ is cleared when the LED extinguish request is made. Data at address $102_H$ remains as it was written.**

**(3) If the cause of the error has not been corrected when the LED extinguish request is made, the LED will light once more.**



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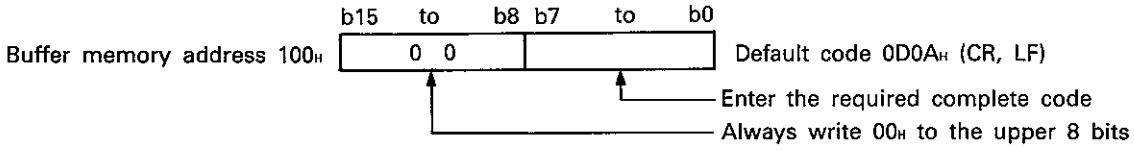
## 5.4 Settings in the No-Protocol Mode

This chapter describes the method for specifying setting items and examples in the no-protocol mode.

### 5.4.1 Setting the no-protocol mode receive-complete code

This shows the method of specifying receive-complete code settings and changes and a sequence program example.

How to specify the setting




**POINT**

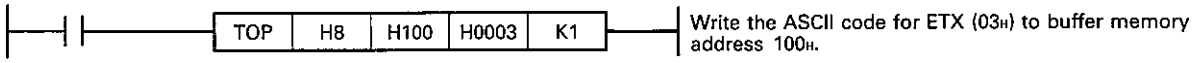
**(1) The complete code can be selected from any value in the range 00H to FFH.**

**(2) If the length of data to complete receiving data is also set (address 108H) the receive is completed by the receiving of the end code or the specified length of data to complete receive, whichever occurs first.**

Example

To set the end code to ETX (03H) (AJ71C24 I/O addresses 80 to 9F).

Sequence program




5



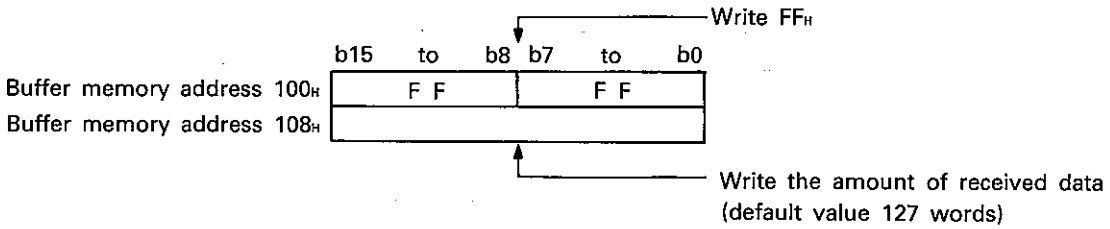
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### 5.4.2 Specifying amount of data to complete data receive (fixed length)

This section shows how to specify the way of completing the data receive and set the amount of data received. A sequence program example is also given.

**How to specify the setting**




**POINT**

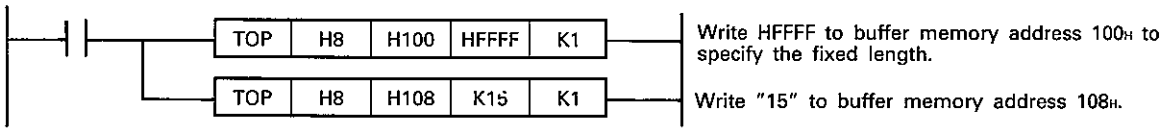
**(1) Set the length of data to complete the data receive in the following ranges:**
**Length of data received ≦ no-protocol mode buffer memory length −1 (when word units are set)**
**Length of data received ≦ (no-protocol mode buffer memory length −1) × 2 (when byte units are set)**
**If a the length of data received setting is larger than the no-protocol mode buffer memory length, then it is automatically set equal to the no-protocol mode buffer memory length.**

**(2) The selection of word or byte units is described in Section 5.4.3.**

**Example**

To set the fixed length at which data receive is complete to 15 words (AJ71C24 I/O addresses 80 to 9F).

Sequence program




5



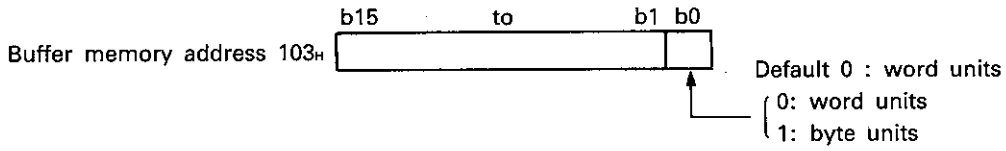
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### 5.4.3 Specifying word or byte units in no-protocol mode

This section shows how to specify word or byte units for data communication and gives an example.

**How to specify the setting**




**POINT**

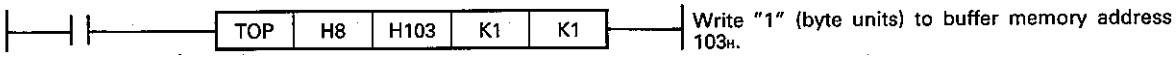
**(1) Word or byte units specified here apply only to communication data in the no-protocol mode and on-demand data using a dedicated protocol.**

**(2) Bits b1 to b15 of address 103H may be set either to 0 or 1**
**They are ignored by the AJ71C24.**

**Example**

To specify byte units (AJ71C24 I/O addresses 80 to 9F).

Sequence program




5



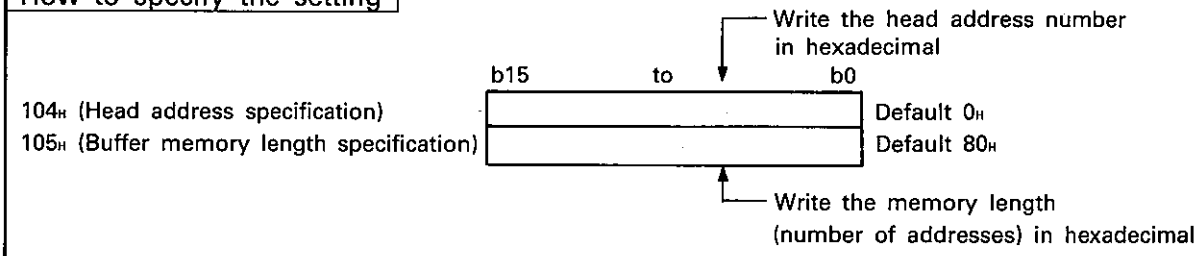
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### 5.4.4 Setting buffer memory area for transmission in no-protocol mode

This section shows how to specify the setting of the AJ71C24 buffer memory area to store data transmitted from the PC CPU to an external device, and gives an example.

**How to specify the setting**




**POINT**

**(1) The buffer memory addresses are for the special-application area. Addresses in this range should not be specified.**

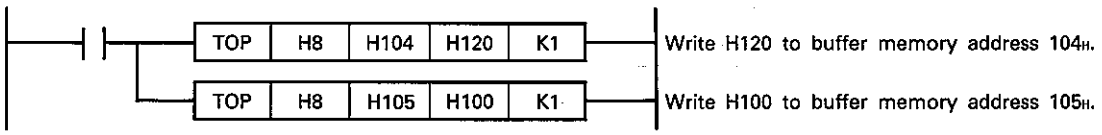
**(2) Make sure that the specified range does not overlap the no-protocol mode buffer memory area or the on-demand data area.**

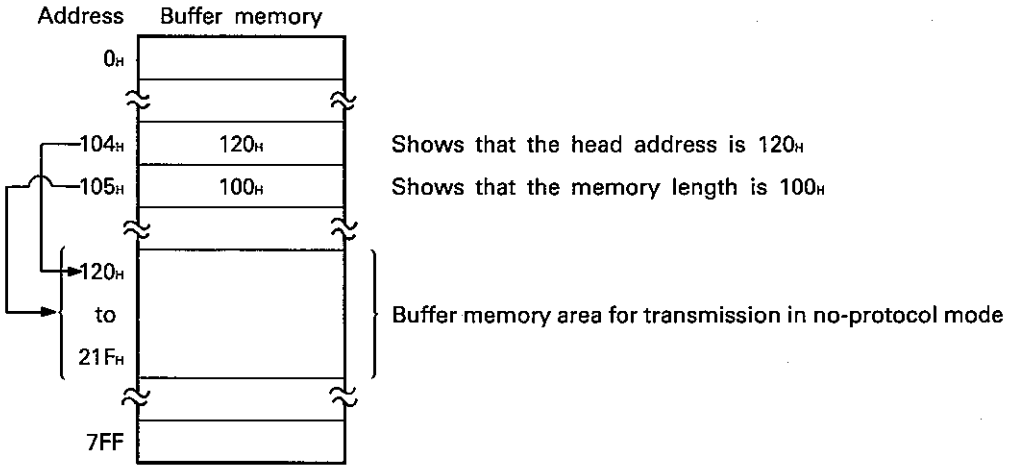
**(3) If addresses are specified out of range (00 to 7FF), the AJ71C24 uses the default values.**

**Example**

To set the head address to 120H and the memory length to 100H (AJ71C24 I/O addresses 80 to 9F).

Sequence program



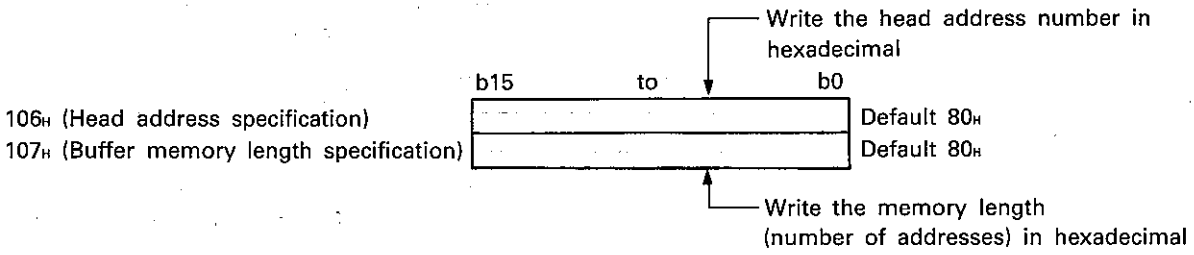



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### 5.4.5 Setting buffer memory area for receiving in no-protocol mode

This section shows how to specify the setting of the AJ71C24 buffer memory area to store data transmitted to an external device from the PC CPU and gives an example.

**How to specify the setting**



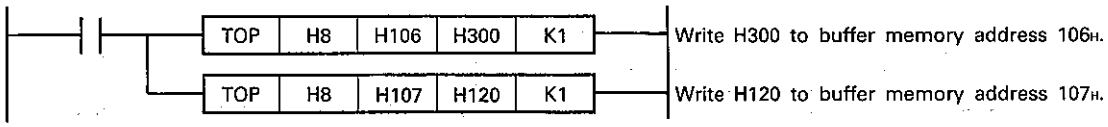

**POINT**

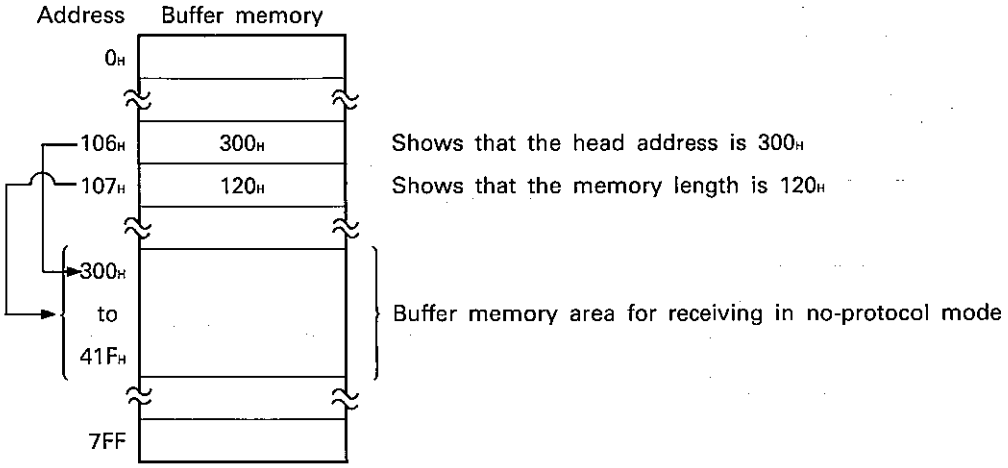
**(1) The buffer memory addresses are for the special-application area and should not be specified.**
**(2) Make sure that the specified range does not overlap the no-protocol mode buffer memory area or the on-demand data area.**
**(3) If addresses are specified out of range (00 to 7FF), the AJ71C24 uses the default values.**

**Example**

To set the head address to 300H and the memory length to 120H (AJ71C24 I/O addresses 80 to 9F).

Sequence program






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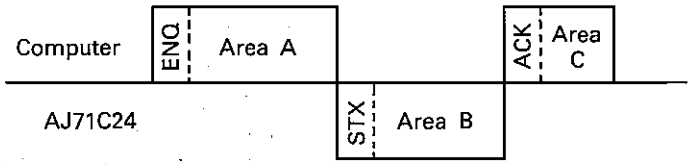
# 6. COMPUTER COMMUNICATION USING THE DEDICATED PROTOCOLS

The details and method of specifying the control protocols 1 to 4 are explained in this chapter and example are given.

## 6.1 Basics of Control Protocol

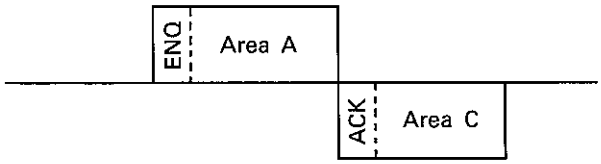
This section explains the transmission control protocol basics.

(1) Understanding the control protocols
(a) Computer reading data from the AJ71C24




1) Areas A and C indicate transmission from the external device to the AJ71C24.
2) Area B indicates transmission from the AJ71C24 to the external device.
3) Computer programs are created such that all data is transmitted from left to right.
(Example: In area A, data is transmitted to the right after the ENQ signal.)
4) Area C of the program completes data communication (if communication is being carried out or not) and permits the next data communication to be carried out.

(b) Computer writing data to the AJ71C24




1) Areas A indicate transmission from the external device to the AJ71C24.
2) Area B indicates transmission from the AJ71C24 to the external device.
3) Computer programs are created such that all data is transmitted from left to right.
(Example: In area A, data is transmitted to the right after the ENQ signal.)

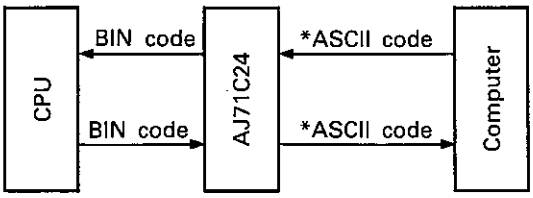




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(2) Data codes for data communication
This section explains the data codes for data communication using the protocols.




*The hexadecimal control codes shown in 6.3.5 are communicated unchanged.

(a) Computer reading data from the PC CPU
The data read from the PC CPU is converted to ASCII code by the AJ71C24 and transmitted to the computer.

(b) Writing data from the computer to the PC CPU
Data input from the computer as ASCII code is converted to BIN code (binary) by the AJ71C24 and transmitted to the PC CPU.



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## 6.2 Precautions Regarding Computer Communications

The following precautions are important to ensure normal computer communications.

(1) Make sure that the transmission specifications of the AJ71C24 in each station of a 1:n ratio computer link system are set the same. A normal link cannot be established if these settings are not correct.

(2) Make sure that no AJ71C24 station numbers in a 1:n ratio computer link system are duplicated. A normal link cannot be established and data may be destroyed if station numbers are overlapping.

(3) The settings of switches (for station number setting, mode setting and transmission specifications) on the AJ71C24 are read and processed when the power is turned on. As a result, changes in the switch settings made after the power is turned on are ignored.
If it is necessary to change the switch settings, move the switches and then reset the PC CPU.

(4) The conditions under which the AJ71C24 transfer sequence is initialized are as follows:
- when the power supply is turned on or the CPU reset with the reset switch on the CPU
- when the control code EOT or CL is received using a protocol
- when the CD pin is turned OFF (the ON/OFF status of the CD pin is ignored if the CD pin check function is disabled)
- when data communication has completed normally
- when a NAK control code is sent.

(5) If nothing is sent from an RS-422 port in a 1:n ratio computer link system, in some cases a framing error occurs and $00_H$ data (NULL code) is transmitted. These NULL codes should be ignored by the computer.
The computer should also be made to ignore all data sent from the AJ71C24 prior to an STX, ACK or NAK code.

(6) PC CPU scan time
When the AJ71C24 requests an access to the PC CPU, if the PC CPU is running, the access is processed once only after the END instruction.
Therefore the scan time is increased by this processing time. Refer to Appendix 5 for details of the intervening times and process times required for AJ71C24 and PC CPU communication.
Even if there is no link, the scan time increases by 0.2 ms if AJ71C24 is mounted.



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(7) The PC CPU can carry out only one process for each END instruction. If other accesses are made simultaneously from other AJ71C24's to the same PC CPU, one module must wait until the other processing ends so that the required scan time increases.

(8) The AJ71C24 enters the STANDBY mode (refer to section 3.4 I/O List for Programmable Controller CPU) if a data link error occurs during data communication with a PC CPU (with a station number not equal to $FF_H$) on MELSECNET.
The computer carries out a time check and sends a CLEAR instruction (EOT or CL-refer to section 6.3.5 (1)) to initialize the transmission sequence if an error is detected.

## 6.3 Transmission Control Protocol

There are 4 formats of control protocol. These formats are selected by the mode setting switch (Rotary switch).
The differences between formats can be summarized basis on format 1 as follows:

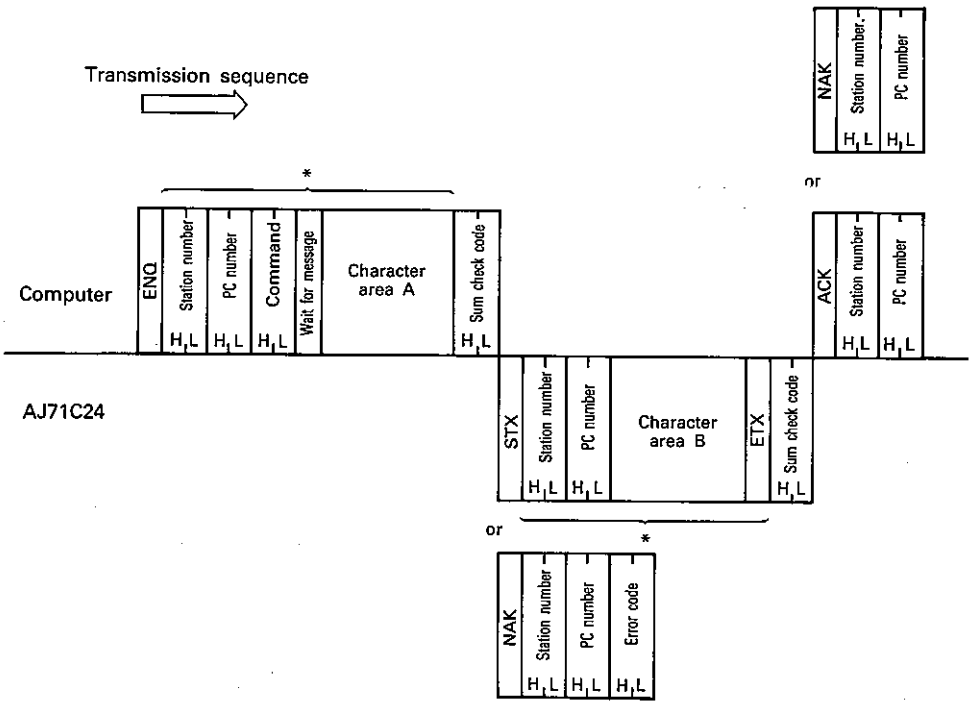
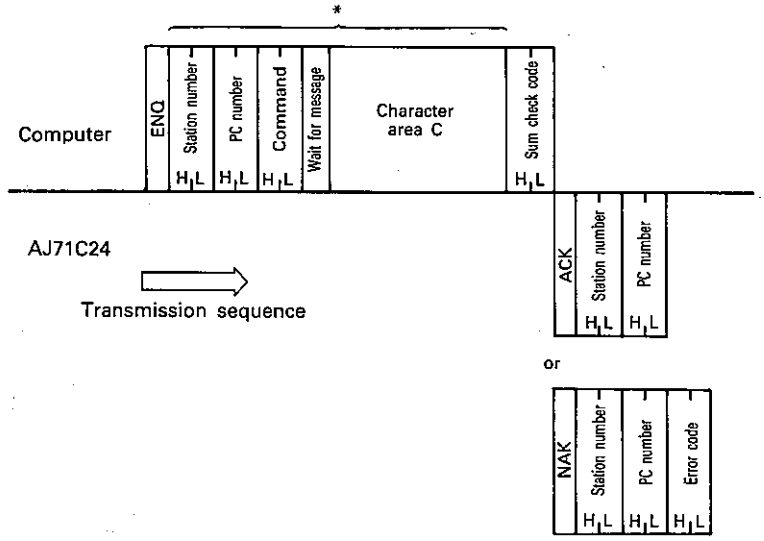
Format 2 : Format 1 with block number added.
Format 3 : Format 1 with STX and ETX added.
Format 4 : Format 1 with CR and LF added.

Details of the four control protocols and the meanings of individual items are explained below.



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### 6.3.1 Control protocol format 1

| Description | Control Protocol |
|---|---|
| To read data from PC to computer |  |
| To write data from computer to PC |  |
| Remarks | (1) The sum check is enabled by DIP switch 21.<br>The sum check code only exists when the sum check is enabled by turning on DIP switch 21.<br>(2) The sum check is made for characters marked * in the above diagram.<br>(3) In the above diagram, the contents of "character area A", "character area B" and "character area C" depend on the individual system. For details, refer to relevant sections. The contents of all character areas are the same for all 4 formats. |

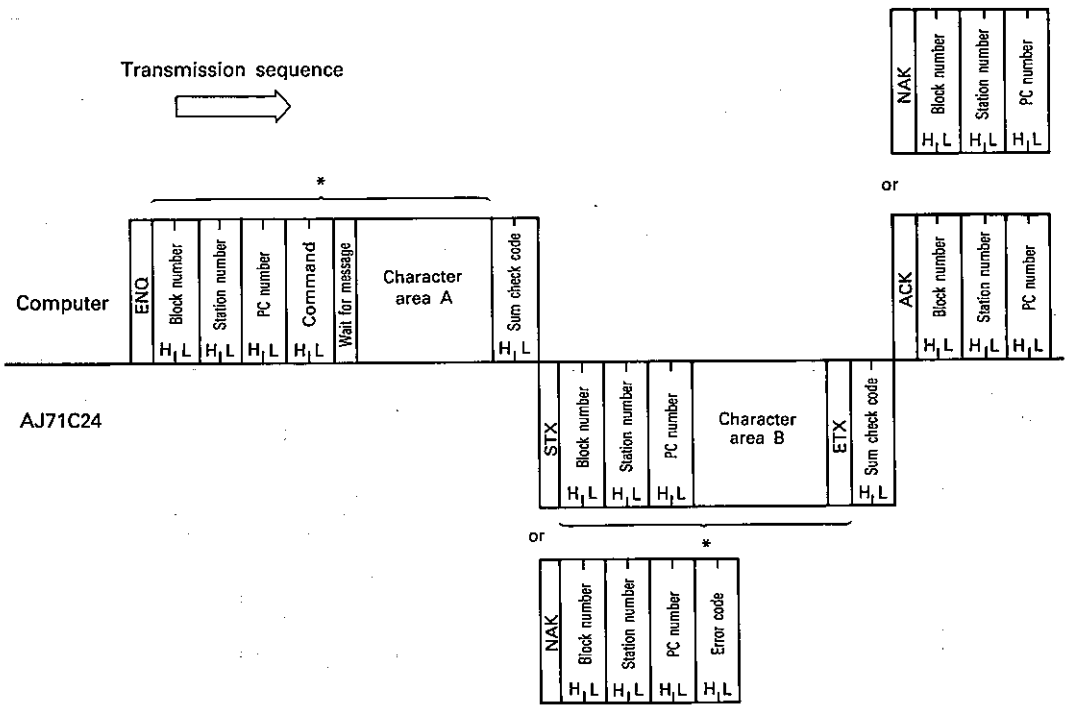
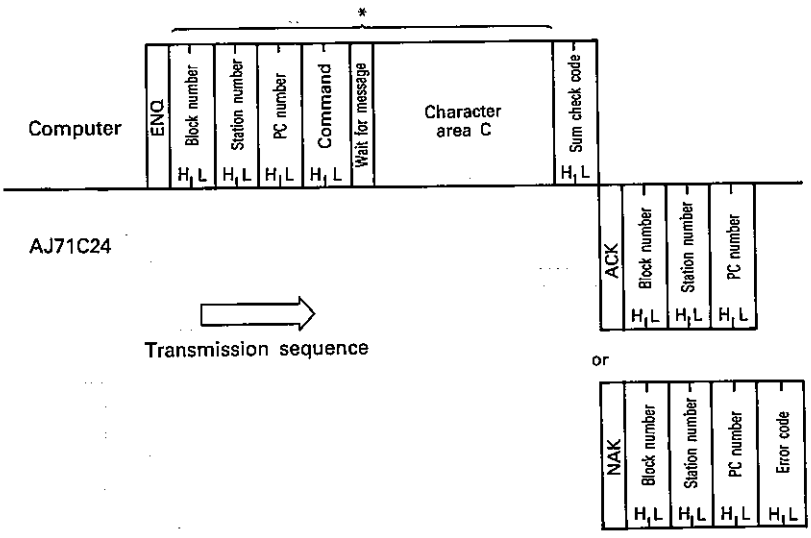






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### 6.3.2 Control protocol format 2

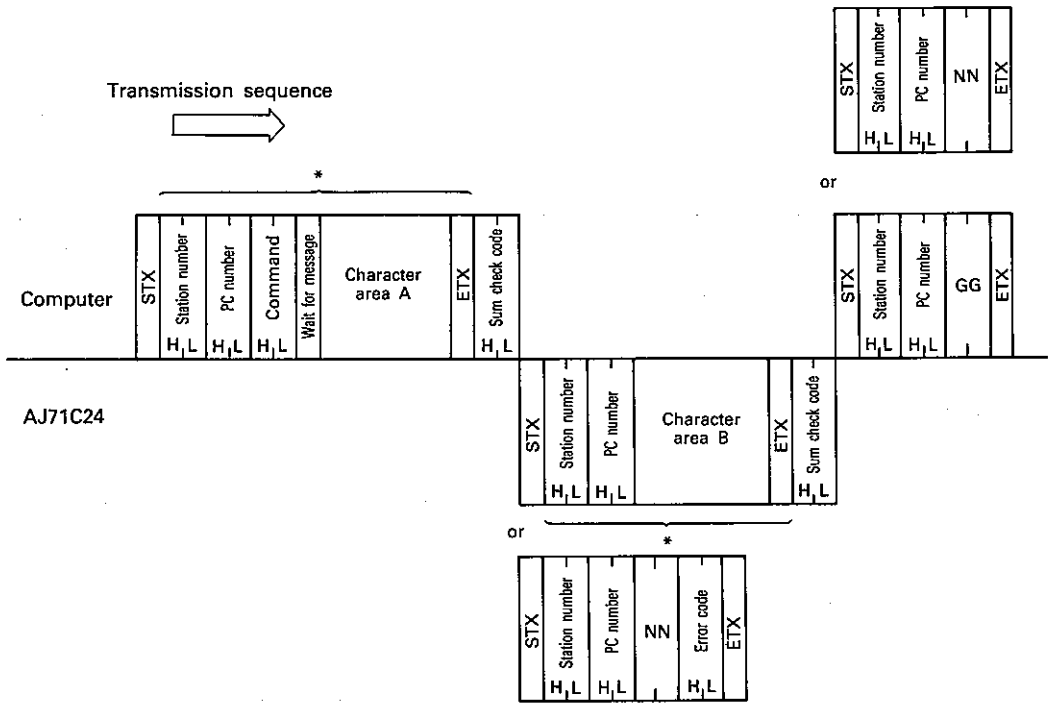
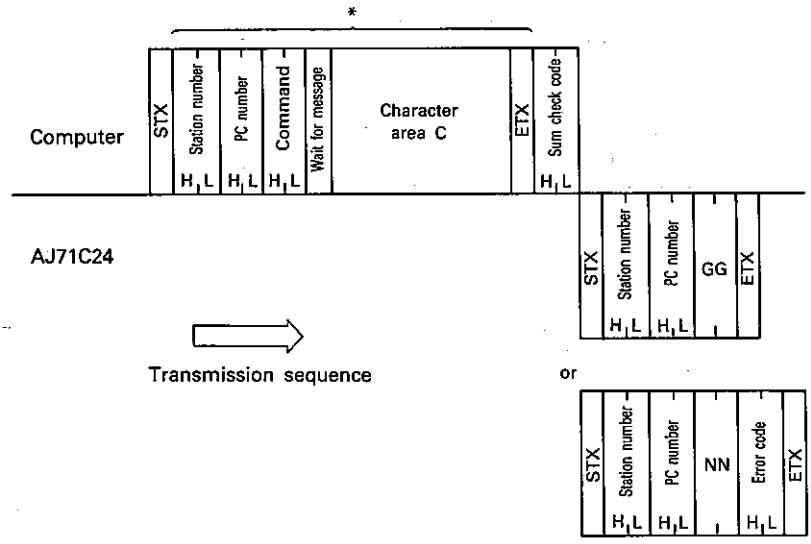
| Description | Control Protocol |
|---|---|
| To read data from PC to computer |  |
| To write data from computer to PC |  |
| Remarks | (1) The sum check is enabled by DIP switch 21.<br>The sum check code only exists when the sum check is enabled by turning on DIP switch 21.<br>(2) The sum check is made for characters marked * in the above diagram.<br>(3) In the above diagram, the contents of "character area A", "character area B" and "character area C" depend on the individual system. For details, refer to relevant sections. The contents of all character areas are the same for all 4 formats. |





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### 6.3.3 Control protocol format 3

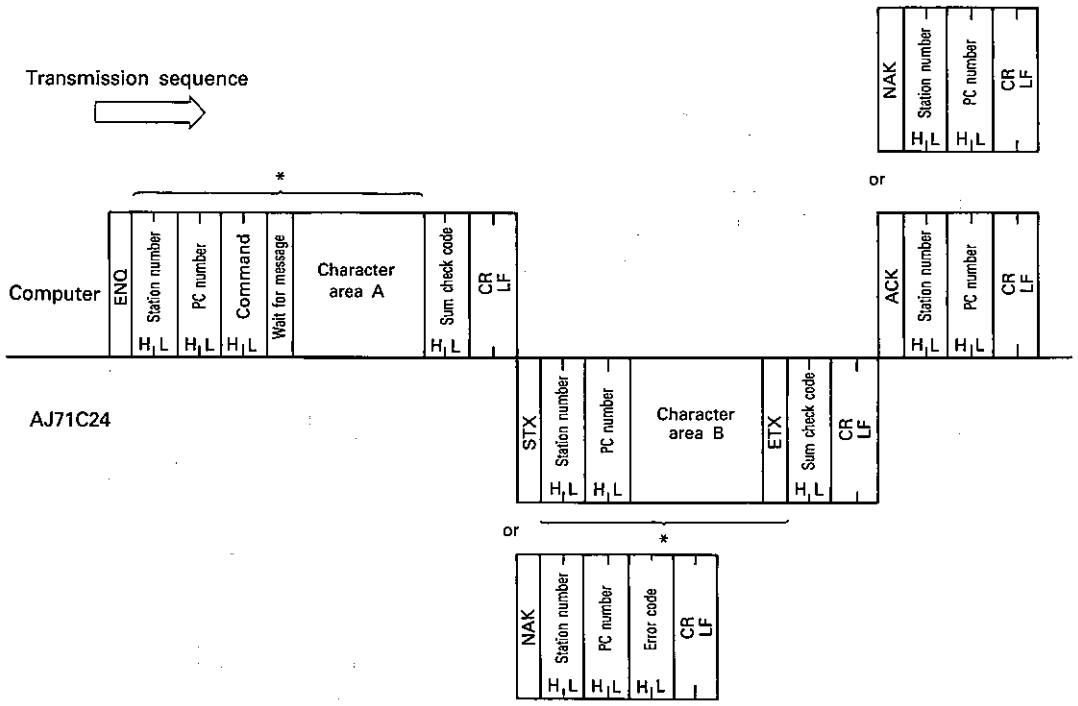
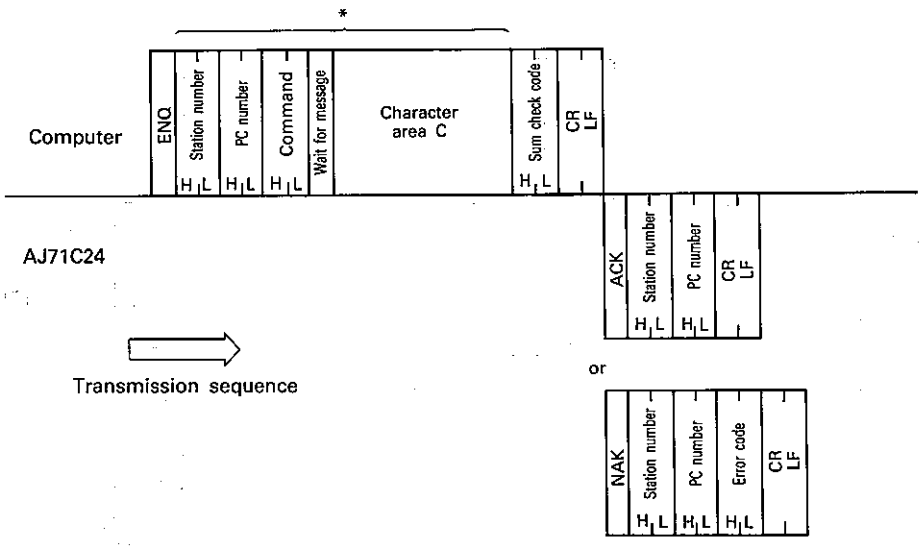
| Description | Control Protocol |
|---|---|
| To read data from PC to computer |  |
| To write data from computer to PC |  |
| Remarks | (1) The sum check is enabled by DIP switch 21.<br>The sum check code only exists when the sum check is enabled by turning on DIP switch 21.<br>(2) The sum check is made for characters marked * in the above diagram.<br>(3) In the above diagram, the contents of "character area A", "character area B" and "character area C" depend on the individual system. For details, refer to relevant sections. The contents of all character areas are the same for all 4 formats. |





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### 6.3.4 Control protocol format 4

| Description | Control Protocol |
|---|---|
| To read data from PC to computer |  |
| To write data from computer to PC |  |
| Remarks | (1) The sum check is enabled by DIP switch 21.<br>The sum check code only exists when the sum check is enabled by turning on DIP switch 21.<br>(2) The sum check is made for characters marked * in the above diagram.<br>(3) In the above diagram, the contents of "character area A", "character area B" and "character area C" depend on the individual system. For details, refer to relevant sections. The contents of all character areas are the same for all 4 formats. |





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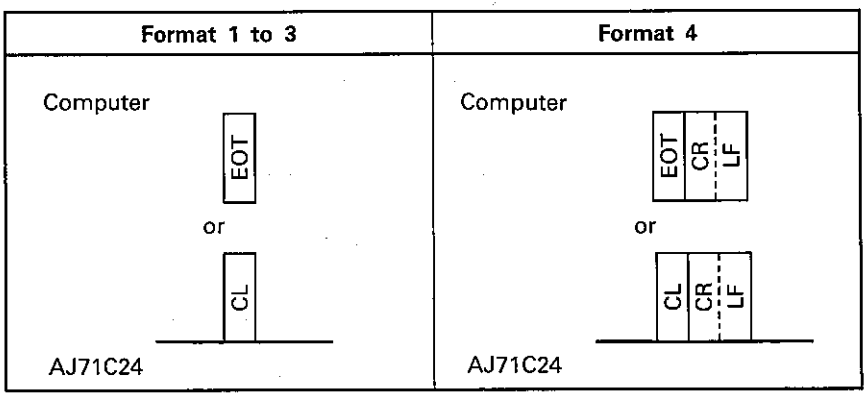
### 6.3.5 Protocol data codes

Details of the meanings of individual items of the four control protocols are explained below.

(1) Control codes
All control codes are sent and received in hexadecimal, they are shown in the following table.

| Signal | Code (Hexadecimal) | Description | Signal | Code (Hexadecimal) | Description |
|---|---|---|---|---|---|
| NUL | 00H | Null | LF | 0AH | Line Feed |
| STX | 02H | Start of Text | CL | 0CH | Clear |
| ETX | 03H | End of Text | CR | 0DH | Carriage Return |
| EOT | 04H | End of Transmission | NAK | 15H | Negative Acknowledge |
| ENQ | 05H | Enquiry | G | 47H | Good |
| ACK | 06H | Acknowledge | N | 4EH | No Good |

(a) The NULL code (00H) is ignored in all messages. If a NULL code is included in a message, it is processed as if it did not exist.
(b) In format 3, control code "GG" is equivalent to ACK and "NN" is equivalent to NAK.
(c) On receiving an EOT or CL code, the AJ71C24 initializes transmission but does not answer. The initializing code depends on the format as indicated below. At this time there is no answer from the AJ71C24.




(2) Block number
The block number is an optional number assigned as a data reference number for the computer. Block numbers are used to arrange data, etc. Block numbers may be from 00H to FFH (in 2-digit ASCII (hexadecimal)).



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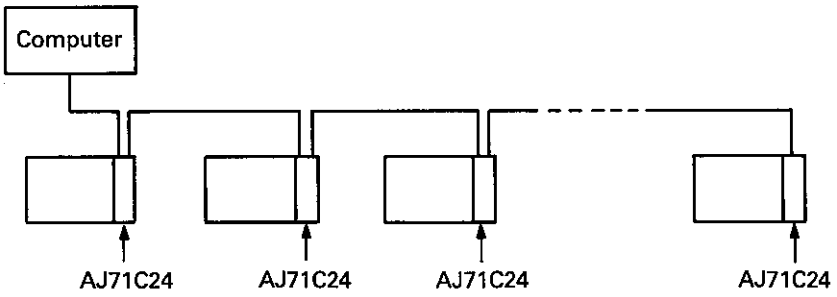
(3) Station number

The station number is set by the station number setting switch on the front of the AJ71C24 and used to identify to which AJ71C24 in a station access will be made.
Station numbers must be in the range $00_H$ to $1F_H$ (0 to 31) (in 2-digit ASCII (hexadecimal)

**POINT**

**(1) The local station setting switch is set to a decimal values but the station number is specified in hexadecimal. Example**
**Switch setting "10" corresponds to a station number of "$0A_H$" specified in the protocol.**
**(2) For the global operation, specify station number "$FF_H$". If 0 to 31 ($00_H$ to $1F_H$) is specified, "Xn2" turns on at that station number only. For details, refer to Section 6.12.**

Example:




**REMARKS**

Station numbers do not need to be sequential.

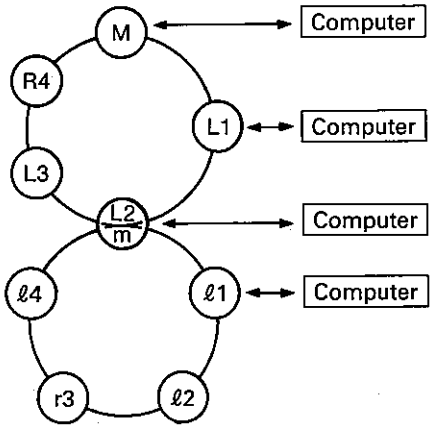
(4) PC number
The PC number is used to determine which PC CPU on MELSECNET to access.
The PC number may be from $00_H$ to $40_H$ (00 to 64) in 2-digit ASCII (hexadecimal).

(a) Accessing PC CPU's equipped with AJ71C24
Set all the PC numbers to $FF_H$ (host).
(b) Accessing PC CPU's on MELSECNET equipped with AJ71C24
MELSECNET master station ····· Set the PC number to $00_H$
MELSECNET local and remote stations ····· Set each link slave station number (1 to 64) in hexadecimal ($01_H$ to $40_H$)



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(c) The range of PC CPU's which can be accessed by setting the PC numbers is described below.




M ····· Master station (1 tier)
L1 ····· Local station (2 tier)
L2/m ···· Local station (2 tier)
Master station
L3 ····· Local station (2 tier)
R4 ····· Remote I/O station (2 tier)
ℓ1 ····· Local station (3 tier)
ℓ2 ····· Local station (3 tier)
r3 ····· Remote I/O station (3 tier)
ℓ4 ····· Local station (3 tier)

| PC CPU loaded with AJ71C24 connected to computer | PC's to which a link is possible (PC number) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Host (FF) | M (0) | L1 (1) | L2/m (2/0) | L3 (3) | R4 (4) | ℓ1 (1) | ℓ2 (2) | r3 (3) | ℓ4 (4) |
| M | ○ | — | ○ | ○ | ○ | (*1) | × | × | × | × |
| L1 | ○ | ○ | — | × | × | × | × | × | × | × |
| L2/m | ○ | ○ | × | — | × | × | ○ | ○ | (*1) | ○ |
| ℓ1 | ○ | × | × | ○ | × | × | — | × | × | × |

○ ····· Access to all devices possible by setting appropriate PC numbers
(*1) ····· Access to special-function module buffer memory possible by setting appropriate PC numbers

**POINT**

**Communication is not possible with A0J2CPUP23/R25 or A0J2CPUP25/R25 modules.**

6



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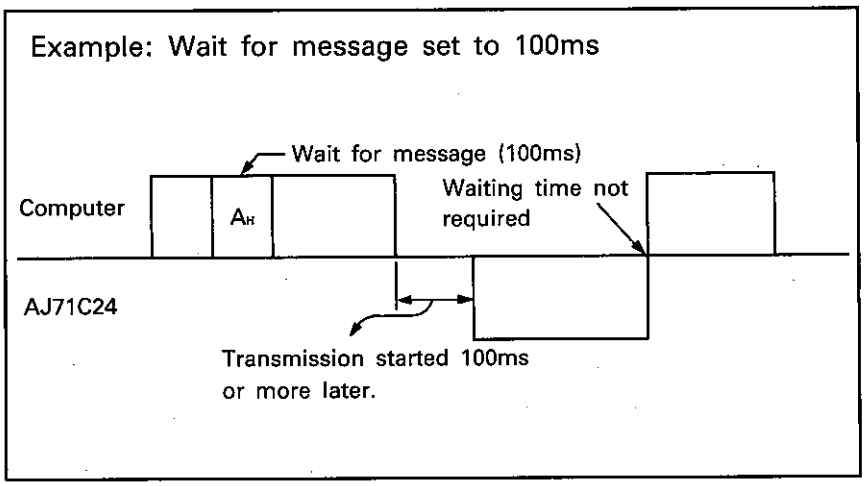
(5) Command

Used to specify the operation required, e.g. read, write, etc. Commands must be in 2 digit ASCII.

(6) Wait for message

This is a time delay required for some computers to switch from transmission to reception states. Wait for message determines the minimum waiting time before the AJ71C24 sends data after receiving it from the computer. Set this time in accordance with the computer specifications.
The wait for message time may be set between 0 and 150ms in units of 10ms. The time is set from $0_H$ to $F_H$ (0 to 15) in 1-digit hexadecimal, where 1 corresponds to 10ms etc.

Example: Wait for message set to 100ms



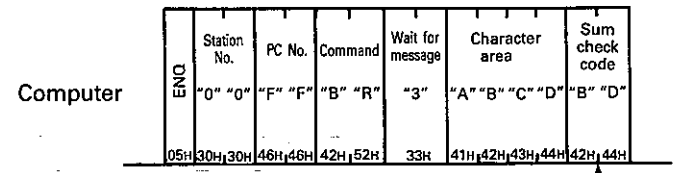



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(7) Sum check code

The sum check code is 2 digit ASCII representing the lower 1 byte (8 bits) of the sum derived from the BIN code representing the checked data.
With DIP switch SW21 OFF, the sum check code is not added.

Example: A, B, C, and D are transferred in format 1, setting station number 0, PC number FF, command BR (batch read of device memory), and wait for message to 30ms, the sum check code value is as shown below.




$30_H + 30_H + 46_H + 46_H + 42_H + 52_H + 33_H + 41_H + 42_H + 43_H + 44_H = 2BD_H$

(8) Error code

- Indicates the error following a NAK transmission.
- Error codes are transmitted as 2 digit ASCII (hexadecimal) in the range $00_H$ to $FF_H$.
- If two or more errors occur simultaneously, the lower one is transmitted.
- For details of error codes, refer to Section 8.1.



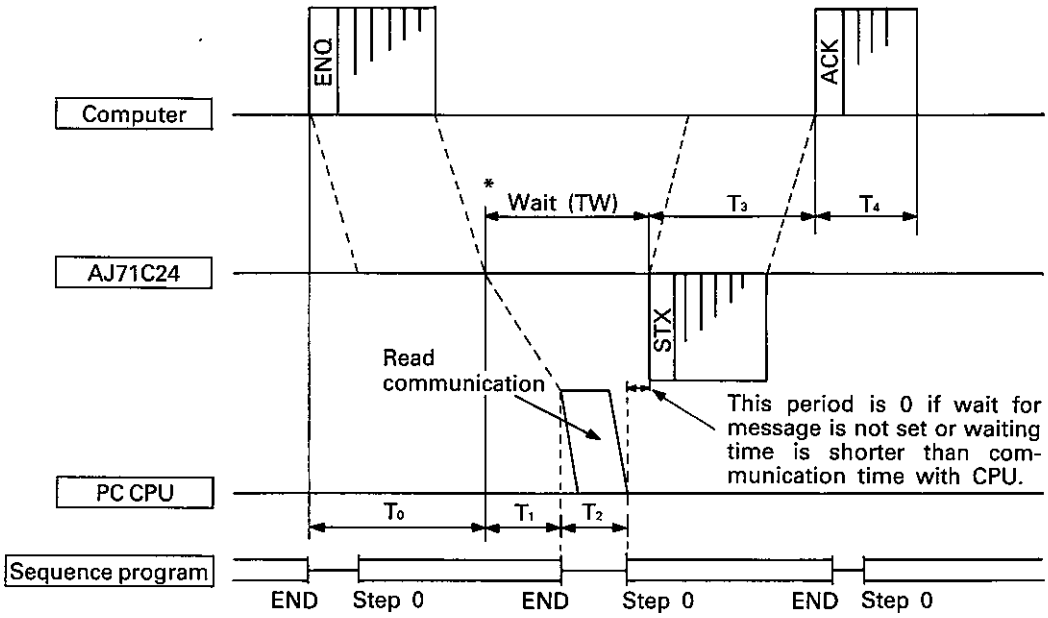




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## 6.4 Transmission Sequence Timing Chart and Communication Times

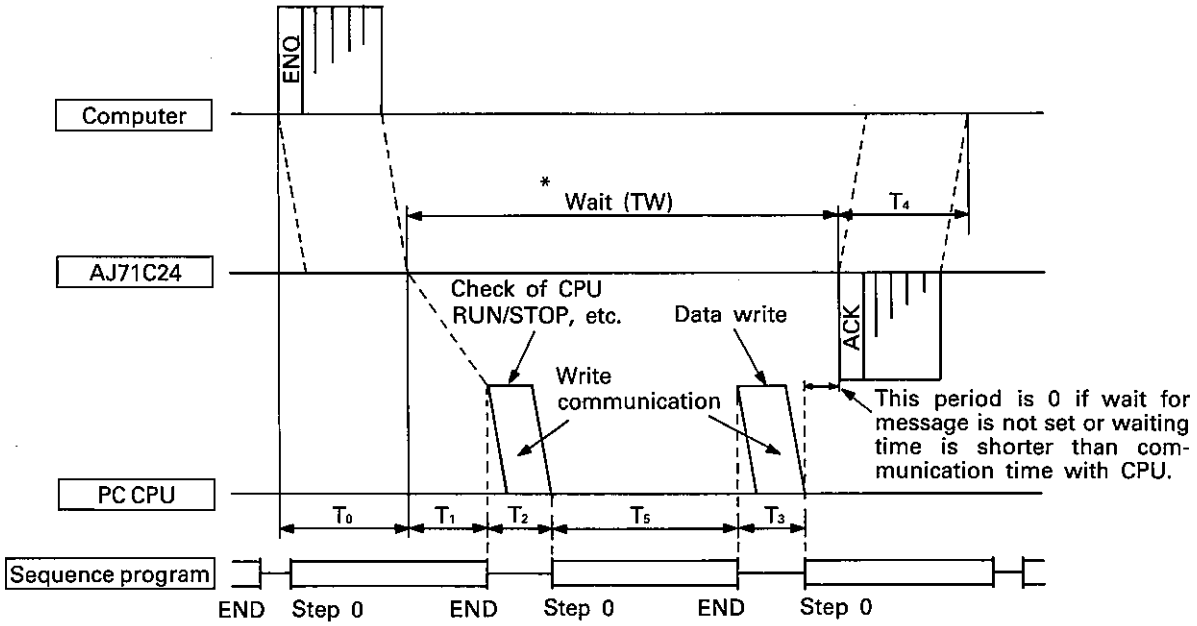
(1) To read data from PC CPU to computer
(*: Indicates that wait for message has been set.)




**REMARKS**

For file register and parameter, an extra 1 scan plus T2 is required.

(2) To write data from computer to PC CPU
(*: Indicates that wait for message has been set.)




**REMARKS**

As shown above, communication between AJ71C24 and PC CPU is always made after END. Therefore, scan time increases by communication time.
For communication time, refer to Appendix 5.
For the number of points processed per communication after END, refer to Section 3.3.1.



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(3) Transmission time

This section describes how to calculate approximate communication time from the start of data transmission from the computer to the completion of all communications after a reply is sent from the AJ71C24.
For $T_0$ to $T_4$, refer to (1) and (2) on the preceding page.

(a) To read data from PC CPU to computer

Communication time = $T_0$ + (longer time of $T_1 + T_2$ or TW) + $T_3$ + $T_4$

where,
$T_0$, $T_3$, $T_4$ = $\frac{1}{\text{baud rate}}$ × number of bits per character

$(1 + \underline{7/8} + \underline{0/1} + \underline{1/2})$ × character length

Start bit; Data length (7 or 8); Parity bit (0 or 1); Stop bit (1 or 2)

$T_1$ = maximum 1 scan time (since data entry to PC CPU is made after END processing. If the PC is not running, $T_1$ is 0.)
$T_2$ = value in Appendix 5
TW = wait for message set time.

(b) To write data from computer to PC CPU

Communication time = T0 + (longer time of $T_1 + T_2 + T_3 + T_5$ or TW) + $T_4$

where,
$T_0$, $T_4$ = $\frac{1}{\text{baud rate}}$ × number of bits of 1 character

$(1 + \underline{7/8} + \underline{0/1} + \underline{1/2})$ × character length

Start bit; Data length (7 or 8); Parity bit (0 or 1); Stop bit (1 or 2)

$T_1$ = maximum 1 scan time (since data entry to PC CPU is made after END processing. If the PC is not running, $T_1$ is 0.)
$T_2$, $T_3$ = values in Appendix 5
(For functions processed in 1 scan, $T_3$ is 0.)
TW = setting time when wait for message has been set.
$T_5$ = 1 scan time
(For functions processed in 1 scan, $T_5$ is 0.)



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(4) Transmission time through MELSECNET

(a) The transmission time ($T_1$) for data transmission by specifying the PC number to a PC CPU on MELSECNET not equipped with AJ71C24 is calculated as follows:

- Local station
  Transmission time ($T_1$) = (LRDP instruction processing time + scan time for station 1 loaded with AJ71C24) × 2
- Remote station
  Transmission time ($T_1$) = (RFRP instruction processing time + MELSECNET master station scan time) × 2
  Substitute "3" for the factor "2" in the equations above (underlined ~~~) for the first data communication after the power supply is turned on or for the relevant station after the PC CPU has been reset.
  If there are no more than 10 stations in communication, use a factor of "1" for the second, and subsequent, communications.
- Causes of delayed transmission time ($T_1$)
  Instructions requiring 2 scans for transmission (writing to device "R", etc.) need double the time derived from the equations above.
  When other stations in the link are being monitored by A6GPP, the transmission time doubles for each station to be monitored.

* Refer to the Data Link User's Manual for details of the data link.

Example

The transmission time for a MELSECNET master station equipped with AJ71C24 to read a local station device memory:
(Conditions: L<LS<M, M : 80msec α1 : 10msec)

Transmission time ($T_1$) = (M×4+α1×4+M)×2
= (80×4+10×4+80)×2 = 880

The transmission time is 880 ms. Where:

M : MELSECNET master station scan time
α1 : MELSECNET master station link refresh time
LS : Link scan time
L : MELSECNET local station scan time

**POINT**

**Under some conditions, data transmission to a PC CPU on MELSECNET not equipped with AJ71C24 can cause a considerable time delay.**
**This time delay can be reduced by carrying out all communication from computer to PC CPU's to stations equipped with AJ71C24 (PC station number $FF_H$) and all other data communication using the MELSECNET data link (B, W).**



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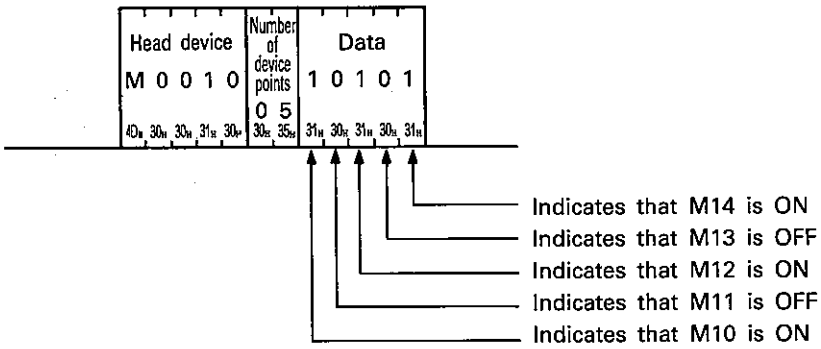
## 6.5 Principle of Character Area Data Transmission

The principle of the transmission data handled as character areas when using commands to carry out data communication between the computer and PC CPU is explained in this section. The data shown in the examples is contained in character area B in the case of read and monitor and in character area C in the case of write, test, and monitor data register.

(1) Bit device memory read and write
The bit device memory can be handled in bit units (one device point) or word units (16 device points).
The principles of these types of data are described below.

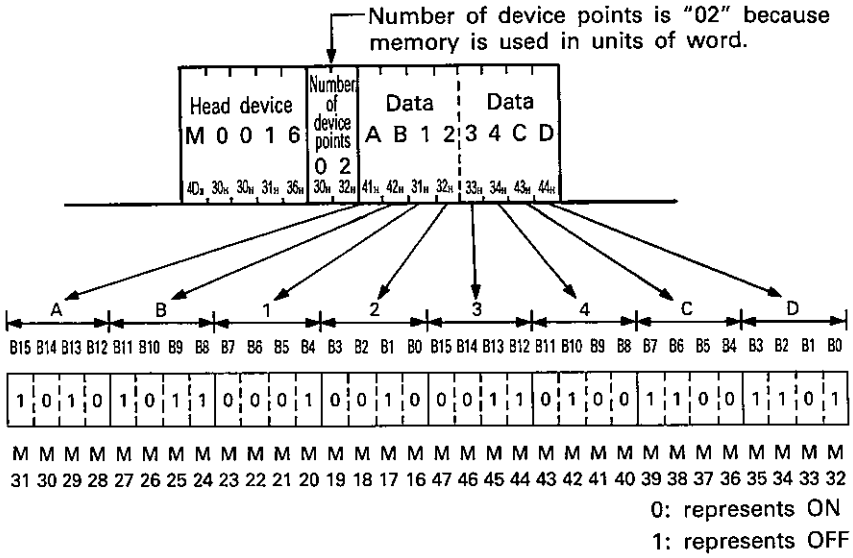
(a) Bit units (one point)
When the bit device memory is handled as bit units, the specified number of device points from the specified head device in sequence from the left are represented as 1 ($31_H$) if the device is on, or 0 ($30_H$) if the device is off.

Example
Indication of ON/OFF status of five points from M10




(b) Word units (16 points).
When the bit device memory is handled as word units, each word is expressed sequentially in hexadecimal values in 4-bit units from the upper bit.

Example
Indication of ON/OFF status of 32 points from M16






IB (NA) 66175-A

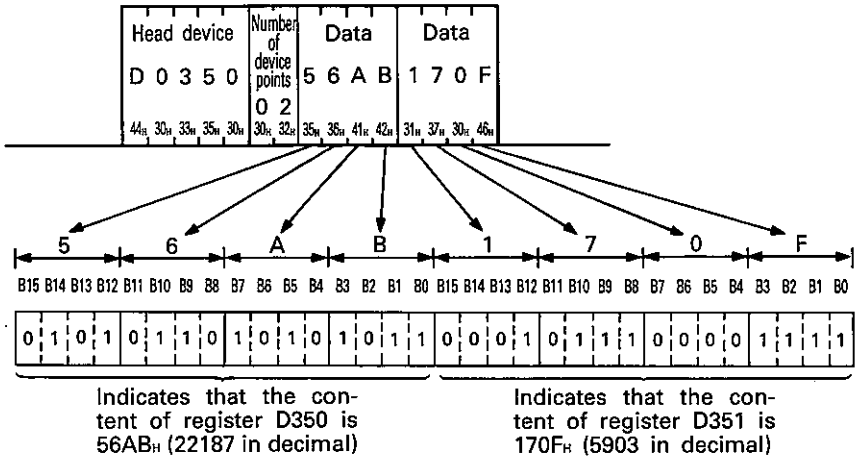
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(2) Word device memory read and write

In the word device memory, each word is expressed sequentially in hexadecimal values in 4-bit units from the upper bit.

Example

Indication of the contents of the D350 and D351 registers




**REMARKS**

Extension file memory read and write, buffer memory read and write and on-demand data when word units are specified are handled according to the same principle as the word device memory.



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## 6.6 Device Memory Link

### 6.6.1 Command and device ranges

(1) Commands used for device memory transactions are shown below.

| Item | | Command | | Processing | Number of Points Processed Per Communication | State of PC CPU | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | During STOP | During RUN | |
| | | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Batch read | Bit unit | BR | 42H, 52H | Reads bit device (such as X, Y, M) in units of 1 point. | 256 points* | ○ | ○ | ○ |
| | Word unit | WR | 57H, 52H | Reads bit device (such as X, Y, M) in units of 16 points. | 32 words (512 points) | | | |
| | | | | Reads word device (such as D, R, T, C) in units of 1 point. | 64 points | | | |
| Batch write | Bit unit | BW | 42H, 57H | Writes bit device (such as X, Y, M) in units of 1 point. | 160 points | ○ | ○ | × |
| | Word unit | WW | 57H, 57H | Writes bit device (such as X, Y, M) in units of 16 points. | 10 words (160 points) | | | |
| | | | | Writes word device (such as D, R, T, C) in units of 1 point. | 64 points | | | |
| Test (Random write) | Bit unit | BT | 42H, 54H | Specifies bit device (such as X, Y, M) and device number in units of 1 point at random and sets/resets the device. | 20 points | ○ | ○ | × |
| | Word unit | WT | 57H, 54H | Specifies bit device (such as X, Y, M) and device number in units of 16 points at random and sets/resets the device. | 10 words (160 points) | | | |
| | | | | Specifies word device (such as D, R, T, C) and device number in units of 1 point at random and writes the device | 10 points | | | |
| Monitor data entry | Bit unit | BM | 42H, 4DH | Sets bit device (such as X, Y, M) to be monitored in units of 1 point. | 40 points* | ○ | ○ | ○ |
| | Word unit | WM | 57H, 4DH | Sets bit device (such as X, Y, M) to be monitored in units of 16 points. | 20 words* (320 points) | | | |
| | | | | Sets word device (such as D, R, T, C) to be monitored in units of 1 point. | 20 points | | | |
| Monitor | Bit unit | MB | 4DH, 42H | Reads data from device for which monitor data entry has been made. | —— | ○ | ○ | ○ |
| | Word unit | MN | 4DH, 4EH | | | | | |

Key : ○ Available
× Unavailable

Values marked * in the Number of Points Processed Per Communication column must be halved if the specified device is × (input).



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(2) Devices

The devices that can be accessed form device memory and device number ranges are listed in the table. Each device is comprised of 5 characters:

{ Device: 1 character (2 characters for T/C) } + { Device number: 4 characters (3 characters for T/C) } = 5 characters

| Bit Device | | | Word Device | | |
|---|---|---|---|---|---|
| Device | Device number range (character) | Decimal/hexadecimal representation | Device | Device number range (character) | Decimal/hexadecimal representation |
| Input X | X0000 to X07FF | Hexadecimal | Timer (present value) T | TN000 to TN255 | Decimal |
| Output Y | Y0000 to Y07FF | Hexadecimal | Counter (Present value) C | CN000 to CN255 | Decimal |
| Internal relay M | M0000 to M2047 | Decimal | Data register D | D0000 to D1023 | Decimal |
| Latch relay L | L0000 to L2047 | Decimal | Link register W | W0000 to W03FF | Hexadecimal |
| Step relay S | S0000 to S2047 | Decimal | File register R | R0000 to R8191 | Decimal |
| Link relay B | B0000 to B03FF | Hexadecimal | Special register D | D9000 to D9255 | Decimal |
| Annunciator F | F0000 to F0255 | Decimal | | | |
| Special relay M | M9000 to M9255 | | | | |
| Timer (contact) T | TS000 to TS255 | | | | |
| Timer (coil) T | TC000 to TC255 | | | | |
| Counter (contact) C | CS000 to CS255 | | | | |
| Counter (coil) C | CC000 to CC255 | | | | |

**POINT**

**(1) Bit devices and word devices are differentiated as follows:**
**Bit device — X, Y, M, L, B, F, T (contact), T (coil), C (contact), C (coil)**
**Word device — T (present value), C (present value), D, W, R**

**(2) When specifying word units, always make sure that the bit device numbers are divisible by 16.**

**(3) Zeros ("0") in the upper digits of the device number (e.g., X0070 - the zeros underlined ~~) may be replaced by the blank code ($20_H$).**

**(4) The ranges for specifying M, L and S are limited. However, the processing does not change if a device number originally allocated to M is specified by L or S, or vice versa.**

**(5) The special relays (M9000 to M9255) and special registers (D9000 to D92550) are divided for read-only, write-only and system use.**
**A PC CPU error may occur if a write operation is carried out outside the permitted write range. Refer to the ACPU programming manual for details of the special relays and special registers.**

**(6) Carry out reading and writing to the file register (R) with the commands described in section 6.7 when using the software utility package SW0GHP-UTLPC-FN1.**

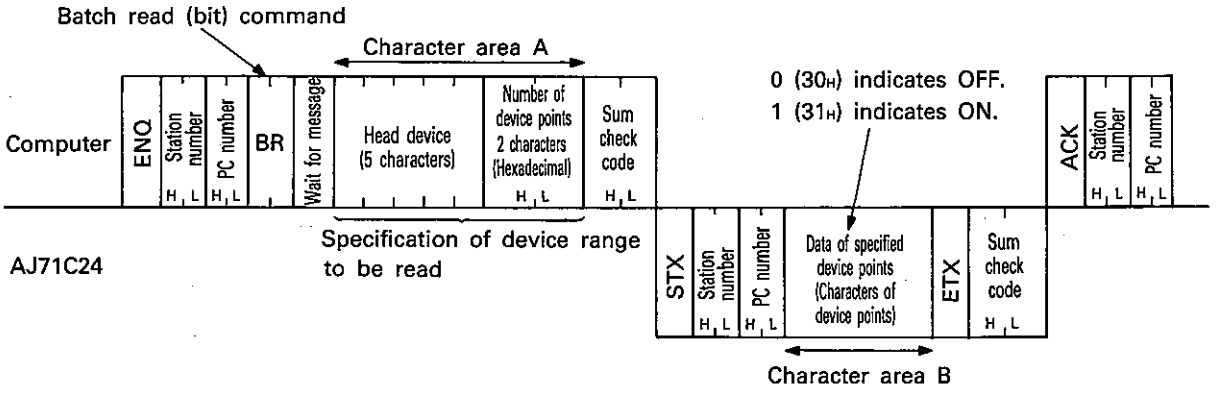


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### 6.6.2 Batch bit read

**Specifying Method**

The following example uses protocol format 1.

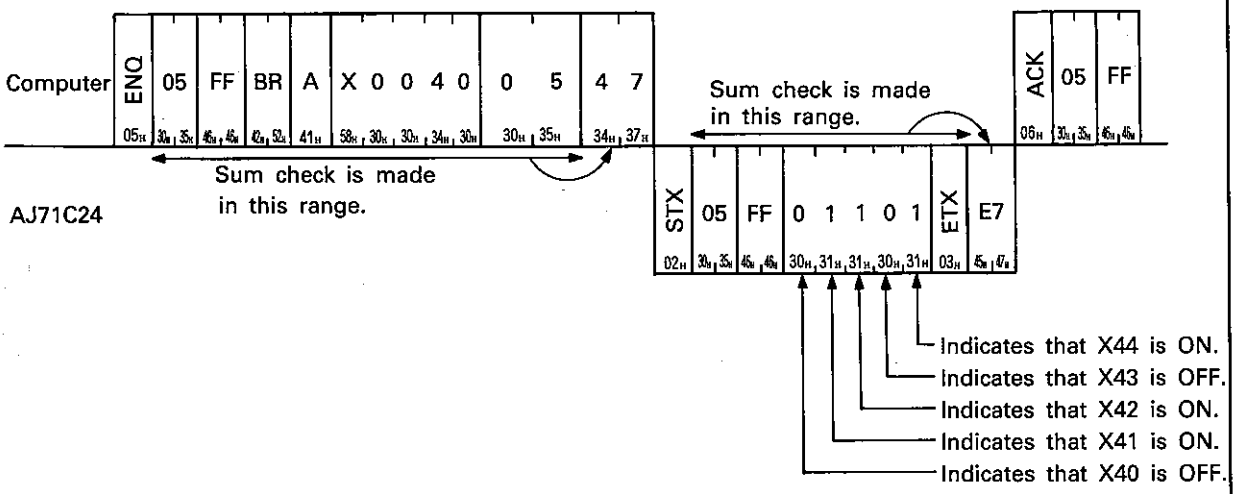



**POINT**

**Specify the number of device points, n, such that:**
**• 1 ≦ n ≦ 256 (Specify 256 points with FFH.)**

**Example**

To read the states of 5 devices, X40 to X44 from station number "5". (Wait for message 100ms)
(X40 and X43 are off and others are on)




**POINT**

**The wait for message time is set between 0 and 150ms in units of 10ms as a 1-digit hexadecimal value 0H to FH. Therefore, a setting of 100ms is "A".**





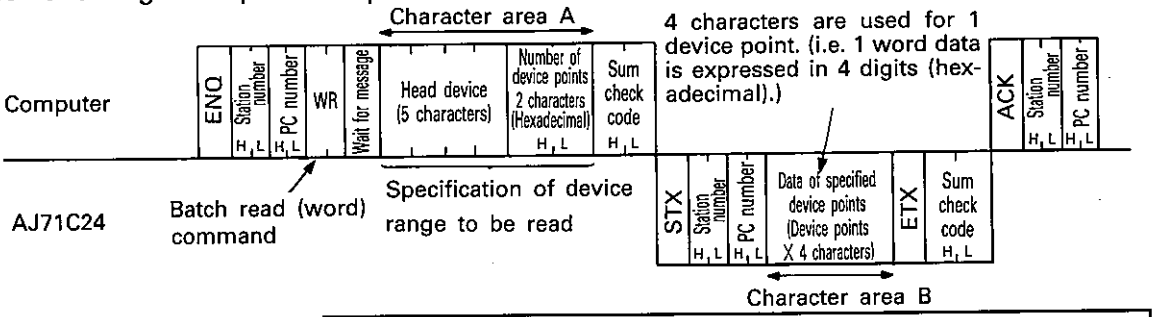
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### 6.6.3 Batch word read

The method for specifying the control protocol and examples are shown below for a batch read of word device memory and a batch read of bit device memory (16 point units).

**Specifying Method**

The following example uses protocol format 1.



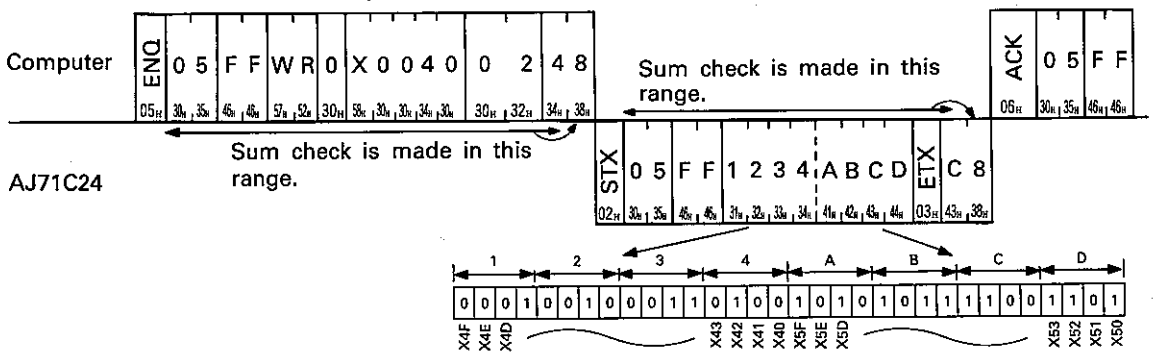

**POINT**

**Specify the number of device points, n, such that:**
- **1 ≦ n ≦ 64 (32 for bit device)**
- **Head device number + n (n × 16 for bit device) − 1 ≦ maximum device number.**

**Example**

Example 1

To read the states of 32 devices, X10 to X2F from station number "5" (Wait for message 0ms)

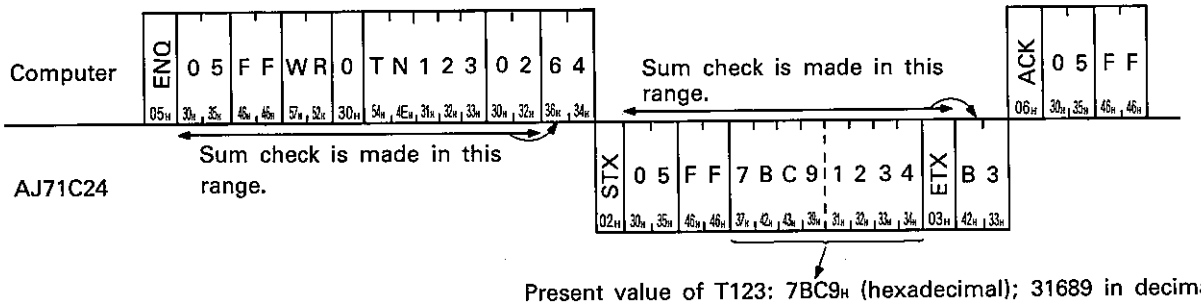



**POINT**

**WR specifies word reading (i.e. 16 bits), hence to read X40 to X5F, specify "02" for device points.**

Example 2

To read the present values of 2 devices, T123 and T124 from station number "5".




Present value of T123: 7BC9H (hexadecimal); 31689 in decimal.
Present value of T124: 1234H (hexadecimal); 4660 in decimal.



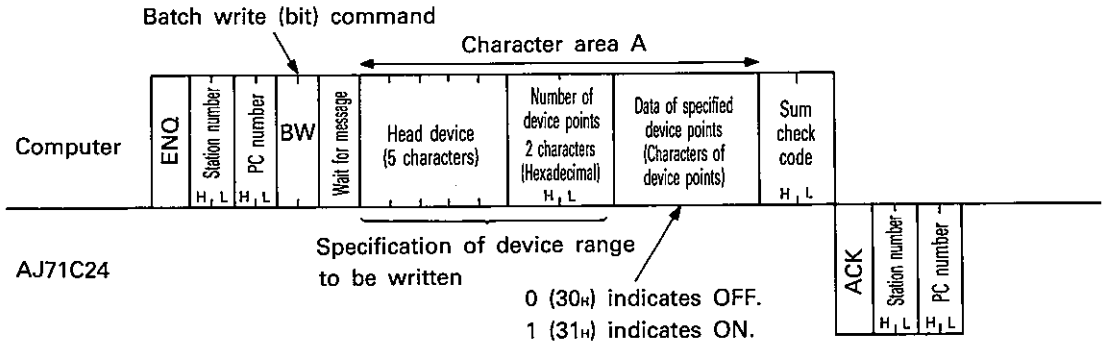
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### 6.6.4 Batch bit write

**Specifying Method**

The following example uses protocol format 1.

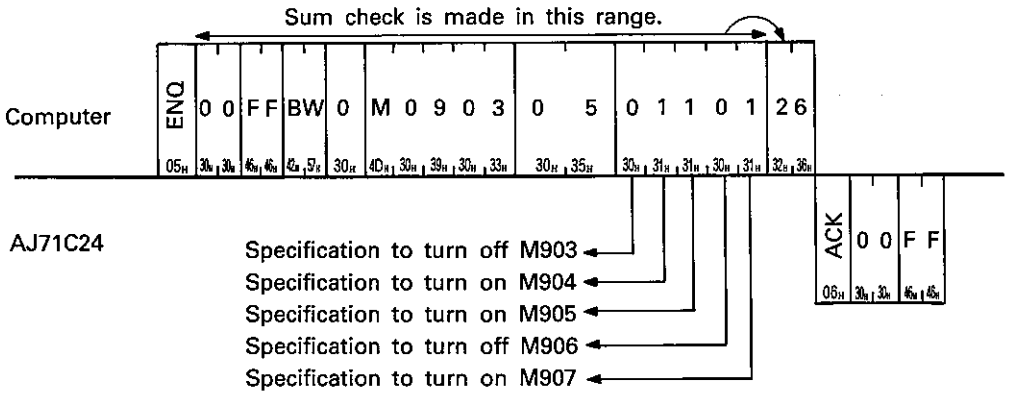



**POINT**

**Specify the number of device points, n, such that:**
- **$1 \leqq n \leqq 160$**
- **Head device number + n − 1 ≦ maximum device number.**

**Example**

To write data to 5 points, M903 to M907 at station "0" (Wait for message is 0ms)






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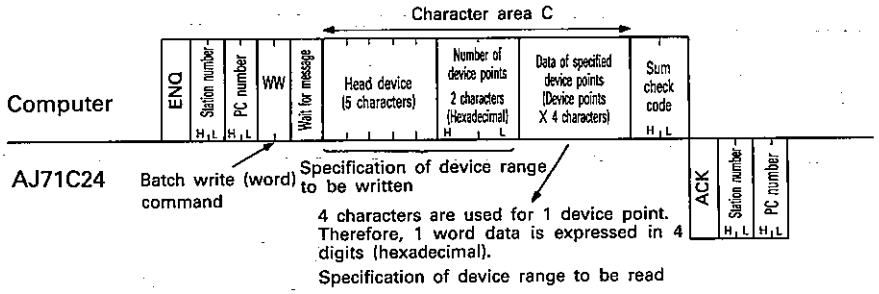
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### 6.6.5 Batch word write

The method for specifying the control protocol and examples are shown below for a batch write to word device memory and a batch write to bit device memory (16 point units).

**Specifying Method**

The following example uses protocol format 1.



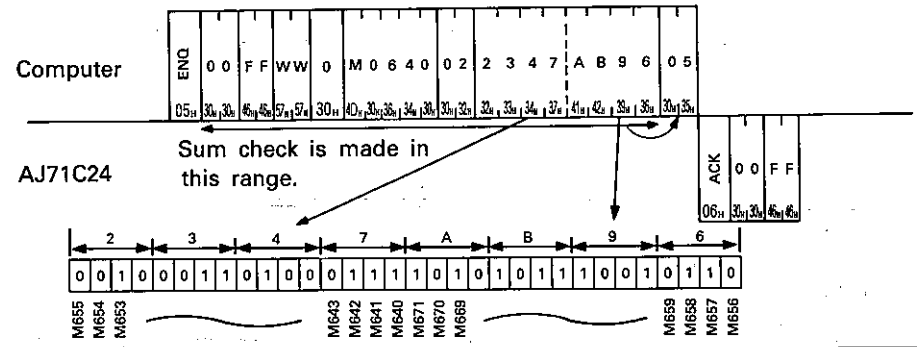

**POINT**

**Specify the number of device points, n, such that:**
- **$1 \leqq n \leqq 64$ (10 for bit device)**
- **Head device number + n (n × 16) − 1 ≦ maximum device number.**

**Example**

Example 1

To write data to the 32 points, M640 to M671 at station "0" (Wait for message is 0ms)

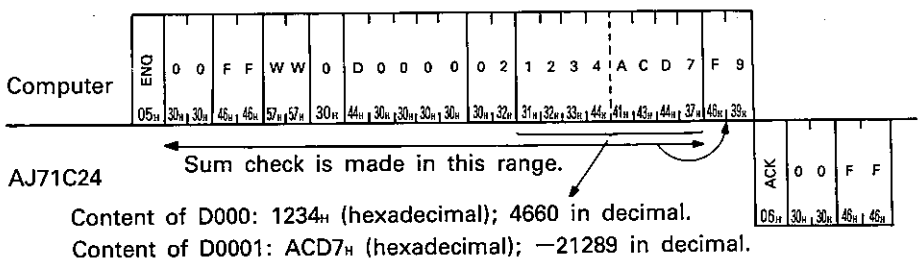



**POINT**

**WW specifies word writting (i.e. 16 bits), hence to read M640 to M671, specify "02" for device points.**

Example 2

To write data to D000 and D0001 at station "0" (Wait for message is 0ms)




Content of D000: $1234_H$ (hexadecimal); 4660 in decimal.
Content of D0001: $ACD7_H$ (hexadecimal); −21289 in decimal.

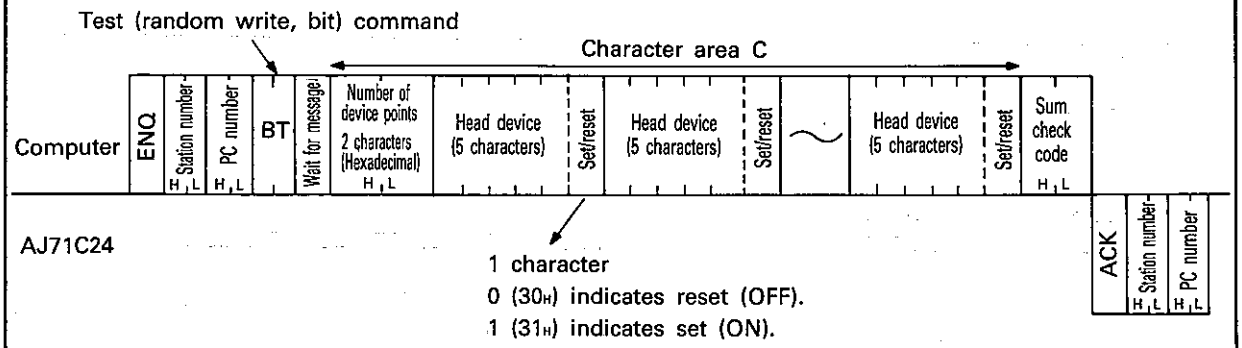


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### 6.6.6 Test — bit write

**Specifying Method**

The following example uses protocol format 1.

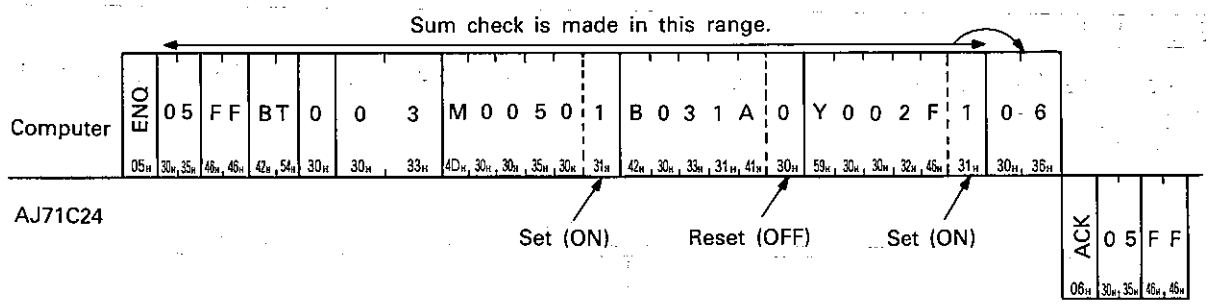



**POINT**

**Specify the number of device points, n, such that:**
**• 1 ≦ n ≦ 20**

**Example**

To switch on M50, turn off B31A, and turn on Y2F at station "5" (Wait for message is 0ms)







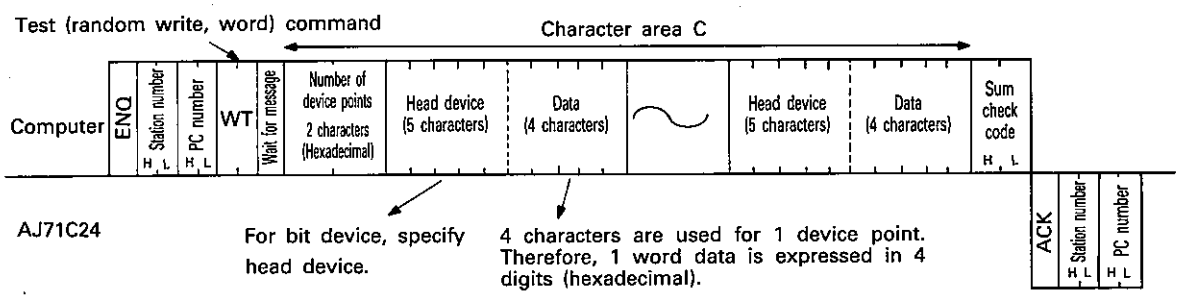

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### 6.6.7 Test — word write

The method for specifying the control protocol and examples are shown below for a random write to word device memory and bit device memory (16 point units).
Word devices and bit devices may be specified together.

**Specifying Method**

The following example uses protocol format 1.

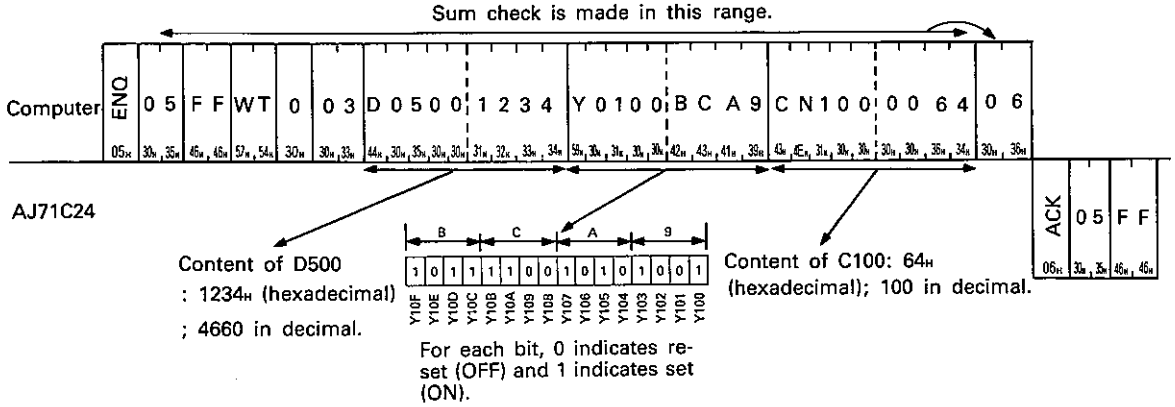



**POINT**

**Specify the number of devie points, n, such that:**
**• 1 ≦ n ≦ 10 units (16 points in 1 unit) for bit devices**

**Example**

To change the present value of D500 at station "5" to $1234_H$, Y100 to Y10F to $BCA9_H$, and the present value of C100 to $64_H$.
(Wait for message is 0ms)



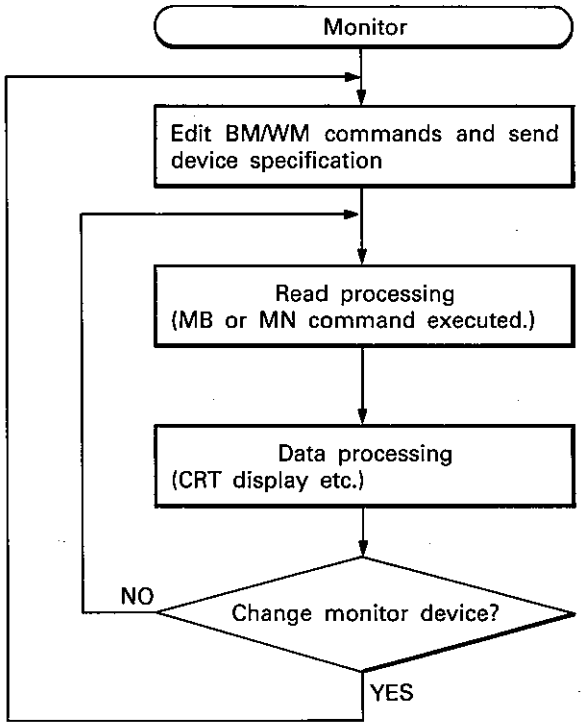



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### 6.6.8 Device memory monitor

"Monitor data entry" is the function to specify to the AJ71C24 the devices and numbers to be monitored by a computer. "Monitor" refers to the function whereby a computer monitors the data contents of the devices specified by the monitor data entry function, which are read from the PC CPU when the computer sends a monitor read instruction.
Continuous device numbers are read by batch read instructions (BR, WR). However, this function allows random device numbers to be specified for reading and monitoring of the data.
The method for specifying the control protocol and examples are shown below for the monitor function operating procedure and for entering the numbers of the devices to be monitored into the AJ71C24.

(1) Monitor operation procedure




**POINT**

**(1) The monitor data entry must be completed before executing the monitor function, as shown above. A protocol error occurs if monitor data entry is not completed before the monitor function is executed.**
**(2) The monitor data entry settings are lost when the power is turned off or the PC CPU reset.**
**(3) Three types of monitor data entry may be made: for the device memory (bit units) (BM), device memory (word units) (WM) and the expansion file register (EM), respectively.**





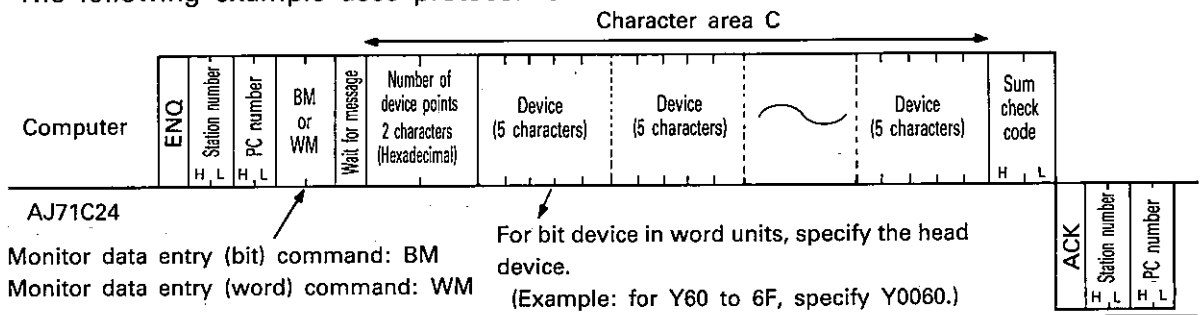


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(2) Monitor data entry

## Specifying Method

The following example uses protocol format 1.




**POINT**

**(1) Specify the number of device points, n, such that:**
- **Command BM : 1 ≦ n ≦ 40**
- **Command WM : 1 ≦ n ≦ 20 units**

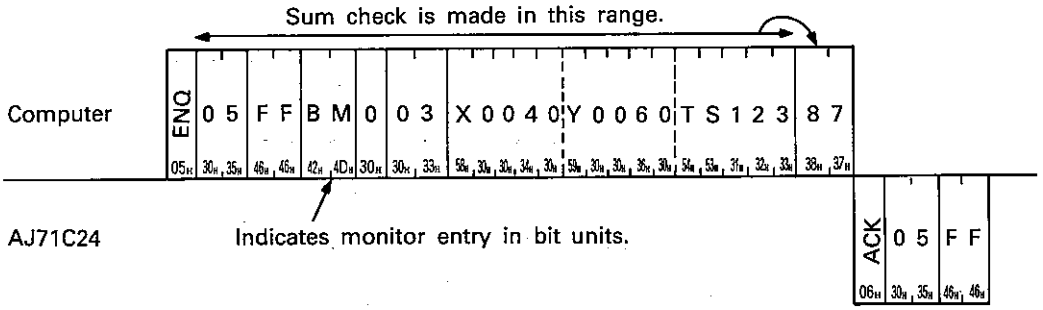
**When specifying inputs X, these values must be halved (except for A3H).**

**(2) As shown in Example 2, word devices and bit devices (16 point units) can be specified together when using command WM.**

## Example

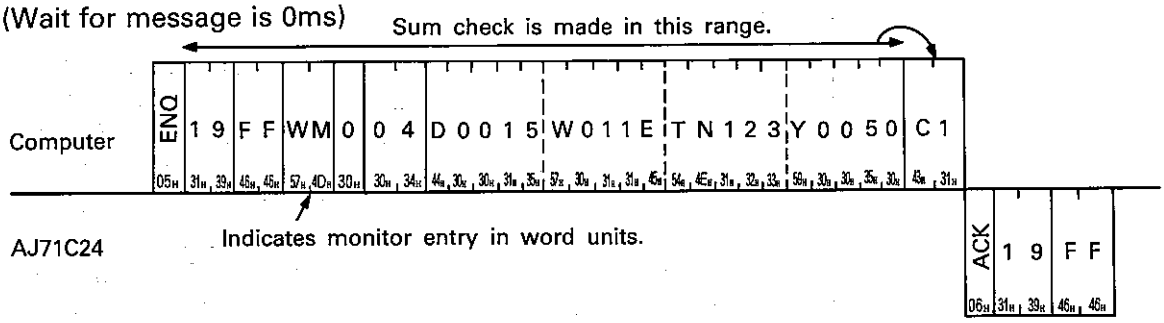
Example 1

To monitor X40, Y60, and T123 (contact) at station "5". (Wait for message is 0ms)




Example 2

To monitor D15, W11E,T123 (present value), and Y50 to 5F at station "25".
(Wait for message is 0ms)




**POINT**

**Station number is specified in hexadecimal, 19H.**



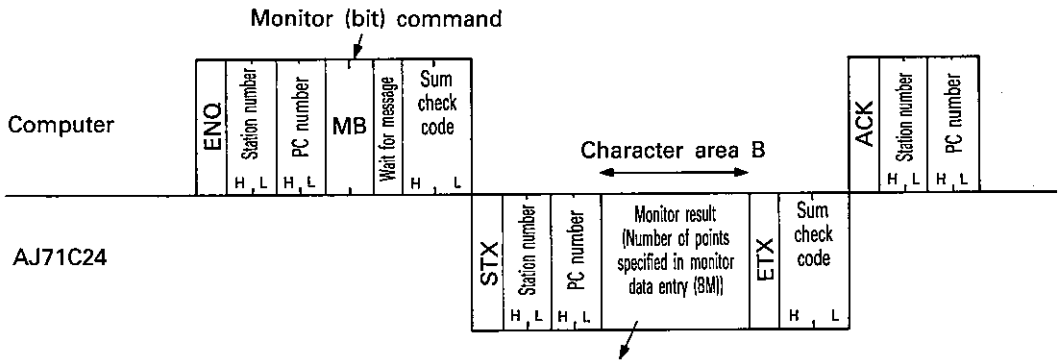
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(3) Bit monitor

The method for specifying the control protocol and examples are shown below for monitoring all the devices specified to the AJ71C24 with the monitor data entry (bit units :BM) function in (2) above.

**Specifying Method**

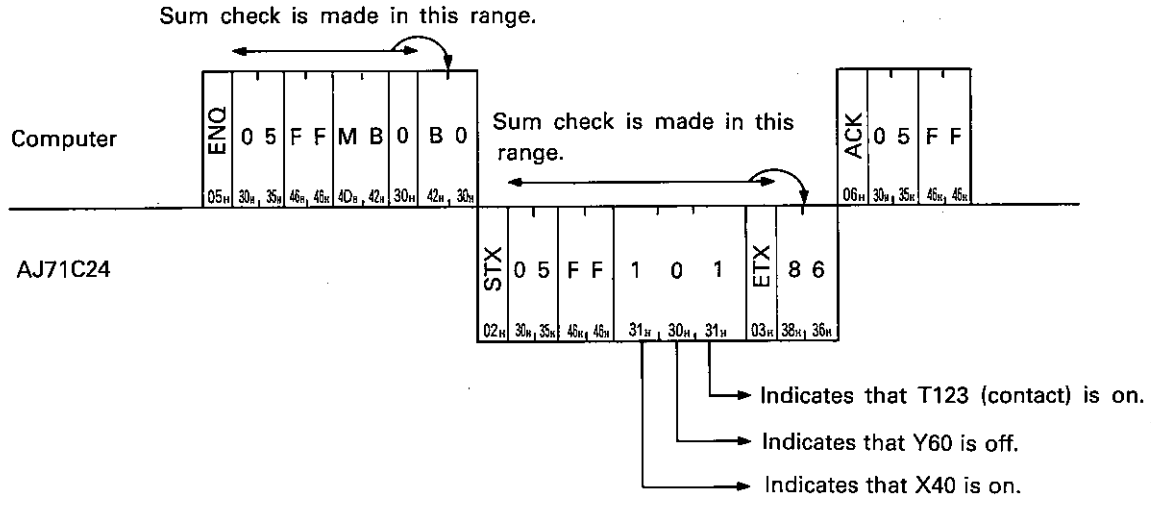
The following example uses protocol format 1.




**Example**

Example 1

To monitor the devices (bit units) specified in Example 1 in the monitor data entry section. (Wait for message is 0ms)





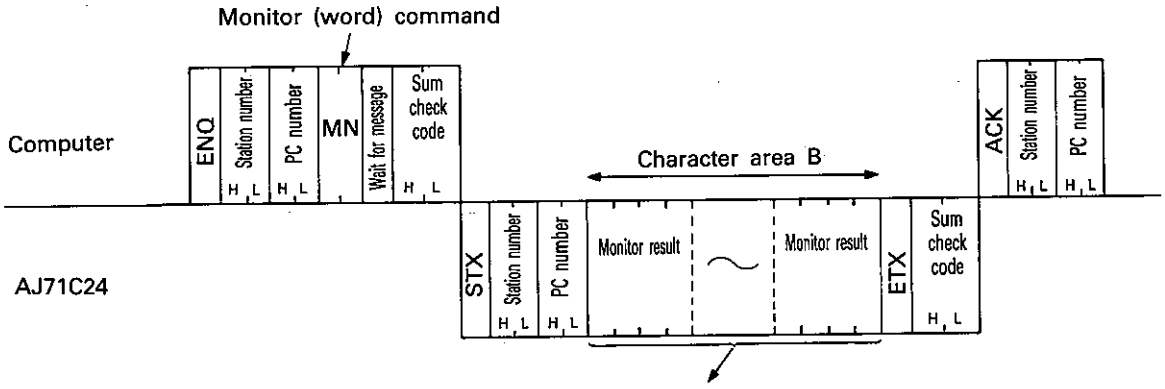

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(4) Word monitor

The method for specifying the control protocol and examples are shown below for monitoring all the devices specified to the AJ71C24 with the monitor data entry (word units :WM) function in (2) above.

**Specifying Method**

The following example uses protocol format 1.

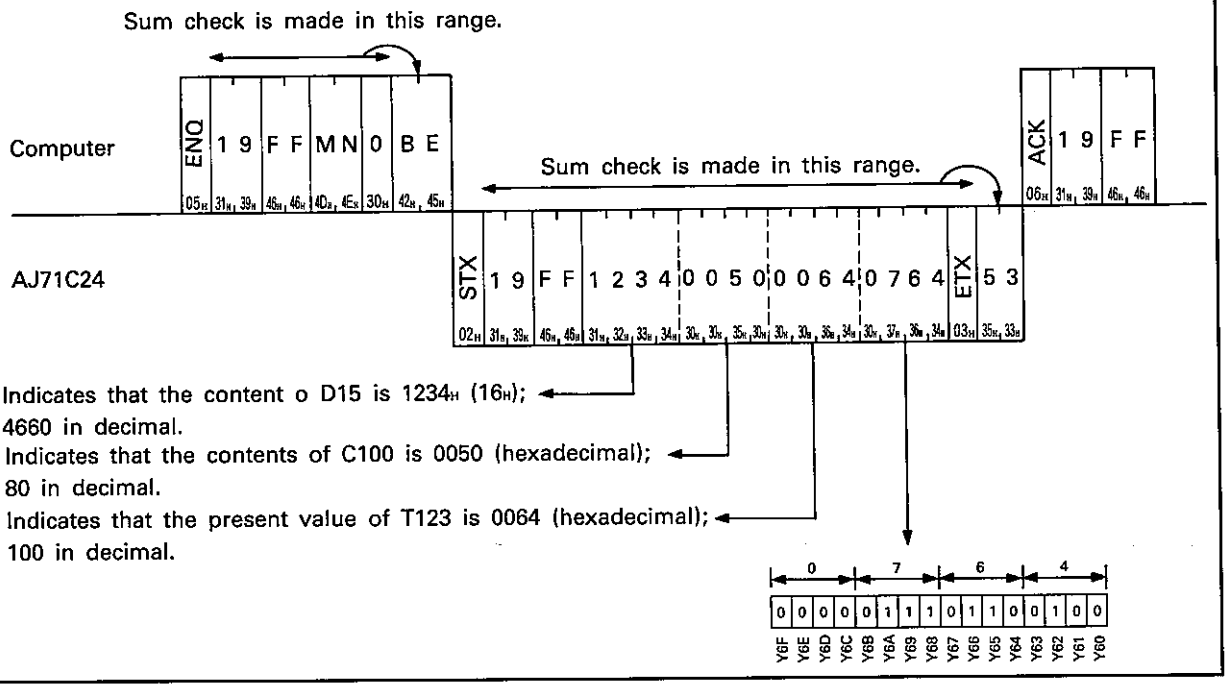



- Data of device points specified in monitor data entry (WM)
- 4 characters are used for 1 device. Therefore, 1 word data is expressed in 4 digits (hexadecimal).

**Example**

Example 2

To monitor the devices (word units) specified in Example 2 in the Monitor data entry section. (Wait for message time is 0ms.)






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## 6.7 Extension file register read and write

Extension file register refers to an empty area of the PC CPU user memory area used as a file register. The extension file register is used to store necessary data and results of calculations for data processing carried out with the software utility package SW0GHP-UTLPC-FN1 (hereafter referred to as UTLP-FN1).
The method for specifying the control protocol, explanations and examples are shown below for reading and writing to and from the extension file register.

### 6.7.1 Commands and addresses

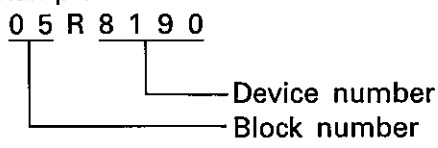
(1) The commands used for extension file register read and write operations are listed in the table below.

| Item | Command | | Processing | No. of Points Processed Per Access | State of PC CPU | | |
|---|---|---|---|---|---|---|---|
| | | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Batch read | ER | 45H, 52H | Reads extension file register (R) in units of 1 point. | 64 | ○ | ○ | ○ |
| Batch write | EW | 45H, 57H | Writes to extension file register (R) in units of 1 point. | 64 | ○ | ○ | × |
| Test (random write) | ET | 45H, 54H | Specifies the extension file register (R) in units of 1 point using block or device number and makes a random write. | 10 | ○ | ○ | × |
| Monitor data entry | EM | 45H, 4DH | Sets the device numbers to be monitored in units of 1 point. | 20 | ○ | ○ | ○ |
| Monitor | ME | 4DH, 45H | Monitors the extension file register after monitor data entry. | —— | ○ | ○ | ○ |

Key: ○ Available
× Unavailable

(2) Extension file register addresses
(a) The extension file register comprises of blocks No. 0 - 28. Block No. 0 contains the number of points specified by the PC CPU parameters and each block No. 1 - 28 has 8192 point registers.
(b) The range of block numbers which can be specified varies according to the type of memory cassette and the PC CPU parameter settings.
Refer to the UTLP-FN1 Operating Manual for details.
(c) The block and device numbers to specify addresses require 7 characters.

Example






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### 6.7.2 Precautions during extension file register read and write

Care is required with the following points when reading and writing to and from the extension file register.

(1) The extension file register is not used by A1(E) and A1NCPU. This function is not available during communication between A1(E) or A1NCPU and the PC CPU.

(2) Some types of memory cassette loaded to the PC CPU are unable to detect an error (character area error $06_H$) if an attempt is made to read or write after specifying a block number which does not exist. In this case, data which is read may not be correct and a write operation may destroy the PC CPU user memory.
Always check the type of memory cassette and the parameter settings before using this function.

| Type of Memory Cassette | Block Numbers which do not Cause a Character Area Error ($06_H$) | | |
|---|---|---|---|
| | A2(E), A3(E)CPU | A2N, A3NCPU | A3HCPU |
| A3MCA-12 | No. 10, No. 11 | | |
| A3MCA-18 | —— | No. 10 to No. 28 | |
| A3MCA-24 | —— | No. 13 to No. 20 | No. 13 to No. 28 |
| A3MCA-40 | —— | | No. 21 to No. 28 |

Refer to the UTLP-FN1 manual for details.

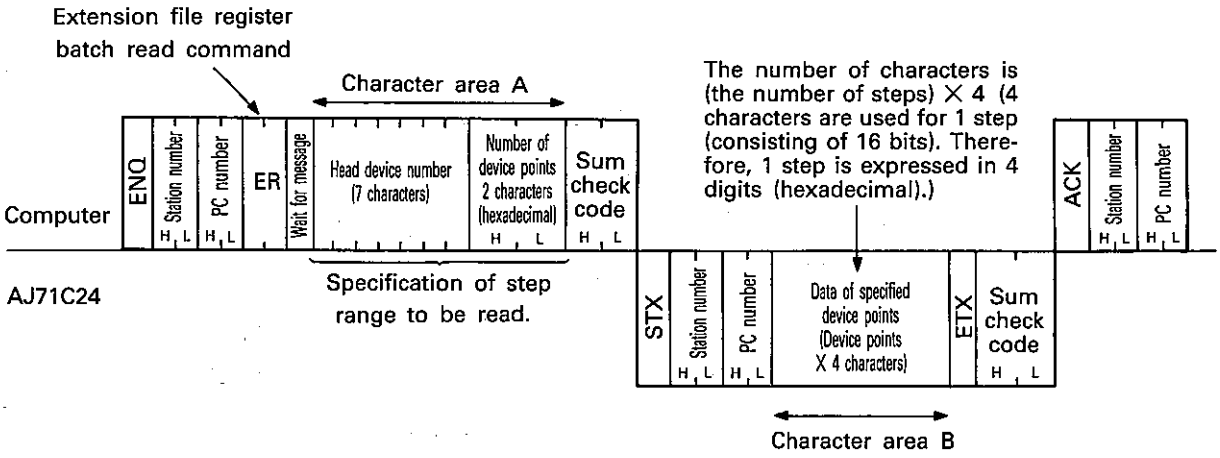


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### 6.7.3 Extension file register, batch read

**Specifying Method**

The following example uses protocol format 1.

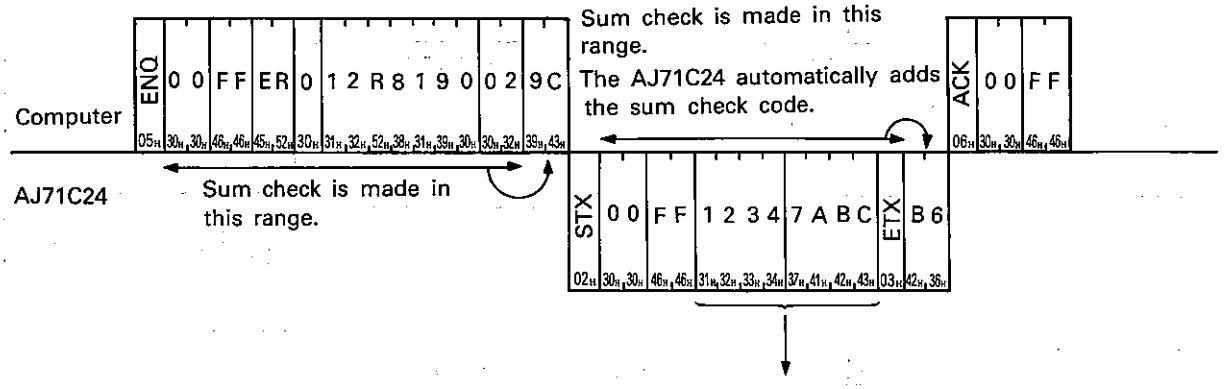



**POINT**

**Specify the number of device points, n, such that:**
- **1 ≦ n ≦ 64**
- **Head device number + n ≦ maximum device number**

**Example**

To read data from 2 points, R8190 and R8191 of block No. 12 of the station number 0 CPU extension file register. (Wait for message is 0ms)




Indicates that:
hexadecimal 1234H (decimal 4660) is written to R8190 of block No. 12
hexadecimal 7ABCH (decimal 31420) is written to R8191 of block No. 12



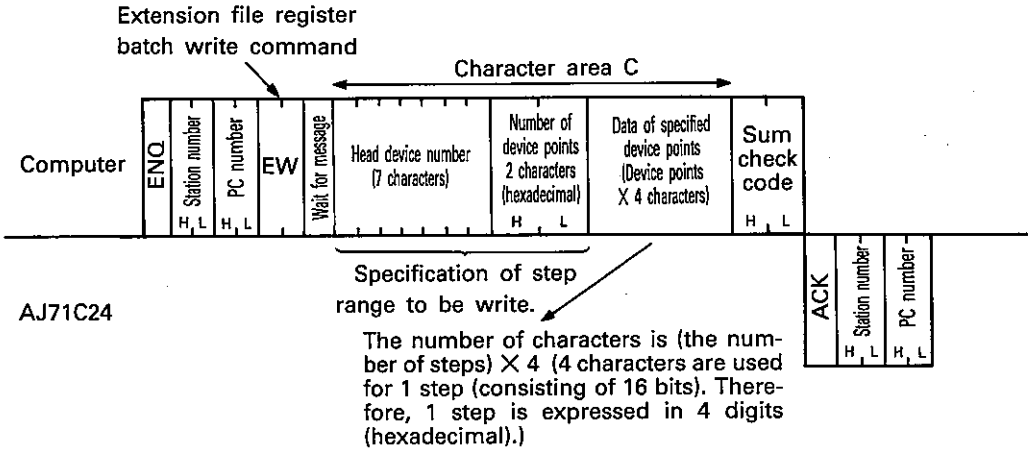


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### 6.7.4 Extension file register, batch write

**Specifying Method**

The following example uses protocol format 1.

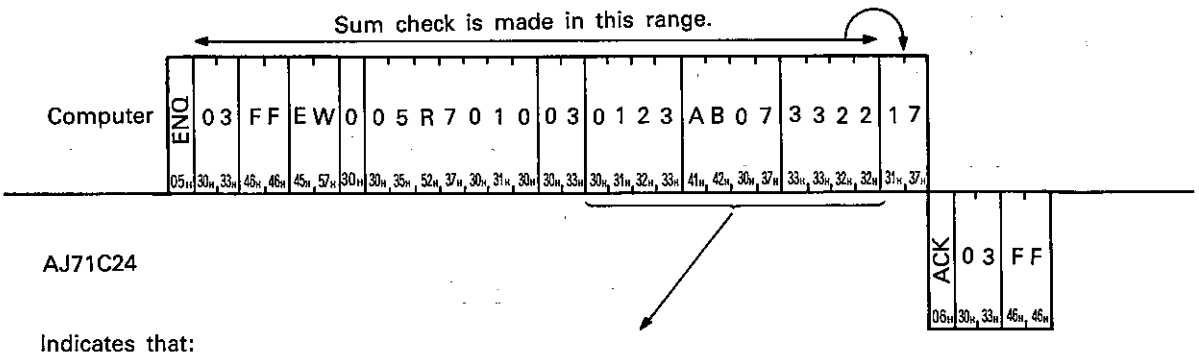



**POINT**

**Specify the number of device points, n, such that:**
- **1 ≦ n ≦ 64**
- **Head device number + n ≦ maximum device number**

**Example**

To write data to 3 points R7010 - R7012 of block No. 05 of the station number 3 CPU extension file register. (Wait for message is 0ms)




Indicates that:
hexadecimal 0123H (decimal 291) is written to R7010 of block No. 05
hexadecimal AB07H (decimal −21753) is written to R7010 of block No. 05
hexadecimal 3322H (decimal 13090) is written to R7010 of block No. 05
The AJ71C24 automatically adds the sum check code.

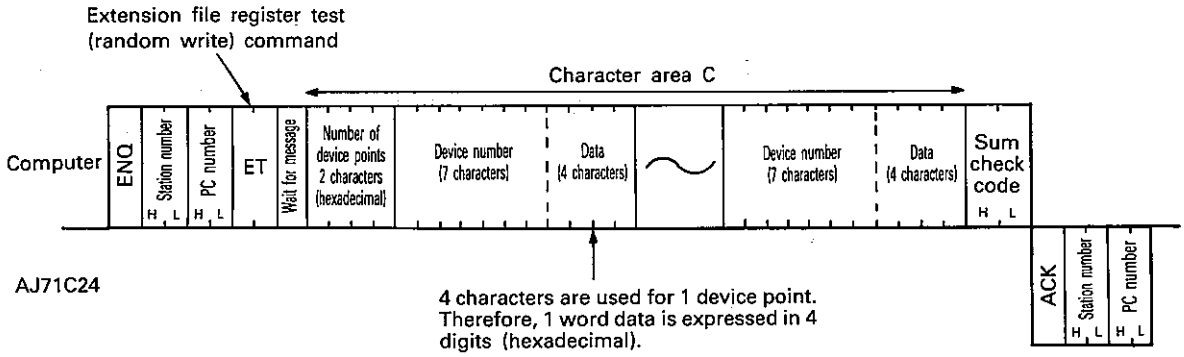


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### 6.7.5 Extension file register test - random write

**Specifying Method**

The following example uses protocol format 1.

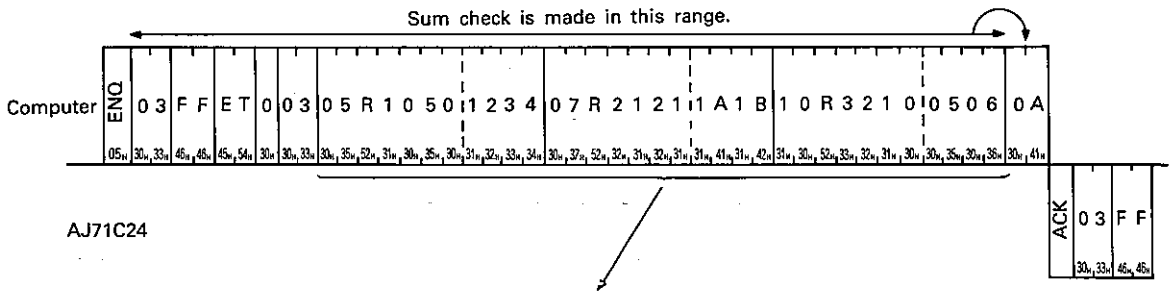



**POINT**

**Specify the number of device points, n, such that:**
**• 1 ≦ n ≦ 10 units**

**Example**

To write data to R1050 of block No. 5, R2121 of block No. 7 and R3210 of block No. 10 of the station number 3 CPU extension file register. (Wait for message time is 10ms.)




Indicates that:
hexadecimal $1234_H$ (decimal 4660) is written to R1050 of block No. 05
hexadecimal $1A1B_H$ (decimal 666883) is written to R2121 of block No. 07
hexadecimal $0506_H$ (decimal 12866) is written to R3210 of block No. 10

6



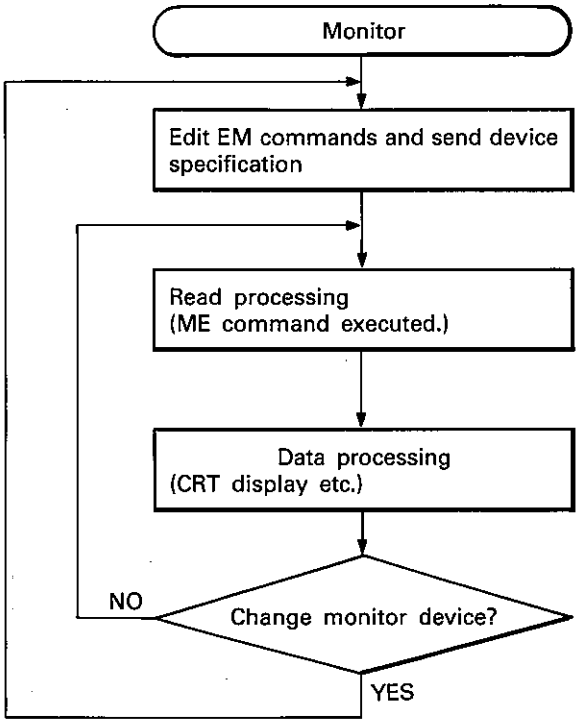
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### 6.7.6 Extension file register monitor

"Monitor data entry" is the function to specify to the AJ71C24 the devices and numbers to be monitored by a computer. "Monitor" refers to the function whereby a computer monitors the data contents of the devices specified by the monitor data entry function, which are read from the PC CPU when the computer sends a monitor read instruction.
Continuous device numbers are read by batch read instructions (ER). However, this function allows random device numbers to be specified for reading and monitoring of the data.
The method for specifying the control protocol and examples are shown below for the monitor function operating procedure and for entering the numbers of the devices to be monitored into the AJ71C24.

(1) Monitor operation procedure




**POINT**

**(1) The monitor data entry must be completed before executing the monitor function, as shown above. A protocol error occurs if monitor data entry is not completed before the monitor function is executed.**
**(2) The monitor data entry settings are lost when the power is turned off or the PC CPU reset.**
**(3) Three types of monitor data entry may be made: for the expansion file register (EM), device memory (bit units) (BM) and device memory (word units) (WM).**

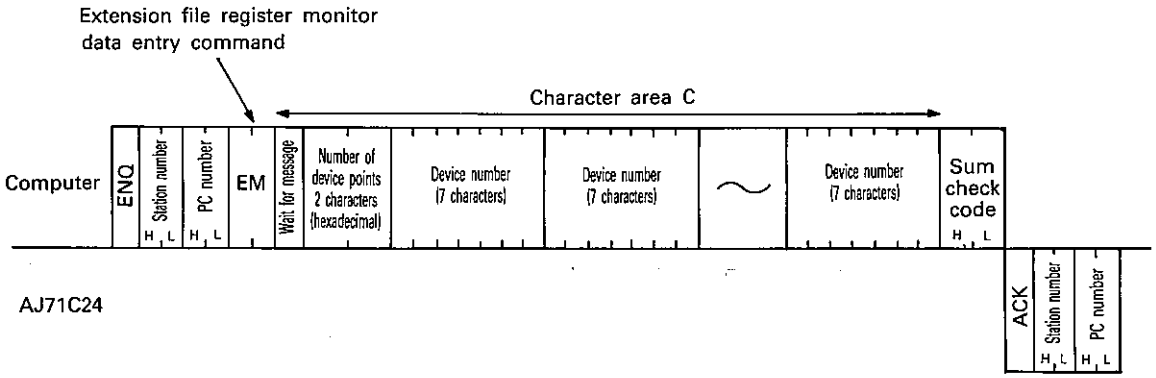


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(2) Extension file register monitor data entry
The method for specifying the control protocol and an example are shown below for entering the extension file register device numbers to be monitored into the AJ71C24.

## Specifying Method

The following example uses protocol format 1.

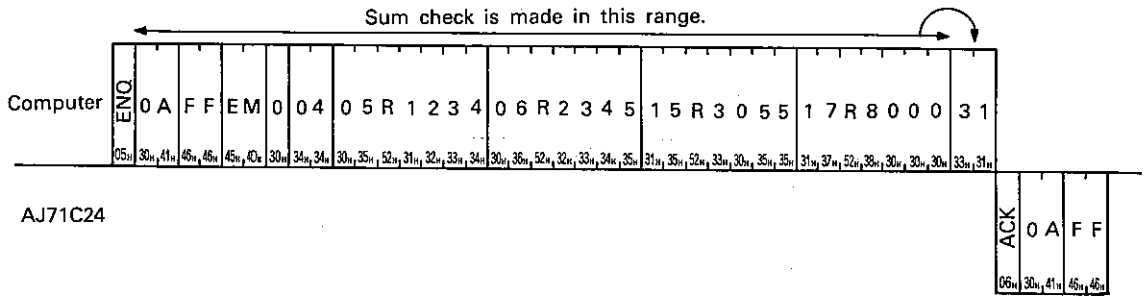



**POINT**

**Specify the number of device points, n, such that:**
**• 1 ≦ n ≦ 20 units**

## Example

To write data to R1234 of block No. 5, R2345 of block No. 6, R3055 of block No. 15 and R8000 of block No. 17 of the station number 10 CPU extension file register. (Wait for message is 0ms.)




**POINT**

**Station number 10 is specified in hexadecimal, 0A$_{H}$.**

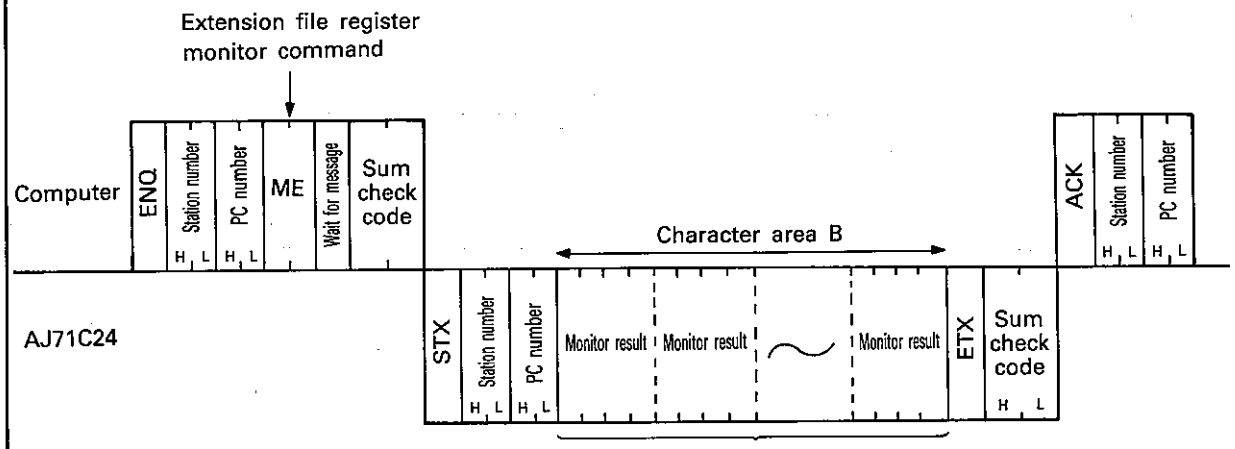


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(3) Extension file register monitor
The method for specifying the control protocol and examples are shown below for monitoring all the devices specified to the AJ71C24 with the monitor data entry (EM) function in (2) above.

**Specifying Method**

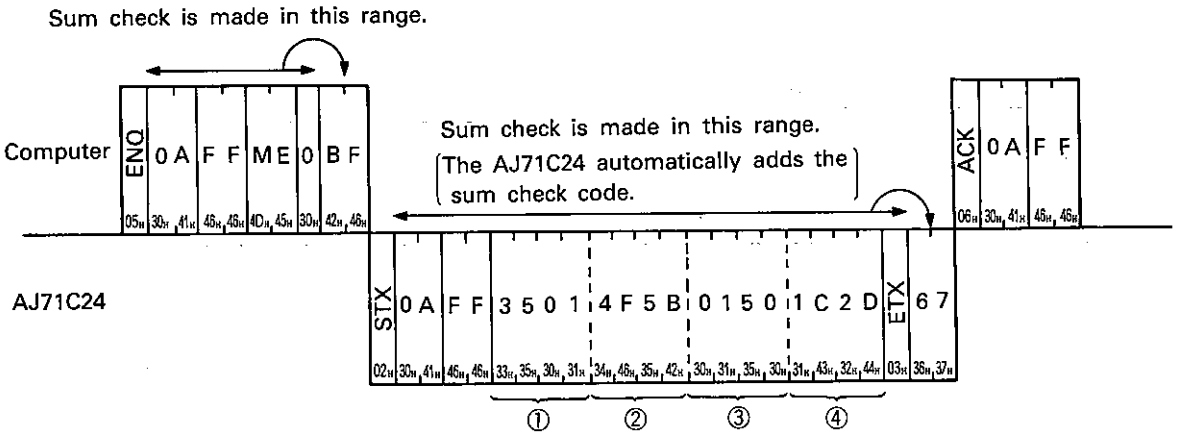
The following example uses protocol format 1.




- Characters of points specified in monitor data entry (EM)
- 4 characters are used for 1 device point. Therefore, 1 data word is expressed in 4 digits (hexadecimal).

**Example**

To monitor the devices specified by the monitor data entry in (2) above. (Wait for message is 0ms.)




①hexadecimal 3501H (decimal 13569) is written to R1234 of block No. 05
②hexadecimal 4F5BH (decimal 20315) is written to R2345 of block No. 06
③hexadecimal 0150H (decimal 336) is written to R3055 of block No. 15
④hexadecimal 1C2DH (decimal 7213) is written to R8000 of block No. 17



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## 6.8 Buffer Memory Transfer

This function is used to read from and write to the AJ71C24 buffer memory. When this function is used, communication between the computer and AJ71C24 commences immediately the computer sends a read or write request, without waiting for the PC CPU END processing. Therefore, the time T1, described in section 6.4, is always equal to zero. The PC CPU carries out reads and writes of the buffer memory using TO and FROM instructions.
The method for specifying the control protocol, meanings and examples are shown below for carrying out this function.

### 6.8.1 Commands and buffer memory

This section explains the read/write operations to the AJ71C24 buffer memory.

(1) Commands

| Item | Command | | Processing | Number of Points Processed Per Communication | State of PC CPU | | |
|---|---|---|---|---|---|---|---|
| | | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Batch read | CR | 43H, 52H | Reads buffer memory. | 64 words (128 bytes) | ○ | ○ | ○ |
| Batch write | CW | 43H, 57H | Writes to buffer memory. | | | | |

Key : ○ Available

(2) Buffer memory
Buffer memory addresses are 0H to 7FFH (Section 3.5).
One address consists of 1 word (16 bits).
Read and write are both carried out in word units, regardless of the word/byte unit setting.

**POINT**

**(1) When the no-protocol mode (see Chapter 7) is used at the same time as this function, make sure that buffer memory addresses are not duplicated.**
**(2) Buffer addresses 100H to 11FH comprise the special-application area. The AJ71C24 will not operate correctly if any operations other than those described in the sections are carried out.**

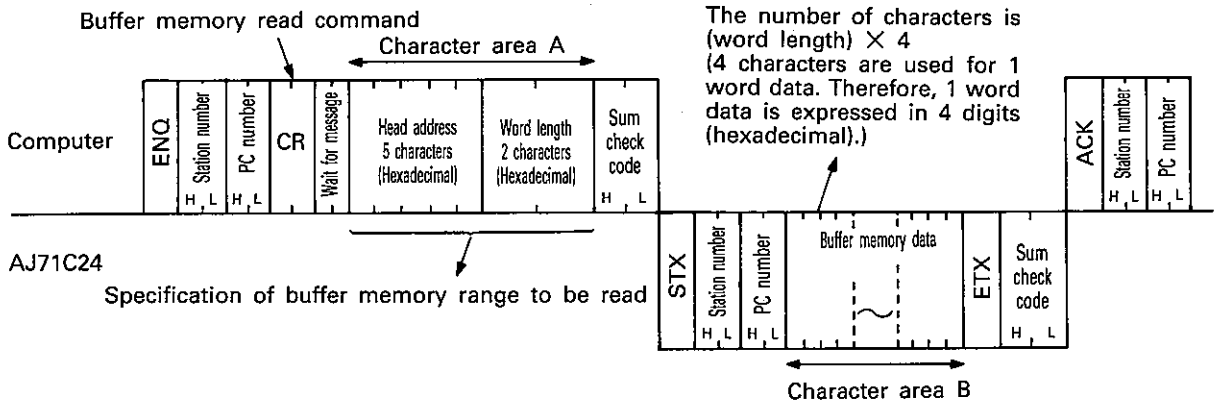


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### 6.8.2 Buffer memory read

**Specifying Method**

The following example uses protocol format 1.

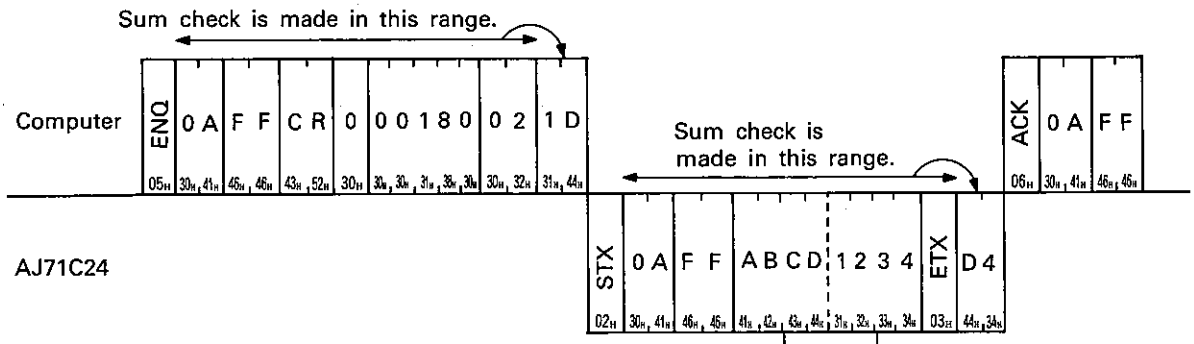



**POINT**

**Specify word length, L, such that:**
- **1 ≦ word length ≦ 64**
- **Head address + L − 1 ≦ maximum address number ($7FF_H$)**

**Example**

To read buffer addresses $180_H$ to $181_H$ at station "10". (Wait for message is 0ms)




Indicates that the content of buffer memory address $180_H$ is $ABCD_H$ (21555).
Indicates that the content of buffer memory address $181_H$ is $1234_H$ (4660).

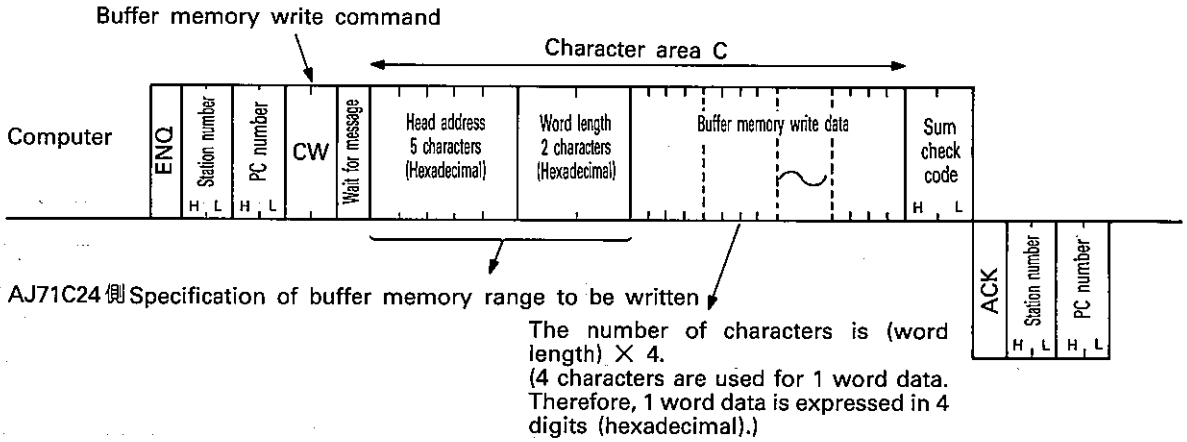


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### 6.8.3 Write to buffer memory

**Specifying Method**

The following example uses protocol format 1.

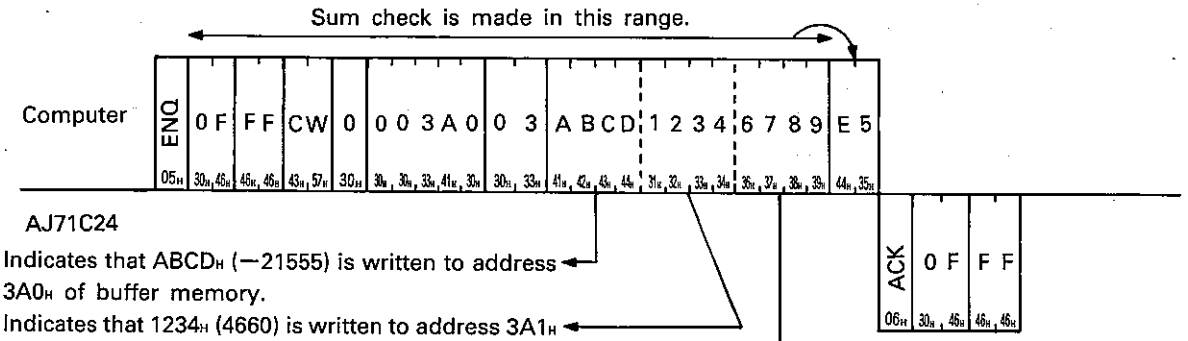



**POINT**

**Specify the word length, L, such that:**
- **1 ≦ L ≦ 64**
- **Head address + L − 1 ≦ maximum address number ($7FF_H$)**

**Example**

To write data to buffer addresses $3A0_H$ to $3A2_H$ at station "15".
(Wait for message is 0ms)






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## 6.9 Special-function module buffer memory transfer

The method for specifying the control protocol and examples are shown below for reading data to and writing data from the special-function module buffer memory.
These commands all access the special-function module buffer memory in byte units.

### 6.9.1 Commands

(1) Commands

| Item | Command | | Processing | Number of Points Processed Per Communication | State of PC CPU | | |
|---|---|---|---|---|---|---|---|
| | | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Batch read | TR | 54H, 52H | Reads special-function module buffer memory | 64 words (128 bytes) | ○ | ○ | ○ |
| Batch write | TW | 54H, 57H | Writes to special-function module buffer memory | | ○ | ○ | × |

Key : ○ Available

(2) Linkable special-function modules, buffer memory head address, module numbers

| Special-Function Module Name | Buffer Memory Head Address (hexadecimal) | Module Number when Mounted in Slot No. 0 |
|---|---|---|
| A68AD analog/digital converter module | 80H | 01H |
| A62DA digital/analog converter module | 10H | 01H |
| A84AD analog/digital converter module | 10H | 02H |
| AD61 high-speed counter module | 80H | 01H |
| AD71(S1) positioning module | 200H | 01H |
| AD72 positioning module | 200H | 02H |
| AD51 intelligent communication module | 800H | 02H |
| AJ71C24-S3 computer link module | 1000H | 01H |
| A81CPU PID control module | 200H | 03H |



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(3) Principle of the special-function module buffer memory

The special-function module buffer memory comprises of 16-bit (one word) addresses. Read and write of the special-function module buffer memory is carried out by TO and FROM instructions sent between the PC CPU and special-function module.

When the computer makes a read from and write to the special-function module buffer memory via the AJ71C24, they are carried out in byte units (1 address = 8 bits).

The addresses specified in the computer (hexadecimal) are converted from FROM / TO instruction addresses as shown below:

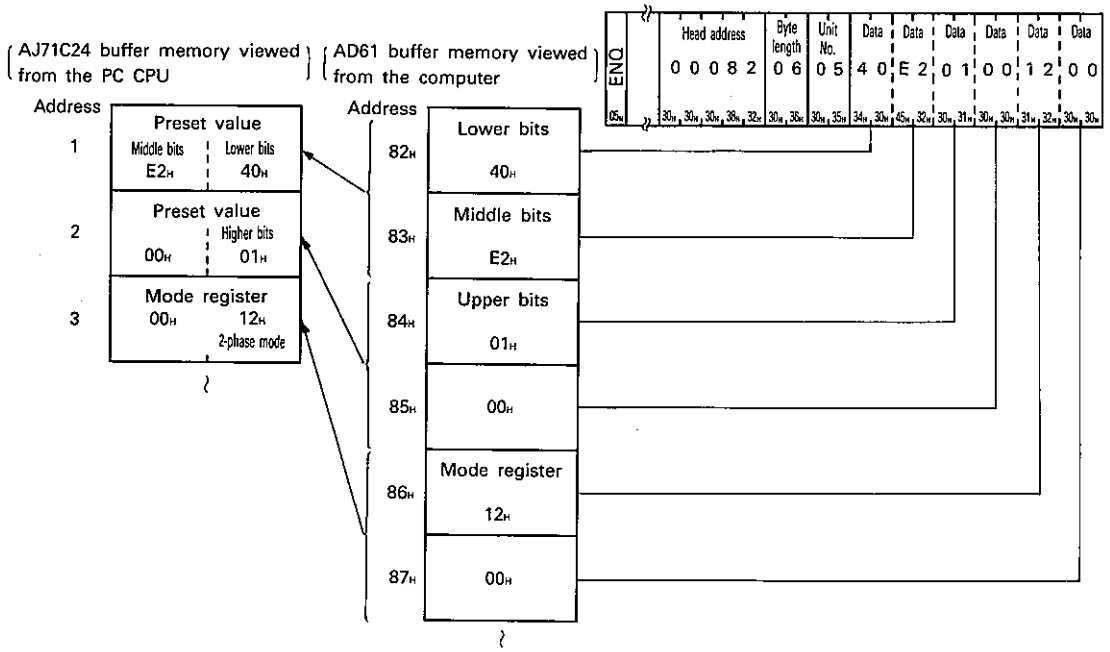
| Specified address (hexadecimal) = Module head address + {(FROM / TO instruction address × 2) converted into hexadecimal} |
|---|

Example

To specify AD61 high-speed counter module FROM / TO instruction addresses (CH.1 preset value).

Specified address $82_H$ = FROM / TO instruction address $2_H$ × 1 + Head address $80_H$

The data format when the computer makes a read or write to or from the special-function module buffer memory via the AJ71C24, is explained below using the AD61 module as an example.




**POINT**

**The buffer memory in each special-function module has its read and write area, read-only and write-only areas and areas reserved for OS use, which are not available to the user. Refer to the manual for each module before using this function.**

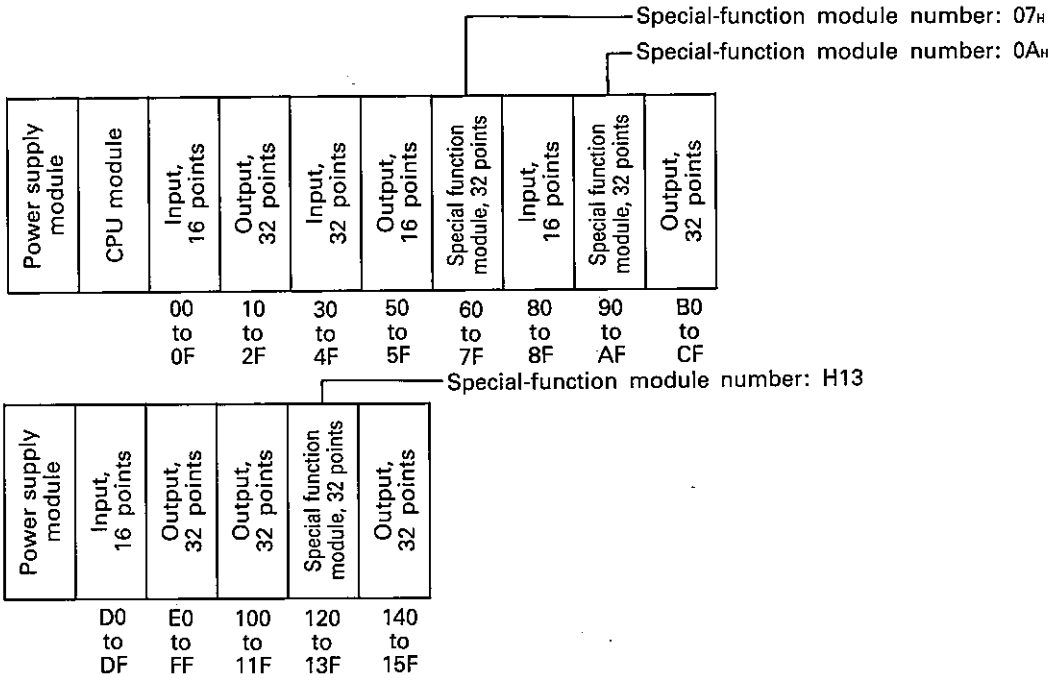
**PC CPU or special-function module errors may occur if reading or writing is carried out incorrectly.**



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### 6.9.2 Principle of special-function module numbers in control protocols

(1) Special-function module numbers specified in control protocols are the upper 2 digits of the last special-function module I/O address expressed in 3 digits.

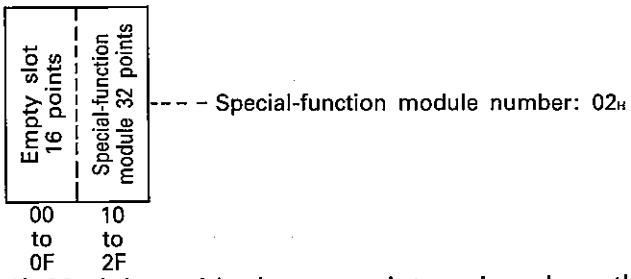



(2) Precautions with special-function modules occupying two slots

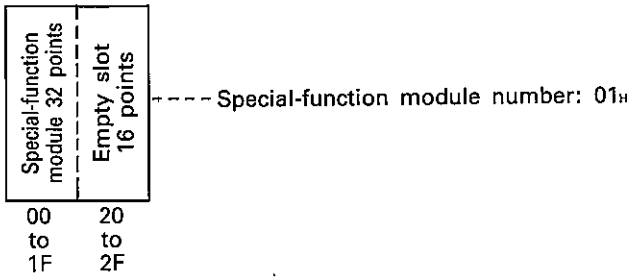
For special-function modules occupying two slots, the number of points occupied by each slot is fixed for each module. The special-function module number is the upper 2 digits of the last address of the slot assigned to the special-function module.

Refer to the User's manual for each special-function module for details of the allocation of slots to each module.

1) Modules with the front slot assigned as the empty slot (AD72, A84AD, etc.)



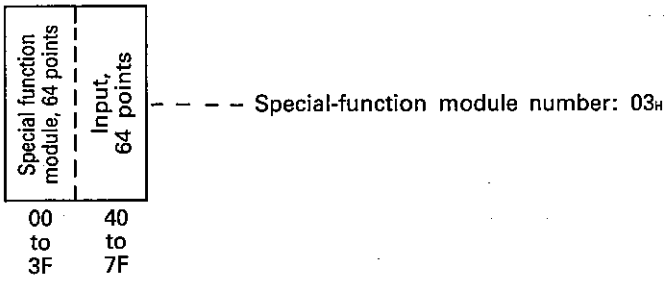

2) Modules with the rear slot assigned as the empty slot






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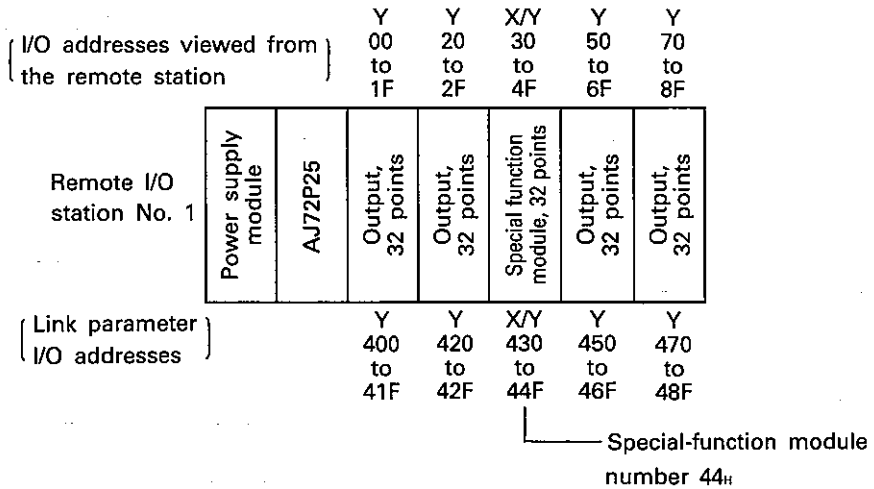
3) Modules with the special-function module assignment and I/O assignment mixed (A81CPU, etc.)




(3) Module numbers of special-function modules at MELSECNET remote stations

The module numbers of special-function modules at MELSECNET remote stations are determined by the setting of the link parameters at the MELSECNET master station.

| L/R No. | M ← L | | M → R | M ← R | M → L/R | | M ← L/R | |
|---|---|---|---|---|---|---|---|---|
| | B | W | W | W | Y | X/Y | X | Y/X |
| R1 | ------ | ------ | 29C—309 | 0F9—15E | 400—48F | 000—08F | 430—44F | 030—04F |
| R2 | ------ | ------ | 215—24F | 080—0A3 | 510—67F | 010—17F | 500—65F | 000—15F |
| R3 | ------ | ------ | 1B6—214 | 15F—1B5 | 270—32F | 050—10F | 220—28F | 000—06F |
| | — | — | — | — | — | — | — | — |
| | — | — | — | — | — | — | — | — |
| | — | — | — | — | — | — | — | — |
| | — | — | — | — | — | — | — | — |
| | — | — | — | — | — | — | — | — |





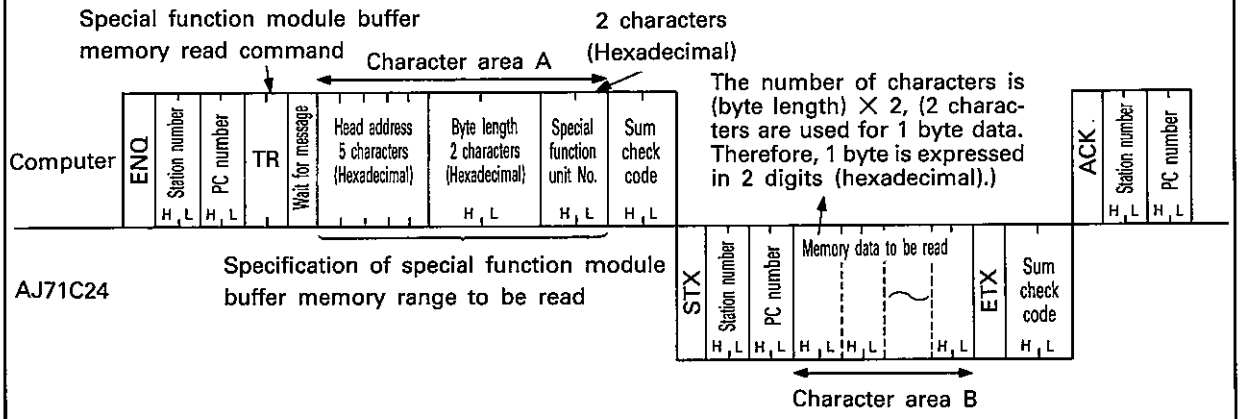

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### 6.9.3 Special function module buffer read

**Specifying Method**

The following example uses protocol format 1.



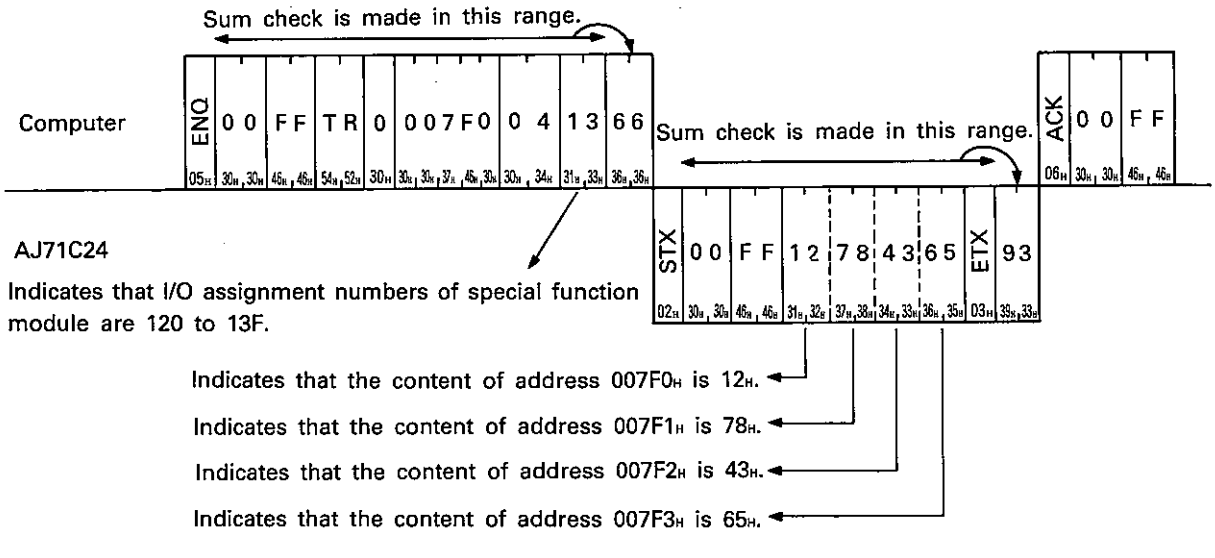

**POINT**

**(1) Specify the byte length, L, such that:**
**• 1 ≦ L ≦ 128**

**(2) Data may consist of 2 or 3 bytes depending on the special function module being used. Refer to the User's manual for each special-function module for details of specifying the byte length.**

**Example**

To read 4 bytes, 07F0H to 07F3H of the buffer memory of special function module (No. 13H) assigned to 120 to 13F at station "0". (Wait for message is 0ms)





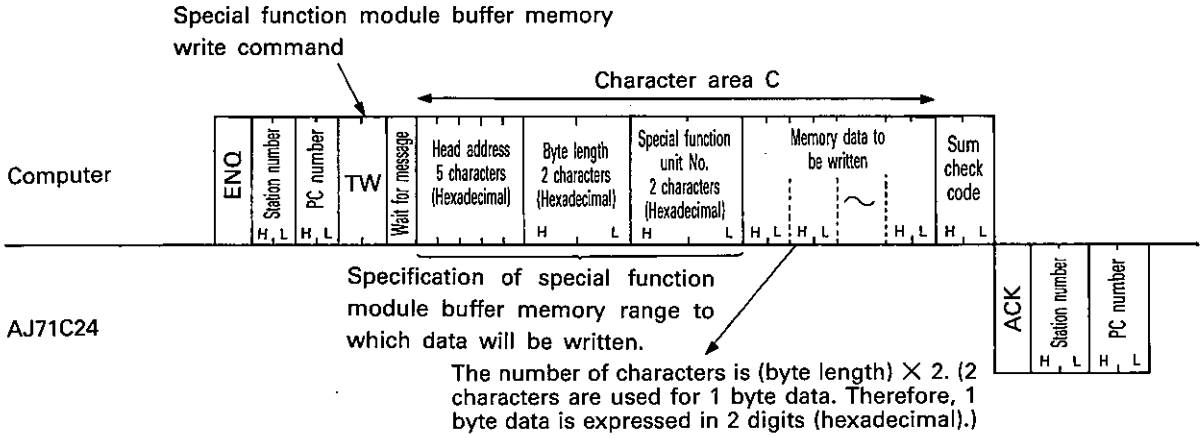

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### 6.9.4 Write to special function module buffer

**Specifying Method**

The following example uses protocol format 1.



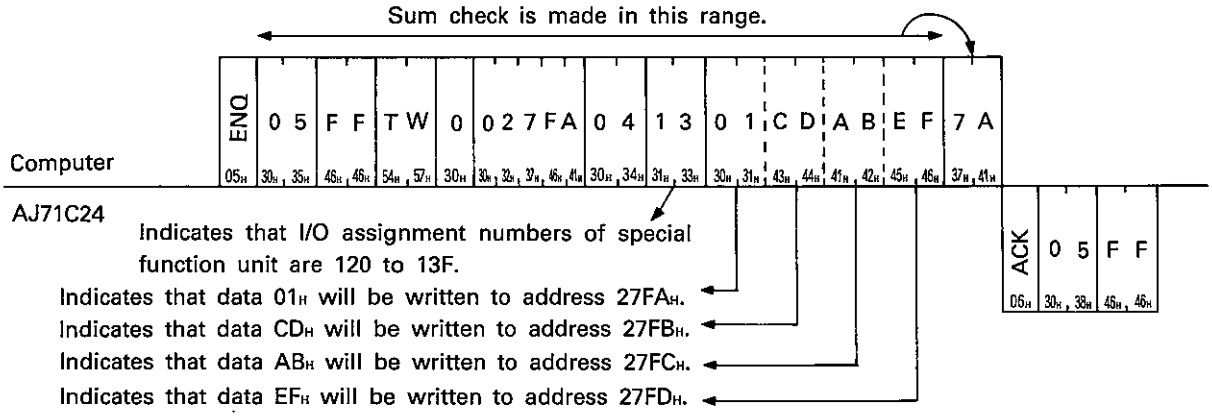

**POINT**

**(1) Specify the byte length, L, such that:**
**• 1 ≦ L ≦ 128**

**(2) Data may consist of 2 or 3 bytes depending on the special function module being used. Refer to the User's manual for each special-function module for details of specifying the byte length.**

**Example**

To write data to bytes, 27FA$_H$ to 27FD$_H$ of the special function module (13$_H$) buffer memory assigned to 120 to 13F in station "5". (Wait for message is 0ms)






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## 6.10 Control of the Programmable Controller CPU

This function is used for the remote RUN/STOP control of the PC CPU and to read the type of PC CPU linked to the computer. The method for specifying the control protocol, meaning and examples are shown below.

### 6.10.1 Commands

(1) The commands used for remote RUN/STOP control and to read PC CPU type are listed in the table below.

| Item | Command | | Processing | PC CPU State | | |
|---|---|---|---|---|---|---|
| | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | SW22 ON | SW22 OFF |
| Remote run | RR | $52_H$, $52_H$ | Demands remote run of PC CPU. | ○ | ○ | ○ |
| Remote stop | RS | $52_H$, $53_H$ | Demands remote stop of PC CPU. | ○ | ○ | ○ |
| PC type mode | PC | $50_H$, $43_H$ | Reads if the PC CPU is type A1N, A2N, A3N, A3H or AJ72P25/R25. | ○ | ○ | ○ |

Key : ○ Available



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### 6.10.2 Remote RUN/STOP

(1) Remote RUN/STOP control

(a) Remote RUN/STOP commands from the computer are valid as follows for different CPU key switch positions:

| | | PC CPU Key Switch Position | | | |
|---|---|---|---|---|---|
| | | RUN | STOP | PAUSE | STEP-RUN |
| Command from computer | Remote RUN | RUN | STOP | PAUSE | STEP-RUN |
| | Remote STOP | STOP | STOP | STOP | STOP |

**REMARKS**

(a) When remote stop has been executed at a given PC CPU from another source, e.g. an A6GPP etc., that CPU cannot be switched to run mode by the host computer.

(b) The clearing of data memories on receiving a remote run instruction depends on the states of special relays M9016 and M9017.

| Special Relay | | Data Memory State |
|---|---|---|
| M9016 | M9017 | |
| OFF | OFF | CPU is run without clearing data memory. |
| OFF | ON | Data memory is cleared outside the latch range set in parameters. (In this case, Link X image is not cleared.) |
| ON | ON/OFF | CPU is run after data memory is cleared. |

**REMARKS**

Always reset special relays M9016 and M9017 where data memory clearing is not required.

**POINT**

**After carrying out remote RUN/STOP control with the computer, the remote data is deleted when the power supply is turned off or the PC CPU is reset.**



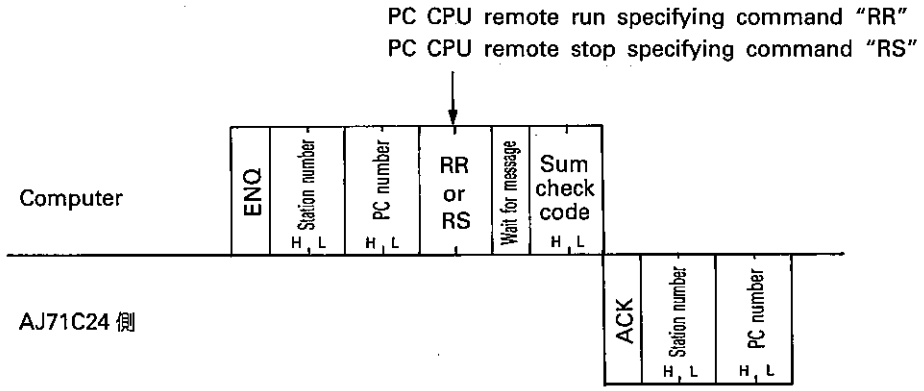


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(2) Remote RUN/STOP specification and examples
The method for specifying the control protocol and examples are shown below for remote RUN/STOP control of the PC CPU by the computer.

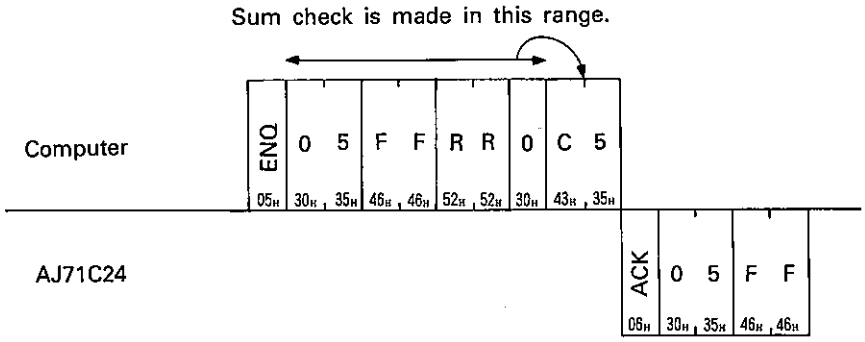
**Specifying Method**

The following example uses protocol format 1.

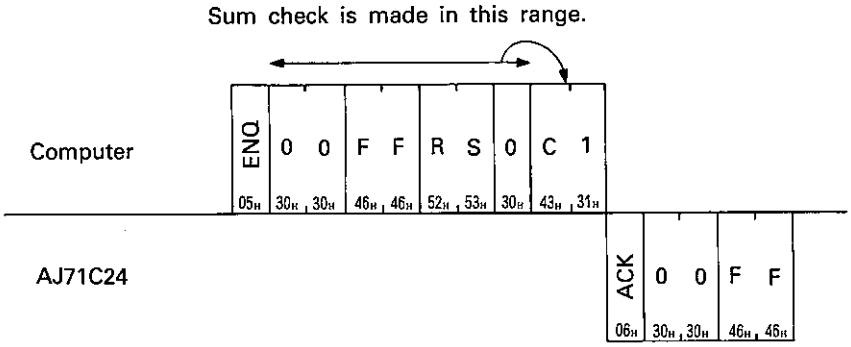



**Example**

Example 1
Remote run of station "5". (Wait for message is 0ms)




Example 2
Remote stop of station "0". (Wait for message is 0ms)




6



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### 6.10.3 PC type read

This function indicates the type of PC CPU linked to the computer.

(1) Returned code and PC CPU types

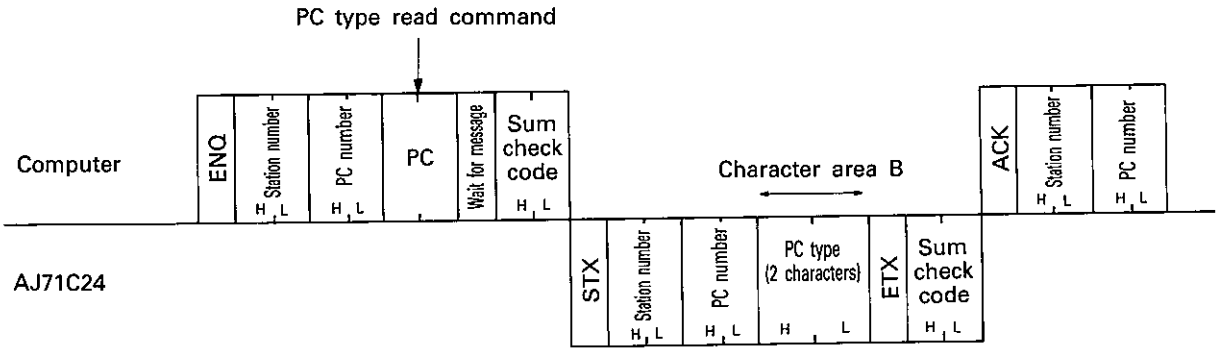
| PC CPU Type | Code Specified for Protocol (Hexadecimal) |
|---|---|
| A3HCPU | A4H |
| A3NCPU, A3(E)CPU | A3H |
| A2NCPU, A2(E)CPU | A2H |
| A1NCPU, A1(E)CPU | A1H |
| AJ72P25/R25 | ABH |

(2) PC type read

The method for specifying the control protocol and examples are shown below for reading the type of PC CPU linked to the computer.

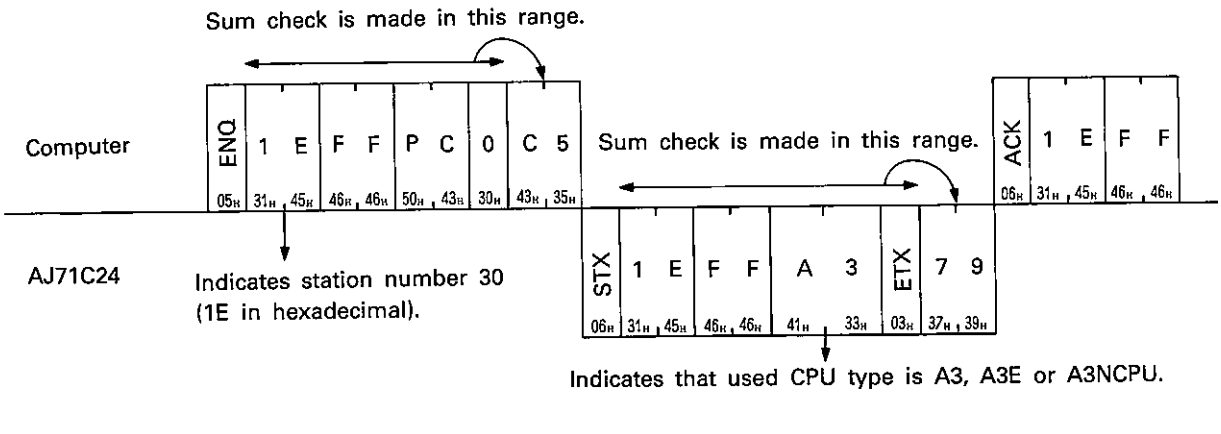
Specifying Method

The following example uses protocol format 1.




Example

To read the type of station "30". (Wait for message is 0ms)






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## 6.11 Program Transfer

This function is used to transfer all types of program (main and subsequence programs, microcomputer main and sub programs), parameters and comment data from the PC CPU and store them in the computer. The computer then carries out the appropriate control by writing programs, parameters and comment data to the PC CPU.

### 6.11.1 Precautions during program transfer

Care is required with the following points when reading and writing programs.

(1) When reading programs that have been written to the PC CPU, read all sequence programs, microcomputer programs, parameter data and comment data from all areas.
When writing programs, write all stored data to the PC CPU. The PC CPU will not work correctly if all areas are not written.

(2) Before writing programs, write parameter data and execute a parameter analysis request, otherwise the parameters in CPU user memory will be changed but the parameters stored in the work area by the ACPU for operation will remain unchanged. Therefore, if a peripheral device is loaded and operated after the parameters are changed, processing will be carried out with the previous parameters, which are still stored in the work area.

(3) The number of points which can be processed per communication is fixed. When reading or writing data, divide the data up into a number of groups to read or write the entire area.

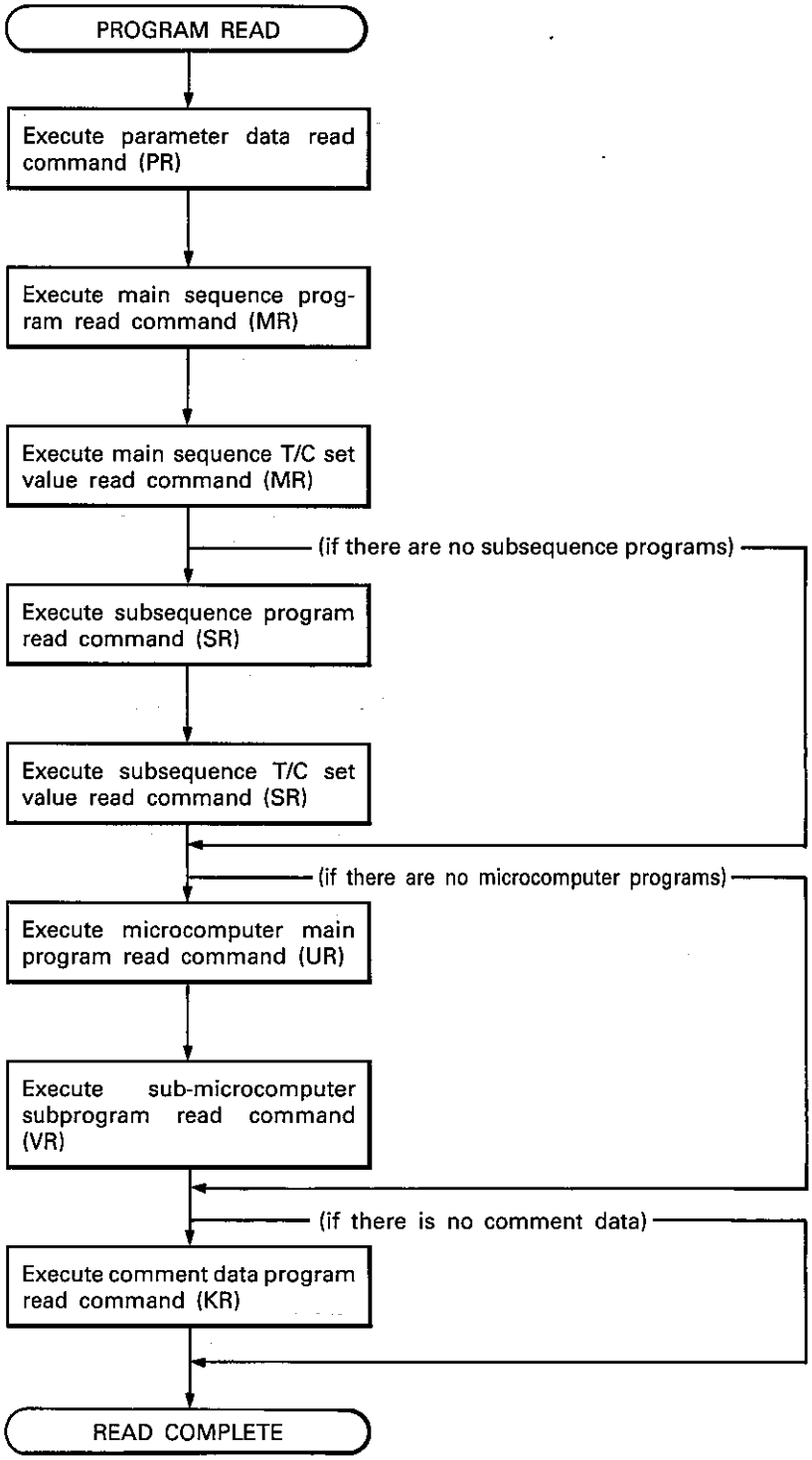


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### 6.11.2 Program transfer procedure

Flowcharts are shown below to describe the operation procedure to read and write programs.

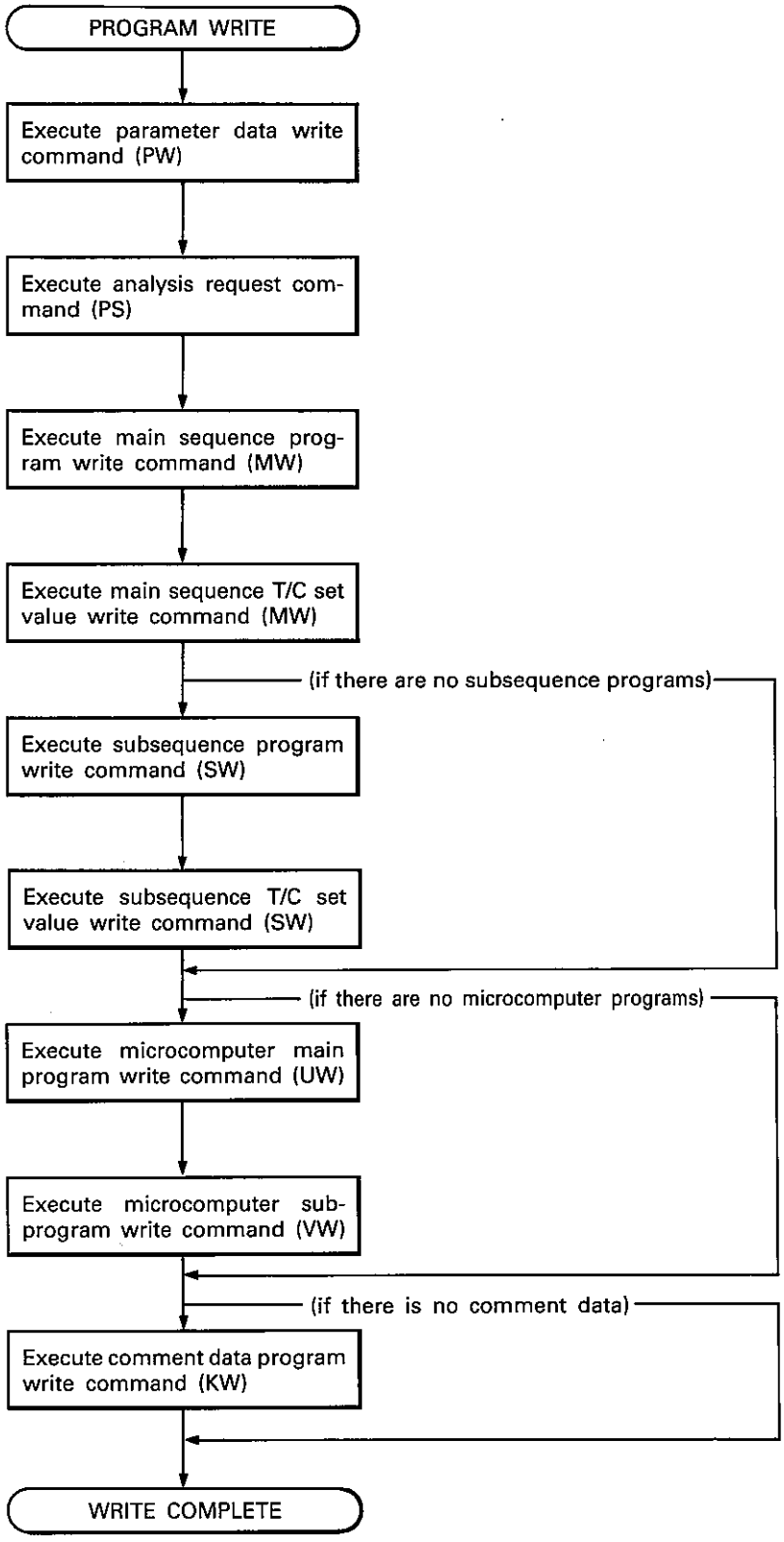
(1) Reading






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(2) Writing






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### 6.11.3 Parameter memory read and write

The method for specifying the control protocol, meanings and an example are shown below for reading the content of the PC CPU parameter memory and writing data to the parameter memory.

(1) Commands and addresses
(a) Commands

| Item | Command | | Processing | Number of Points Processed Per Communication | PC CPU State | | |
|---|---|---|---|---|---|---|---|
| | | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Batch read | PR | 50H, 52H | Reads parameters. | 128 bytes | ○ | ○ | ○ |
| Batch write | PW | 50H, 57H | Writes parameters. | | ○ | × | × |
| Analysis request | PS | 50H, 53H | Causes PC CPU to acknowledge and check rewritten parameters. | | ○ | × | × |

Key: ○ Available
× Unavailable

(b) Parameter addresses
There are 3K bytes of parameter memory, addresses $00000_H$ to $00BFF_H$. For addresses, use 5 digit ASCII (hexadecimal).

**POINT**

**After changing parameters, always call the parameter analysis request command (PS).**
**If not, the parameters in CPU user memory will be changed but the parameters stored in the work area by the ACPU for operation will remain unchanged. Therefore, if a peripheral device is loaded and operated after the parameters are changed, processing will be carried out with the previous parameters, which are still stored in the work area.**





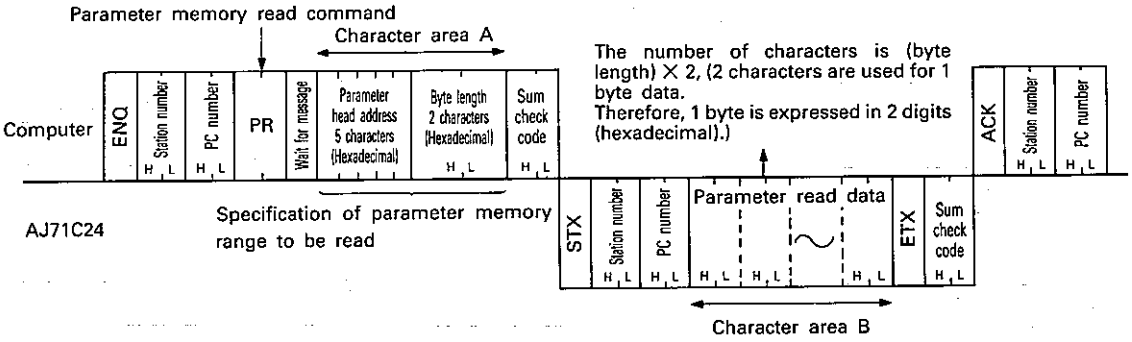
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(2) Parameter memory batch read

## Specifying Method

The following example uses protocol format 1.

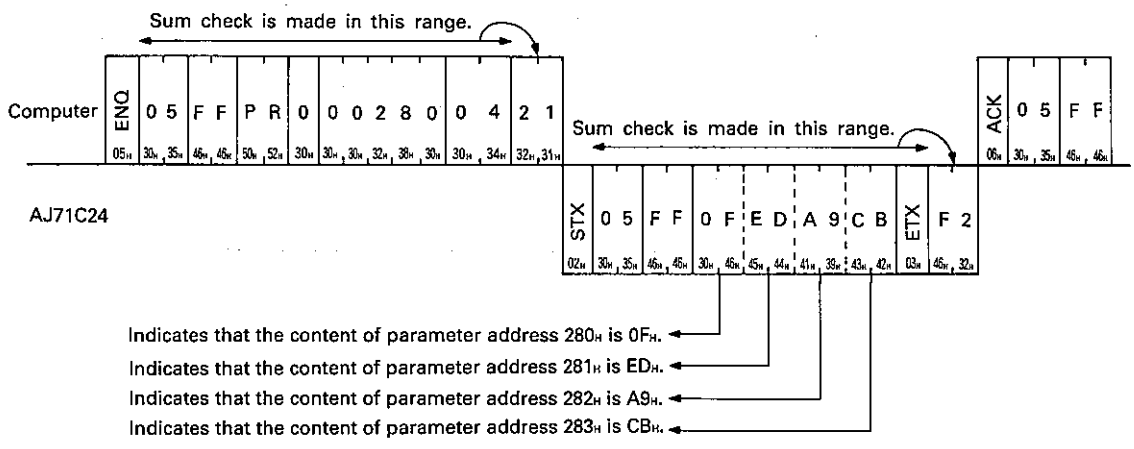



**POINT**

**Specify byte length, L, such that:**
**• 1 ≦ L ≦ 128**

## Example

To read 4 bytes of parameter data from memory addresses $280_H$ to $283_H$ of station "5". (Wait for message is 0ms)



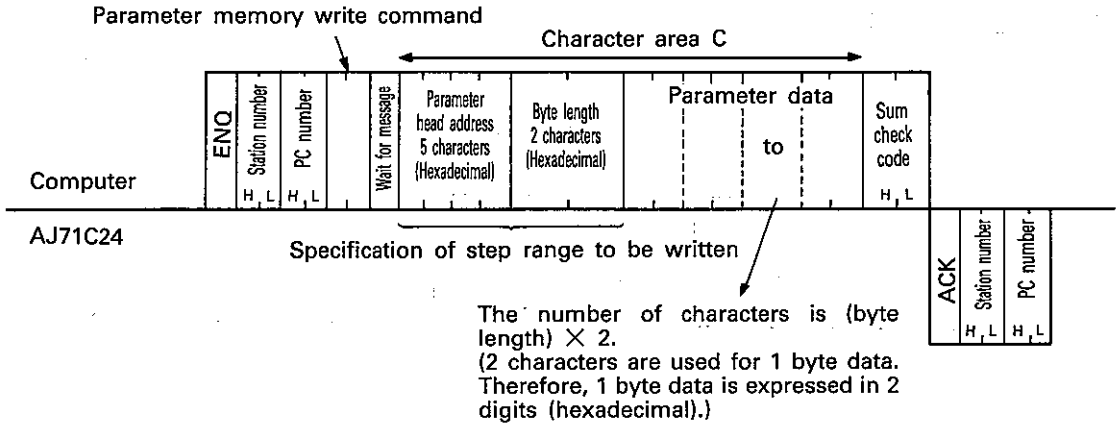



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(3) Batch write to parameter memory

**Specifying Method**

The following example uses protocol format 1.

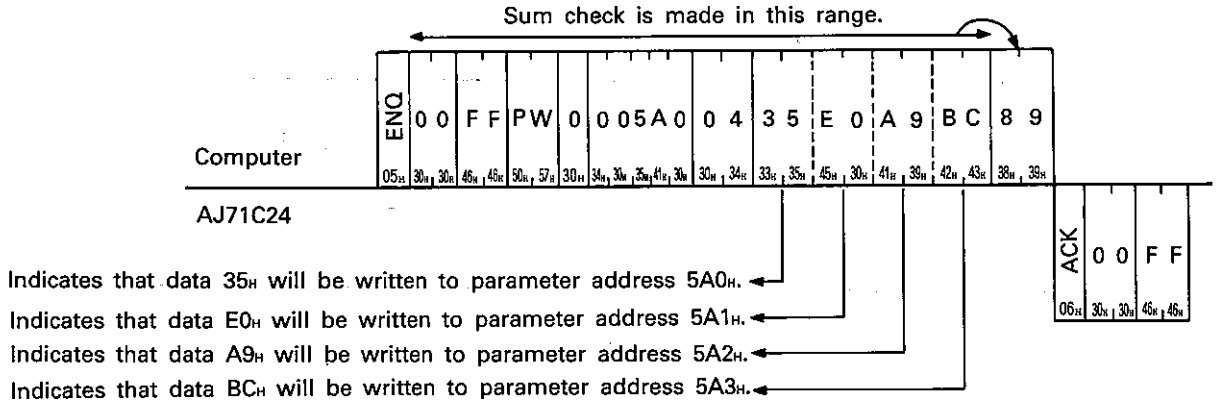



**POINT**

**Specify byte length, L, such that:**
**• 1 ≦ L ≦ 128**

**Example**

To write 4 bytes of parameter data from memory addresses 5A0H to 5A3H of station "0". (Wait for message is 0ms)




6



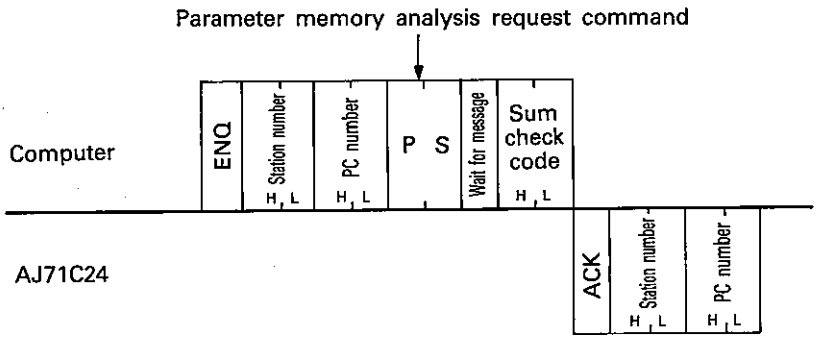
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(4) Parameter memory analysis request
When parameter memory data has been changed, this function allows the PC CPU to recognize this change and to store the new parameters into the work area.

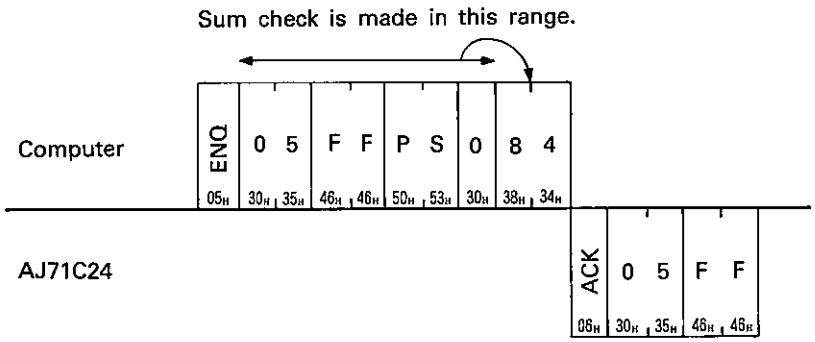
**Specifying Method**

The following example uses protocol format 1.




**Example**

To execute analysis request after writing parameters to station "5". (Wait for message is 0ms)




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### 6.11.4 Sequence program read and write

(1) Commands and step assignment
(a) Commands

| Item | | | Command | | Processing | Number of Points Processed Per Communication | PC CPU state | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | Symbol | ASCII code | | | During STOP | During RUN SW22 ON | During RUN SW22 OFF |
| Batch read | Main | not T/C set value | MR | 4DH, 52H | Reads main sequence program. | 64 steps | ○ | ○ | ○ |
| | | T/C set value | | | Reads T/C set values used in main sequence programs. | 64 points | | | |
| | Sub | not T/C set value | SR | 53H, 52H | Reads subsequence program. | 64 steps | ○ | ○ | ○ |
| | | T/C set value | | | Reads T/C set values used in subsequence programs. | 64 points | | | |
| Batch write | Main | not T/C set value | MW | 4DH, 57H | Writes main sequence program. | 64 steps | ○ | ○* | × |
| | | T/C set value | | | Writes T/C set values used in main sequence programs. | 64 points | ○ | ○ | × |
| | Sub | not T/C set value | SW | 53H, 57H | Write subsequence program. | 64 steps | ○ | ○* | × |
| | | T/C set value | | | Writes T/C set values used in subsequence programs. | 64 points | ○ | ○ | × |

Key: ○ Available
× Unavailable

* Writing during a program run may be carried out if all the following conditions are met:
1) the PC CPU is type A3(E), A3N or A3H
2) the program is not the currently running program (indicates a subprogram called by the main program if a main program is being run)
3) the PC CPU special relay is in the following status:
(a) M9050 (signal flow conversion contact) ····· OFF (A3CPU only)
(b) M9051 (CHG instruction disable) ····· ON







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(b) Specifying the head step

The division between sequence programs and T/C set values, and their addresses in 4-digit ASCII are shown in the table below.

Example

To read the set values T0 to T63

Head address = $FE00_H$ Command = MR

| Sequence Program | Specified Step for Control Protocol |
|---|---|
| T0 set value<br>T1 set value<br>to<br>T255 set value | $FE00_H$<br>$FE01_H$<br>to<br>$FEFF_H$ |
| C0 set value<br>C1 set value<br>to<br>C255 set value | $FF00_H$<br>$FF01_H$<br>to<br>$FFFF_H$ |
| Step 0<br>Step 1<br>to<br>Step 30719 (30K) | $0000_H$<br>$0001_H$<br>to<br>$77FF_H$ |

Calculation of specified step

Timer : Tm= $FE00_H$ + n

Counter : Cm= $FF00_H$ + n

where, m= device number

n= hexadecimal value of device number

(c) Meaning of T/C set values

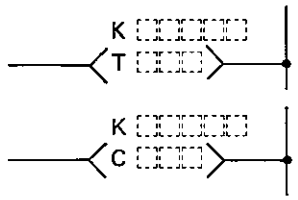
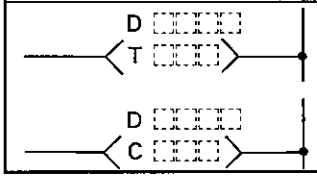
T/C set values are stored as hexadecimal values as shown in the table below.

When rewriting the PC CPU set values from the computer via the AJ71C24, specify the set value in 4-digit ASCII.

Example

Data specified to change T10 setting value K10 to K20 ····· $0014_H$

Data specified to change T11 setting value D30 to D10 ····· $800A_H$

| Ladder Example in Program | Setting in Program | Setting in Control Protocol |
|---|---|---|
|  | K0<br>K1<br>to<br>K9<br>K10<br>to<br>K32767 | $0000_H$<br>$0001_H$<br>to<br>$0009_H$<br>$000A_H$<br>to<br>$7FFF_H$ |
|  | D0<br>D1<br>D2<br>to<br>D1023 | $8000_H$<br>$8002_H$<br>$8004_H$<br>to<br>$87FE_H$ |

Calculation of Control Protocol value

Km= $0000_H$ + n

Dm= $8000_H$ + 2n

where, m= device number

n= hexadecimal value of device number

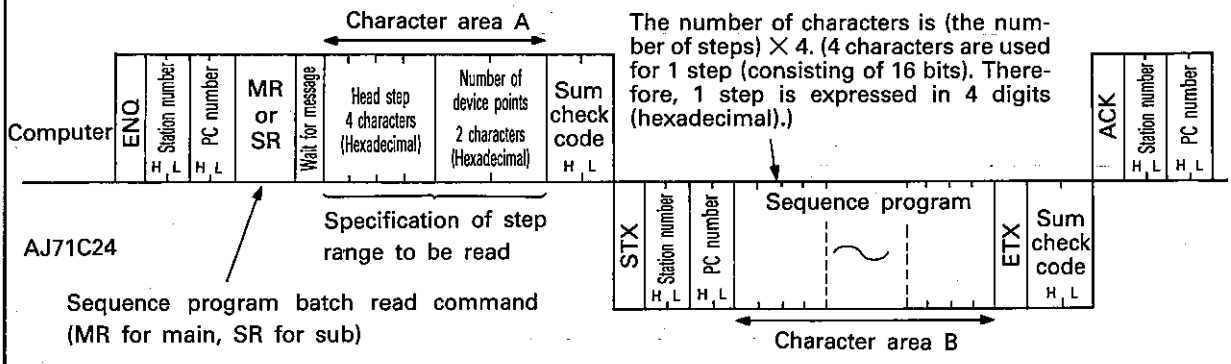


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(2) Sequence program, batch read

## Specifying Method

The following example uses protocol format 1.




**POINT**

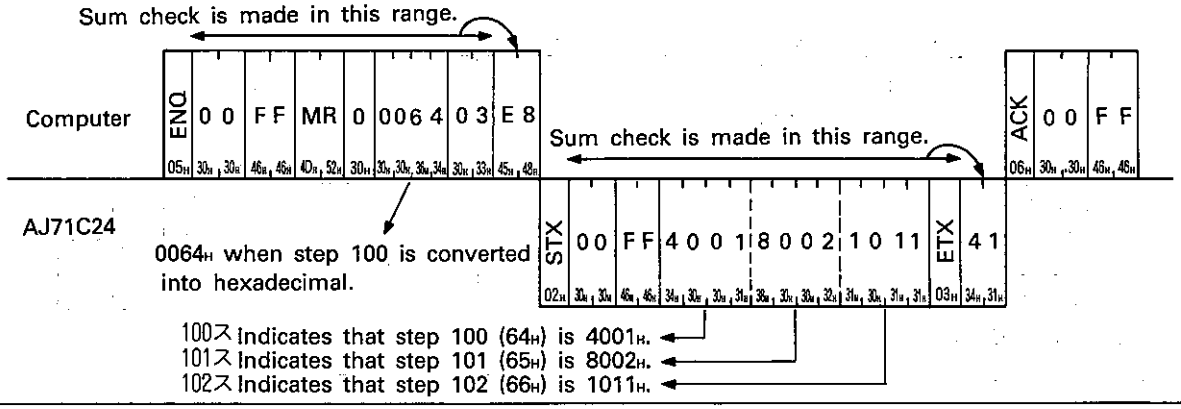
**(1) Specify the number of steps, n, such that:**
**• 1 ≦ n ≦ 64**

**(2) Timer, counter, and sequence program cannot be specified simultaneously.**

## Example

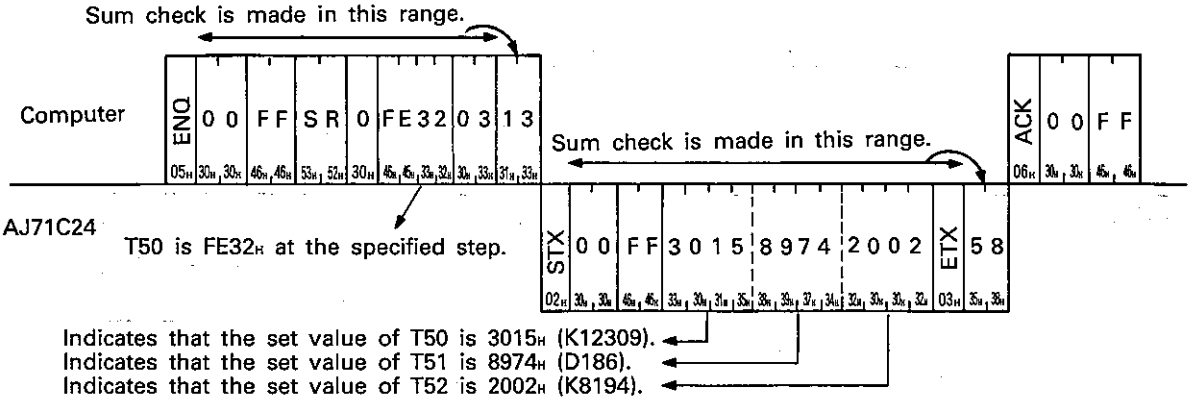
Example 1

To read steps 100 to 102 of main sequence program in station "0" (Wait for message is 0ms)




Example 2

To read the set values of T50 to T52 in the subsequence program at station "0" (Wait for message is 0ms)



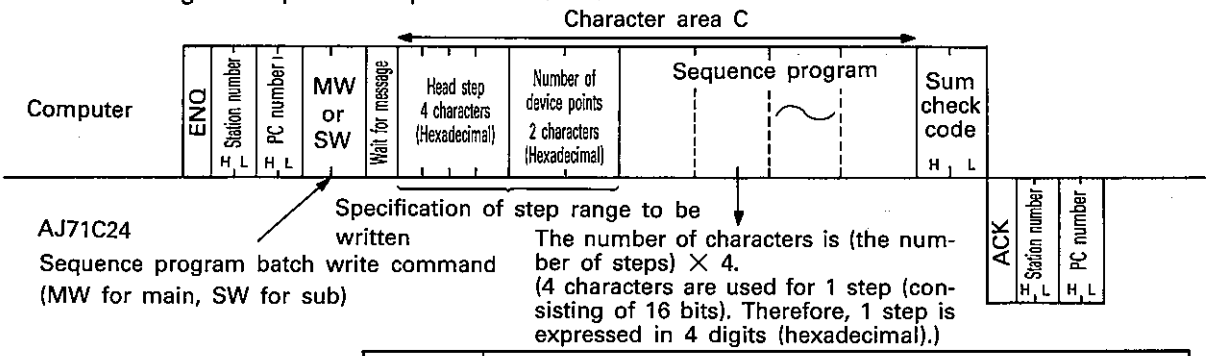



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(3) Sequence program, batch write

## Specifying Method

The following example uses protocol format 1.




**POINT**

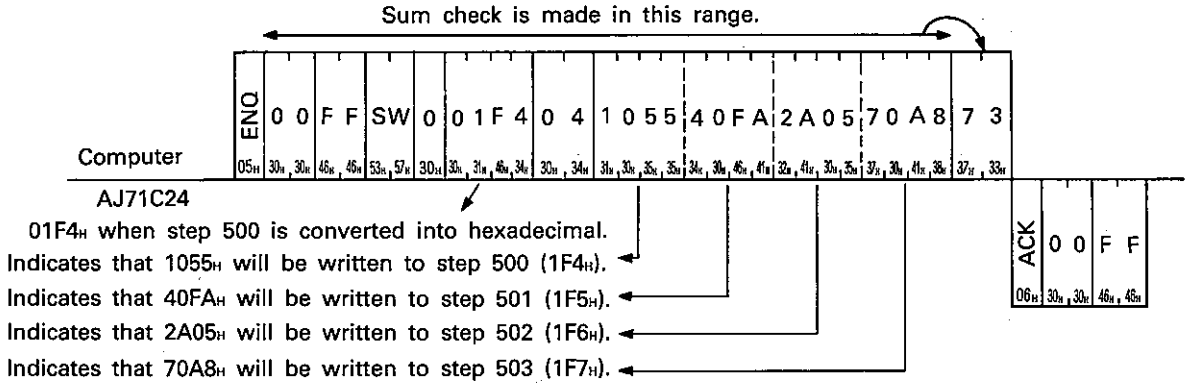
**(1) Specify the number of steps, n, such that:**
**• 1 ≦ n ≦ 64**

**(2) Timer, counter, and sequence program cannot be specified simultaneously.**

## Example

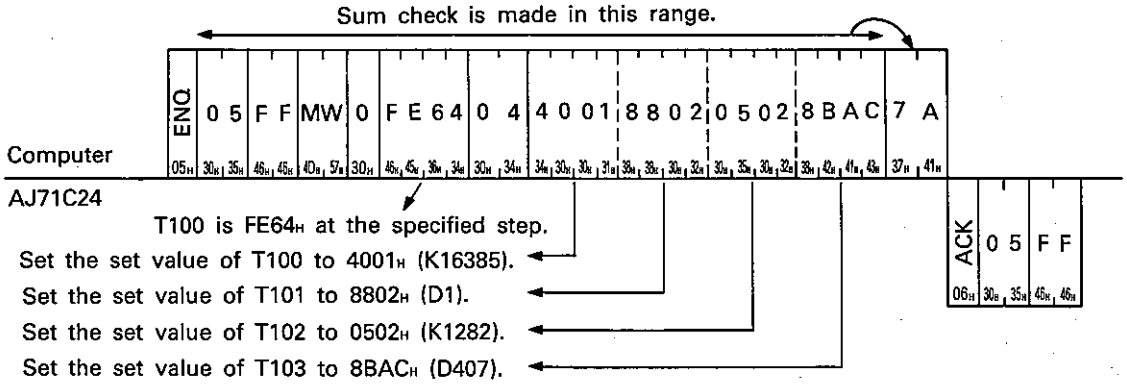
Example 1

To write steps 500 to 503 to the subsequence program in station "0" (Wait for message is 0ms)




Example 2

To write set values of T100 to T103 to the subsequence program in station "5" (Wait for message is 0ms)




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### 6.11.5 Microcomputer program transfer

The method for specifying the control protocol, meanings and examples are shown below to read and write PC CPU microcomputer programs.

(1) Commands and addresses
Commands and program addresses to read and write microcomputer programs are explained below.
(a) Commands

| Item | | Command | | Processing | No. of Points Processed Per Access | State of PC CPU | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | During STOP | During RUN | |
| | | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Batch read | Main | UR | 55H, 52H | Reads microcomputer main programs | 128 bytes | ○ | ○ | ○ |
| | Sub | VR | 56H, 52H | Reads microcomputer subprograms | | | | |
| Batch write | Main | UW | 55H, 57H | Writes microcomputer main programs | 128 bytes | ○ | ○ * | × |
| | Sub | VW | 56H, 57H | Writes microcomputer subprograms | | | | |

Key: ○ Available
× Unavailable

* Writing during a program run may be carried out if all the following conditions are met:
1) the PC CPU is type A3, A3E, A3N or A3H
2) the program is not the currently running program (indicates a subprogram called by the main program if a main program is being run)
3) the PC CPU special relay is in the following status:
(a) M9050 signal flow conversion contact ····· OFF (A3CPU only)
(b) M9051 (CHG instruction disable) ····· ON

(b) Microcomputer program addresses
Microcomputer addresses are specified in the control protocol as follows:
1) The range of addresses that can be specified for each CPU is shown in the table below.

| CPU Type | Microcomputer program capacity | Microcomputer addresses |
|---|---|---|
| A1(E)CPU<br>A1NCPU | Max. 10K bytes | 000H to 27FFH |
| A2(E)CPU<br>A2NCPU | Max. 26K bytes | 000H to 67FFH |
| A3(E)CPU<br>A3NCPU<br>A3HCPU | Main and sub<br>Max. 58K bytes | 000H to E7FFH |

2) Addresses are specified in 4-digit ASCII.
3) A character area error 06H occurs if the following condition is not fulfilled:
Head address + n ≦ program capacity



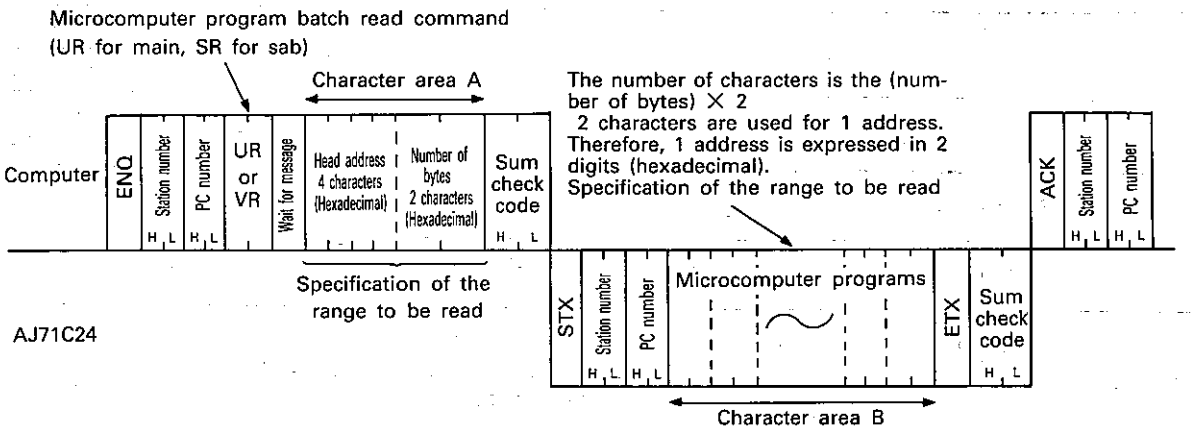
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(2) Microcomputer program, batch read

The method for specifying the control protocol and an example are shown below for carrying out a batch read of a microcomputer program.

## Specifying Method

The following example uses protocol format 1.



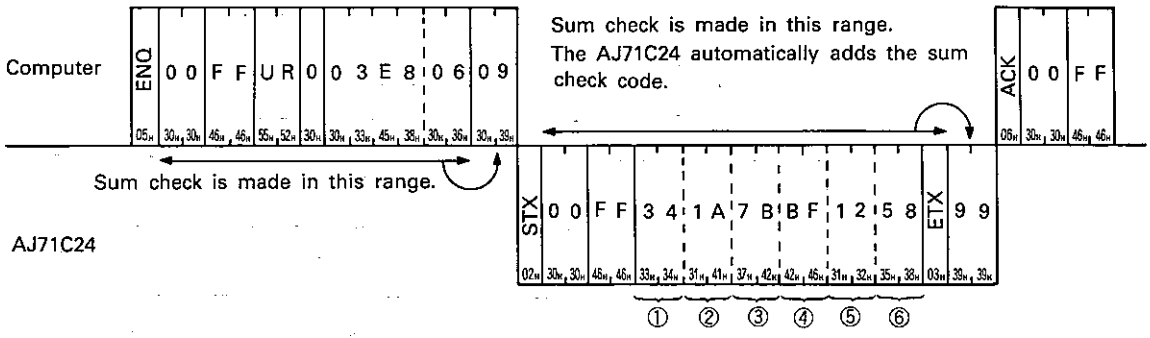

**POINT**

**Specify the number of bytes, n, such that:**

- **$1 \leqq n \leqq 128$**
- **Head address + n ≦ microcomputer program capacity**

## Example

To read six bytes from the CPU microcomputer from address $03E8_H$ (decimal 1000) in station "0". (Wait for message is 0ms.)




①indicates that the content of address $03E8_H$ is $34_H$
②indicates that the content of address $03E9_H$ is $1A_H$
③indicates that the content of address $03EA_H$ is $7B_H$
④indicates that the content of address $03EB_H$ is $BF_H$
⑤indicates that the content of address $03EC_H$ is $12_H$
⑥indicates that the content of address $03ED_H$ is $58_H$



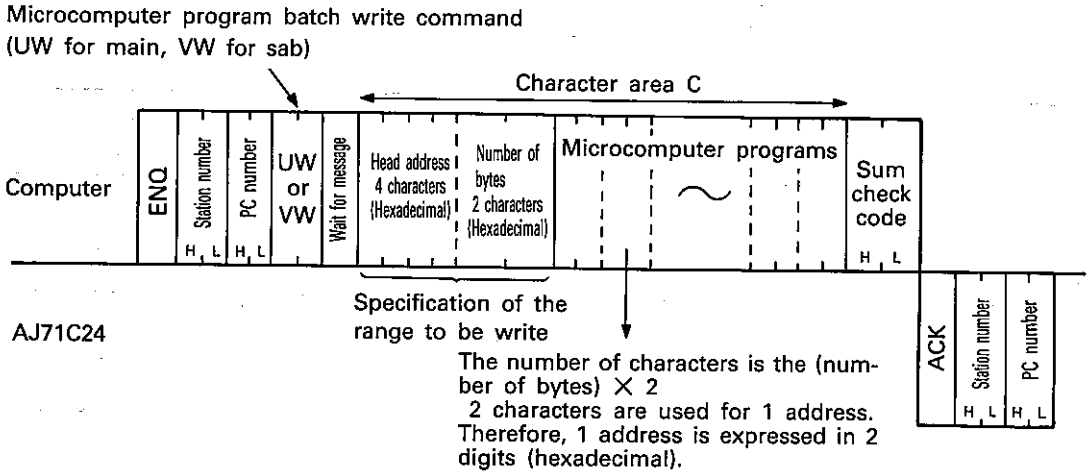
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(3) Microcomputer program, batch write

The method for specifying the control protocol and an example are shown below for carrying out a batch write of a microcomputer program.

**Specifying Method**

The following example uses protocol format 1.



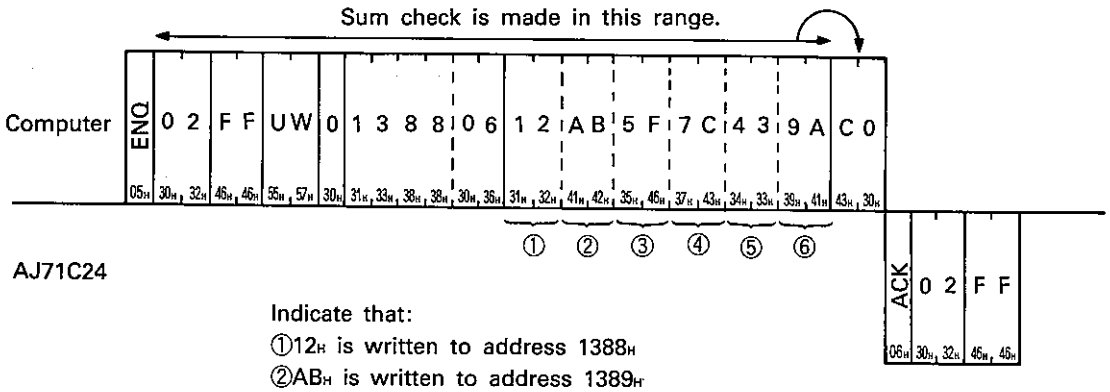

**POINT**

**Specify the number of bytes, n, such that:**

- **$1 \leqq n \leqq 128$**
- **Head address + n ≦ microcomputer program capacity**

**Example**

To write six bytes to the CPU microcomputer address from $1388_H$ (decimal 5000) in station "2". (Wait for message is 0ms.)




Indicate that:

①$12_H$ is written to address $1388_H$
②$AB_H$ is written to address $1389_H$
③$5F_H$ is written to address $138A_H$
④$7C_H$ is written to address $138B_H$
⑤$43_H$ is written to address $138C_H$
⑥$9A_H$ is written to address $138D_H$



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### 6.11.6 Comment memory transfer

The method for specifying the control protocol, meanings and examples are shown below to read and write PC CPU comment data.

(1) Commands and addresses
Commands and comment data addresses to read and write comment data are explained below.
(a) Commands

| Item | Command | | Processing | No. of Points Processed Per Access | PC CPU State | | |
|---|---|---|---|---|---|---|---|
| | | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Batch read | KR | 4B$_H$, 52$_H$ | Reads comment memory | 128 bytes | ○ | ○ | ○ |
| Batch write | KW | 4B$_H$, 57$_H$ | Writes to comment memory | 128 bytes | ○ | ○ | × |

Key: ○ Available
× Unavailable

(b) Comment memory addresses
The area to store comment data is managed using relative addresses from the head address of 00$_H$.
For example, for 2 KBytes of parameter comments, the range in which the addresses may be specified for the head address is 00$_H$ - 7FF$_H$.
1) Comment memory capacity is 64 KBytes
The comment data address range is determine by the parameter setting.
2) Comment memory addresses are specified in 4-digit ASCII.
3) A character area error 06$_H$ occurs if the following condition is not fulfilled:
Head address + specified number of bytes ≦ comment memory capacity.

**POINT**

**It is not possible to specify a particular device or device number when reading or writing comment data.**
**Always read or write all data from address 00$_H$.**



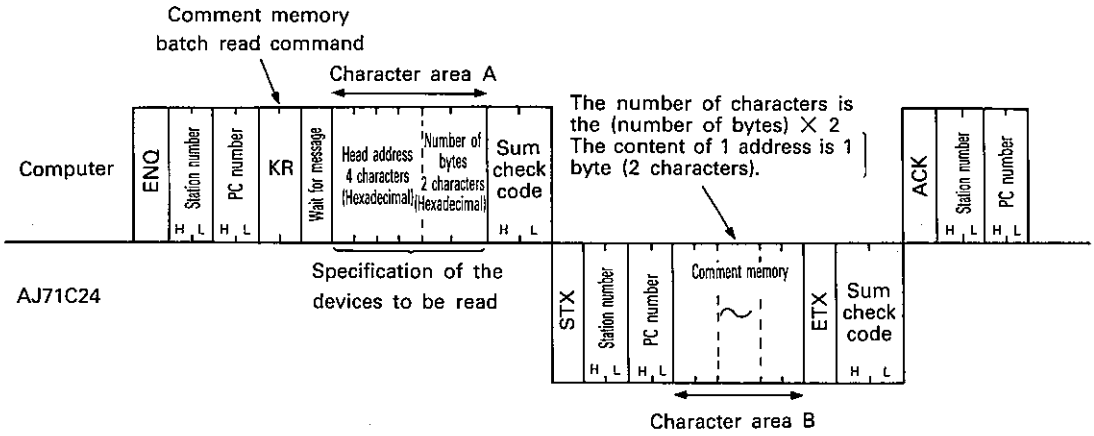
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(2) Comment memory, batch read

The method for specifying the control protocol and an example are shown below for carrying out a batch read of the comment memory.

## Specifying Method

The following example uses protocol format 1.



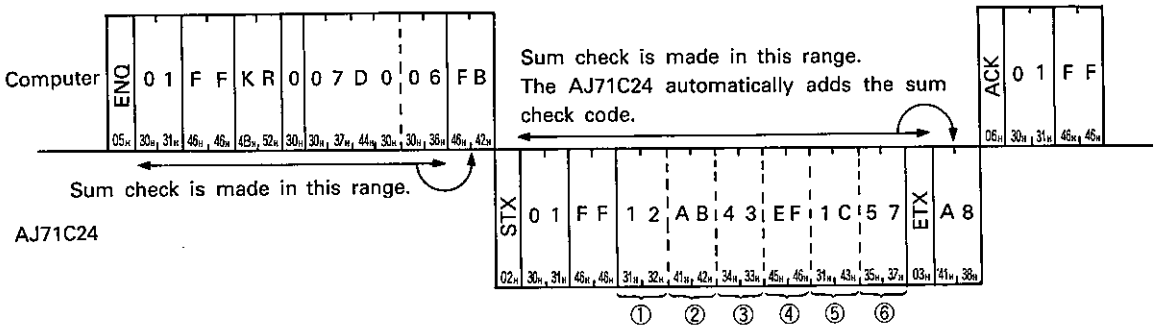

**POINT**

**Specify the number of bytes, n, such that:**

- **$1 \leqq n \leqq 128$**
- **Head address + n $\leqq$ comment memory capacity**

## Example

To read six bytes from the CPU comment memory from address 7D0H (decimal 2000) in station "1". (Wait for message is 0ms.)




①indicates that the content of address 07D0H is 12H
②indicates that the content of address 07D1H is ABH
③indicates that the content of address 07D2H is 43H
④indicates that the content of address 07D3H is EFH
⑤indicates that the content of address 07D4H is 1CH
⑥indicates that the content of address 07D5H is 57H



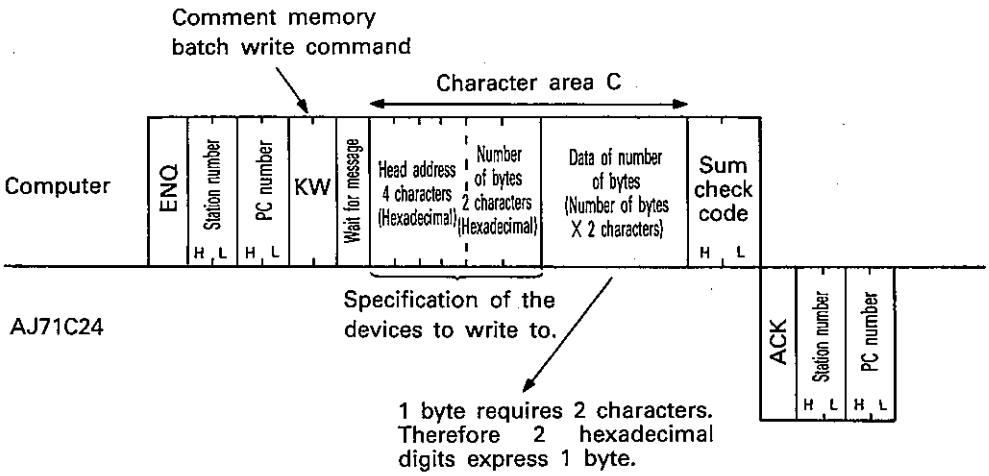
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(3) Comment memory, batch write

The method for specifying the control protocol and an example are shown below for carrying out a batch write of the comment memory.

**Specifying Method**

The following example uses protocol format 1.



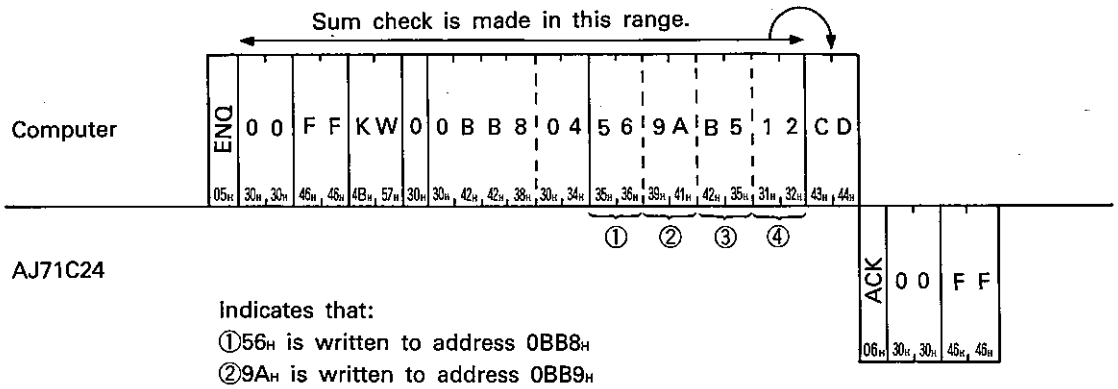

**POINT**

**Specify the number of bytes, n, such that:**

- **$1 \leqq n \leqq 128$**
- **Head address + n ≦ comment memory capacity**

**Example**

To write four bytes to the CPU comment memory from address 0BB8H (decimal 3000) in station "0". (Wait for message is 0ms.)




Indicates that:

①56H is written to address 0BB8H

②9AH is written to address 0BB9H

③B5H is written to address 0BBAH

④12H is written to address 0BBBH



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## 6.12 Global Function

The global function is used to switch the Xn2 input signal at each AJ71C24 in all stations which are linked to the computer by the multidrop link.
This function is used for emergency instructions etc., to the PC CPU.
"n" in Xn2 is determined by the slot location of the AJ71C24.
The method for specifying the control protocol, meanings and an example are shown below for executing the global function.

### 6.12.1 Commands and control

(1) Commands

| Item | Command | | Processing | PC CPU State | | |
|---|---|---|---|---|---|---|
| | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | SW22 ON | SW22 OFF |
| Global | GW | 47H, 57H | Turns on/off Xn2 of the AJ71C24s loaded in each PC CPU system. | ○ | ○ | ○ |

Key : ○ Available

(2) Control
This function switches the Xn2 input signal at each AJ71C24 in all stations which are linked to the computer.
(a) Xn2 is determined by the I/O addresses of the AJ71C24s.
Example: If the I/O addresses are 90 to AF, Xn2 is X92.
(b) Specify the station number in the control protocol as FFH.
Specifying a number other than FFH causes, Xn2 of the AJ71C24 at the specified station number to turn on/off.
(c) This function is a command from the computer. A reply is not given by the AJ71C24.
(d) Xn2 is cleared of any station when the power supply is turned off or when it is reset.

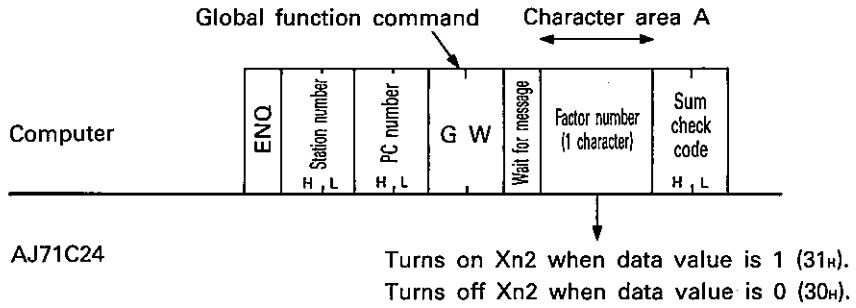


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### 6.12.2 Global function specifying method

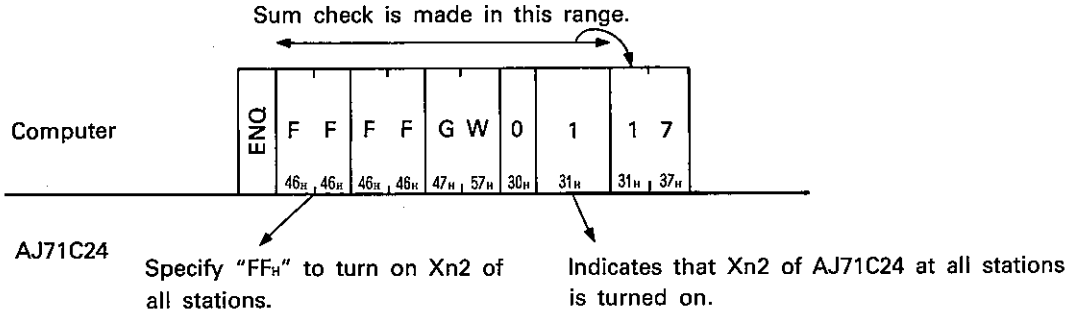
**Specifying Method**

The following example uses protocol format 1.




**Example**

To turn on Xn2 of AJ71C24 at all stations. (Wait for message is 0ms)




6

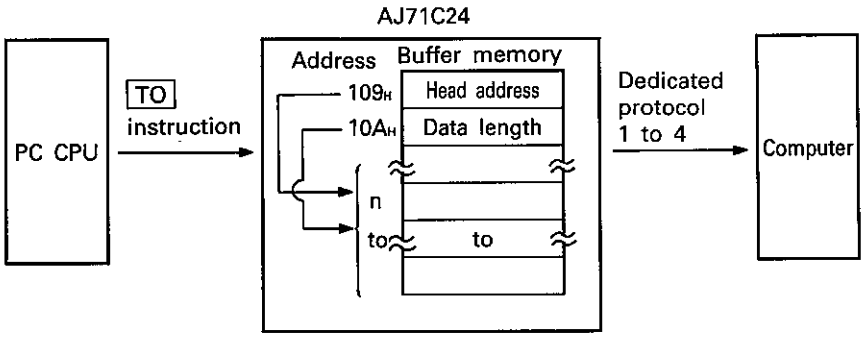


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## 6.13 On-demand Function

During data transfer between the computer and PC CPU using the dedicated protocols 1 - 4, communication is normally initiated by the computer.
If the PC CPU has emergency data to send to the computer, transfer is impossible unless the computer has a start program. The on-demand function is used when the PC CPU has data to send to the computer. In this case, the PC CPU specifies the buffer memory area in which the data to be transferred is stored and then starts the transfer.




**POINT**

**This function is available when there is a 1:1 ratio of computer to PC CPU and the computer is using the full-duplex communication method.**

### 6.13.1 On-demand handshake signal and buffer memory

The handshake signal and buffer memory used by the on-demand function are explained in this section.

(1) On-demand handshake signal
The on-demand handshake signal turns ON when the PC CPU sends a data transmission request to the computer to start transmission, and turns OFF when transmission of the data specified by the AJ71C24 is complete. It acts and an interlock to prevent on-demand requests being made simultaneously in two directions.

| Handshake signal | Description | Signal turned ON/OFF by |
|---|---|---|
| Xn3 | During execution of on-demand function<br>ON : transmission underway<br>OFF: transmission complete | AJ71C24 |

* "n" in Xn3 is determined by the slot location of the AJ71C24.



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(2) Buffer memory used by on-demand function

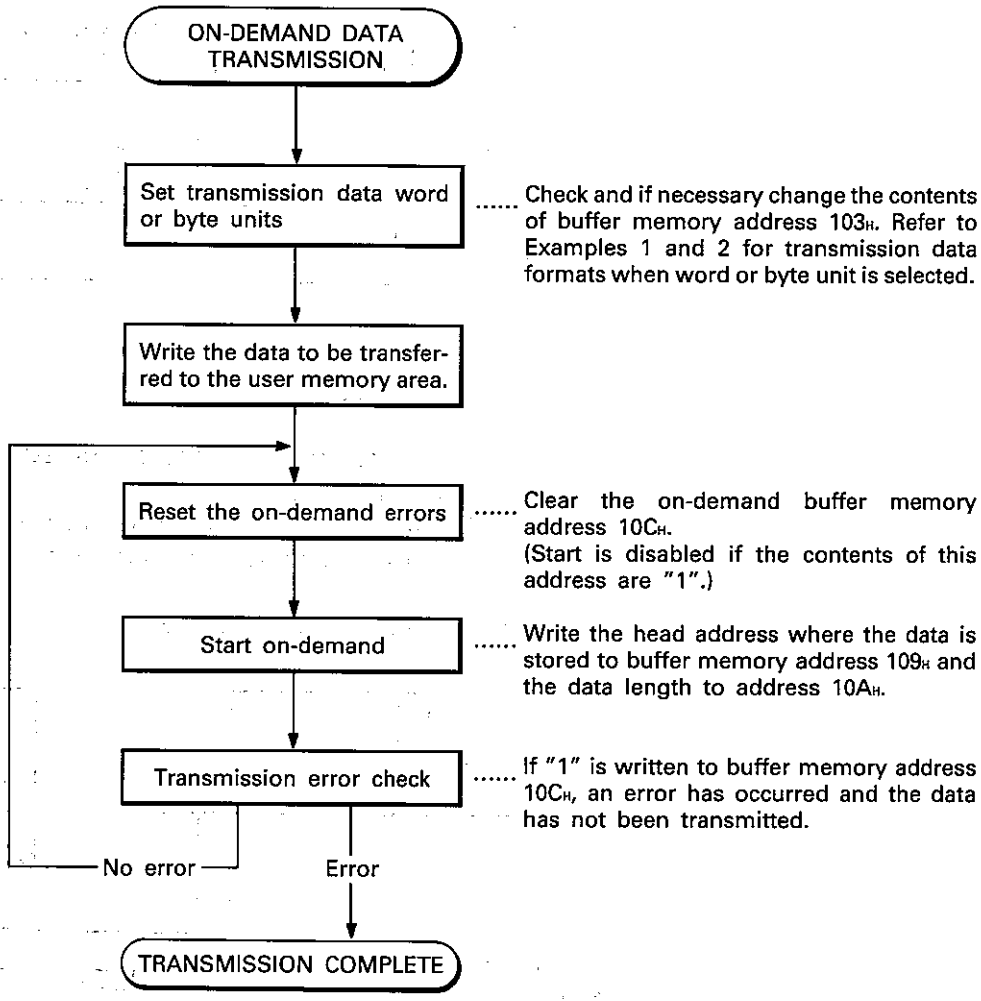
| Address | Name | Description |
|---|---|---|
| $109_H$ | Area to specify head address in on-demand buffer memory | The head address of the data stored in the buffer memory to be transmitted by the on-demand function is specified by the PC CPU [TO] instruction. |
| $10A_H$ | Area to specify length of data | The length of the data to be transmitted by the on-demand function is specified by the PC CPU [TO] instruction. |
| $10C_H$ | On-demand error storage area | The AJ71C24 writes a "1" to this address if a transmission error occurs during on-demand data transmission.<br>0 : No error<br>1 : Error |



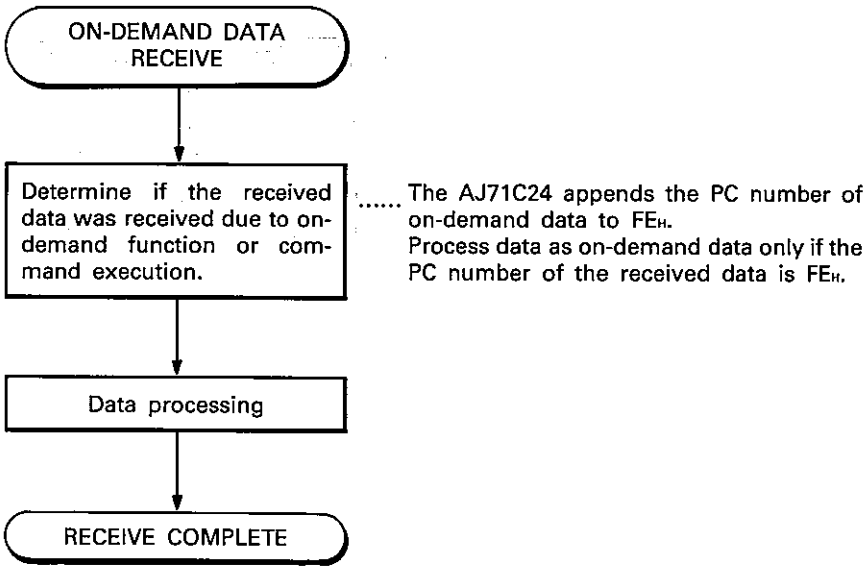
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### 6.13.2 On-demand function operating procedure

(1) PC CPU operating procedure




(2) Computer operating procedure

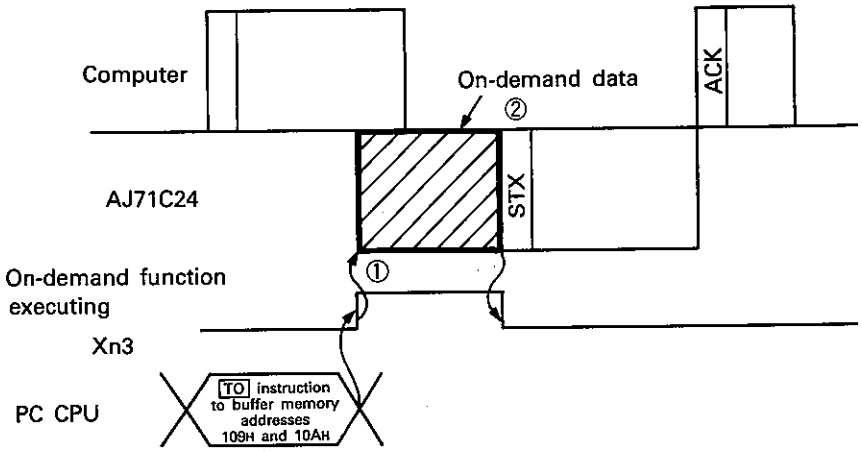





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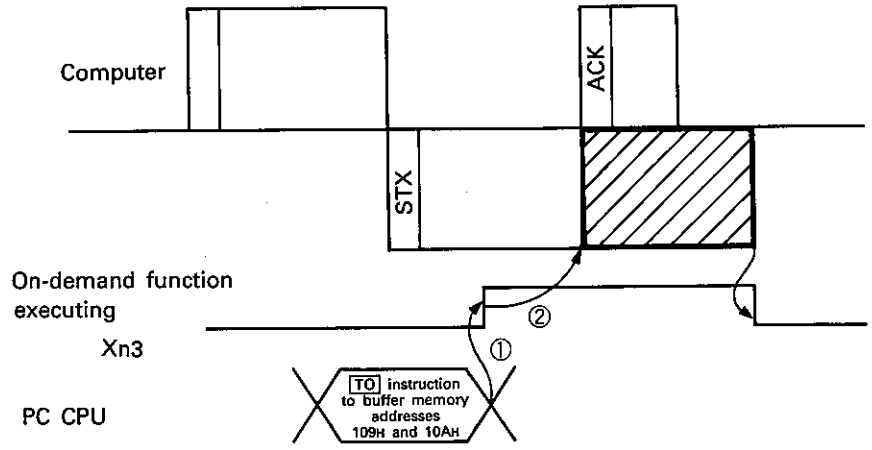
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(3) The timing charts for an on-demand request are shown below.
(a) If computer is transmitting data




①Transmission commences immediately after the on-demand request is made.
②Command data (STX to) has to wait for completion of the on-demand data transmission.

(b) If computer is receiving data




① TO instruction turns ON the on-demand busy signal. Transmission commences immediately the on-demand request is made.
②When the on-demand request is made, the on-demand data transmission has to wait for completion of command data transmission.

6



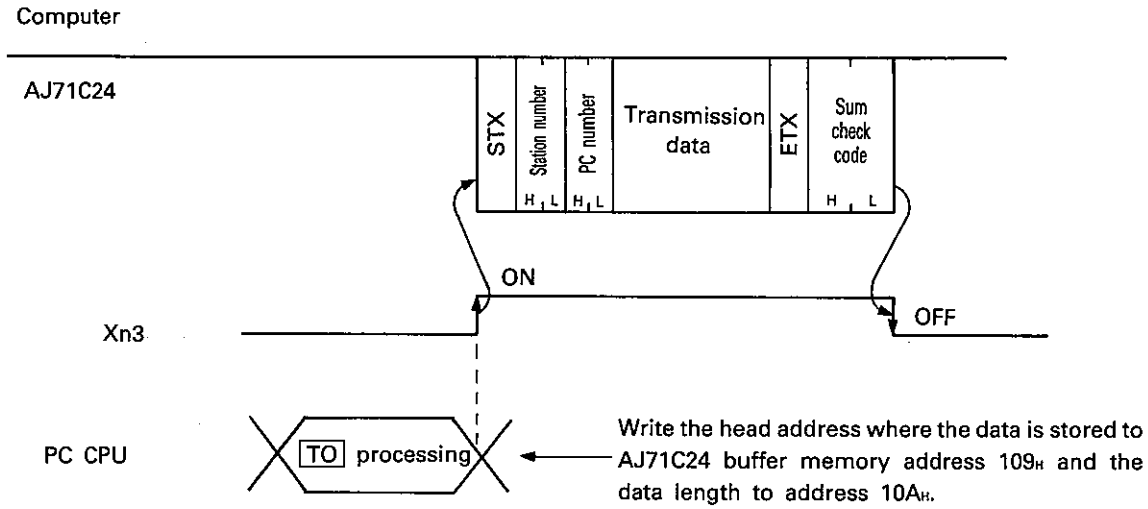
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### 6.13.3 Method and examples for specifying on-demand function

**Specifying Method**

The following example uses protocol format 1.




**POINT**

**(1) Buffer memory addresses 100H - 11FH are the special-application area.**
**Do not use this area to store the data to be transmitted with the on-demand function.**
**(2) Specify the data length in the following range:**
**Head address + specified data length ≦ 7FFH**
**(3) The AJ71C24 appends as the PC number.**
**(4) When using transfer control protocol 2, the block number becomes 00H.**

**IMPORTANT**

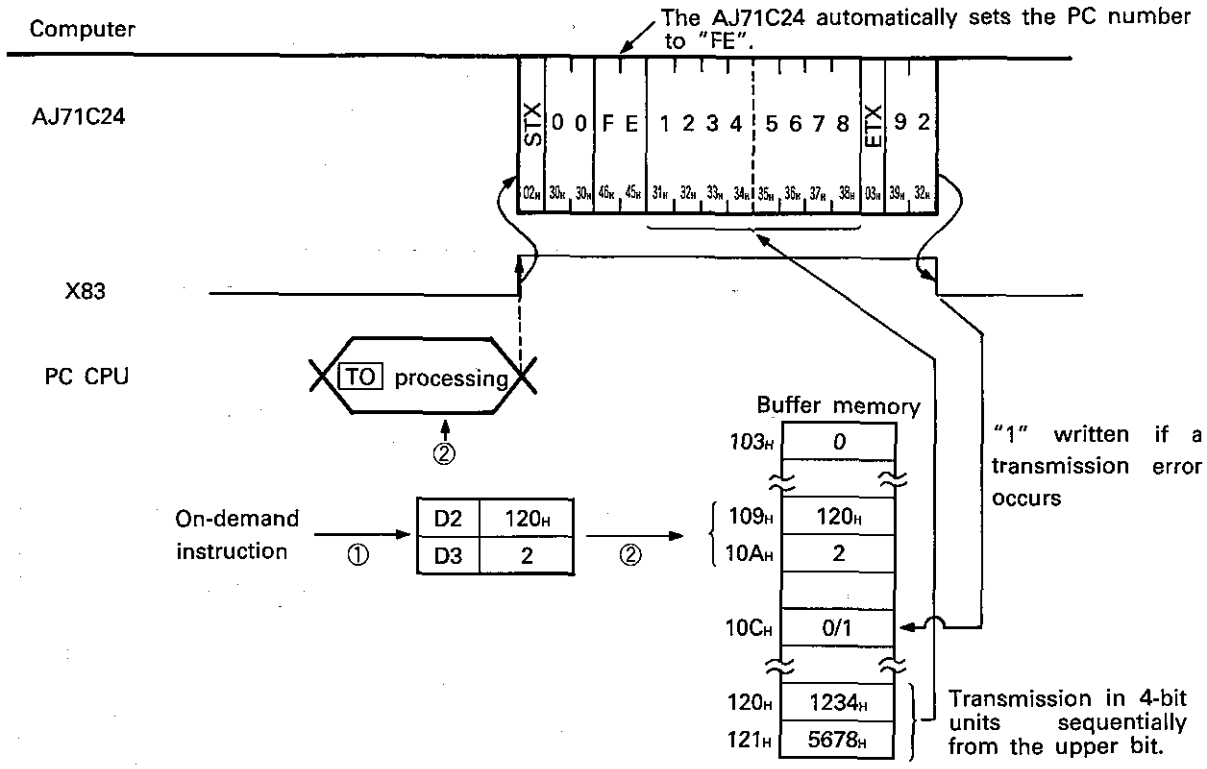
**If the on-demand function is used in a multidrop link with a 1:n or 2:n ratio of computer to PC CPU's, control protocol 1-4 communication data and on-transmission data will be destroyed and correct communication impossible.**
**Only use the TO instruction to write data to buffer memory addresses 109H and 10AH when the system is configured in a 1:1 ratio.**

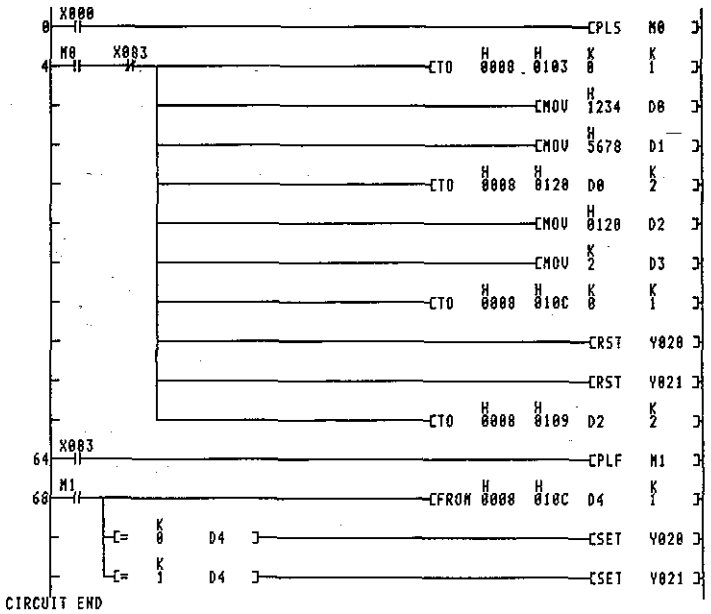


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Example 1

To start transmission with the PC CPU of data stored in the buffer memory at addresses $120_H$ -$121_H$.
(Station number 0, AJ71C24 I/O addresses 80 - 9F, transmission data specified in word units)




Convert start signal to pulse

Set word units for transmission data

Set transmission data

①Specify head address where the data is stored and data length

Reset the on-demand error

(Start is disabled if the contents of address $10C_H$ are "1".)

②On-demand start

Transmission complete flag

Read transmission storage area and check transmission status

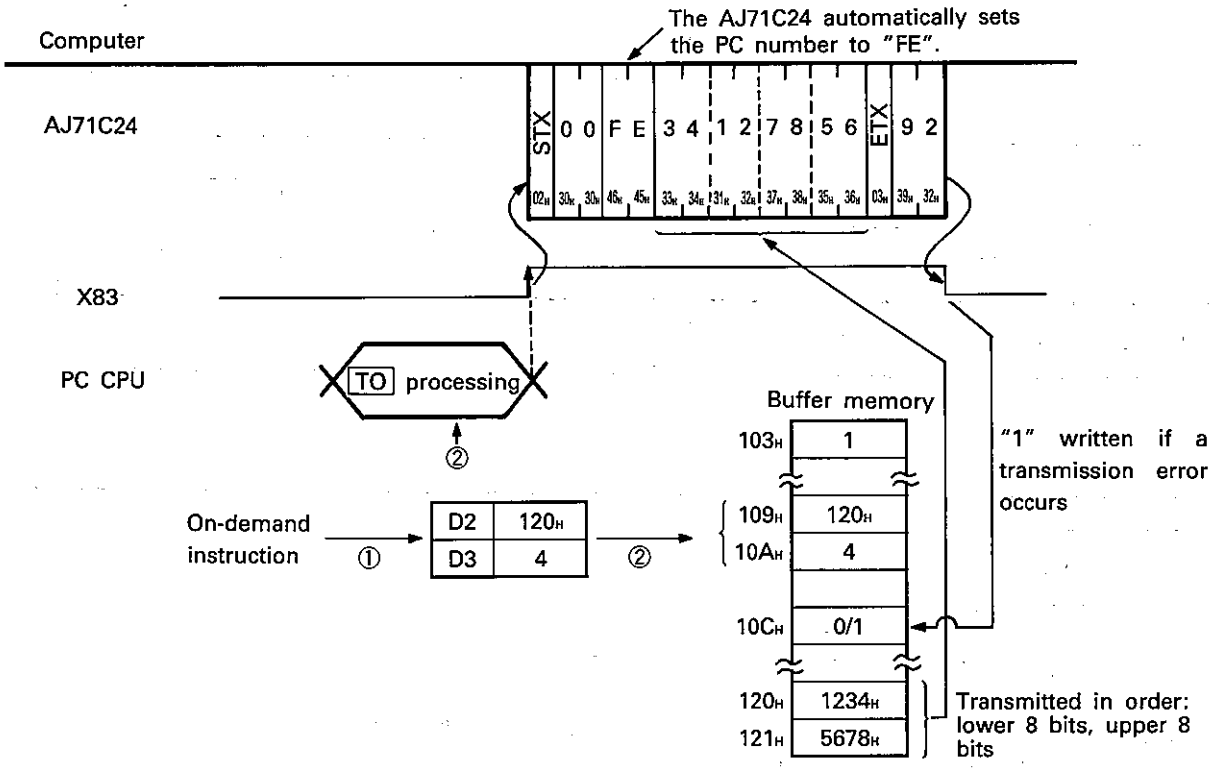
Address $10C_H$
- 0 : normal transmission
- 1 : data not transmitted due to an error

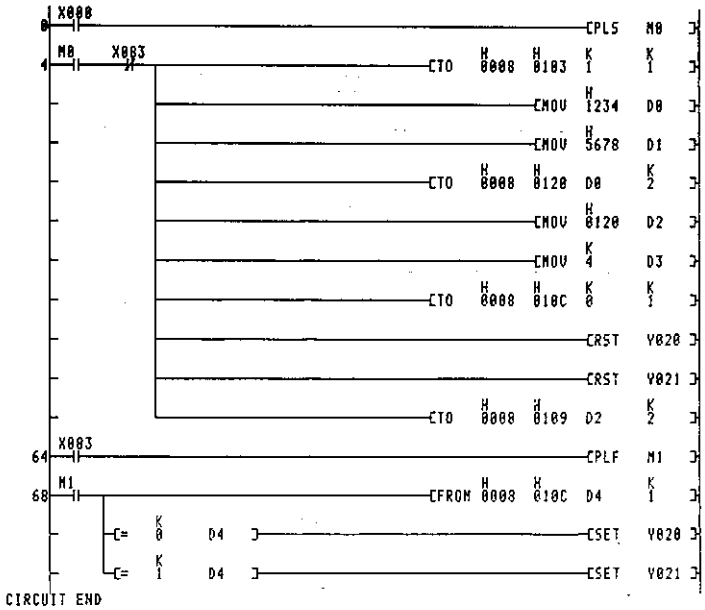


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Example 2

To start transmission with the PC CPU of data stored in the buffer memory at addresses $120_H$ -$121_H$.
(Station number 0, AJ71C24 I/O addresses 80 - 9F, transmission data specified in byte units)




Convert start signal to pulse

Set byte units for transmission data

Set transmission data

①Specify head address where the data is stored and data length

Reset the on-demand error
(Start is disabled if the contents of address $10C_H$ are "1".)

②On-demand start

Transmission complete flag

Read transmission storage area and check transmission status

Address $10C_H$
- 0 : normal transmission
- 1 : data not transmitted due to an error



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## 6.14 Loopback Test

The loopback test is a function to determine if the communication between the computer and AJ71C24 is correct.
The method for specifying the control protocol, meaning, and an example are shown below for running the loopback test.

(1) Commands
The commands used for the loopback test are shown in the table below.

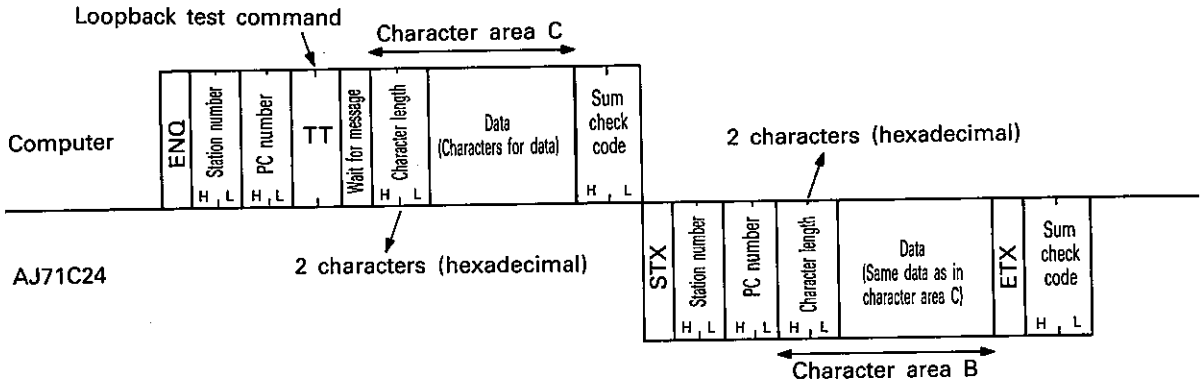
| Item | Command | | Processing | Number of Points Processed Per Communication | PC CPU state | | |
|---|---|---|---|---|---|---|---|
| | | | | | During STOP | During RUN | |
| | Symbol | ASCII code | | | | SW22 ON | SW22 OFF |
| Loopback test | TT | $54_H$, $54_H$ | Echoes character back to the computer. | 254 characters | ○ | ○ | ○ |

Key : ○ Available

(2) Loopback test call

**Specifying Method**

The following example uses protocol format 1.

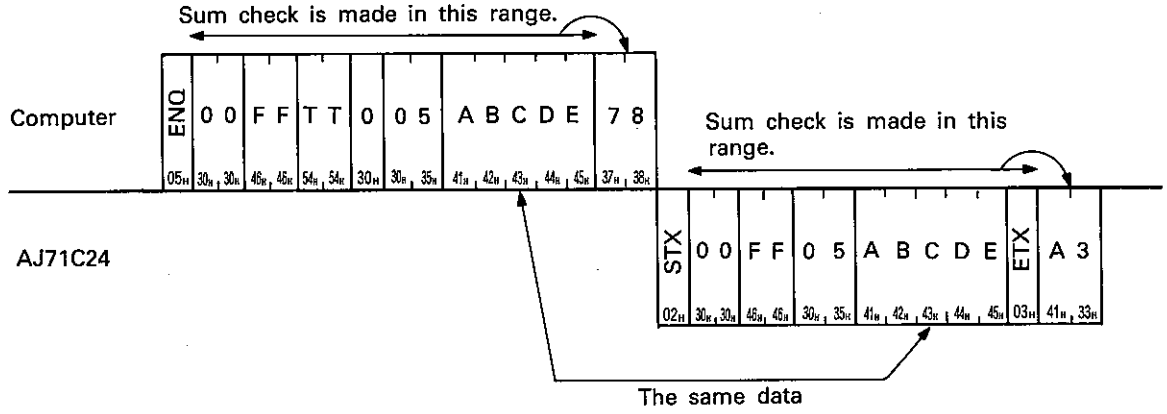



**POINT**

**Specify character length, L, such that:**
**• 1 ≦ L ≦ 254**

**Example**

To conduct a test with loopback data "ABCD" at station "0". (Wait for message is 0ms)








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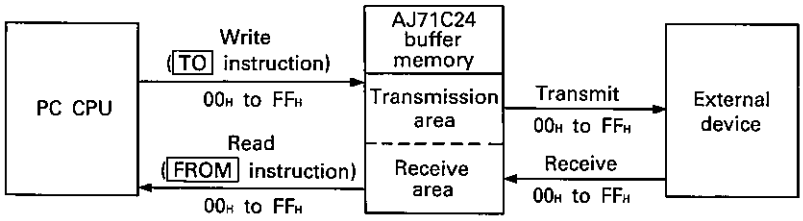
# 7. COMMUNICATIONS IN THE NO-PROTOCOL MODE

Communications between external devices (such as a computer, printer) and the PC CPU in the no-protocol mode are explained in this chapter.

## 7.1 Basics of the No-protocol Mode

This section explains the basics of the link between external devices (such as a computer, printer) and the PC CPU in the no-protocol mode.

(1) What no-protocol means
In no-protocol communication:
- the PC CPU uses TO instructions to read data from the no-protocol mode transmission buffer memory area, and output the data in unchanged code to an external device
- the PC CPU uses FROM instructions to read data received from an external device which has been stored in the AJ71C24 no-protocol mode receive buffer memory area.




**POINT**

**In the no-protocol mode, data is not converted to ASCII in the AJ71C24. If ASCII code is required, the data must be handled as ASCII code, respectively, in the PC CPU.**

(2) Setting word or byte units for no-protocol communication
It is possible to select word or byte units for transmission data in the no-protocol mode. Word units are selected by default, but byte units can be set by writing "1" or word units by writing "0" to the buffer memory special-application area address 103H.
(Refer to section 5.4.3 for details of program to make this setting.)

**POINT**

**The byte or word units set for the no-protocol mode also apply to the on-demand function.**

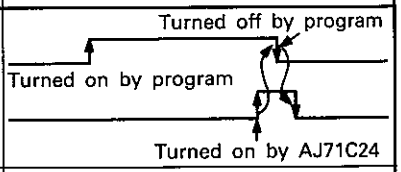
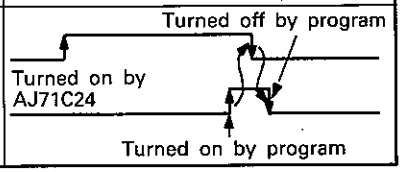


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## 7.2 Handshake I/O Signals

Signals known as I/O handshake signals are required for communication in the no-protocol mode.

These signals output data received from the PC CPU to an external device and detect signals sent from an external device to enable the PC CPU to read them.
The I/O handshake signals are shown in the table below.

| | Signal | Timing |
|---|---|---|
| PC CPU ↓ Outside | $Y_{(n+1)}$ 0 (Sending request)<br>$X_n0$ (Sending complete) |  |
| Outside ↓ PC CPU | $X_{n1}$ (Receiving request)<br>$Y_{(n+1)}$ 1 (Receiving complete) |  |



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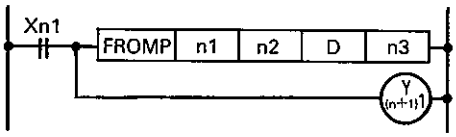
## 7.3 Read and Write of Buffer Memory by PC CPU

The following gives a brief description of a basic PC CPU program to read and write data to and from the AJ71C24 buffer memory in the no-protocol mode.

(1) FROM, FROMP, DFRO, DFROP instructions to write to the transmission area

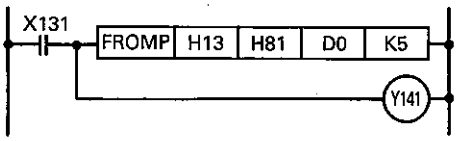
Read data from the no protocol receive data area (addresses $80_H$ to $FF_H$) of the buffer memory.

Form




| Symbol | Description | Usable Device |
|---|---|---|
| n1 | Upper 2 digits of head I/O number assigned to AJ71C24 | K, H |
| n2 | Buffer memory head address of stored data ($81_H$) | K, H |
| D | Head number of device to which read data will be written | T, C, D, W, R |
| n3 | Number of data words to be read (maximum 127 words) | K, H |

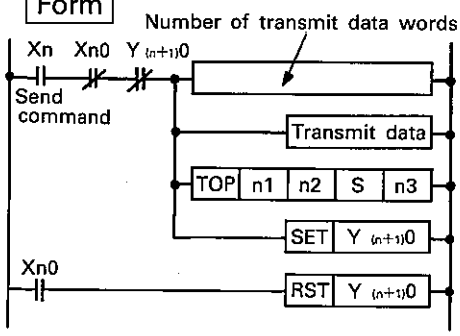
Example: To read 5 data words starting at buffer memory address $81_H$, with the AJ71C24 located in slot number 130 to 14F




(2) TO, TOP, DTO, DTOP instructions to read from the receive area

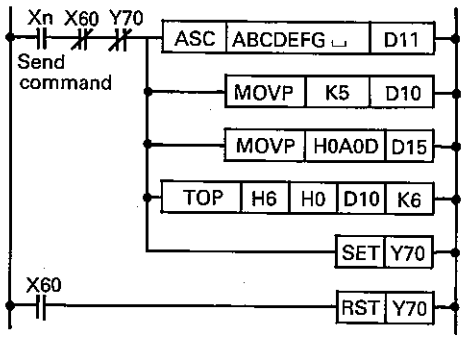
Write data to the no protocol data transmit area (addresses $0_H$ to $7F_H$) of the buffer memory.

Form




| Symbol | Description | Usable Device |
|---|---|---|
| n1 | Upper 2 digits of head I/O number assigned to AJ71C24 | K, H |
| n2 | Head address ($0_H$) of buffer memory in which data will be stored | K, H |
| S | Head device number or constant which stores data to be written | T, C, D, W, R |
| n3 | Number of words of data to be written | K, H |

Example: To write "ABCDEFG␣CR.LF" to addresses $1_H$ to 6 words of the buffer memory, with the AJ71C24 located in slot number 60 to 7F.








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## 7.4 Receiving Data in the No-protocol Mode (external device → AJ71C24)

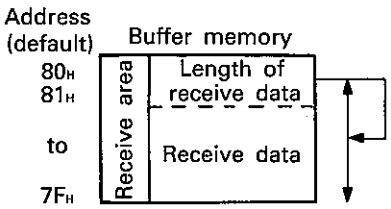
"Receiving" refers to the process to store the data received from an external device in the no-protocol mode receive buffer memory area (hereinafter abbreviated to "receive area"), and then read them by the PC CPU using the FROM instruction.

(1) Receive area

The receive area stores the length of data received and the data itself. By default, addresses $80_H$ to $FF_H$ is allocated to the receive area.

It is however possible to change the receive area to suit the purpose of the data communication and specifications of the external devices. (Refer to section 5.4.5.)

If the receive data is longer than the buffer memory (default length 127 words), the data is divided and sent piece by piece. It is recommended that the receive area should be larger than the amount of data received. (Refer to example programs and remarks.)




- The actual amount of data received is written when the receive-complete code is received or the fixed length of data has been received.
- Data received is stored sequentially from the lowest address until the complete code is received or the fixed length of data has been received.

(2) Receiving data

There are two methods to complete receiving data:
- receiving the receive-complete code
- receiving the pre-set amount of data (fixed length).

(a) Completion with the receive-complete code

Receiving data is complete when the AJ71C24 receives the data which specifies the receive-complete code.

The default receive-complete code is CR, LF ($0D0A_H$) but this may be changed to any value in the range $0000_H$ - $00FF_H$ to suit the specifications of external devices. (Refer to section 5.4.1 for details of how to change the code.)

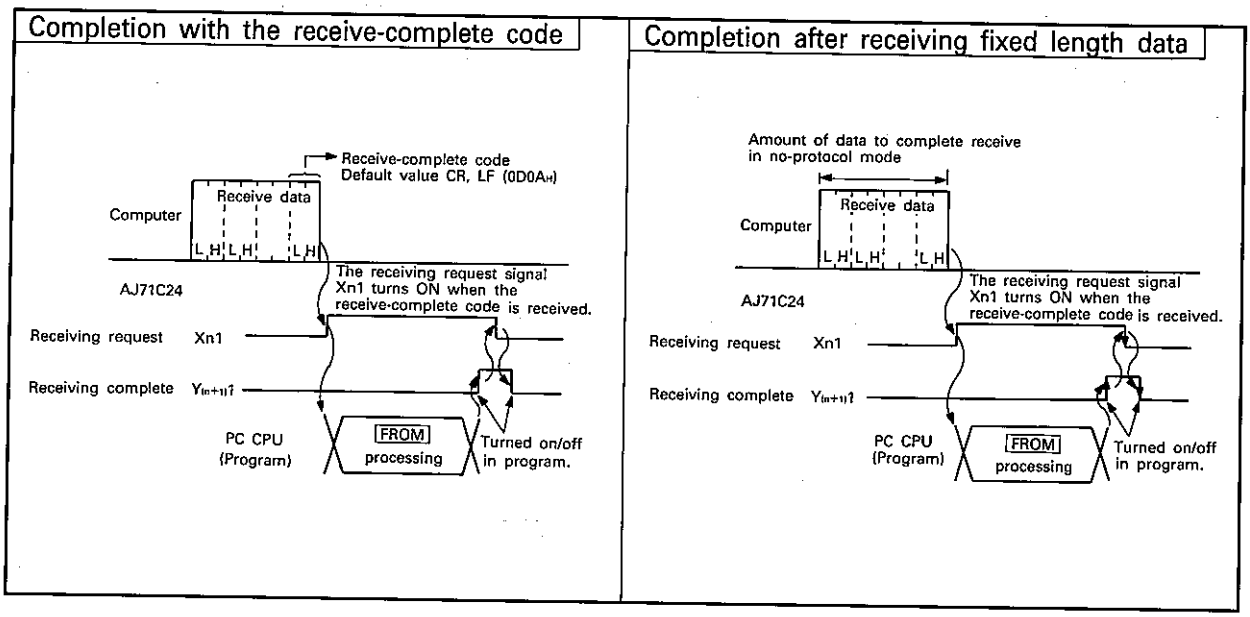
(b) Completion after receiving fixed length data

Receiving data is complete when the AJ71C24 receives the preset amount of data. When using the fixed data length to complete data receive it is not necessary to set a code such as the receive-complete code, so that all data from $00_H$ to $FF_H$ can be received. (Refer to section 5.4.2 for details of how to set the fixed data length.)



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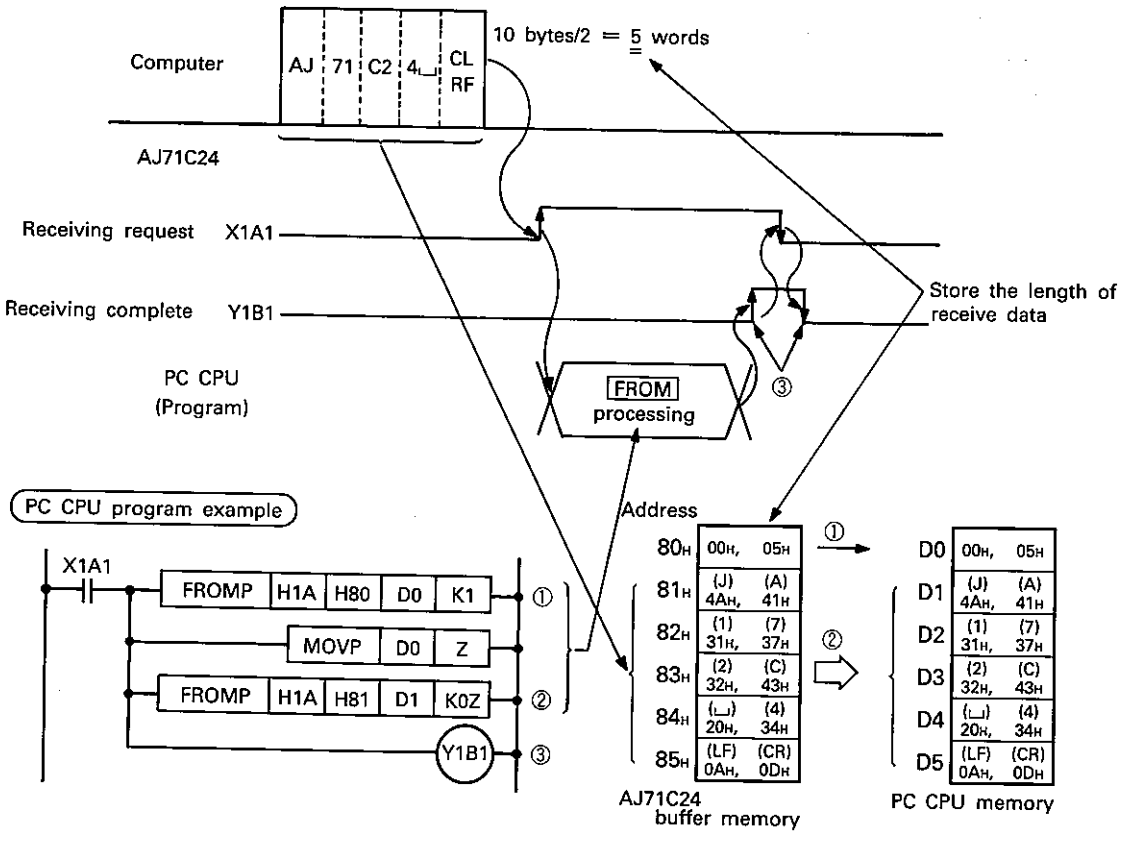
(3) Receiving procedure




(4) Receive program example

Example 1: word units, complete-receive code, default buffer memory assignment values

To receive the characters "AJ71C24" CR, LF from an external device and store them at D0 to D5 in the PC CPU (AJ71C24 I/O addresses 1A0 to 1BF).



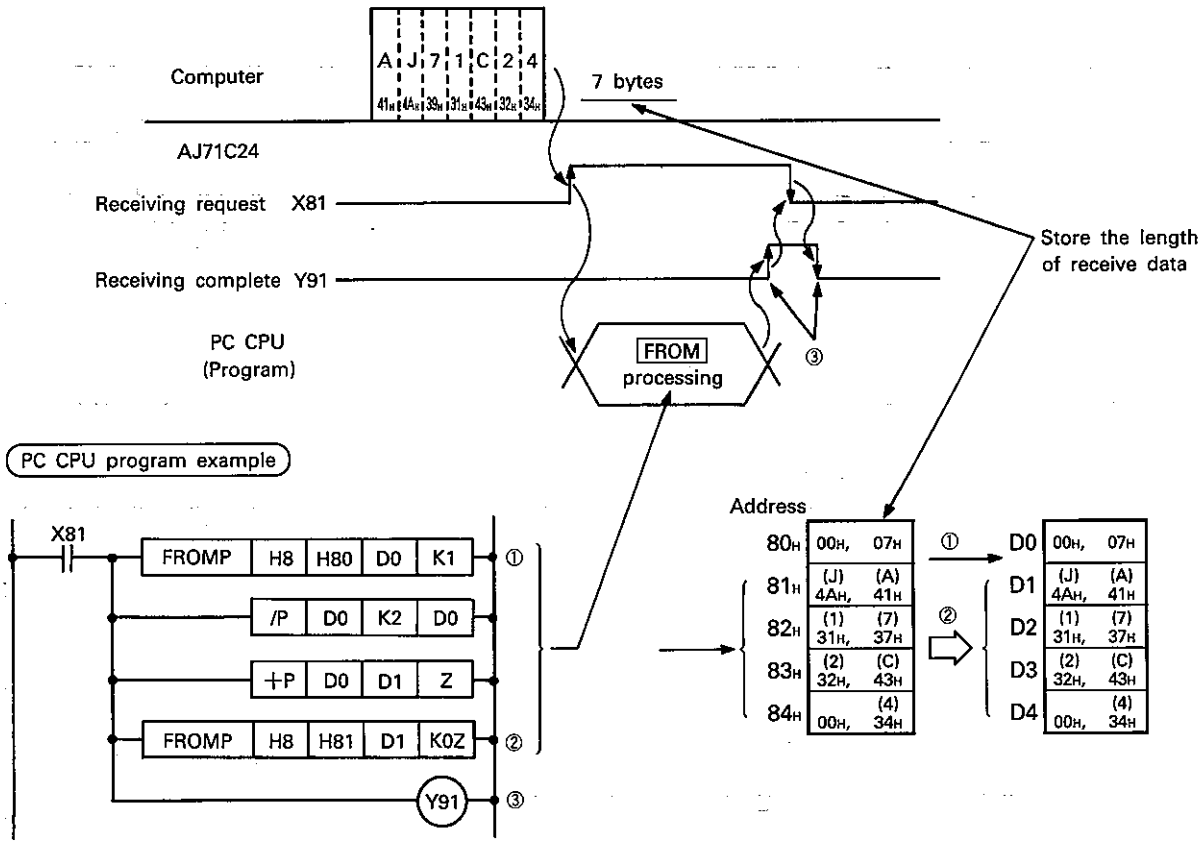



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Example 2: byte units, fixed data length, default buffer memory assignment

Specify the units as byte units. Set the fixed data length to complete data receive to 7. To receive the characters "AJ71C24" from an external device and store them at D0 to D4 in the PC CPU (AJ71C24 I/O addresses 80 to 9F).




**POINT**

- **Even if transmission data units are set to byte units the PC CPU FROM instruction operates using word units. Therefore, the length of receive data must be converted to the number of buffer memory points required (word units).**
  **In the example above, 7 bytes of data are received: 7 ÷ 2 = 3.5 ··· 4 words required**
- **When an odd number of bytes are received, the upper 8 bits of last address read by the FROM instruction contain 00H.**



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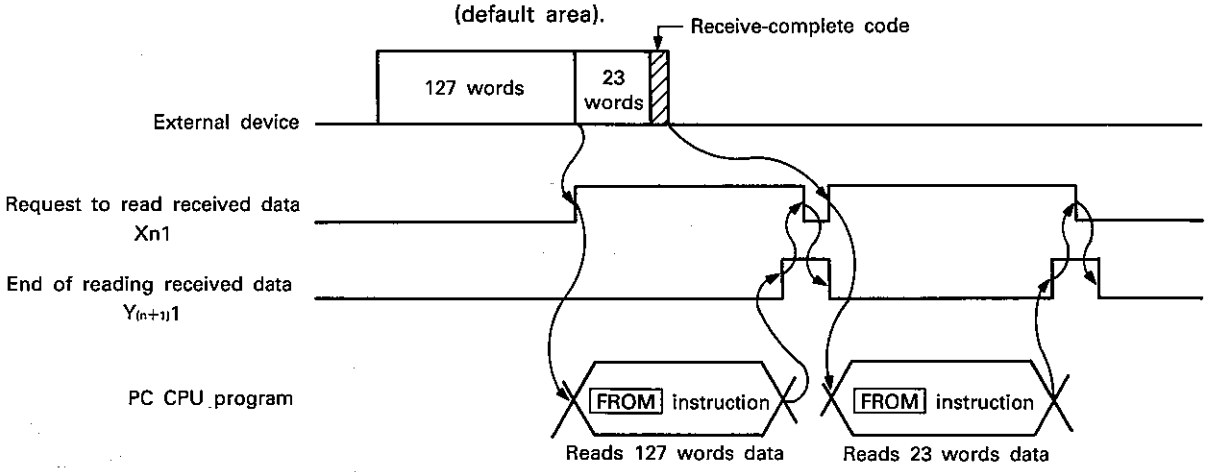
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**REMARKS**

If the length of receive data is greater than the length of no-protocol mode receive buffer memory, the data is processed as described below.

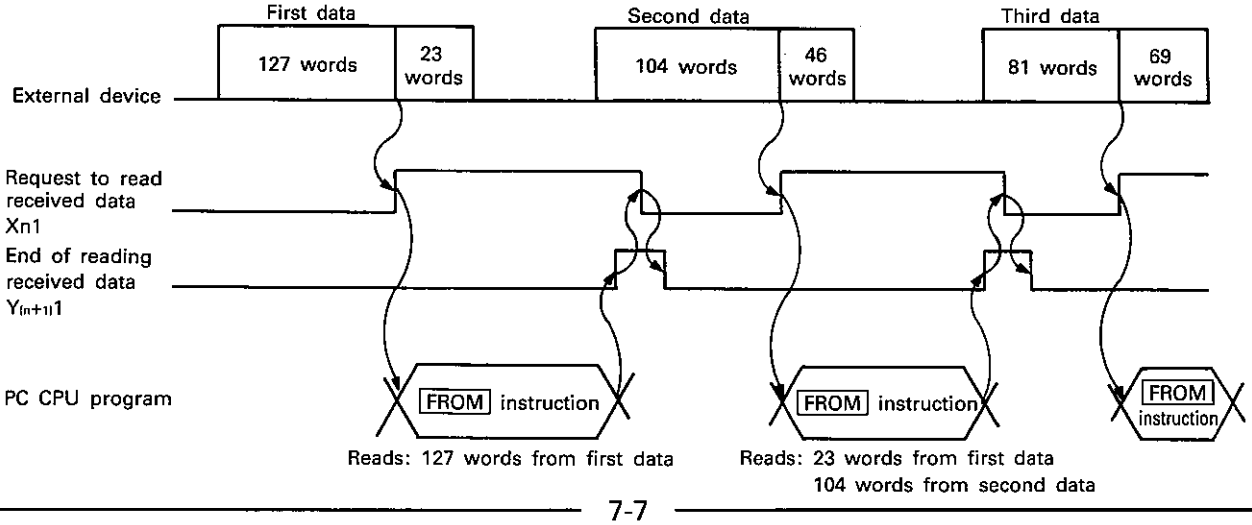
(1) Receiving data with the receive-complete code
If the AJ71C24 receives data which is longer than the receive area, it receives the amount of date to fill the receive area and then turns ON the receiving request signal Xn1.
When the PC CPU turns ON the receiving complete signal $Y_{(n+1)}$ the remaining data can be read.
These two operations are repeated until the receive-complete code is received.
Set the receive area so that the length of receive data is less than the length of the receive buffer memory for the no-protocol mode (specified in buffer memory address $107_H$).

Example: To receive 150 words of data when the receive area is from $80_H$ to $FF_H$ (default area).




(2) Receiving fixed length data
If the setting of the length of data to complete the receive is larger than the receive area, then the length of data is taken as the length of receive buffer memory for the no-protocol mode, specified in buffer memory address $107_H$ (default length 127 words).
Set the receive area so that the length of receive data is less than the length of the receive buffer memory for the no-protocol mode.

Example: To receive 150 words of data when the receive area is from $80_H$ to $FF_H$ (default area).








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(5) Clearing the receive buffer memory

If an error occurs due to failure of an external device, for example, while receiving data from an external device in the no-protocol mode, the data received up to the error may be incorrect or interrupted. To recover after an error has occurred it is possible to clear all received data and initialize the AJ71C24 buffer memory.

(a) Error detection

The following methods are used to detect errors while data is being received.

1) Reading the error LED display area

To detect errors the PC CPU can read the LED ON/OFF statuses, stored at buffer memory address $101_H$ as transmission error data.

2) PC input signals

Signals such as READY signals from external devices are connected to the PC CPU as input signals. The PC CPU can detect errors from the ON/OFF status of these signals.

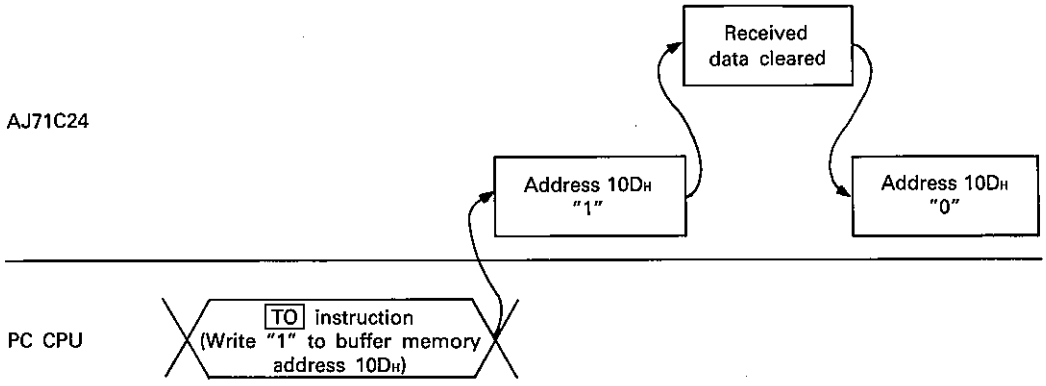
(b) Clearing received data

1) Range of data cleared

All data already received by the AJ71C24 is cleared and the no-protocol mode receive buffer memory area is initialized (refer to Appendix 4 for details).

2) How to clear received data

Received data is cleared by writing "1" to buffer memory address $10D_H$ using the TO instruction.
After clearing received data, the AJ71C24 clears the "1" that was written to buffer memory address $10D_H$.






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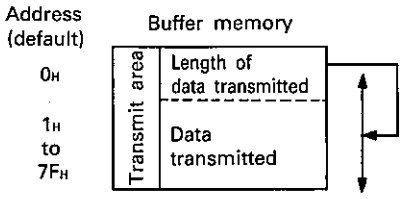
## 7.5 Transmitting Data in the No-protocol Mode (AJ71C24 → external device)

"Transmitting" refers to outputting data which was written to the no-protocol mode transmit buffer memory area (hereinafter abbreviated to "transmit area"), from the AJ71C24 to an external device in response to the PC CPU send request signal ($Y_{(n+1)}0$).

(1) Transmit area

The transmit area stores the length of data to be transmitted and the data itself. By default, addresses $0_H$ to $7F_H$ is allocated to the transmit area.

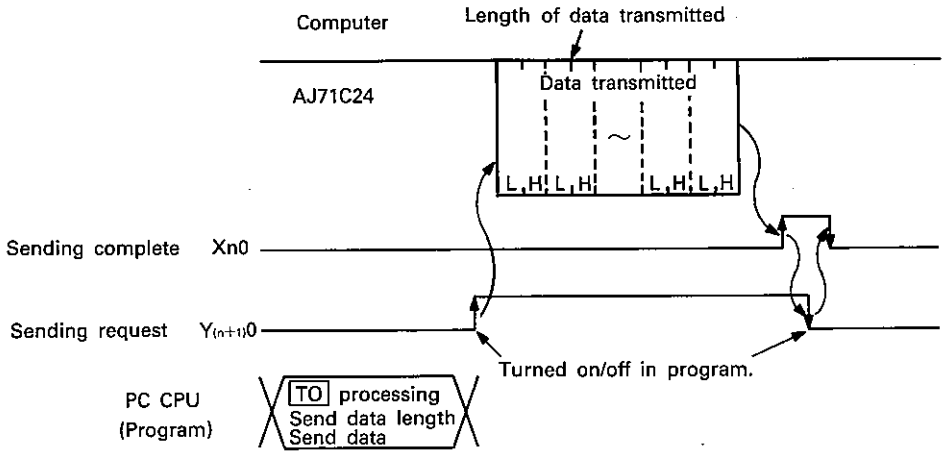
It is however possible to change the transmit area to suit the purpose of the data communication and specifications of the external devices. (Refer to section 5.4.4.)




- Specify the length of data to be transmitted with the TO instruction.
- Data is transmitted sequentially from the lowest address.

(2) Transmitting procedure

Protocol




**POINT**

**(1) An error occurs if the send data length is greater than the transmit area, or equal to "0". In this case "1" is written as transmission error data to the highest order bit (b15) of address $101_H$ (error LED display area) in the special-application memory area (refer to section 5.3.1 for details.)**

**(2) The send data length written in the head address is not transmitted.**

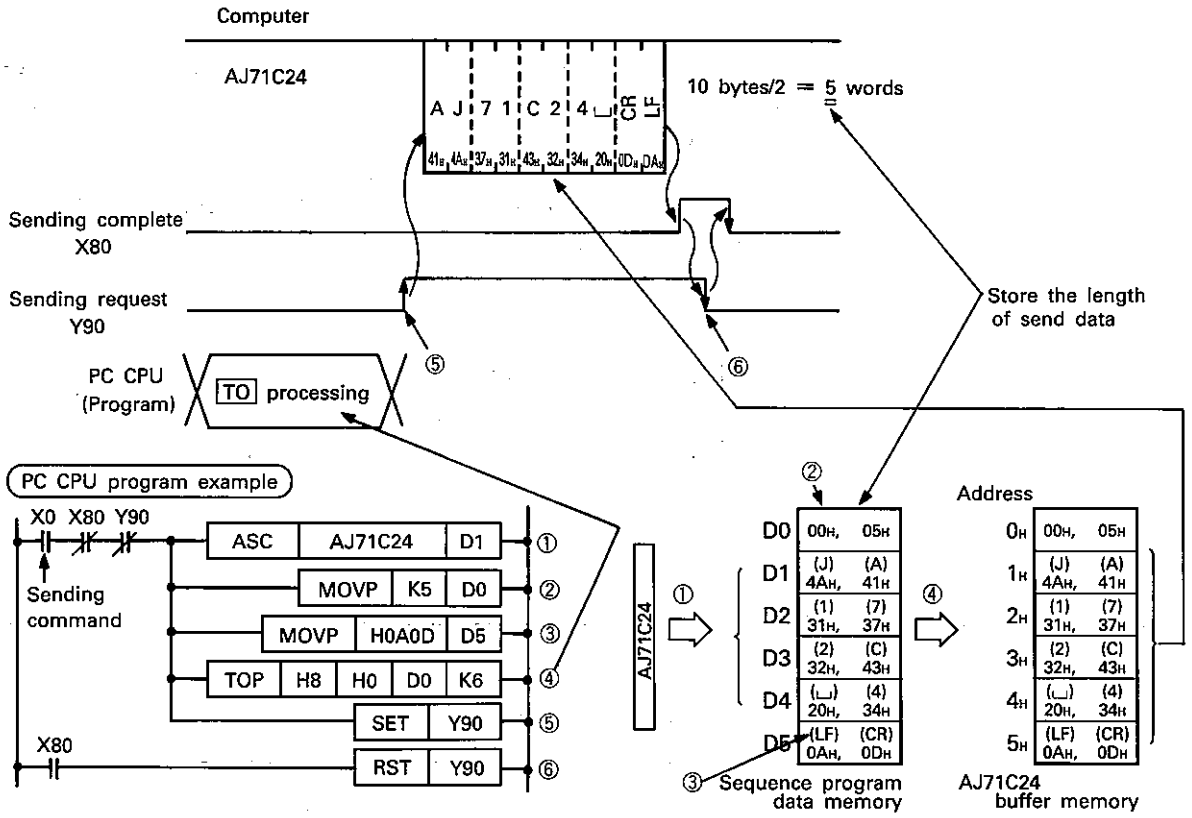


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(3) Transmit program example

Example 1: word units, default buffer memory assignment values

To transmit the characters "AJ71C24" CR, LF sent from the PC CPU to an external device (AJ71C24 I/O addresses 80 to 9F).



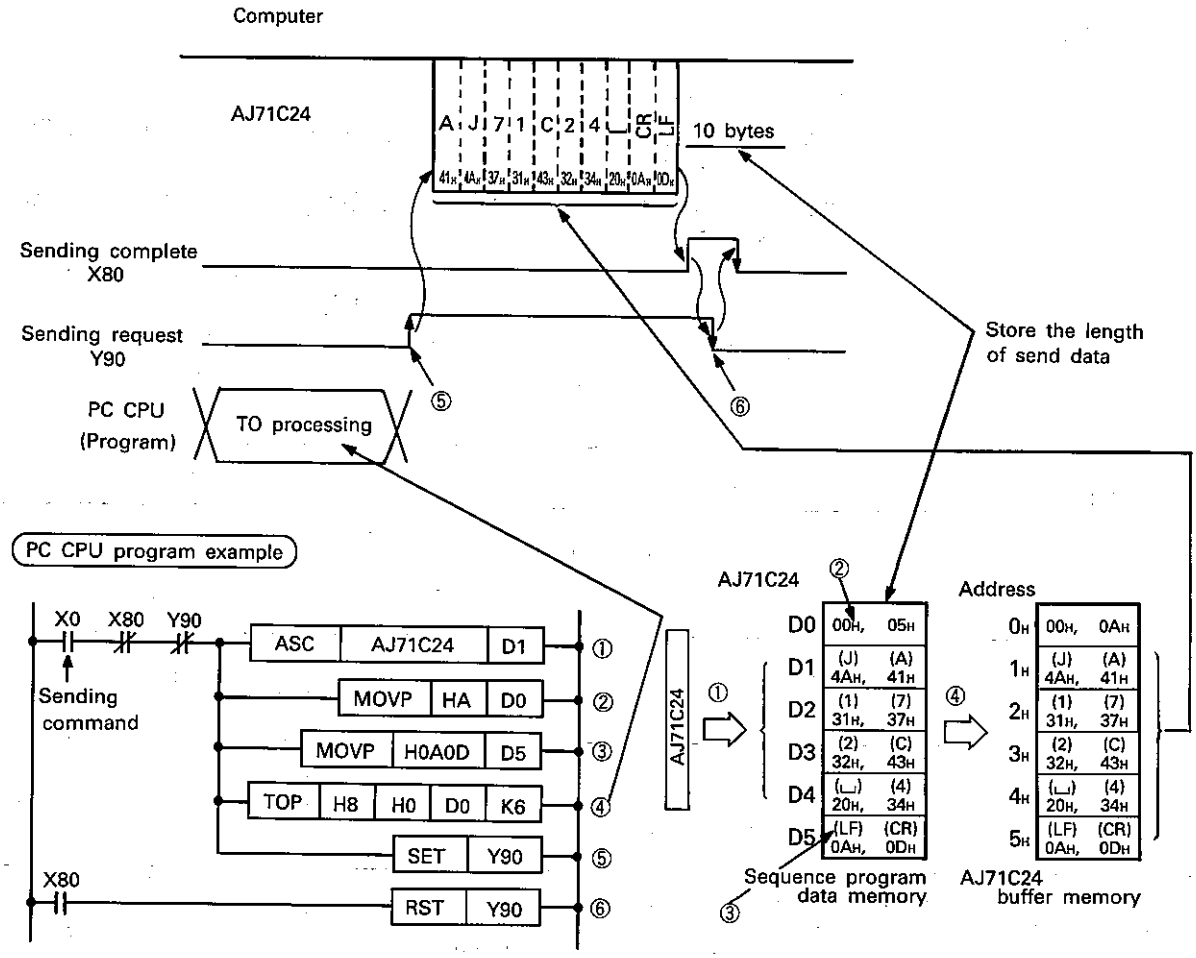





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Example 2: byte units, default buffer memory assignment values

To transmit the characters "AJ71C24" CR, LF sent from the PC CPU to an external device (AJ71C24 I/O addresses 80 to 9F).




**POINT**

**Even if transmission data is specified in byte units, the PC CPU TO instruction operates in word units. Therefore the length of the send data differs from the TO instruction specified data length.**



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# 8. TROUBLESHOOTING

Errors which can occur with the AJ71C24 and troubleshooting procedures are described in this chapter.

## 8.1. NAK Error Codes

Error codes and their definitions when an NAK code is transmitted during data communication between the computer and PC CPU are listed in Table 8.1.
The error codes are transmitted as 2-digit ASCII (hexadecimal) between $00_H$ and $FF_H$.
When several errors occur simultaneously, the code with the lowest number takes preference and is transmitted.
If any of the following errors occurs, the transmission sequences are initialized and LED's 2-NEU and 4-NEU (LED No. 4 and 7).

| Error Code (Hexadecimal) | Error | Error Definition | Relevant LED No. | Corrective Action |
|---|---|---|---|---|
| $00_H$ | Disable during run | Invalid access has been made during run.<br>(1) Data has been written to PC CPU with SW22 OFF (write disable during run).<br>(2) Sequence program and parameters have been written. | 2-C/N (LED No. 16)<br>4-C/N (LED No. 20) | (1) Start communication after turning on SW22.<br>(2) Write parameters after setting PC CPU to STOP. |
| $01_H$ | Parity error | Parity error<br>With SW16 ON (parity present), parity check result does not match the state of SW17 (odd/even parity). | 2-P/S (LED No. 17)<br>4-P/S (LED No. 21) | Check control protocol, change the SW setting or data. |
| $02_H$ | Sum check error | Sum check error<br>With SW21 ON (sum check present), sum check result of received data does not match the sum check code of sent data, i.e. send data is different from receive data. | 2-P/S (LED No. 17)<br>4-P/S (LED No. 21) | Check data sent from computer and sum check result, correct invalid data. |
| $03_H$ | Protocol error | Communications protocol not valid.<br>Communication has been made in protocol different from the one set by the mode setting switch. | 2-PRO (LED No. 18)<br>4-PRO (LED No. 22) | Check and correct the mode setting switch position and control protocol. Repeat data communication. |
| $04_H$ | Framing error | Framing error<br>Data does not comply with the setting of SW18 (stop bit). | 2-SIO (LED No. 19)<br>4-SIO (LED No. 23) | Change the setting of SW18 or control protocol. |
| $05_H$ | Overrun error | Overrun error<br>New data has been sent before AJ71C24 completes receiving the preceding data. | 2-SIO (LED No. 19)<br>4-SIO (LED No. 23) | Allow more time between transmitting data. |
| $06_H$ | Character area error | Character area A, B, or C error, or specified command does not exist<br>(1) The specification of the character area A, B, or C for the control protocol set with the mode setting switch is not correct.<br>(2) A command used in the protocol does not exist. (For example, a subsequence program was specified for A1N or A2NCPU.) | 2-PRO (LED No. 18)<br>4-PRO (LED No. 22) | (1) Check and correct the character area A, B, or C. Repeat data communication.<br>(2) Refer to the function list in section 3.3 and the ACPU User's Manual and correct the specified commands. Repeat data communication. |
| $07_H$ | Character error | Character error<br>Character other than "A to Z", "0 to 9", "␣" and control codes in Section 6.3.5 (1) has been received. | 2-PRO (LED No. 18)<br>4-PRO (LED No. 22) | Check and correct data. |
| $08_H$ | PC access error | Buffer memory is unable to make communication with PC.<br>CPU is not an A1(E), A1N, A2(E), A2N, A3(E), A3N, A3HCPU, or AJ72P25/R25. | 2-C/N (LED No. 16)<br>4-C/N (LED No. 20) | Change to a PC CPU which can carry out data communication. |

**Table 8.1 Error Code List (Continue)**



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| Error Code (Hexadecimal) | Error | Error Definition | Relevant LED No. | Corrective Action |
|---|---|---|---|---|
| 10H | PC number error | Defined PC number does not exist.<br>The PC number specified in the protocol was not "host" (FFH) or a station number set with the MELSECNET link parameters. | 2-C/N (LED No. 16)<br>4-C/N (LED No. 20) | Change the PC number to "host" (FFH) or a station number set with the MELSECNET link parameters. Repeat data communication. |
| 11H | Mode error | Incorrect communication between AJ71C24 and PC CPU<br>(1) After the AJ71C24 has correctly received a request from the computer, normal data communication is not carried out between the AJ71C24 and PC CPU due to noise, or some other reason. | —— | Repeat the data communication. If the error reoccurs, check for noise and other causes or replace the AJ71C24. Repeat the data communication. |
| 12H | Special function unit specification error | Special function unit specification error<br>A special function module, having buffer memory, which has the communication capability is not placed in the special function module number area. | 2-C/N (LED No. 16)<br>4-C/N (LED No. 20) | Check control protocol data or change the special function unit I/O location. |
| 13H | Program step No. specification error | Error in specification of a sequence program step number.<br>(1) A step number was specified which lies outside of the program range specified by the programmable controller CPU parameters. | 2-C/N (LED No. 16)<br>4-PRO (LED No. 20) | Specify a step number which lies within the specified range, or change the parameters and transfer them again. |
| 18H | Remote error | Remote run/stop impossible.<br>Remote stop/pause has already been implemented from another unit (such as another AJ71C24). | 2-PRO (LED No. 18)<br>4-PRO (LED No. 22) | Check for and reset remote stop/pause from another unit. |
| 21H | Special function unit bus error | Memory access to special function unit cannot be made (for command TR, TW).<br>(1) Special function unit control bus error<br>(2) Special function unit faulty. | 2-C/N (LED No. 16)<br>4-C/N (LED No. 20) | PC CPU, base unit, special function unit, or AJ71C24 hardware fault. Consult the nearest Mitsubishi representative. |

**Table 8.1 Error Code List**

**REMARKS**

(1) Error codes, 0H to 08H are transmitted to the external device after diagnosis by the AJ71C24 when access is made by the computer to AJ71C24.

(2) Error codes, 10H to 21H are generated by the PC CPU when access is made by the AJ71C24 to the PC CPU.



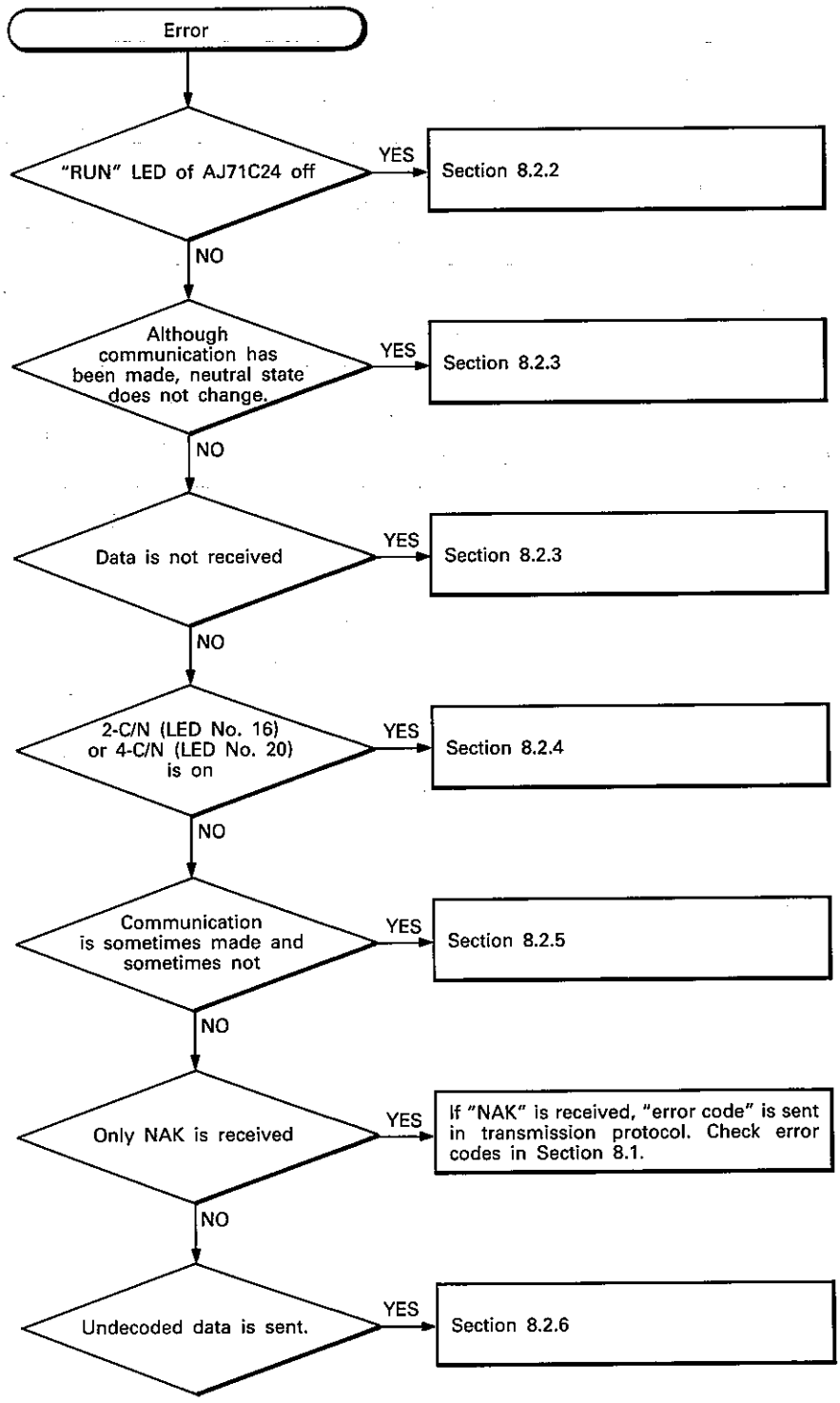
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## 8.2 Troubleshooting

This section describes basic troubleshooting procedures for the AJ71C24. for information on CPU module troubleshooting, refer to the A1, A2, A3CPU User's Manual.

### 8.2.1 Troubleshooting flow chart

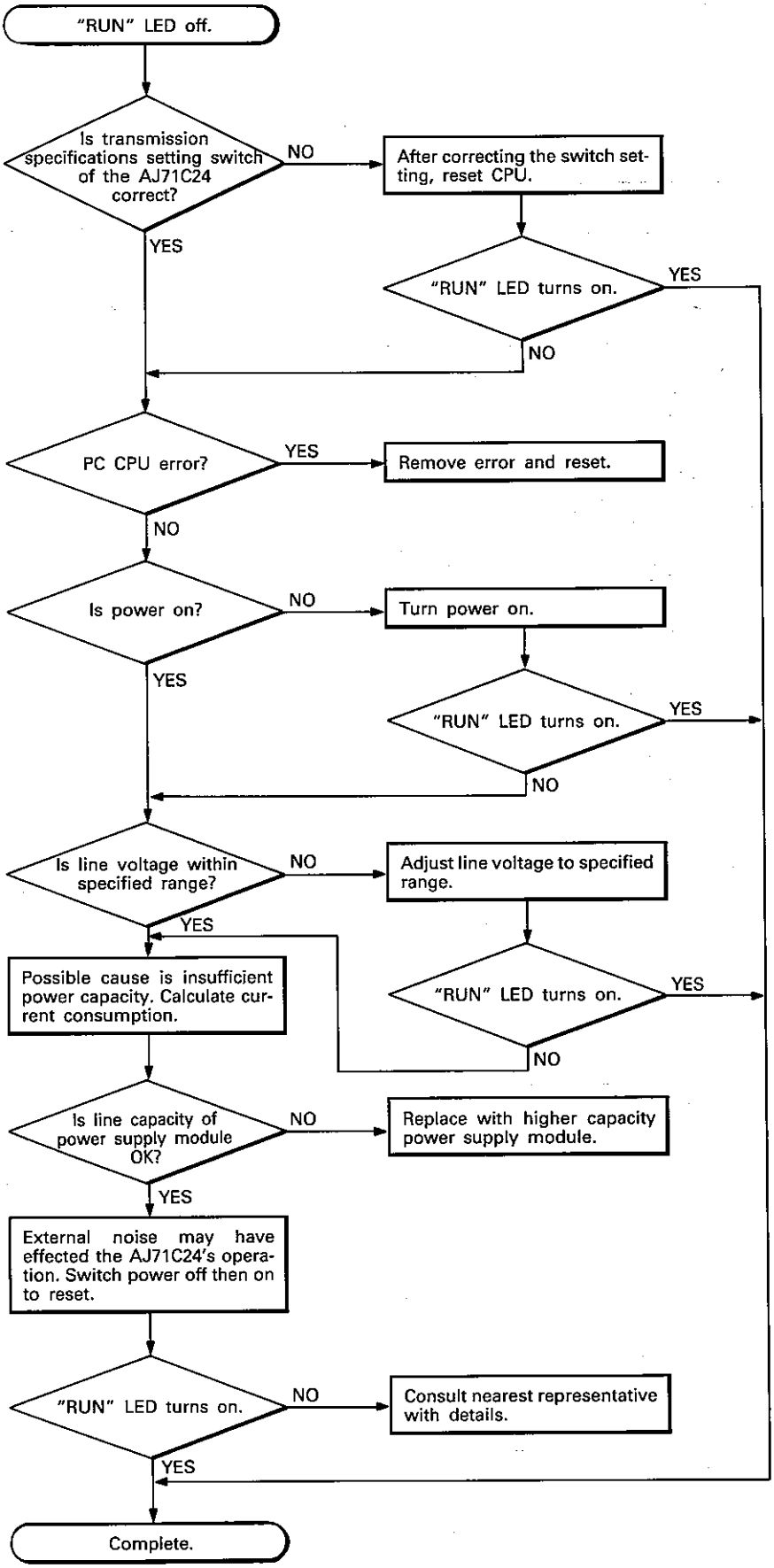
Errors are divided by phenomena.






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### 8.2.2 RUN LED turns off



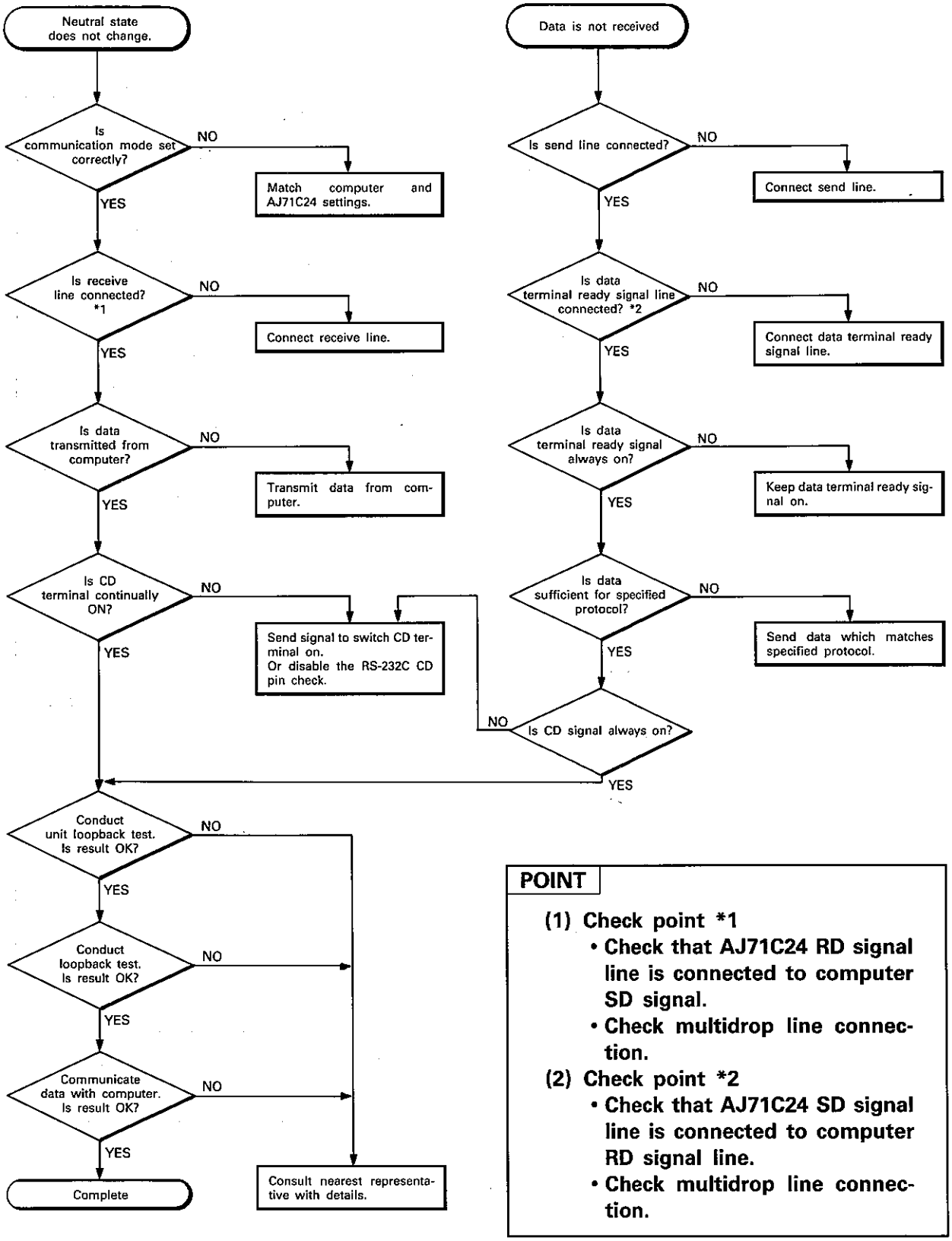





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### 8.2.3 Neutral state does not change or data is not received although communication has been normal

Despite apparently normal communication, the neutral state remains on and further communication is halted or data is not received.




**POINT**

**(1) Check point *1**
- **Check that AJ71C24 RD signal line is connected to computer SD signal.**
- **Check multidrop line connection.**

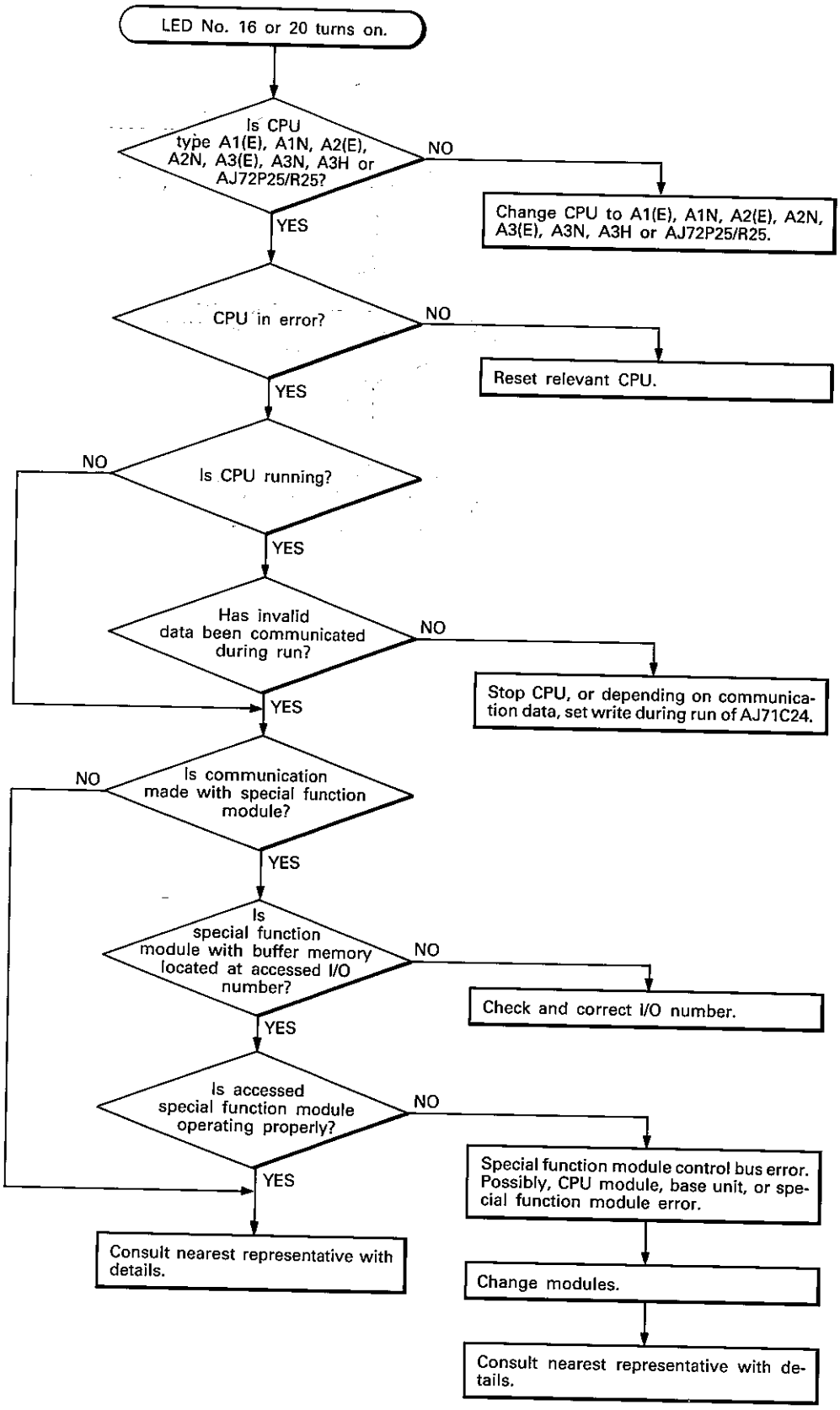
**(2) Check point *2**
- **Check that AJ71C24 SD signal line is connected to computer RD signal line.**
- **Check multidrop line connection.**



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### 8.2.4 2-C/N (LED No. 16) or 4-C/N (LED No. 20) turns on

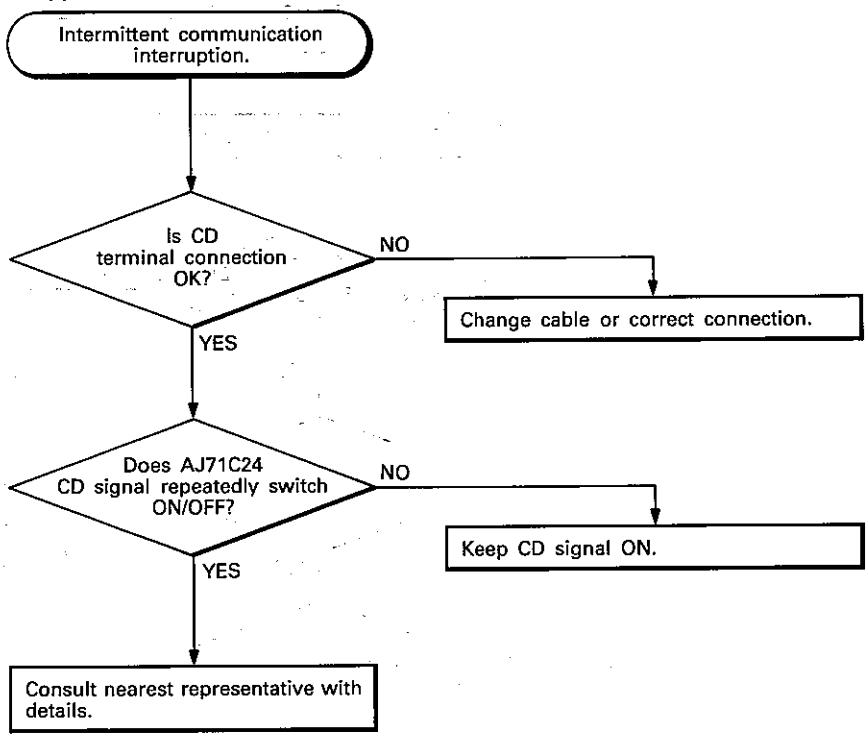
Flow chart for use when 2-C/N (LED No. 16) or 4-C/N (LED No. 20) on the AJ71C24 panel turns on.






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### 8.2.5 Intermittent communication interruption

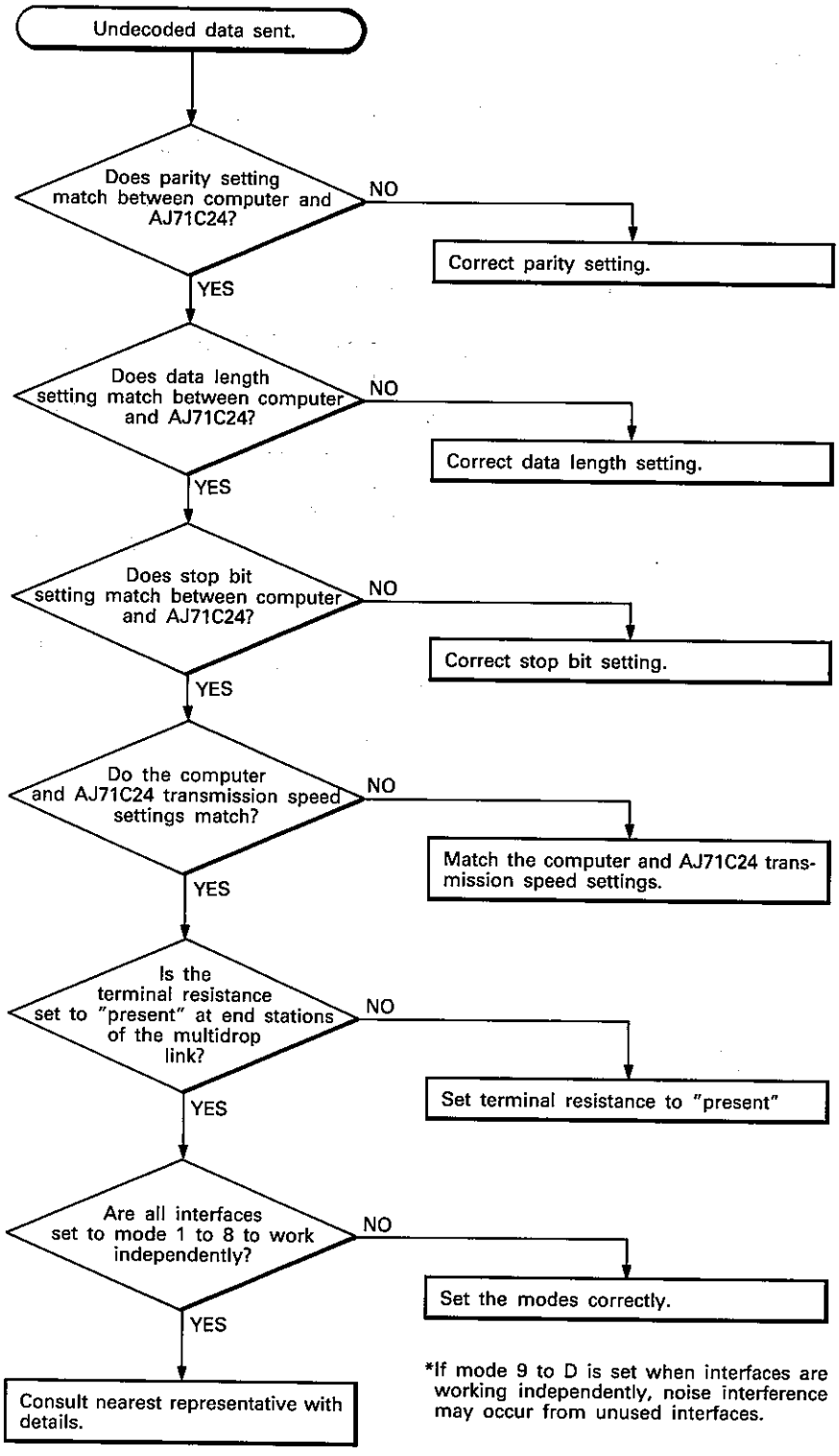





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### 8.2.6 Transmission of undecoded data

Flow chart for use when the AJ71C24 sends code and data, which is not included in the control code, in response to data sent from the computer.




*If mode 9 to D is set when interfaces are working independently, noise interference may occur from unused interfaces.

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# APPENDICES

## APPENDIX 1 AJ71C24-S3 and AJ71C24 Compatibility and Precautions Regarding Programs

Precautions that need to be observed when switching AJ71C24-S3 and AJ71C24 programs are described below.

### 1.1 Compatibility

External dimensions, method of attachment and basic programs (in the PC CPU and computer) are identical between the AJ71C24-S3 and AJ71C24.
They have full compatibility in the range of AJ71C24 functions.

### 1.2 Precautions when switching AJ71C24-S3 and AJ71C24 programs

Take care of the following points when replacing an AJ71C24 with an AJ71C24-S3.

(1) Buffer memory read and write (commands CR and CW)
Addresses $100_H$ to $11F_H$ in the AJ71C24-S3 buffer memory make up the special-application area.
Only use commands CR and CW to read from and write to the user area, with addresses higher than $120_H$.

(2) I/O to the PC CPU
The AJ71C24-S3 has a READY signal (Xn7).
In a link in the no-protocol mode, it is recommended that the READY signal be inserted into the AJ71C24 sequence program as an interlock signal.

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## APPENDIX 2 AJ71C24-S3 and AJ71C24 Function Comparison

Improved and added functions of the AJ71C24-S3 compared to the AJ71C24 are shown in the table below.

| Function | | | | AJ71C24 | AJ71C24-S3 | Reference Section |
|---|---|---|---|---|---|---|
| Unit READY signal | | | | ——— | ● READY signal is the I/O signal Xn7 to the PC CPU. | 3.4 |
| RS-232C CD pin check | | | | Normal CD pin check | ● The AJ71C24-S3 permits the CD pin to be carried out or disabled. | 3.3.3 |
| Transmission error data | | Display area | | ● It can be seen from the LED status on the front panel if an error has occurred or not. | ● The ON/OFF status of the LED's is stored in the buffer memory so that the sequence program can read the buffer memory for the PC CPU to check if a data communication error has occurred. | 3.3.4 |
| | | LED extinguish requests | | ● The PC CPU has to be reset. | ● The sequence program can make LED extinguish requests. | |
| Dedicated protocols 1 to 4 | | | Command | | | |
| | Extension file register | Batch read | ER | | Reads extension file register (R) in units of 1 point. | 6.7 |
| | | Batch write | EW | | Writes extension file register (R) in units of 1 point. | |
| | | Test (random write) | ET | | Specifies the extension file register (R) in units of 1 point using block or device number and makes a random write. | |
| | | Monitor data entry | EM | | Sets the extension file register (R) device numbers to be monitored in units of 1 point. | |
| | | Monitor | ME | | Monitors the extension file register after monitor data entry. | |
| | Micro-computer program | Batch read | Main | UR | Reads microcomputer main programs | 6.11.5 |
| | | | Sub | VR | Reads microcomputer subprograms | |
| | | Batch write | Main | UW | Writes microcomputer main programs | |
| | | | Sub | VW | Writes microcomputer subprograms | 6.11.6 |
| | Comment | Batch read | | KR | Reads comment memory | |
| | | Batch write | | KW | Writes comment memory | |
| | On-demand | | | | ● All transmission initiated by the computer | ● The PC CPU can make transmission requests during data communication with using dedicate protocols 1 to 4. | 6.13 |
| | Data communication with PC CPU on MELSECNET | | | | ● Communication only possible with PC CPU's loaded with AJ71C24. | ● Communication possible with PC CPU's on MELSECNET which are not loaded with AJ71C24. | 6.3.5 (4) |

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| Function | | AJ71C24 | AJ71C24-S3 | Reference Section |
|---|---|---|---|---|
| No-protocol | Receive-complete setting | ● Fixed as CR, LF (0D$_H$, 0A$_H$) | ● Can be set to desired value. (Default setting: CR, LF (0D$_H$, 0A$_H$)) | 5.4.1 |
| | Length of data to receive (receive with fixed data length) | ● Fixed as 127 words (254 bytes) | ● Can be set to desired value. (Default setting: 127 words) | 5.4.2 |
| | Data word/byte unit setting | ● Fixed as word units | ● Data can be handled as word units or byte units (default value: word units) | 5.4.3 |
| | Transmission buffer memory | Fixed as:<br>Head address<br>·····0$_H$<br>Buffer memory length<br>·····80$_H$ | ● Can be set to desired values, excluding memory area 100$_H$ to 11F$_H$<br>Default: Head address 0$_H$<br>Buffer memory length 80$_H$ | 5.4.4 |
| | Receive buffer memory | Fixed as:<br>Head address<br>·····80$_H$<br>Buffer memory length<br>·····80$_H$ | ● Can be set to desired values, excluding memory area 100$_H$ to 11F$_H$<br>Default: Head address 80$_H$<br>Buffer memory length 80$_H$ | 5.4.5 |
| | Receive data clear request | ● Necessary to reset the PC CPU to clear received data after an error occurs. All dedicated protocol communication data also lost. | ● No-protocol data only can be cleared by the sequence program. No effect on dedicated protocol communication data. | 7.4 |

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## APPENDIX 3 ASCII Code Table

Character codes used for the computer link are shown below. (7-bit codes)

| LSD \ MSD | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|---|
| | | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 0 | 0000 | NUL | DLE | SP | 0 | @ | P | ` | p |
| 1 | 0001 | SOH | DC1 | ! | 1 | A | Q | a | q |
| 2 | 0010 | STX | DC2 | !! | 2 | B | R | b | r |
| 3 | 0011 | ETX | DC3 | # | 3 | C | S | c | s |
| 4 | 0100 | EOT | DC4 | $ | 4 | D | T | d | t |
| 5 | 0101 | ENQ | NAK | % | 5 | E | U | e | u |
| 6 | 0110 | ACK | SYN | & | 6 | F | V | f | v |
| 7 | 0111 | BEL | ETB | ' | 7 | G | W | g | w |
| 8 | 1000 | BS | CAN | ( | 8 | H | X | h | x |
| 9 | 1001 | HT | EM | ) | 9 | I | Y | i | y |
| A | 1010 | LF | SUB | * | : | J | Z | j | z |
| B | 1011 | VT | ESC | + | ; | K | [ | k | { |
| C | 1100 | FF | FS | , | < | L | ¥ | l | \| |
| D | 1101 | CR | GS | - | = | M | ] | m | } |
| E | 1110 | SO | RS | . | > | N | ↑ | n | ~ |
| F | 1111 | SI | VS | / | ? | O | ← | o | DEL |

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## APPENDIX 4 DTR CONTROL

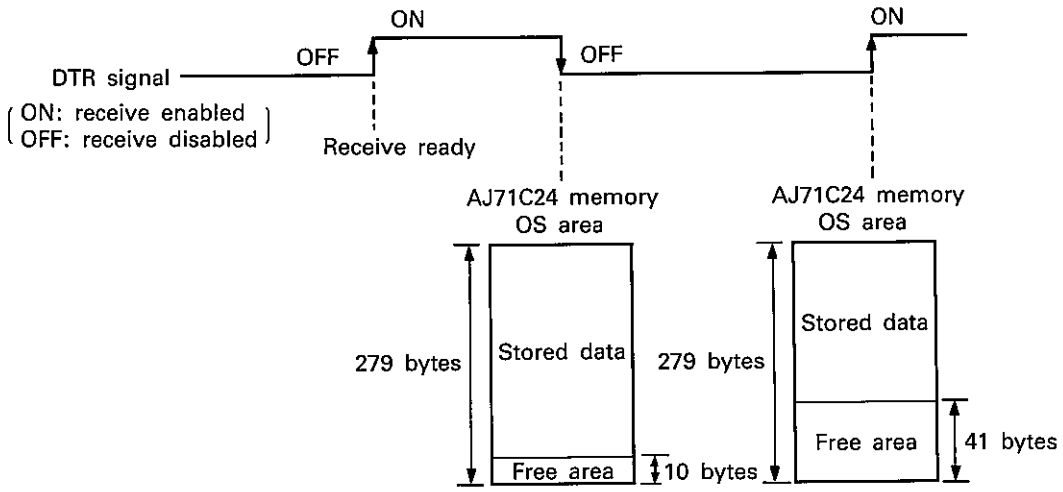
This appendix explains DTR control.

(1) Explanation of DTR control
DTR control enables and disables data communication with an external device via the AJ71C24 RS-232C by means of the DSR and DTR signals.
DTR control is not available for the RS-422.

(2) The AJ71C24 stores data received from and external device to the no-protocol receive buffer memory via its OS memory area.
Under the conditions below, the AJ71C24 temporarily stores received data to its OS area. When transfer to the no-protocol receive buffer memory is enabled (read request signal Xn1 is OFF), it transfers the data until the receive-complete code or until the fixed length of data has been transmitted.
Conditions:
1) When there is too much data for the buffer memory because the length of data received exceeds the no-protocol receive buffer memory area.
2) When data is transmitted from an external device before the PC CPU sends the data received previously.

(3) AJ71C24 DTR control
The size of the AJ71C24 data storage area is 279 bytes. It turns the DTR signal ON and OFF as follows:
less than 10 bytes storage area free : OFF
more than 41 bytes storage area free : ON

(4) When received data is cleared as described in (5) section 7.4, all data in the OS area is cleared simultaneously with the data in the no-protocol receive buffer memory.




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## APPENDIX 5 Communication Times between Programmable Controller CPU and AJ71C24.

During PC CPU run, data is processed after the execution of the END instruction in response to a request from the AJ71C24. The maximum number of points processed per communication are given in Section 3.3.1.
The intervening time (i.e. by how much the san time increases) for each processing operation and its corresponding processing time (indicated in numbers of scans) is shown below.

| Item | | | | | Intervening Time (Scan time increase) | | | Scan Count Required for Processing |
|---|---|---|---|---|---|---|---|---|
| | | | | | A1N, A2N, A3N | A3H | Access points | |
| Device data | Device memory | Batch read | Bit units | BR | 0.76m sec | 0.57m sec | 256 points | 1 scan<br>2 scans for device "R" only |
| | | | Word units | WR | 1.13m sec | 0.81m sec | 64 points | |
| | | Batch write | Bit units | BW | 1.13m sec | 0.94m sec | 256 points | 2 scans<br>1 scan for "enable during run" setting (excluding R) |
| | | | Word units | WW | 1.13m sec | 0.84m sec | 64 points | |
| | | Test Random write | Bit units | BT | 1.13m sec | 0.90m sec | 20 points | 2 scans<br>1 scan for "enable during run" setting (excluding R) |
| | | | Word units | WT | 1.13m sec | 0.90m sec | 10 points | |
| | | Monitor data entry | Bit units | BM | — | — | — | — |
| | | | Word units | WM | | | | 1 scan for device "R" only |
| | | Monitor | Bit units | MB | 1.51m sec | 0.93m sec | 20 points | 1 scan |
| | | | Word unit | MN | 1.51m sec | 0.96m sec | 10 points | |
| | Extension file register | Batch read | | ER | 1.27m sec | 0.76m sec | 64 points | 2 scans |
| | | Batch write | | EW | 1.27m sec | 0.76m sec | 64 points | |
| | | Test Random write | | ET | 1.31m sec | 0.87m sec | 10 points | |
| | | Monitor data entry | | EM | — | — | — | — |
| | | Monitor | | ME | 1.75m sec | 0.98m sec | 20 points | 1 scan |
| | Buffer memory | Batch read | | CR | — | — | — | — |
| | | Batch write | | CW | | | | |
| Special function module Buffer memory | | Batch read | | TR | FROM instruction processing time+ 1.13m sec | FROM instruction processing time+ 0.81m sec | 128 bytes | 1 scan |
| | | Batch write | | TW | | | | 2 scans<br>1 scan when "enable during run" is set |
| Program | Sequence program | Batch read | Main | MR | 1.20m sec | 0.78m sec | 64 steps | 1 scan |
| | | | Sub | SR | 1.20m sec | 0.84m sec | | |
| | | Batch write | Main | MW | 0.67m sec | 0.55m sec | | 2 scans<br>1 scan when "enable during run" is set |
| | | | Sub | SW | 0.67m sec | 0.55m sec | | |
| | Micro-computer program | Batch read | Main | UR | 1.35m sec | 0.76m sec | 128 bytes | 2 scans |
| | | | Sub | VR | 1.35m sec | 0.76m sec | | |
| | | Batch write | Main | UW | 1.35m sec | 0.76m sec | | |
| | | | Sub | VW | 1.53m sec | 0.73m sec | | |
| | Comment | Batch read | | KR | 1.35m sec | 0.76m sec | 128 bytes | 2 scans |
| | | Batch write | | KW | 1.53m sec | 0.73m sec | | |
| | Parameter | Batch read | | PR | 0.68m sec | 0.50m sec | 128 bytes | 2 scans |
| | | Batch write | | PW | — | — | — | — |
| | | Analysis request | | PS | | | | |
| PC CPU | | Remote run | | RR | — | — | — | — |
| | | Remote stop | | RS | | | | |
| | | PC type read | | PC | 0.34m sec | 0.34m sec | — | 1 scan |
| Global | | | | GW | — | — | — | — |

**POINT**

**(1) The PC CPU can only process one of the above operations at each END instruction. If the A6GPP and AJ71C24 access a given PC CPU at the same time, one unit must wait until the other unit terminates processing. Therefore, scan count required for processing increases.**

**(2) With no AJ71C24 communication, scan time increases 0.2m sec (A3HCPU is 0.1m sec).**

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## APPENDIX 6 Special Function Module Buffer Memory Addresses

The special function module buffer memory addresses specified for reading and writing (commands TR, TW) data to and from special function module buffer memory with protocols 1 to 4 are listed below.
Refer to the unit manuals for details of the buffer memory contents.

(1) Type A68AD analog-digital converter module

| Buffer Memory Contents | Address (Hexadecimal) | | Address for FROM/TO Instruction |
|---|---|---|---|
| | Lower 8 bits | Higher 8 bits | |
| Number of channels | 80H | 81H | 0 |
| Averaging processing specification | 82H | 83H | 1 |
| CH1 averaging time, count | 84H | 85H | 2 |
| CH2 averaging time, count | 86H | 87H | 3 |
| CH3 averaging time, count | 88H | 89H | 4 |
| CH4 averaging time, count | 8AH | 8BH | 5 |
| CH5 averaging time, count | 8CH | 8DH | 6 |
| CH6 averaging time, count | 8EH | 8FH | 7 |
| CH7 averaging time, count | 90H | 91H | 8 |
| CH8 averaging time, count | 92H | 93H | 9 |
| CH1 digital output value | 94H | 95H | 10 |
| CH2 digital output value | 96H | 97H | 11 |
| CH3 digital output value | 98H | 99H | 12 |
| CH4 digital output value | 9AH | 9BH | 13 |
| CH5 digital output value | 9CH | 9DH | 14 |
| CH6 digital output value | 9EH | 9FH | 15 |
| CH7 digital output value | A0H | A1H | 16 |
| CH8 digital output value | A2H | A3H | 17 |
| Write data error code | C4H | C5H | 34 |

(2) Type A62DA digital-analog converter module

| Buffer Memory Contents | Address (Hexadecimal) | | Address for FROM/TO Instruction |
|---|---|---|---|
| | Lower 8 bits | Higher 8 bits | |
| CH1 digital value | 10H | 11H | 0 |
| CH2 digital value | 12H | 13H | 1 |
| CH1 voltage set value check code | 14H | 15H | 2 |
| CH2 voltage set value check code | 16H | 17H | 3 |
| CH1 current set value check code | 18H | 19H | 4 |
| CH2 current set value check code | 1AH | 1BH | 5 |

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## (3) Type A84AD analog-digital converter module

| Buffer Memory Contents | Address (Hexadecimal) | | Address for FROM/TO Instruction |
|---|---|---|---|
| | Lower 8 bits | Higher 8 bits | |
| Unused area | 10H | 11H | 0 |
| Averaging processing specification | 12H | 13H | 1 |
| CH1 averaging time, count | 14H | 15H | 2 |
| CH2 averaging time, count | 16H | 17H | 3 |
| CH3 averaging time, count | 18H | 19H | 4 |
| CH4 averaging time, count | 1AH | 1BH | 5 |
| Unused area (reserved) | ——— | ——— | ——— |
| CH1 digital I/O value | 24H | 25H | 10 |
| CH2 digital I/O value | 26H | 27H | 11 |
| CH3 digital I/O value | 28H | 29H | 12 |
| CH4 digital I/O value | 2AH | 2BH | 13 |
| CH1 internal set mode flag | 2CH | 2DH | 14 |
| CH2 internal set mode flag | 2EH | 2FH | 15 |
| CH3 internal set mode flag | 30H | 31H | 16 |
| CH4 internal set mode flag | 32H | 33H | 17 |
| CH1 temperature detector value | 34H | 35H | 18 |
| CH2 temperature detector value | 36H | 37H | 19 |
| CH3 temperature detector value | 38H | 39H | 20 |
| CH4 temperature detector value | 3AH | 3BH | 21 |
| CH1 set value check code | 3CH | 3DH | 22 |
| CH2 set value check code | 3EH | 3FH | 23 |
| CH3 set value check code | 40H | 41H | 24 |
| CH4 set value check code | 42H | 43H | 25 |
| Write data error code | 44H | 45H | 26 |
| Analog output permitted signal enable/disable flag | 46H | 47H | 27 |
| CH1 loaded module code | 48H | 49H | 28 |
| CH2 loaded module code | 4AH | 4BH | 29 |
| CH3 loaded module code | 4CH | 4DH | 30 |
| CH4 loaded module code | 4EH | 4FH | 31 |
| CH1 temperature set range (offset) | 50H | 51H | 32 |
| CH1 temperature set range (gain) | 52H | 53H | 33 |
| CH2 temperature set range (offset) | 54H | 55H | 34 |
| CH2 temperature set range (gain) | 56H | 57H | 35 |
| CH3 temperature set range (offset) | 58H | 59H | 36 |
| CH3 temperature set range (gain) | 5AH | 5BH | 37 |
| CH4 temperature set range (offset) | 5CH | 5DH | 38 |
| CH4 temperature set range (gain) | 5EH | 5FH | 39 |

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(4) Type AD61(S1) high-speed counter module

| Buffer Memory Contents | Address (Hexadecimal) | | Address for FROM/TO Instruction | |
|---|---|---|---|---|
| | Channel 1 | Channel 2 | CH1 | CH2 |
| Unused area (reserved) | 80H | C0H | 0 | 32 |
| | 81H | C1H | | |
| Preset value write (lower bits) | 82H | C2H | 1 | 33 |
| Preset value write (middle bits) | 83H | C3H | | |
| Preset value write (higher bits) | 84H | C4H | 2 | 34 |
| | 85H | C5H | | |
| Mode register | 86H | C6H | 3 | 35 |
| | 87H | C7H | | |
| Present value read (lower bits) | 88H | C8H | 4 | 36 |
| Present value read (middle bits) | 89H | C9H | | |
| Present value read (higher bits) | 8AH | CAH | 5 | 37 |
| | 8BH | CBH | | |
| Set value read, write (lower bits) | 8CH | CCH | 6 | 38 |
| Set value read, write (middle bits) | 8DH | CDH | | |
| Set value read, write (higher bits) | 8EH | CEH | 7 | 39 |
| | 8FH | CFH | | |

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## (5) Type AD71(S1) positioning module

| Buffer Memory Contents | | Address (Hexadecimal) | Address for FROM/TO Instruction |
|---|---|---|---|
| X axis positioning start data | | 200H to 391H | 0 to 200 |
| Error reset | | 392H 393H | 201 |
| Y axis positioning start data | | 458H to 5E9H | 300 to 500 |
| Positioning data | X axis positioning data | 2040H to 235FH | 3872 to 4271 |
| Positioning speed | X axis positioning data | 2360H to 267FH | 4272 to 4671 |
| Dwell time | X axis positioning data | 2680H to 299FH | 4672 to 5071 |
| Positioning address | X axis positioning data | 29A0H to 2FDFH | 5072 to 5871 |
| Positioning data | Y axis positioning data | 2FE0H to 32FFH | 5872 to 6271 |
| Positioning speed | Y axis positioning data | 3300H to 361FH | 6272 to 6671 |
| Dwell time | Y axis positioning data | 3620H to 393FH | 6672 to 7071 |
| Positioning address | Y axis positioning data | 3940H to 3F7FH | 7072 to 7871 |
| X axis parameter | | 3F80H to 3F9FH | 7872 to 7887 |
| Y axis parameter | | 3FA8H to 3FC7H | 7892 to 7907 |
| X axis zero return data | | 3FD0H to 3FDDH | 7912 to 7917 |
| Y axis zero return data | | 3FE4H to 3FF1H | 7922 to 7928 |

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(6) Type AD72 positioning module

| Buffer Memory Contents | Address (Hexadecimal) | Address for FROM/TO Instruction |
|---|---|---|
| X axis positioning start data | 200H to 391H | 0 to 200 |
| Error reset | 392H 393H | 201 |
| Y axis positioning start data | 458H to 5E9H | 300 to 500 |
| Monitor area | 6B0H to 6BFH | 600 to 607 |
| X axis positioning data | 2040H to 2FDFH | 3872 to 5871 |
| Y axis positioning data | 2FE0H to 3F7FH | 5872 to 7871 |
| X axis parameters | 3F80H to 3F9FH | 7872 to 7891 |
| Y axis parameters | 3FA8H to 3FC7H | 7892 to 7911 |
| X axis zero return data | 3FD0H to 3FDDH | 7912 to 7917 |
| Y axis zero return data | 3FE4H to 3FE1H | 7922 to 7928 |

(7) AJ71C24-S3

| Address Specified by Computer | Address when Connected to Computer | |
|---|---|---|
| 1000H to 11FFH | 0 to FFH | |
| 1200H to 123FH | 100H to 11FH | Special-application area |
| 1240H to 1FFFH | 120H to 7FFH | |

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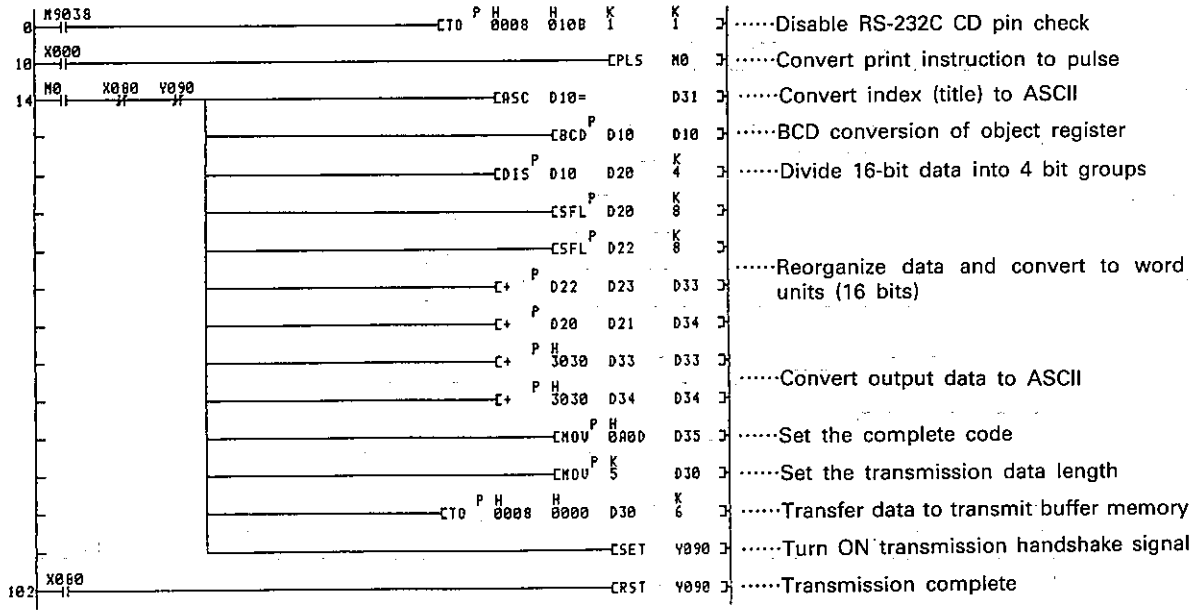
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## APPENDIX 7 Sequence Program Example to Output No-protocol Mode Word Device Data to Printer

This program shows an example of outputting to printer and printing out of the contents of the data registers (D), link registers (W) and file registers (R) and current timer and counter values.

(1) Sequence program example

To output data stored in register D10 to K6PR (printer data D10 = 1234 ).




**REMARKS**

AJ71C24 transmission specification settings for output to printer

| | K6PRE | K7PRE |
|---|---|---|
| Baud rate | 2400 | 9600 |
| Data length | 8 | 8 |
| Stop bits | 1 | 2 |
| Parity check | Even | None |
| Comments | | Baud rate can be changed to 2400 |

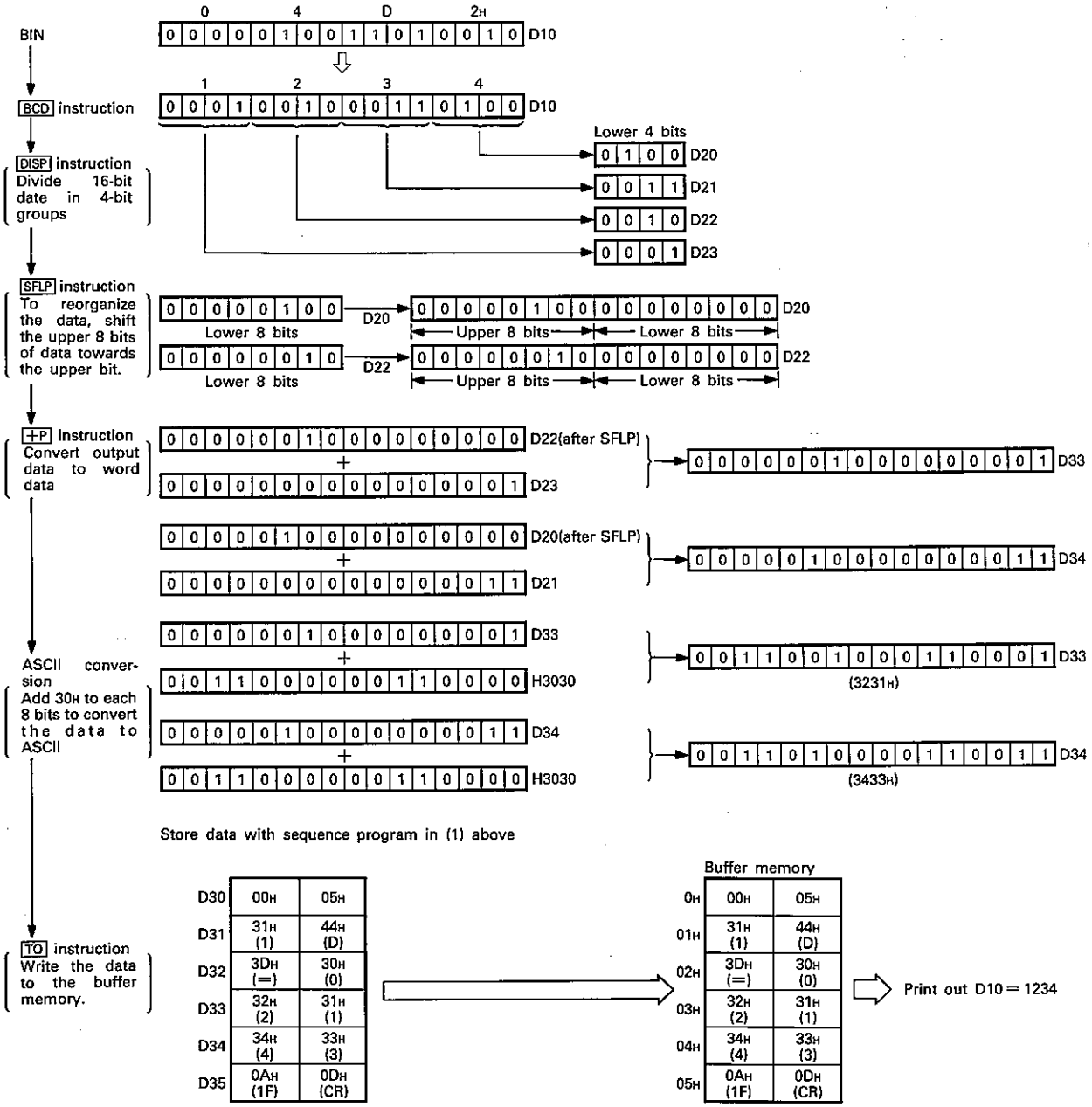
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(2) Procedure to convert data stored in a data register to printer output data.
The PC CPU handles numerical data in binary, so that it is necessary to convert data to be printed out from binary (BIN) to ASCII. Data is output sequentially from the buffer memory to printer from the lowest address (head address) with the lower 8 bits before the upper 8 bits. Therefore the order of the data to be output to the printer has be reorganized by the sequence program. The example for this conversion for the program described in (1) is given below.

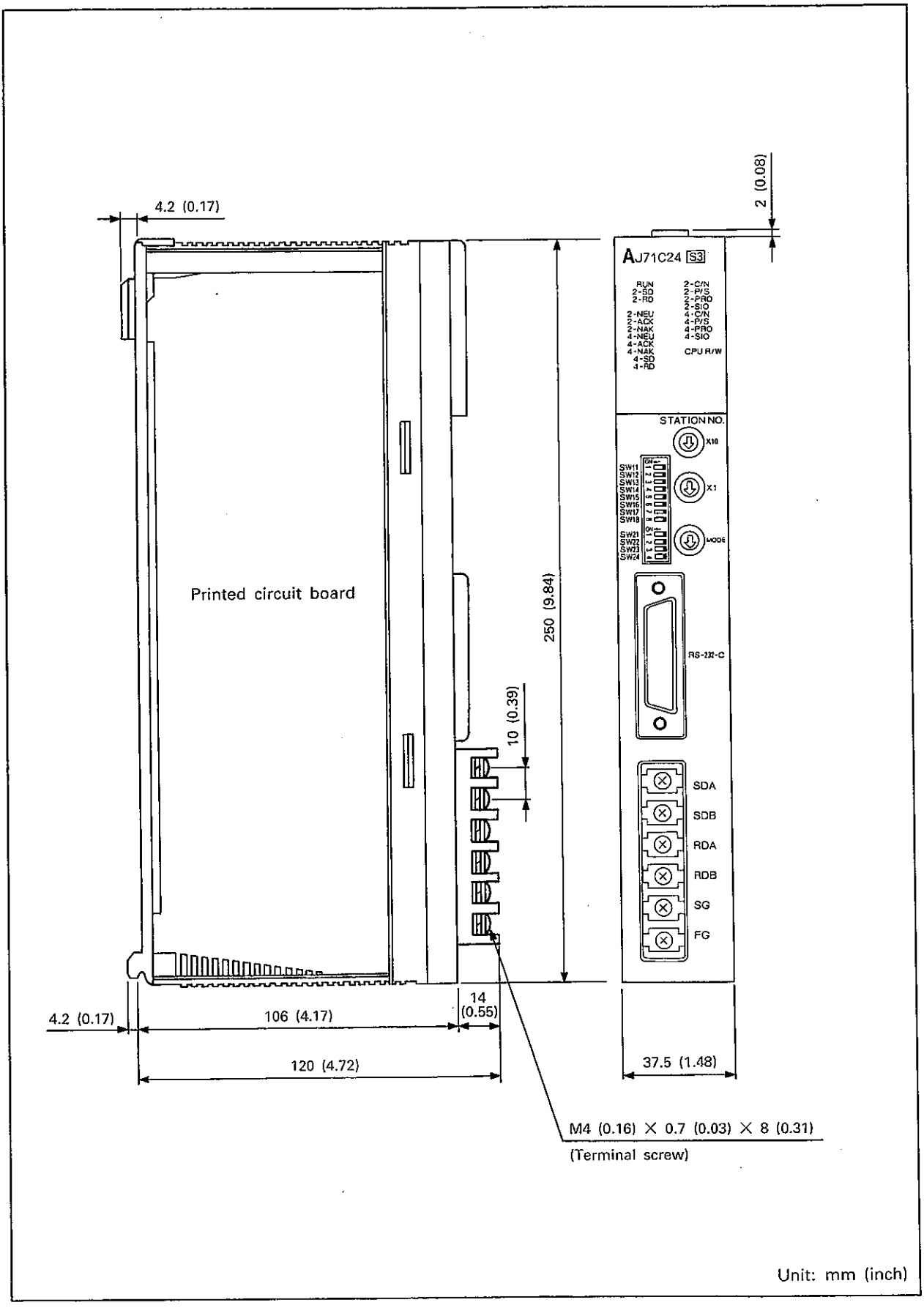
Example: To convert "1234" stored in the data register to ASCII






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## APPENDIX 8 External View




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**IMPORTANT**

**The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.**

**(1) Ground human body and work bench.**

**(2) Do not touch the conductive areas of the printed circuit board and its electrical parts with any non-grounded tools etc.**

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