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MZ 7130 / MZ 7132

68030-Based VMEbus CPU Boards

Hardware Reference Manual

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July 1991

MZ 7130 / MZ 7132

68030-based VMEbus CPU Boards

Hardware Reference Manual

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MZ 7130 / MZ 7132 Product Notes

For technical assistance, contact the Mizar Technical Support Center at 1- 214-446-2664.

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Preface

This manual describes both the MZ 7130 and the MZ 7132 68030-based CPU VMEbus boards, referred to in the manual as the MZ 7130 / MZ 7132. Within this manual, you are provided with functional descriptions, hardware specifications, installation instructions and firmware requirements. It is assumed that you are familiar with the VMEbus specification and the MC68030 CPU.

This manual contains the following sections:

Section 1 **User's Guide**
Describes the MZ 7130 / MZ 7132, its configuration, and its installation.

Section 2 **Programmer's Guide**
Describes the address maps, serial ports, SmartWatch, CPU interrupts and registers.

Section 3 **Hardware Reference Guide**
Describes the clocks, memory devices, SCSI interface, VMEbus interface, connector pin assignments and the schematics.

Manual Conventions

Address and Data Standards

Throughout this manual, the following standards are maintained for data and address prefixes:

%	Signifies a binary number
& or (No Notation)	Signifies a decimal number
$	Signifies a hexadecimal number

Logic States

The terms "assert" and "negate" refer to the logic state of a signal without indicating the associated voltage level. Thus, a signal can be "asserted" and "active low".

"Assert"	Refers to a signal that is active.
"Negate"	Refers to a signal that is inactive.

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SECTION 1
User's Guide

1.0 Overview

This section contains the following information concerning the MZ 7130 / MZ 7132:

1.1 General Description of the Boards
1.2 Unpacking the Boards
1.3 Configuring the Jumpers
1.4 Installing the Boards
1.5 Powering Up and Testing the Boards

1.1 General Description of the Boards

The MZ 7130 / MZ 7132 are high performance CPU boards which incorporate the MC68030 microprocessor chip and the optional 68882 floating point coprocessor. Their features include the following:

- An MC68030 or MC68EC030 processor
- An optional MC68882 floating point co-processor
- Four or sixteen Mbytes of dual-ported DRAM with parity
- Up to one Mbyte of EPROM
- Two serial ports
- A battery backed-up time-of-day clock (SmartWatch)
- A VMEbus system controller
- A SCSI interface
- A VMEbus interrupt handler/generator
- A mailbox interrupt
- A full 32-bit daughter card interface
- A full 32-bit VMEbus master and slave interface
- Five counter/timers
- Up to four Gbytes addressing range

A complete address map for the MZ 7130 / MZ 7132 can be found in Section 2.0 of this manual.

1.2 Unpacking the Boards

Mizar supplies complete systems for end users, as well as hardware and software for OEM and VAR buyers. There is no standard package or prepackaged system to check your shipment against. You must check each item on the packing list against your purchase order and the actual, physical components. Mizar tests all systems, boards and peripherals before these items are shipped to our customers.

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The MZ 7130 / MZ 7132 placement diagram is shown below:

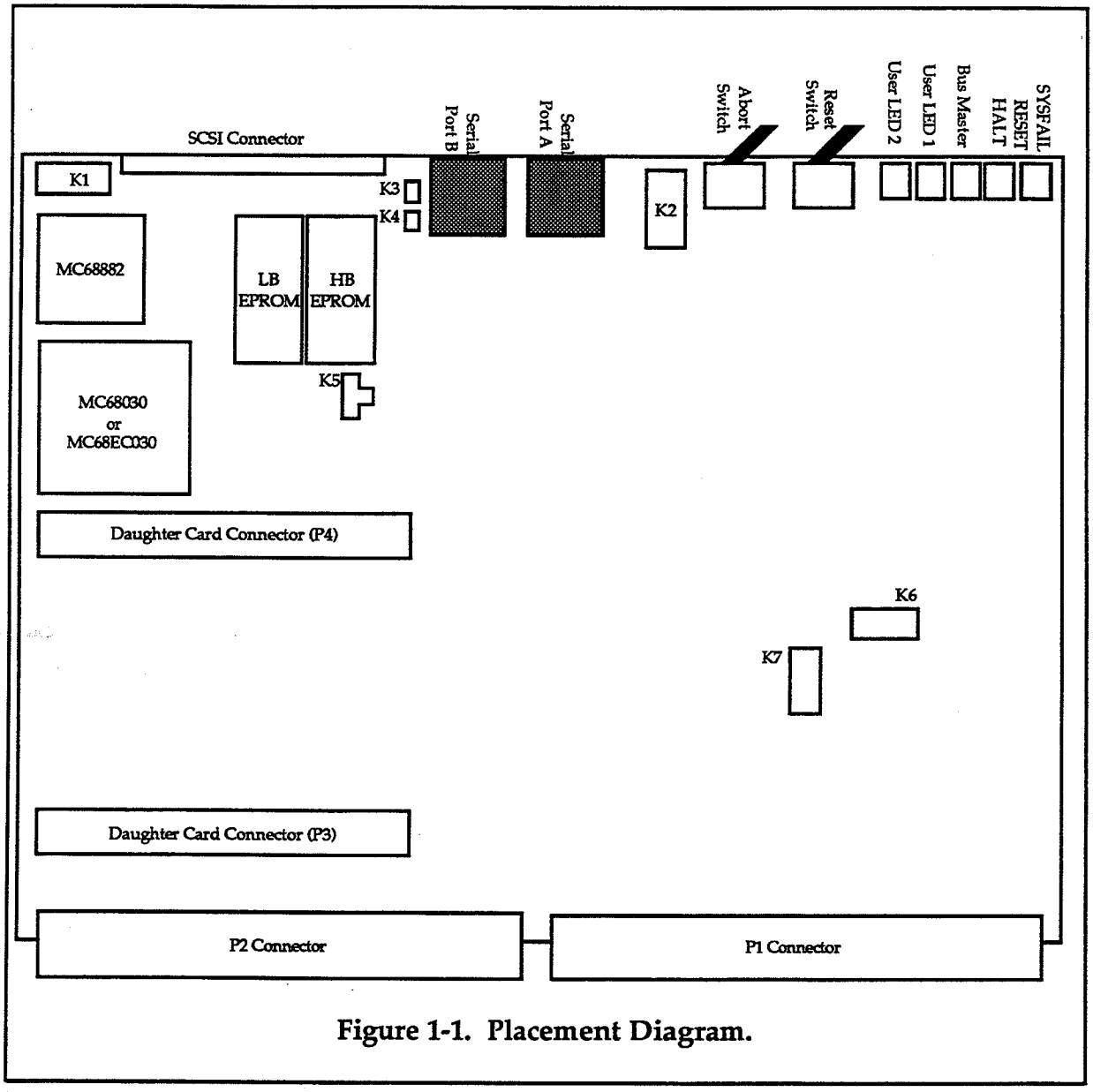


Figure 1-1. Placement Diagram.

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For EPROM devices of type 27512 or smaller (28-pin devices), pin pair 3 and 8 of K1 must be jumpered. This pin pair provides direct connection to VCC. For 32-pin EPROM devices, pin pair 3 and 8 are jumpered for 27010 devices only. There always will be at least one jumper required on K1, regardless of EPROM size. In addition to ensuring that VCC is connected on the 28-pin devices, the K1 jumper block passes along the address lines required for the larger EPROM sizes.

Refer to Figure 1-2 for correct jumpering of the desired EPROM size.

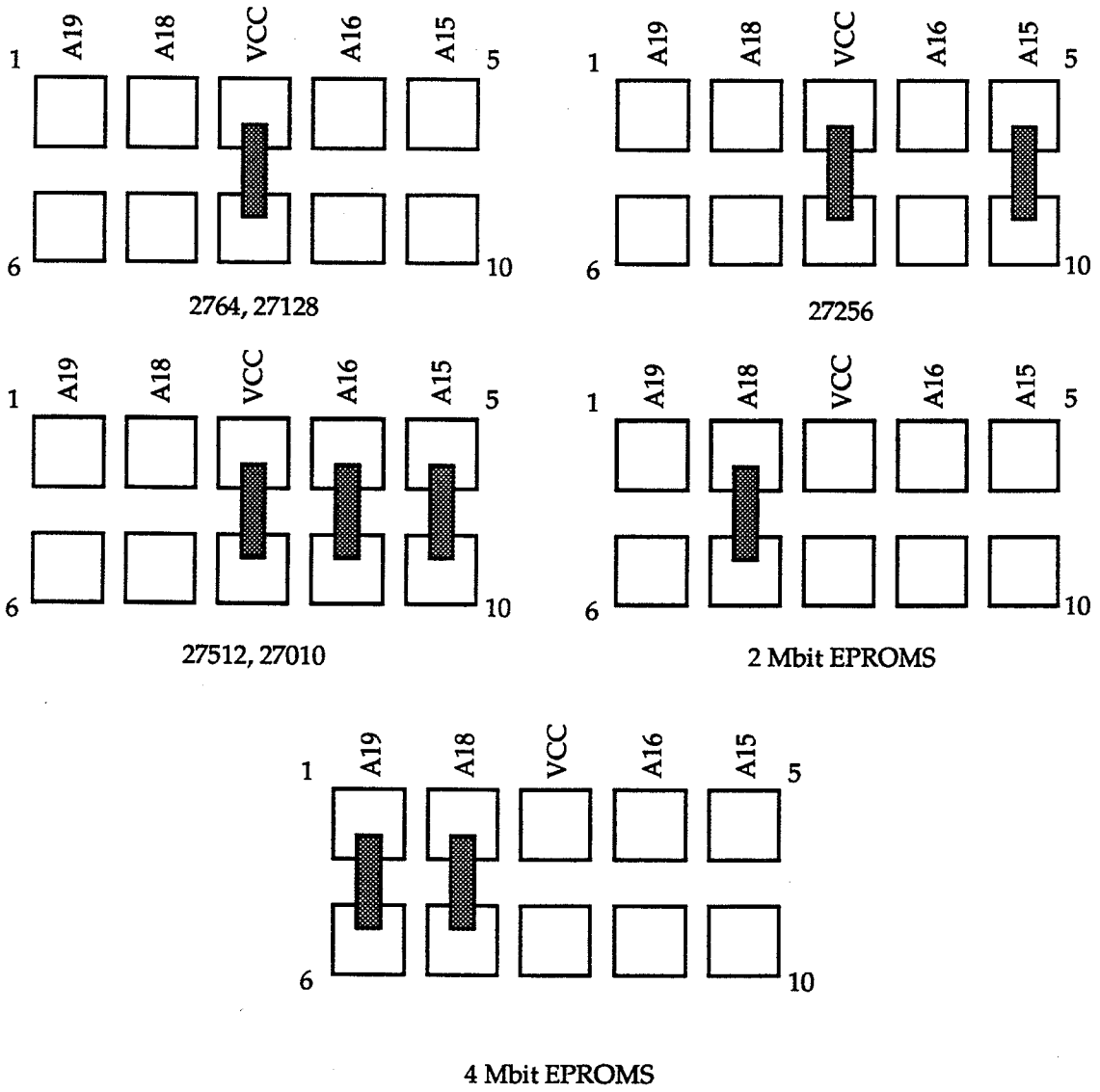


Figure 1-3. K1: EPROM Size Selection

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1.3.3 K3 - 1MB/4MB VME Slave Address Range

This jumper determines the VME slave address range to be one or four MB. If the jumper is installed, the board is set to a 4MB VME slave address range. Without the jumper, the board is set to a 1MB VME slave address range. The VME slave address can still be set on any 1MB address through the ADDRESS SELECT register.

With the MZ 7130, selection of a 1MB range causes VME slave accesses to appear in the address range of $700000 - $7FFFFF, as seen by its processor. Selection of a 4MB range causes VME slave accesses to appear in the address range of $400000 - $7FFFFF, as seen by the processor.

With the MZ 7132, A32 is on a 16 MB boundary. Jumper K3 must be installed for proper operation of the MZ 7132.

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	K3	K4	MISCREG Bit 0 = DPA
MZ 7132:			
A32 (16 MB)	In	Out	0
A32 (16 MB)/A24 (4 MB)	In	Out	1
MZ 7130:			
A32 (4 MB)	In	In	0
A32 (4 MB)	Out	In	0
A32/A24 (4 MB)	In	In	1
A32/A24 (1 MB)	Out	In	1

Table 1-2. DRAM Configuration.

1.3.4 K4 - 4 MB/16 MB DRAM Selection

This jumper distinguishes the board as a MZ 7130 or as a MZ 7132. If the jumper is installed, the board has 4 MB of memory and is a MZ 7130. Without the jumper, the board has 16 MB of memory and is a MZ 7132.

1.3.5 K5 - Daughter Card Clock Selection (Artwork AX4 or Beyond Only)

Jumper block K5 provides three different daughter card clocks as follows:

- 16 MHz Clock independent of CPU clock (factory setting)
- "Sync" CPU Clock (16, 20, or 25 MHz - dependent on CPU clock)
- "Async" CPU Clock (16, 20, or 25 MHz - dependent on CPU clock)

The standard daughter card clock is 16 MHz. Other K5 settings are available for daughter card modules that require a different clock. See the daughter card manual for details. Figure 1-4 shows the three possible jumper settings. No jumper is required if a daughter card is not installed.

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1.3.6 K6 - EPROM Access Time Selection

Jumper block K6 allows you to configure the MZ 7130 / MZ 7132 to operate from EPROMs with 0 to 6 wait states depending on the EPROM's access speed. The following table summarizes the maximum access speeds allowed for the number of wait states selected:

Wait States:	16 MHz	20 MHz	25 MHz
0	115 nsec	95 nsec	75 nsec
1	175	145	115
2	235	195	155
3	295	245	195
4	355	295	235
5		345	275
6		315	

Note that if the DS1216F SmartWatch is used, at least 235 nsec access time must be provided regardless of what speed EPROMs are used. At 16 MHz, two wait states are required and at 25 MHz, four wait states are required.

Figure 1-6 summarizes the operation of K6. A jumper is placed across the pin pair for the desired number of wait states. If no pin pair is jumpered, zero wait states is assumed.

NOTE

Only one set of pins should be jumpered.

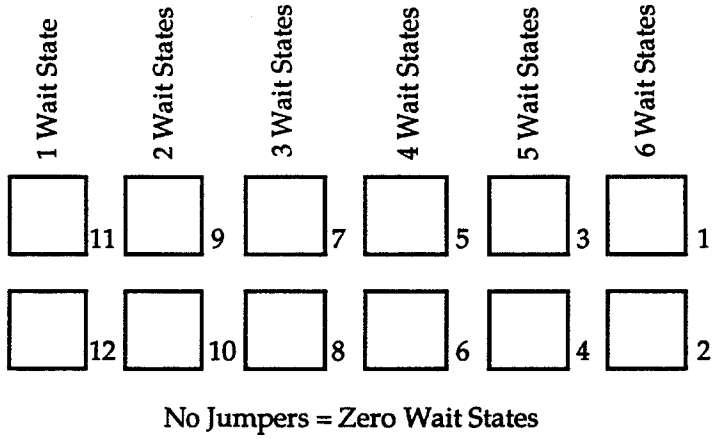


Figure 1-6. K6: EPROM Access Speed

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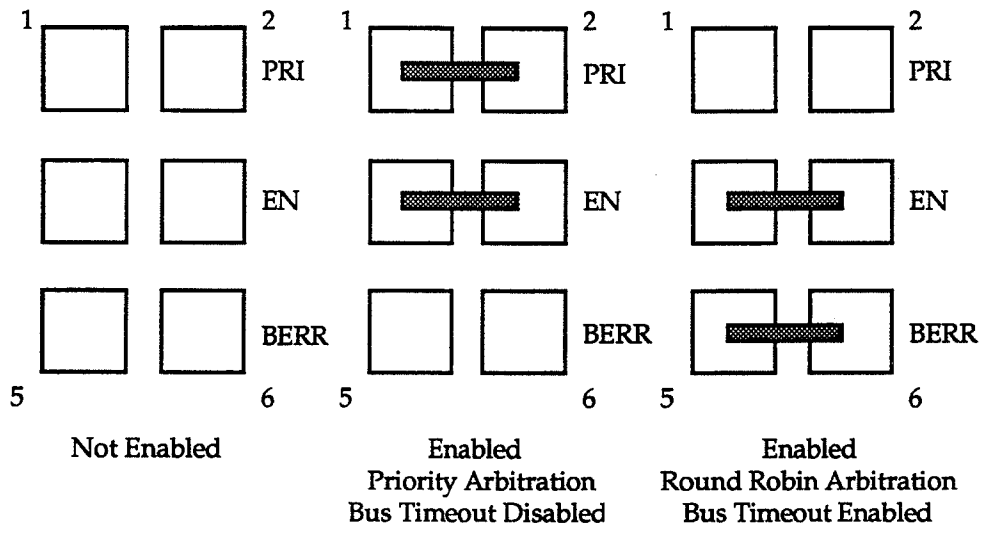


Figure 1-7. K7: System Controller Configuration.

1.4 Installing the Boards

Check the MZ 7130 / MZ 7132 against your shipping list and purchase order to make sure you have received a board with the options you requested. When unpacking, inspect each item for obvious damage. Report any damage to the carrier used to ship the unit.

CAUTION !

Do not apply power to any board that appears to be damaged. Additional damage could result, both to the defective board and to other boards in your VMEbus system.

Carefully check the VMEbus card slot into which you intend to install the MZ 7130 / MZ 7132. The MZ 7130 / MZ 7132 are designed to be used in a double-high P1 and P2 VMEbus backplane. If the MZ 7130 / MZ 7132 is the VMEbus system controller, it must be installed in Slot One. Make sure that the BGIN/BGOUT and the IACKIN/IACKOUT jumpers on the backplane have been removed from the slot being used. Verify that all onboard jumpers are correctly placed for your application. Also verify the serial port DB25 connector cables are correct for your terminal type.

Before inserting the MZ 7130 / MZ 7132 into the VMEbus backplane, make sure that the power supply is turned off. Also, check all power pins on the backplane using a DC voltmeter. All voltages from the +5 VDC power supply must measure between 4.75 VDC and 5.25 VDC on the VMEbus backplane. Refer to Section 3 for the location of the VMEbus P1 and P2 connector +5 VDC power pins.

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SECTION 2
Programmer's Guide

2.0 Overview

This section contains information for installing the MZ 7130 / MZ 7132 CPU card into a VMEbus system and configuring the jumper blocks to your particular requirements. The installation is an integral part of the initial system configuration, reconfiguration or expansion. Care should be taken when installing any board into a VMEbus system.

The section is organized in the following manner:

2.1 MZ 7130 / MZ 7132 Address Maps
2.2 Initializing the MZ 7130 / MZ 7132
2.3 Using the SCN68681 DUART Serial Port Chip
2.4 Using the Am9513 System Timing Controller
2.5 Using the SmartWatch Time-of-Day Clock
2.6 Configuring the Registers
2.7 Interrupts

2.1 MZ 7130 / MZ 7132 Address Maps

The MC68030 or MC68EC030 CPUs can address up to four Gbytes of memory space. Tables 2-1 and 2-2 show how the local addressing range has been divided for the MZ 7130 and MZ 7132, respectively.

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$00000000	–	$000FFFFF	(16)	EPROM, SmartWatch
$00180000	–	$001800FF	(8)	68681 DUART
		$00180103		SCSI Address
		$00180107		SCSI Data
		$00180200	(32)	Address Select Register (ADDRSEL)
		$00180300	(32)	Misc. Configuration Register (MISCREG)
		$00180400	(32)	Status Register (STATUS)
		$00180502	(16)	9513 Data Register (16-Bit Port)
		$00180506	(16)	9513 Control Register (16-Bit Port)
		$00180603	(8)	Interrupt Vector Latch
		$00180703	(8)	Momentary Pulse Switch (MONSWT)
		$00180A00		VMEbus Interrupt Generator register
		$00180B00		SCSI Reset Generator
$00200000	–	$003FFFFF		Reserved (BERR)
$00400000	–	$013FFFFF		Dual-Ported DRAM
$01400000	–	$xxFFFFFF		If DCSEL, then Daughter Card Access, Otherwise, VMEbus Access A24/A32/D32 (xx is set by the ADDRSEL register)
$02000000	–	$FEFFFFFF		VMEbus access A24/A32/D32
$FF000000	–	$FFFEFFFF		VMEbus access A24/D16
$FFFF0000	–	$FFFFFFFF		VMEbus access A16/D16

Table 2-2. MZ 7132 Local Address Map.

The daughter card is selected between 0080 0000 (MZ 7130) or $0140 0000 (MZ 7132) and the upper P2 address programmed in the ADDRSEL register when D30 of the MISCREG register is set to zero.

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Programming the 68681 for normal operation consists of three phases: initialization, transmitting and receiving. A brief discussion of these phases and a programming example is presented. Note that on the MZ 7130, the 68681 DUARTs recovery time of one microsecond between accesses is taken care of in hardware and no software delay loop is required between consecutive accesses.

Table 2 shows the 8-pin RJ45 connector pinout. Serial port A has the required handshaking signals for full modem control. In addition to the TXD, RXD, RTS and CTS signals provided on port B, port A has the additional signals DTR, DCD and DSR required for full modem control. Port B provides +12V pins for user custom cabling requirements.

Port A			Port B	
CPU Board	**Signal**	**Pin**	**CPU Board**	**Signal**
Supplies	DTR	1	Supplies	+12V
Receives	CTS	2	Receives	CTS
Receives	RXD	3	Receives	RXD
	GND	4		GND
Receives	DCD	5		GND
Supplies	TXD	6	Supplies	TXD
Supplies	RTS	7	Supplies	RTS
Receives	DSR	8	Supplies	+12V

Table 2-3. RJ-45 Connector Pinout.

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2.3.1 Initializing the SCN68681 DUART

The 68681 DUART base address is $180000 in the local address space. The 68681 is a byte wide device and requires data to be transferred on the lower byte, D0 - D7. The first byte register location corresponds to local address $180003. Table 2-4 shows the 68681 register addresses. Note that read accesses and write accesses to the same address often access different registers

ADDRESS	READ ACCESSES	WRITE ACCESSES
$180003	Mode Register A (MR1A,MR2A)	Mode Register A (MR1A, MR2A)
$180007	Status Register A (SRA)	Clock-Select Register A (CSRA)
$18000B	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
$180013	Input Port Change Reg. (IPCR)	Aux. Control Register (ACR)
$180017	Interrupt Status Reg. (ISR)	Interrupt Mask Register (IMR)
$18001B	Counter/Timer High Reg. (CTR)	Counter/Timer Upper Reg. (CTUR)
$18001F	Counter/Timer Low Reg. (CTL)	Counter/Timer Lower Reg. (CTLR)
$180023	Mode Register B (MR1B,MR2B)	Mode Register B (MR1B, MR2B)
$180027	Status Register B (SRB)	Clock-Select Register B (CSRB)
$18002B	*Reserved*	Command Register B (CRB)
$18002F	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
$180033	Interrupt-Vector Register	(IVR)Interrupt-Vector Reg. (IVR)
$180037	Input Port	Output Port Conf. Reg. (OPCR)
$18003B	Start-Counter Command	Set Output Port Bits Command
$18003F	Stop-Counter Command	Reset Output Port Bits Command

Table 2-4. 68681 DUART Register Addresses.

To initialize the 68681 DUART for polled mode operation, Mode Registers (MR1A,MR2A), Clock Select Register (CSRA), Command Register (CRA), Interrupt Mask Register (IMR), and Output Port Bits Command Register must be properly initialized. These registers configure the serial port for data length, parity, baud rate, and they mask interrupts, de-assert RTS, CTS, DTR, and DSR, and enable port 0.

For example, to configure port 0 for 8 bits, no parity, one stop bit, 9600 baud, and disabled RTS, CTS, DTR, and DCD, the following control codes should be written:

Step	Activity
1	$13 into MR1A - Sets 8 bits, no parity.
2	$7 into MR2A - Sets 1 stop bit.
3	$BB into CSRA - Sets baud rate for both xmit and receive to 9600 baud.
4	$5 into CRA - Enables transmitter and receiver
5	$0 into IMR - clear interrupt masks register.

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2.3.4 RS-232 Interface Specifications

The MZ 7130 / MZ 7132 RS232 interface circuits have been designed to meet EIA standard specifications. All RS-232 signals generated by the MZ 7130 / MZ 7132 are approximately 10 volts when measured across a 3K load. The RS-232 receiving circuits accept signals in the 3 to 25 volt range. The input impedances of all MZ 7130 / MZ 7132 RS-232 circuits accept signals with DC resistances of 4.7K. Consult the EIA RS-232 specifications for more detailed information. The negative threshold voltage is less than -3 volts with respect to signal ground. The positive threshold voltages is greater than +3 volts with respect to signal ground.

RS-232 Signal States	Negative	Positive
Binary State	One	Zero
Signal Condition	Mark	Space
Control and Timing Functions	Off	On

Table 2-5. RS-232 Signals.

2.4 Using the Am9513 System Timing Controller

The onboard Am9513 system timing controller provides five general purpose 16-bit timer/counters. Each can provide a separate autovectored interrupt request to the 68030 CPU on their assigned interrupt level. Refer to Section 2.7 for information about interrupts.

Each counter/timer can be programmed to count up or down in either binary or BCD. Any of the counters can be internally concatenated to form an effective counter length up to 80 bits. Counters 1 and 2 have additional alarm and compare registers. The counters use a 3.6864 MHz oscillator as their input frequency which results in a 271 nS 'X1' clock period.

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For example, to initialize counter 5 to generate an autovectored interrupt every 0.5 second, the following steps can be taken:

Step	Activity
1	$FFFF into command register - Reset 9513
2	$FF5F into command register - Issue load all counters command.
3	$FFEF into command register - Enable 16-bit data transfers.
4	$FF05 into command register - Point to counter 5 mode register.
5	$1E61 into data port counter 5 mode reg. - Set counter 5 to mode J - no gate, count on falling edge, prescale: osc/4096, no special gate, reload from load or hold, repetitive BCD count, counting down, active high terminal pulse.
6	$0450 into data port counter 5 load reg. - Set counter 5 to 0.5 second count.
7	$0450 into data counter 5 load reg. - Initialize counter 5 hold reg.
8	$0050 into command register - Load counter 5.
9	$0030 into command register - Arm counter 5.

NOTE

Counter 5 output is an active high terminal pulse. All counter/timer outputs must be set for active high terminal pulse to work correctly with the MZ 7130 / MZ 7132 interrupt hardware. The 0.5 second count is derived from 450 count x 271 nS 'X1' osc period x 4096 prescale value equals approximately 0.5 seconds.

2.4.2 Counter/Timers 1-5 Interrupt Operation

Each counter/timer is associated with the following interrupt level:

Timer/Counter	Interrupt/Level
1	1
2	2
3	4
4	6
5	7

These interrupts are latched when they occur and are removed during their interrupt acknowledge cycle by writing to the appropriate bit in the MONSWT register. Note that timers 2, 3, 4 and 5 share their levels with other interrupt sources. In the case where multiple interrupts occur on the same level, the STATUS register must be polled to determine the correct source of the pending interrupt.

CAUTION!

Load operations can cause glitches on the outputs of the Am9513 which can in turn cause the interrupt flip flops to be set when no interrupt is intended.

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2.6.1 Address Select Register - ADDRSEL (R/W)

The ADDRSEL control register is used to house the user-defined base address for three functions: the VMEbus dual-ported DRAM access address, the upper address boundary for daughter card accesses, and the mailbox interrupt base address. For the MZ 7130, the VMEbus dual-ported DRAM address is configurable on any 1 Mbyte boundary in either the standard or extended address space of the VMEbus. The MZ 7132 is configured on a 16 Mbyte boundary in the extended address space and on a 1 Mbyte boundary in the standard address space. The mailbox interrupt address is configurable on any 256 byte boundary in short I/O space. Refer to Section 2.2 for further information.

Base Address: $180200 - Longword Access Only.

31 – 20	DRAM VMEbus Address
19 – 16	Reserved
15 – 8	P2 Upper Address
7 – 0	Mailbox IRQ

ADDRSEL Bit Position Description:

D31-D20: DRAM VMEbus ADDRESS. These bits set the base address for VMEbus access to the dual-ported RAM. These bits are active high and set the upper 12 bits (VMEbus A31 - VMEbus A20) that must be present on the bus in order to access the dual-ported RAM. Note that the VMEbus base address is configurable on a 1 Mbyte boundary.

D19-D17 Not used, reserved for future use.

D16 On the MZ 7132, this bit must be programmed to zero. This bit is not active on the MZ 7130.

D15-D8: DAUGHTER CARD UPPER ADDRESS. These bits set the upper address that selects the daughter card. These bits are active high and correspond to the CPUs A31-A24 address lines. If this field is set to $01 and the daughter card is enabled, the daughter card is selected for the range of $00800000 - $01FFFFFF (MZ 7130) or $01400000 - $01FFFFFF (MZ 7132). Access to some of the A24/A32 address space is blocked.

D7-D0: MAILBOX INTERRUPT. These bits set the base address for the VMEbus address that causes a mailbox interrupt to be generated onboard the MZ 7130. These bits correspond to VMEbus address lines A15-A8 and are active when addressed in the short I/O space. Note that the mailbox interrupt base address is configurable in the VMEbus short I/O space on a 256 byte boundary.

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MISCREG Bit Position Descriptions:

D31: Extended space select. When this bit is programmed low, accesses to the mixed portion of the address map select the A32, extended address space, for VMEbus accesses. When this bit is programmed high, A24 VMEbus accesses are selected.

D30: Daughter card select. When this bit is programmed low, accesses to the mixed portion of the address map select the daughter card connector for addresses between the daughtercard start address and the upper address specified in the ADDRSEL Register. Note that the start address is different for the MZ 7130 and MZ 7132.

D29: RAM Cache disable. Programming this bit low disables the MZ 7130 / MZ 7132 onboard 16K RAM Cache. When enabled, all accesses to DRAM from onboard are cached in the MZ 7130s onboard RAM cache. Slave accesses from the VMEbus to onboard DRAM are not cached. Write slave accesses invalidate the RAM Cache.

D28: SYSFAIL generator. Programming this bit low asserts the VMEbus SYSFAIL signal. Note that on power up, SYSFAIL is automatically set low and must be turned off by programming this bit high.

D27: 68030 MMU disable. When this bit is programmed low, the 68030s MMU is disabled. Please note that 68EC030s do not have a MMU.

D26: 68030 Cache disable. When this bit is programmed low, the 68030s data and instruction caches are disabled. This is a hardware override disabling function and takes precedence over the enabling bits in the 68030s CACR register. This bit must be set to a 1 for the bits in the 68030s cache control register (CACR) to have any effect.

D25: LED2. Programming this bit low turns on front panel LED2. Programming this bit high turns off this LED.

D24: LED1. Programming this bit low turns on front panel LED1. Programming this bit high, turns off this LED.

D23: Parity enable. When this bit is low, DRAM parity error checking is enabled. BERR is generated when a parity error occurs on accesses to RAM from either the MC68030 (local BERR) or the VMEbus (VMEbus BERR).

D22: ACFAIL Interrupt Enable. AX4 artwork or beyond only. When this bit is low, ACFAIL from the VMEbus asserted low causes a nonmaskable interrupt. When this bit is high, ACFAIL interrupts from the VMEbus are disabled. On Board Artwork Revision Ax3 or before, D22 is reserved.

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D8: BCLR interrupt enable. This bit is active low to enable BCLR as a level 6 autovectored interrupt source. Set bit to 0 to enable.

D7-D1: VMEbus IRQ Enable. These bits enable the VMEbus interrupt levels to which the MZ 7130 / MZ 7132 respond. These bits are active low. Set bit to 1 to disable interrupt. Set bit 0 to enable interrupt.

D0: Dual-port A32 or A24/A34 addressing selection. This bit allows the user to configure the address decoder for the VME base address for the dual-ported RAM to respond to VMEbus access in either A24 and A32 address space, or for A32 address space only. If this bit is high, both A24 and A32 address modifier codes are enabled. If low, only the A32 address modifier codes are enabled.

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STATUS Bit Position Description:

BERR Determination:

D19-D16 CPU Identification. These four bits read the state of the K2 jumper block configuration. D19 corresponds to K2 jumper 1-2. With the jumper installed, D19=0, with no jumper, D19=1.

D15: Onboard bus time-out. This bit is set low if any local access (i.e, address between $0 and $7F FFFF) is not terminated within eight µseconds.

D14: VMEbus BERR. This bit is set low if a VMEbus BERR occurred during access to the VMEbus.

D13: CPU breakpoint cycle. This bit is set low if BERR is generated due to execution of the 68030s breakpoint cycle. Even though execution of a breakpoint cycle results in the MZ 7130 / MZ 7132 responding with a BERR, latching this signal low in the BERR register, the actual exception processing by the 68030 is with the illegal instruction vector. This bit then would be read by an illegal instruction routine, not a BERR routine.

D12: DRAM parity error. This bit is low if a DRAM cycle was in progress at the time of the BERR indicating that a parity error occurred.

D11: Daughter Board BERR. As described above for D10, this bit is used to decide if a BERR that occurred during a daughter card access cycle was the result of an actual daughter card BERR , or that a daughter card wasn't plugged in. If this bit is low, a daughter card BERR has occurred.

D10: Daughter Board Select. If this bit is low, then a daughter card cycle was in progress at the time of the BERR. There are only two ways for a daughter card access to result in a BERR. Either there was no daughter card plugged into the daughter card connector or a BERR occurred during a daughter card access. To decide which type of BERR occurred, D11, the daughter card BERR must also be looked at. If D10 is low, and D11 is high, then the BERR occurred because there wasn't a daughter card plugged in.

Misc. Status bits:

D9: Open, Always = 1

D8: 16 or 4 MB (MZ 7132 = 1, MZ 7130 = 0)

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2.6.4 VMEbus Interrupt Vector Latch - IRQVECT (Write Only)

This register holds the interrupt vector that the MZ 7130 / MZ 7132 drives onto the VMEbus during a software initiated VMEbus interrupt generator cycle.

Base Address: $180603 - Byte Access Only

7	Vector D7
6	Vector D6
5	Vector D5
4	Vector D4
3	Vector D3
2	Vector D2
1	Vector D1
0	Vector D0

IRQVECT Bit Description:

D0-D7: These bits hold the interrupt vector driven to the bus during a VMEbus interrupt generator cycle. If a move.b is used to write the single byte to this register, the address is $180603.

2.6.5 Momentary Pulse Switches - MONSWT (Write Only)

This register is used to pulse various soft switches onboard the MZ 7130 / MZ 7132. These soft switches are mainly used to acknowledge (reset) various onboard interrupt sources, such as the timer interrupts and the mailbox interrupt. In addition, a soft switch to release the VMEbus (programmed release) and to reset the VMEbus GR flag (used in the status register above), is also included. Writing a 1 to the desired bit temporarily engages the soft switch. It is not required to write it back to zero.

Base Address: $180703 - Byte Access Only

7	Programmed Release Clear
6	VME Access to DRAM, Flag Clear
5	Mailbox Interrupt Acknowledge
4	Level 7 Interrupt Acknowledge
3	Timer 4 Acknowledge
2	Timer 3 Acknowledge
1	Timer 2 Acknowledge
0	Timer 1 Acknowledge

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NOTE

For a given VMEbus interrupt level, one and only one VMEbus master must be allowed to respond to it.

For example, if two MZ 7130 / MZ 7132 cards resided on the VMEbus backplane, only one of the cards can be configured to respond to VMEbus IRQ3.

All onboard interrupt sources are treated as autovectored interrupts. For an autovectored interrupt, the level of the interrupt itself tells the 68030 where to find the interrupt service routine. Refer to the 68030 user's manual for a complete description of the 68030s exception table vectors.

Since the MZ 7130 / MZ 7132 allows 14 unique interrupt sources, the seven allowable autovectors must be doubled up. The autovector interrupt map for the MZ 7130 / MZ 7132 is seen on the following table:

Level	Interrupt Source
1	Timer 1
2	Timer 2, Mailbox
3	SCSI IRQSCSI RST
4	Timer 3, Daughter Board
5	Serial Port
6	Timer 4, Bus Clear
7	SYSFAIL, ACFAIL, Timer 5, ABORT

Table 2-8. MZ 7130 / MZ 7132 Autovectored Interrupt Map.

To resolve conflicts when more than one interrupt source is used for a given level, the STATUS register must be read to decide which interrupt source is pending. With the exception of the level 7 non-maskable interrupts, which are user prioritized, a priority scheme of TIRQ2, TIRQ3, SCSIIRQ, and TIRQ4 for levels 2, 3, 4 and 6 respectively has been hardwired into the MZ 7130.

2.7.2 Non-maskable Autovectored Interrupts

There are four possible sources of Level 7 nonmaskable interrupts: System FAIL, ACFAIL, Timer 5 and ABORT.

AX3 Revision Artwork and Before Only

The ACFAIL interrupt is always enabled. Any time the ACFAIL line is asserted, a level 7 nonmaskable interrupt occurs.

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2.7.6 Mailbox Autovectored Interrupt

The mailbox autovectored interrupt allows any VMEbus master to interrupt the MZ 7130 / MZ 7132CPU by performing a writing operation to the mailbox's VMEbus address location. The write can be byte, word, or longword. The VMEbus address is selected on any 256-byte boundary in the VMEbus short A16 address space by properly programming the ADDRSEL register. This request is latched until the interrupt is acknowledged by writing a 1 to bit D5 of the MONSWT register.

2.7.7 VMEbus Interrupt Generator

The MZ 7130 / MZ 7132 can be programmed to generate an interrupt to another VMEbus master by using its VMEbus interrupt generator. Note that this is the exact reverse of the mailbox interrupt. The mailbox interrupt allows another VMEbus master to interrupt the MZ 7130 / MZ 7132 using the MZ 7130s mailbox address, whereas the VMEbus interrupter is used to allow the MZ 7130 / MZ 7132 to interrupt another VMEbus master: for example, one that does not have a mailbox interrupt.

To use the VMEbus interrupter, the interrupt vector is first written to the IRQVECT register. The interrupt request itself is generated by writing to location $180A00. This interrupt request is latched low by the MZ 7130s hardware until it has been acknowledged. At this time the request is released and the vector is driven onto the bus.

The interrupt level that the VMEbus interrupt request will occur on is programmed by setting bits D12-D14 of the MISCREG register to the desired level.

2.7.8 SCSI RESET Operation

The MZ 7130 / MZ 7132 SCSI circuit allows for both the hard and soft modes of reset to be used. The reset mode is selected by programming bit D11 of the MISCREG register. When operating in the hard reset mode, any reset generated on the SCSI bus drives the Master Reset signal to the WD33C93A initializing it to its power on state. The WD33C93A must be reinitialized before it can be used again. Any command in progress is immediately cleared.

In the soft reset mode, the WD33C93A does not get reset, and all registers are kept intact. In soft reset mode, detection of a SCSI reset is handled in software by utilizing a SCSI reset as an interrupt source. To enable the SCSI reset as an interrupt source, bit D10 of the MISCREG register must be programmed low. Refer to the SCSI specification for a complete description of hard and soft reset modes on the SCSI bus.

The MZ 7130 / MZ 7132 generate a reset to the SCSI bus either in response to the local onboard RESET switch being depressed, or a SYSRESET occurring on the VMEbus, or if a SCSI reset is programmed. To program the SCSI bus to reset, address location $180B00 must be accessed.

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SECTION 3
Hardware Reference Guide

3.0 Overview

This section provides a functional description of the MZ 7130 / MZ 7132 including general information about the MC68030 CPU chip set, memory, serial ports, system timing controller, control and status register functions, VMEbus interface, daughterboards, and switch and LED definitions. A block diagram of the MZ 7130 / MZ 7132 is shown in Figure 3-1.

The section is organized in the following manner:

3.1 Processors and Coprocessors
3.2 Clocks
3.3 Memory Devices
3.4 Serial Ports
3.5 SCSI Interface
3.6 System Timing Controller
3.7 Registers
3.8 VMEbus Interface
3.9 Daughter Card Connectors
3.10 MZ 7130 / MZ 7132 Specifications
3.11 Schematics

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include an on-chip memory management unit and synchronous two clock cycle operation. Refer to Section 1.2 for additional information.

The MC68EC030 is also available on the MZ 7130 / MZ 7132. The primary difference between the two processors is that the MC68EC030 does not include an on-chip memory management unit.

NOTE

The MZ 7130 / MZ 7132 does not support cache burst fill mode and functions the same regardless of the setting of the cache burst fill mode bit in the cache control register.

The MC68030 performs all functions required in a 32-bit microprocessing system, including system address generation, control, memory access and processing functions. The CPU has separate 32-bit address and data buses along with local bus arbitration signals. Data can be read or written over the 32-bit bus in longword (32 bits), word (16 bits) and byte (8 bits) lengths. The MC68030 interfaces to coprocessors via a coprocessor interface.

The MC68030 CPU also features sixteen 32-bit general purpose registers, two 32-bit supervisor stack pointers, 10 special purpose control registers, pipelined instruction architecture, dynamic bus sizing with unaligned transfers, four Gbytes addressing range, and seven interrupt levels.

3.1.2 On-Chip Memory Management Unit (MMU)

The on-chip memory management unit provides logical to physical address translation, memory organization, control, and access protection for the MC68030. The MMU is not present on the MC68EC030 processor. The MMU supports virtual memory operation systems by mapping virtual memory addresses to physical memory addresses in demand paged memory systems. This allows up to four Gbytes of virtual memory to appear available to each user's program. The MMU also provides protection of supervisor areas from accesses by user programs and allows write protection on a page basis. The MMU's 22 entry on-chip address translation cache (ATC) is a fully associative cache memory that stores recently used page descriptors. The memory management registers are accessed via the CPU address space. Refer to Section 1.2 for further information.

3.1.3 Floating Point Unit (FPU)

The optional MC68882 floating point unit is a 32-bit device that provides floating point capability for the CPU and is fully compatible with the ANSI/IEEE standard 754-1985 for binary floating point arithmetic. It provides single (32-bit), double (64-bit), and double-extended (80-bit) precision. The operand, result, status, and command information transfers take place over a 32-bit local bidirectional data bus. All FPU accesses must be in the coprocessor mode; peripheral mode accesses are not supported. In the coprocessor mode, the addition of the FPU appears to the programmer as an extension of the register set and instruction set of the CPU.

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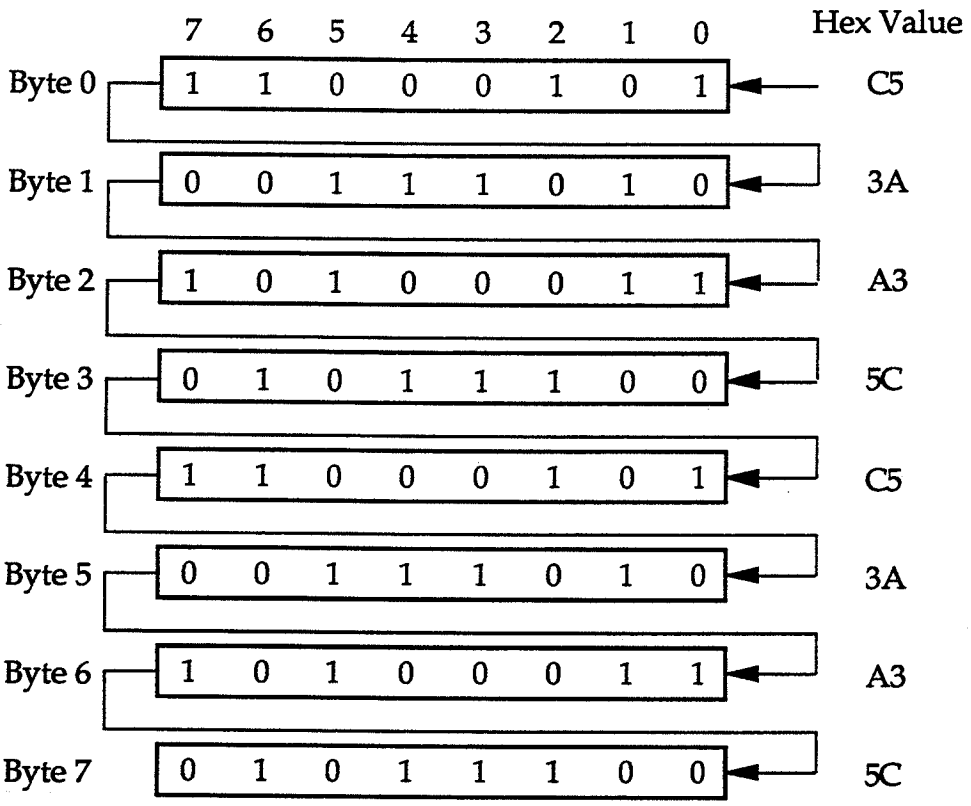


Figure 3-2. Smartwatch Access Cycles.

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3.3 Memory Devices

3.3.1 Dual-Ported DRAM

The MZ 7130 contains four MBytes and the MZ 7132 contains sixteen MBytes of dual-ported dynamic RAM supported with a 16 Kbyte cache that performs zero wait state local CPU read accesses for cache hit cycles. MZ 7130 DRAM is accessed from the local address bus at $400000 to $7FFFFF, and from the VMEbus at the VMEbus address programmed in the control register ADDRSEL. MZ 7132 DRAM is accessed from the local address bus at $400000 to $13fffff. Control register MISCREG bit 0 selects the DRAM to reside in the VMEbus A32 space or A32 and A24 address space for VMEbus accesses. Refer to Section 1.2 for further information.

The DRAM parity circuit generates a parity bit during memory write cycles which is saved in the DRAM. When a memory location is read, the parity circuit again generates a parity bit which is compared with the saved parity bit. If they don't match, a parity error occurs. If parity checking is enabled in the MISCREG register, a BERR exception occurs for local accesses, and a VMEbus BERR signal for VMEbus accesses.

NOTE:

When operating with either parity checking or RAM cache enabled, the DRAM must be initialized before reading.

Before using the RAM cache a 16K area of DRAM must be initialized to fill the TAGRAM with valid entries. As long as DRAM is always written to before reading, explicit initialization is not required. The reason that initialization (explicit or implicit) is required is that the TAGRAM chips used to house the cached addresses are set to zero upon reset which is the zero DRAM page. Any reads from DRAM addressed from $400000 to $404000 is treated as a cache hit until the TAGRAM is initialized.

WARNING:

Access by the local processor of DRAM at the VMEbus address specified in the ADDSEL register can give indeterminate results and should be avoided.

3.3.2 EPROM

The MZ 7130 / MZ 7132 supports up to 1 Mbyte of EPROM space starting at base address $0000 with two 32-pin byte wide sockets. These sockets allow use of standard Jedec pinout EPROMs 2764, 27128, 27256, 27512, 27010 and future 2Mbit and 4Mbit devices. The EPROM sockets are denoted by U11 which is the high byte, and U12 which is the low byte.

WARNING:

Pin 1 of a 28-pin EPROM should be installed into pin 3 of the 32 pin socket. Otherwise, damage can result to the EPROMs or board.

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3.4 Serial Ports

Two independent full-duplex asynchronous RS-232 serial ports are provided by the 68681 Dual Asynchronous Receiver/Transmitter (DUART). These serial ports are brought out of the front panel via two 8-pin RJ45 modular jacks. The 3.6864 MHz crystal used by the 68681 allows the use of 18 standard asynchronous baud rates from 50 baud to 38.4 K baud. The 68681 also has an internal 16-bit programmable timer that can generate custom baud rates.

The 68681 also features: independently programmed receiver and transmitter baud rates; data format: 5 to 8 data bits; odd parity, even parity, no parity, or forced parity; 1, 1.5, or 2 stop bits programmable in 1/16-bit increments; and parity, framing, and overrun error detection.

The 68681 is configured on the MZ 7130 / MZ 7132 to generate a level 5 autovectored interrupt via its normal internal interrupt registers. This interrupt can be used to generate interrupts on receive character, transmit character, or with the internal 16-bit counter/timer.

Consult Section 2.3, "Using the SCN68681 DUART Serial Port Chip," for more information.

3.5 System Timing Controller

The onboard Am9513 provides five general purpose 16-bit timer/counters, each of which can provide a separate local autovectored interrupt request.

Each counter/timer can be programmed to count up or down in either binary or BCD. Any of the counters can be internally concatenated to form an effective counter length up to 80 bits. Counters 1 and 2 have additional alarm/comparator registers. The base address of the timing controller is local address $180802 for the data register and $180806 for the command register. The counters use a 3.6864 MHz oscillator as their input frequency which results in a 271 nS 'X1' clock period.

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The MONSWT register is used to pulse various soft-switches onboard the MZ 7130. These soft-switches are mainly used to acknowledge (reset) various onboard interrupt sources, such as the timer interrupts and the mailbox interrupt. In addition, a soft-switch to release the VMEbus (programmed release) and to reset the VMEbus GR flag (used in the status register above) is also included.

The IRQVECT register is used to hold the interrupt vector driven to the VMEbus during a generated VMEbus interrupt cycle. This register is a write only register used to write the desired interrupt vector. During the actual interrupt cycle the contents of this register is driven onto the bus.

For a more complete detailed description of these five user registers, refer to Section 2.6.

3.8 VMEbus Interface

The MZ 7130 / MZ 7132 provides a full 32-bit master and slave VMEbus interface. As a VMEbus master, the MZ 7130 / MZ 7132 can generate 16-, 24- and 32- bit addresses and byte, word, and longword data sizes. The MZ 7130s DRAM memory accepts 24- and 32-bit addresses with byte, word and longword data sizes.

The MZ 7130 / MZ 7132 meets the VMEbus specification IEEE-1014 including, address pipelining (slave only), read-modify-write cycles, address only cycles, and a full VMEbus system controller with an IACK driver. The MZ 7130 / MZ 7132 has A32/D32 capabilities.

The MZ 1000 gate array system controller provides all necessary VMEbus system controller functions including four level bus arbitration, 16 MHz system clock, and VMEbus time-out signals.

3.8.1 VMEbus Address Modifier Codes

An address modifier code is asserted with each VMEbus address broadcast. It specifies which VMEbus address space, Short (A16), Standard (A24), or Extended (A32), is selected.

When the MZ 7130s DRAM is being accessed by another VMEbus master, the address modifier code is checked according to control register MISCREG bit 0. When bit 0 is set (logical 1), the MZ 7130 / MZ 7132 DRAM checks for a Standard (A24) address modifier code and an Extended (A32) VMEbus address modifier code. When bit 0 is cleared (logical 0), the MZ 7130 / MZ 7132 DRAM checks for an Extended (A32) VMEbus address modifier code only. If the VMEbus address modifier code does not match the modifier denoted by MISCREG bit 0, the MZ 7130 / MZ 7132 DRAM cannot be accessed and a VMEbus error can result.

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3.8.5 VMEbus Requester

The MZ 7130 / MZ 7132 requests to become the VMEbus master when the local CPU bus asserts a VMEbus address. The MZ 7130 / MZ 7132 bus requester circuit then asserts a VMEbus request on the level determined by bits 16-19 of MISCREG. The VMEbus system controller upon receiving the bus request, asserts a bus grant signal after the current bus master relinquishes the bus. When the MZ 7130 / MZ 7132 receives the bus grant signal on the same level as that configured in MISCREG, the MZ 7130 / MZ 7132 acknowledges bus mastership by asserting the VMEbus busy signal, BBSY. The MZ 7130 / MZ 7132 then performs at least one VMEbus cycle.

There are three ways the MZ 7130 / MZ 7132 can be configured to release the VMEbus: Release On Request (ROR) by another VMEbus master, Release When Done (RWD) with current AS* cycle, or Release on Programmed Release (PREL). Bits 20 and 21 in the MISCREG are used to select the desired release mode. If either bit 20 OR bit 21 is set, then the release mode is RWD or ROR, respectively. Otherwise, if neither of these bits are set, the release mode is PREL.

Release On Request (ROR) is the most commonly used and generally most efficient bus release mechanism. The MZ 7130 / MZ 7132 retains bus mastership until a VMEbus request signal is asserted by another master requesting the VMEbus. In this mode the MZ 7130 / MZ 7132 can perform several VMEbus cycles until another master requests the bus, at which time the MZ 7130 / MZ 7132 releases the VMEbus allowing the system controller to arbitrate for the next bus master.

Release When Done (RWD) causes the MZ 7130 / MZ 7132 to release the VMEbus at the end of each bus cycle. If it needs the bus again, it must request it. This mode can create extra VMEbus arbitration, but is useful if the MZ 7130 / MZ 7132 are bus masters on a limited basis or on a low priority level.

Programmed Release (PREL) mode allows the MZ 7130 / MZ 7132 to maintain control of the bus until it decides to release itself in software. This allows uninterrupted use of the bus during block transfers or high priority activity. The MZ 7130 / MZ 7132 releases the bus in software by toggling soft-switch bit 7 of MONSWT. Note that PREL is commonly used in conjunction with the BCLR interrupt when the system controller is used in priority arbitration mode. When used in this fashion the MZ 7130 / MZ 7132 sees BCLR when a higher priority bus level requests the bus. In its BCLR interrupt handling routine, the MZ 7130 / MZ 7132 releases itself in software.

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Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D0	BBSY*	D8
2	D1	BCLR*	D9
3	D2	ACFAIL*	D10
4	D3	BG0IN*	D11
5	D4	BG0OUT*	D12
6	D5	BG1IN*	D13
7	D6	BG1OUT*	D14
8	D7	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A7	IRQ7*	A14
25	A6	IRQ6*	A13
26	A5	IRQ5*	A12
27	A4	IRQ4*	A11
28	A3	IRQ3*	A10
29	A2	IRQ2*	A9
30	A1	IRQ1*	A8
31	-12V	+5 STDBY	+12V
32	+5V	+5V	+5V

* Denotes active low signal.

Table 3-1. VMEbus J1/P1 Pin Assignments.

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3.9 Daughter Card Connections

The two daughter card connectors, P3 and P4, located on the lower-left and middle-left side of the MZ 7130 / MZ 7132 boards, allow custom expansion of the MC68030 CPU bus and access to the user defined pins on the VMEbus P2 connector. All of the address and data, and most of the control signals of the 68030 have been brought out to these connectors in addition to a few specialized signals.

The daughter card is selected in a space on the board's memory map that overlaps a portion of the A24/A32 selectable memory area. To access the daughter card, a mode bit in the MISCREG (bit 30) must be cleared and the daughter card address must be in the range of $800000 to the software defined upper P2 daughter card address boundary for the MZ 7130, or $1400000 to the software-defined upper P2 daughter card address boundary for the MZ 7132. The upper P2 address boundary is defined in the ADDRSEL register. Any access in the mixed A24/A32 space above the upper P2 address selects A24/A32 regardless if the mode bit is set or not.

If the daughter card is not enabled, an A24/A32 VMEbus access is performed.

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Signal Mnemonic	Signal Name	Driver Type
AUTOIACK*	Autovector IRQ Acknowledge	TP
CYCLEI*	CPU Bus Cycle Initiate Signal	TP
DBERR*	Daughter Board Error Signal	TP
DBIRQ*	Daughter Board IRQ Signal	OC
DBSEL*	Daughter Board Select Signal	TP
DSIZE0	Data Transfer Size Signals	TS
ICLK23,ICLK34	CPU Clocks	TP
LA0 - LA31	Local Address Bus	TS
LAS*	Local Address Strobe	TP
LD0 - LD31	Local Data Bus	TS
LDS*	Local Data Strobe	TP
LDTACK*	Local Data Acknowledge Signal	OC
LWRITE*	Local Write Signal	TS
RESETA*	MZ 7130 Reset Signal	OC
RMW*	Read-Modify-Write Signal	TP
SAS0 - SAS3	CPU Bus Status Signals	TS
XMOD0 - XMOD1	CPU Bus Execution Mode Signals	TS

Totem-pole	*TP*
Tri-state	*TS*
Open-collector	*OC*

Table 3-4. Daughtercard Driver Summary.

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VMEbus Interrupt Request:	Software programmable VMEbus interrupt generator on any one of the seven VMEbus levels. Address: $180A00.
VMEbus Interrupt Handler:	Software configurable to handle all seven VMEbus levels as well as a number of onboard autovectored interrupts.
Mailbox Interrupt:	VMEbus Addressable 68030 CPU autovectored interrupt. Base address: software programmable in short I/O space on 256 byte boundary
CPU Identification:	4-bit identification code can be jumper configured and read with the status register.
Daughter Board Interface:	Optional daughter card resides over the user defined pins of the P2 connector to allow easy off-board I/O access. Level 4 autovector interrupt level supported.
Data Transfer Modes:	A32:A24:A16, D32:D16:D8 Master A32:A24:A16, D32:D16:D8 Slave
Operating Conditions:	Temperature: 0 to 55° C, inlet air temp, forced air cooling Humidity: 90% noncondensing Power Consumption: 4.5 A (typical) 6.0 A (maximum).
Physical Size:	6U x 160 mm Eurocard.

3.11 Schematics

(To be provided)

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REVISIONS

LTR	DESCRIPTION	APPD	DATE
X1	Initial 'X' release.		
X1			
X2			
X3	INC XECN 16707	JAN NIX	10-12-88
X4	INC XECN X8960	JAN NIX	10-25-88
X5	INC XECN X16751	JAN NIX	1-17-89
X6	NEW LAYOUT A/W: 4	JAN NIX	9-29-89
X7	RELEASE AS 7130/32 (same as AX6)	John B.	8-6-91

DRAWN/ENG	DATE
CHK	
ENGR	
REL	

MIZAR

TITLE: MZ7130/32-CPU

SIZE	DRAWING NO.	REV
B	6800-04356-0000	X7

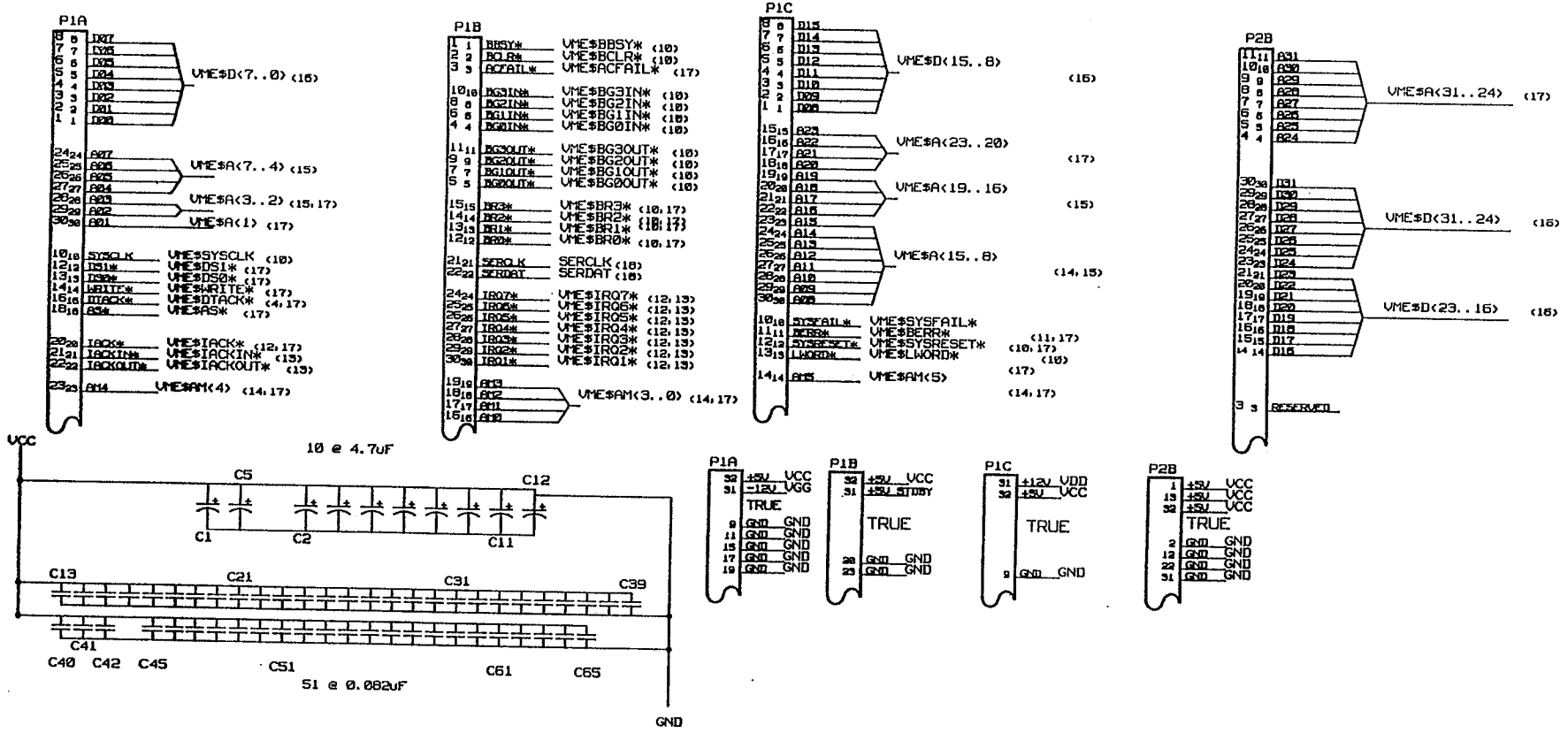
DRAWING

DATE: Fri Aug 9 11:31:15 1991

PAGE: 1 OF 20

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DRAWING

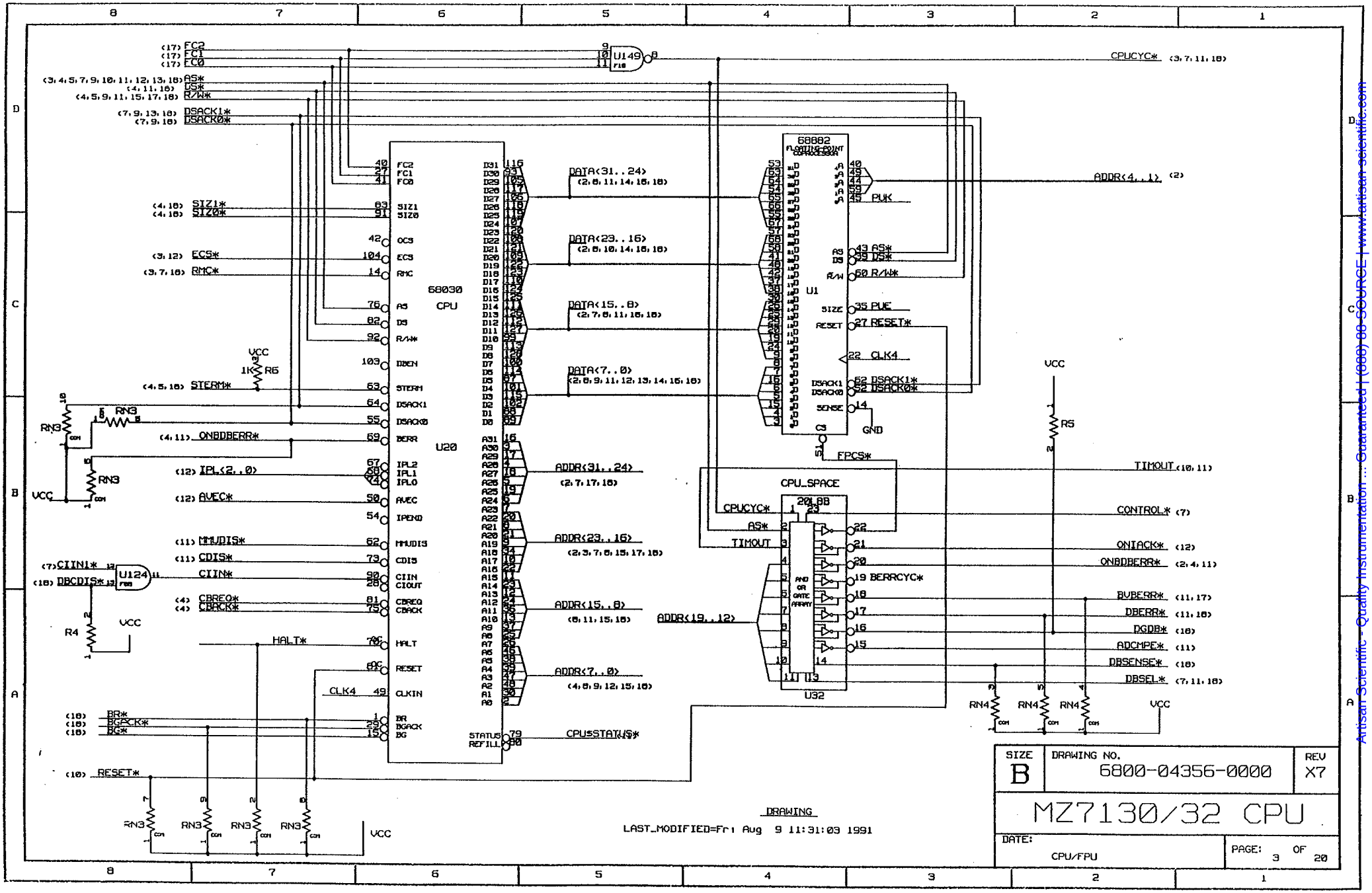
SIZE	DRAWING NO.	REV
B	6800-04356-0000	X7

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DATE: Fri Aug 9 11:31:10 1991

PAGE: 2 OF 20

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DRAWING

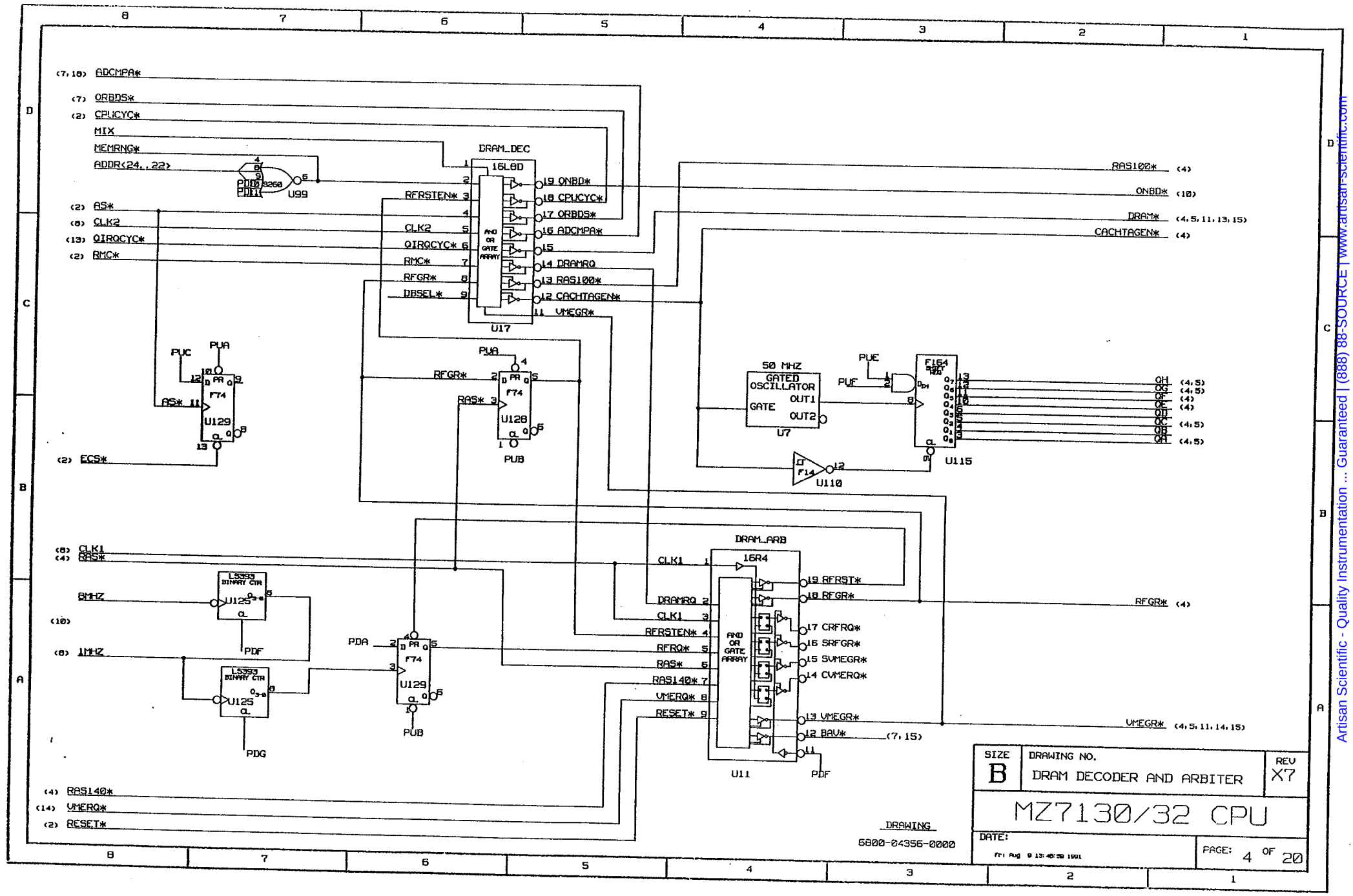
LAST_MODIFIED=Fri Aug 9 11:31:03 1991

SIZE	DRAWING NO.	REV
B	6800-04356-0000	X7

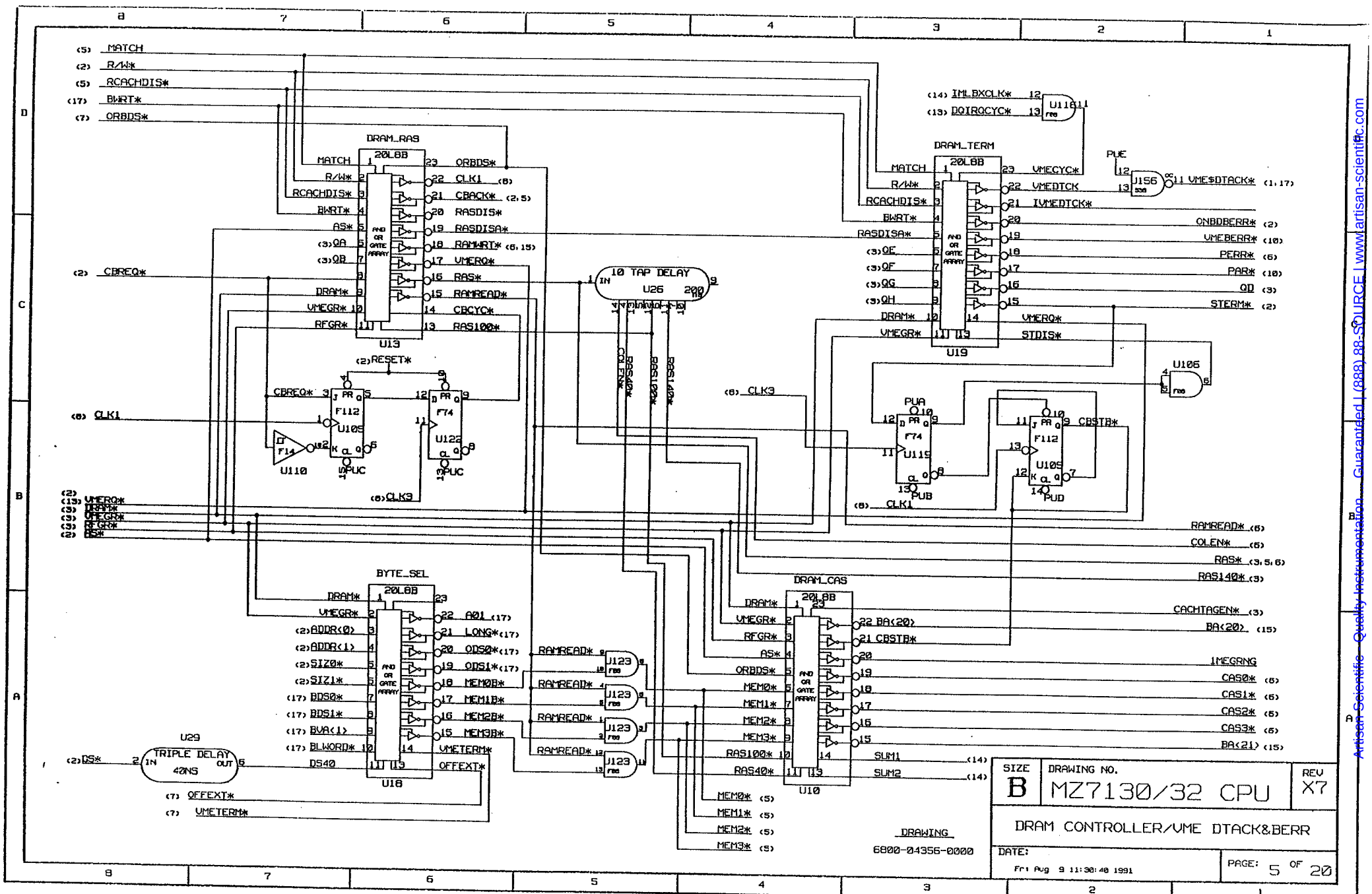
MZ7130/32 CPU

DATE:	PAGE:
CPU/FPU	3 OF 20

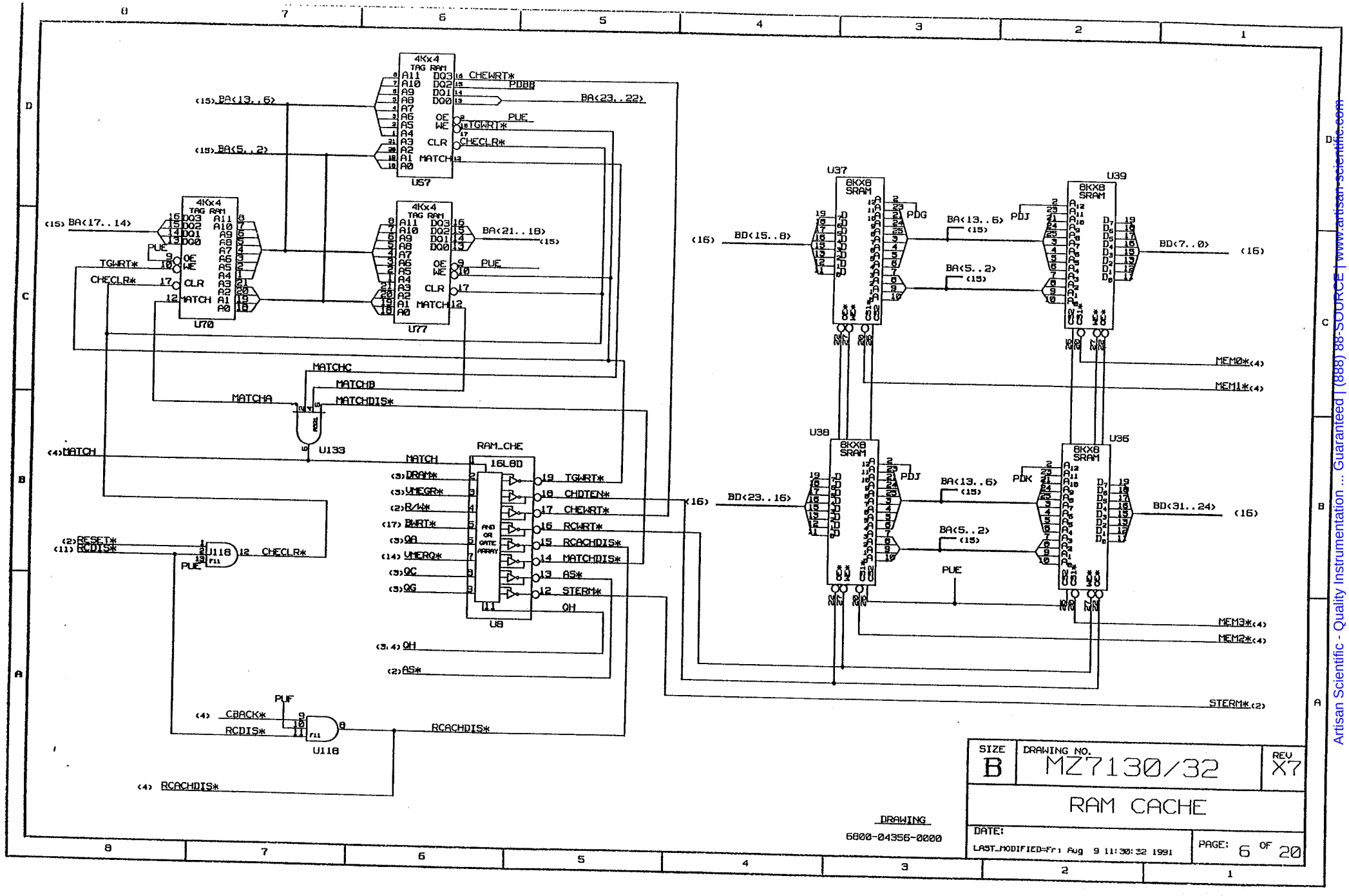
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B	MZ7130/32	X7

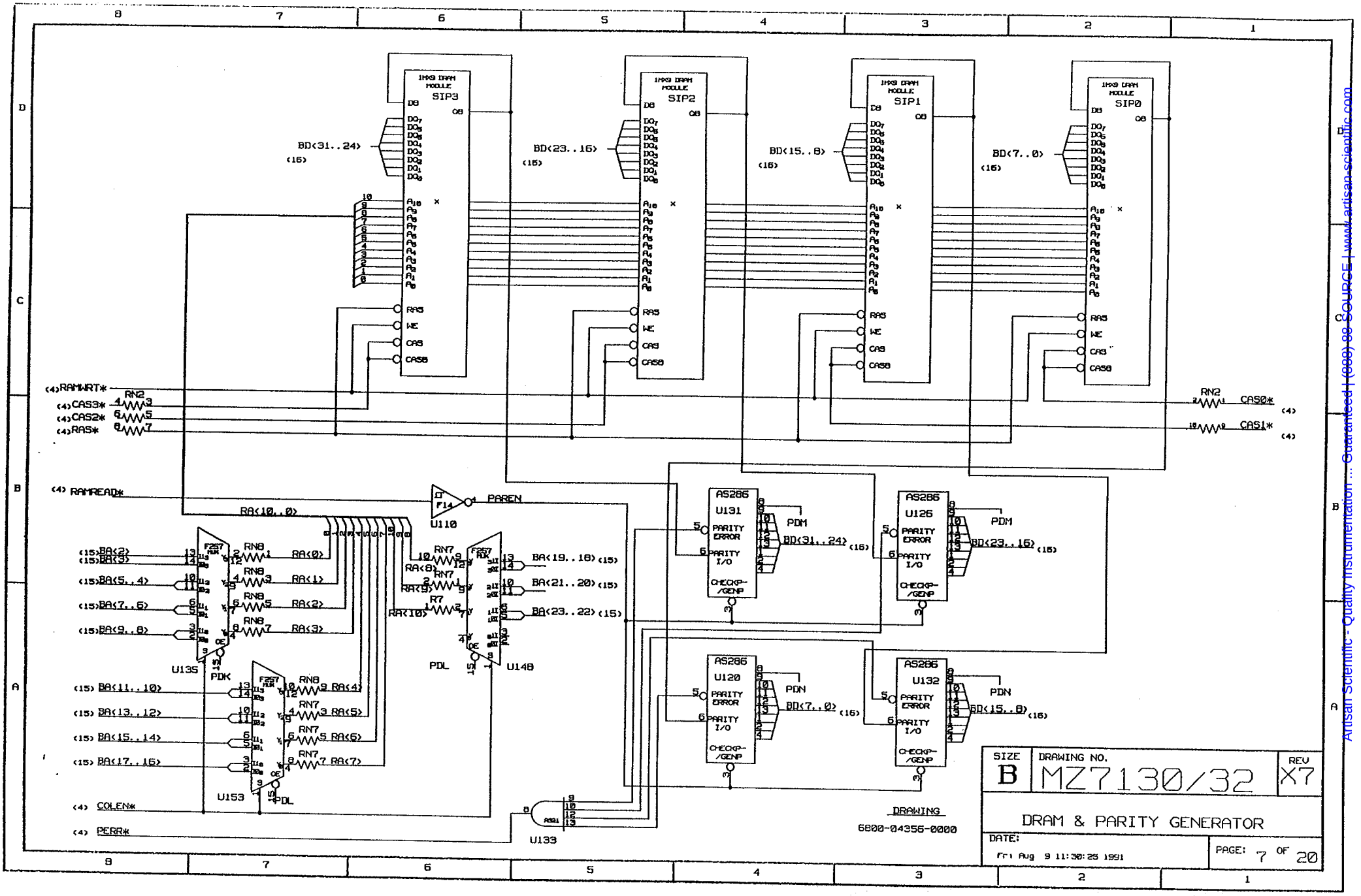
RAM CACHE

DRAWING 6800-04356-0000

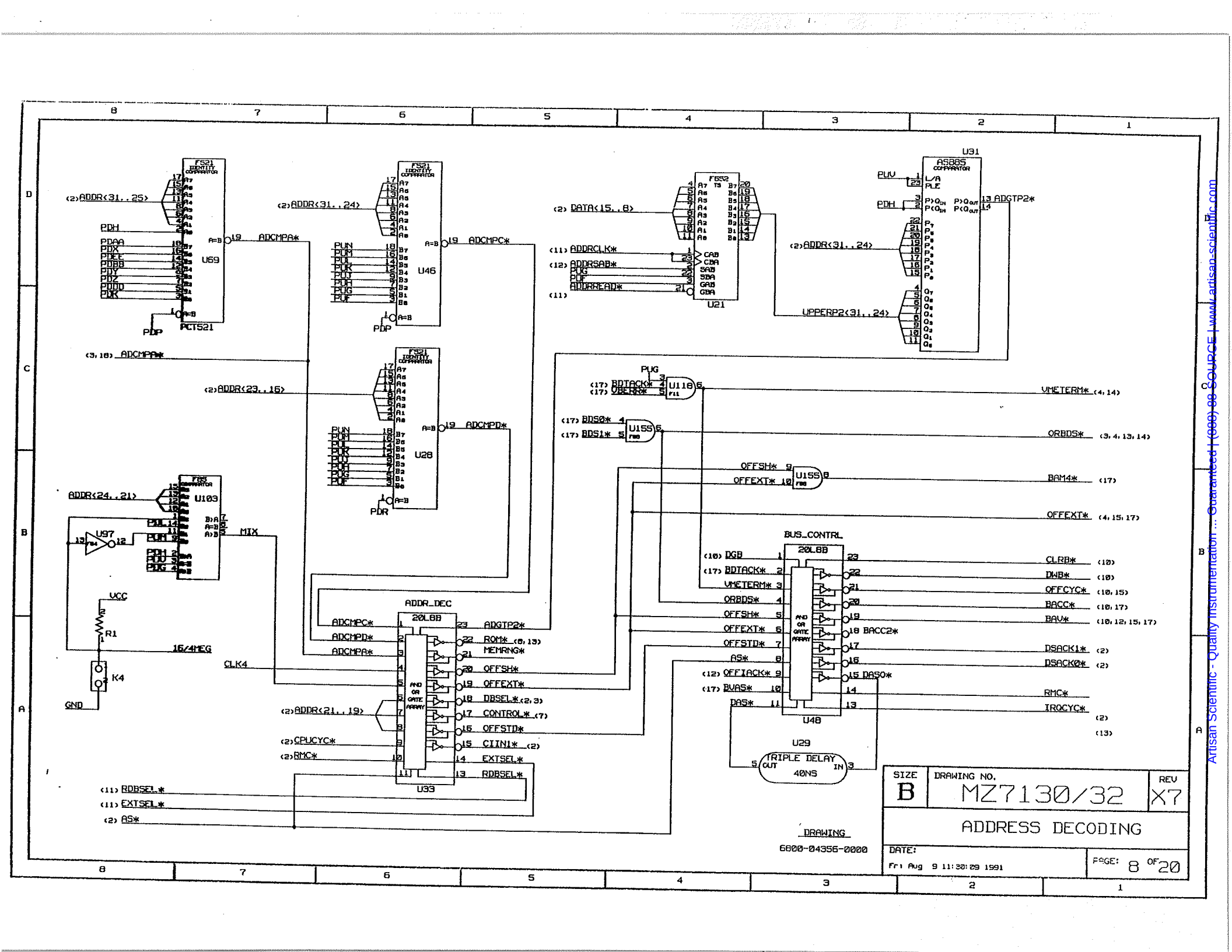
DATE: LAST_MODIFIED=Fri Aug 9 11:30:32 1991

PAGE: 6 OF 20

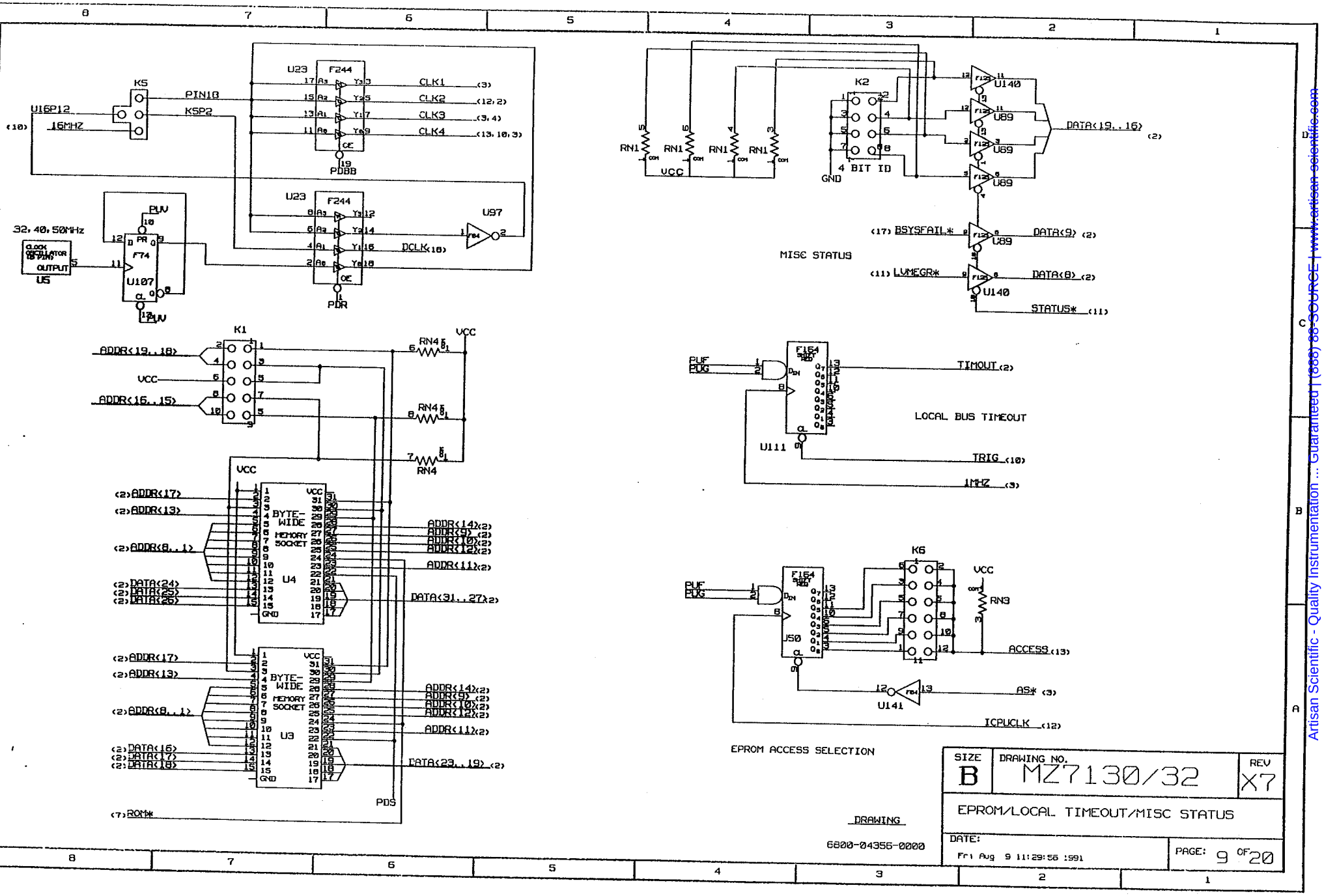
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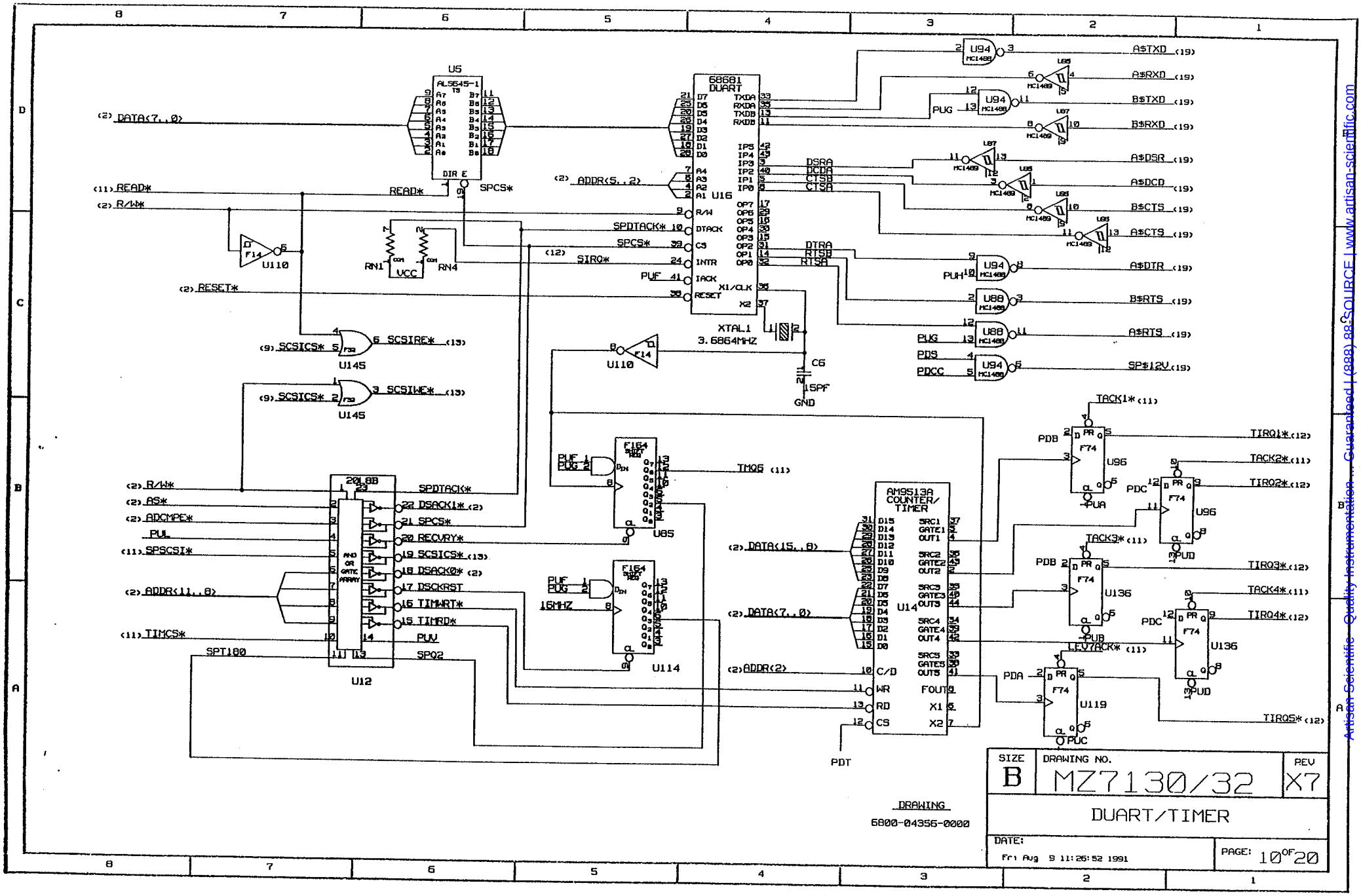
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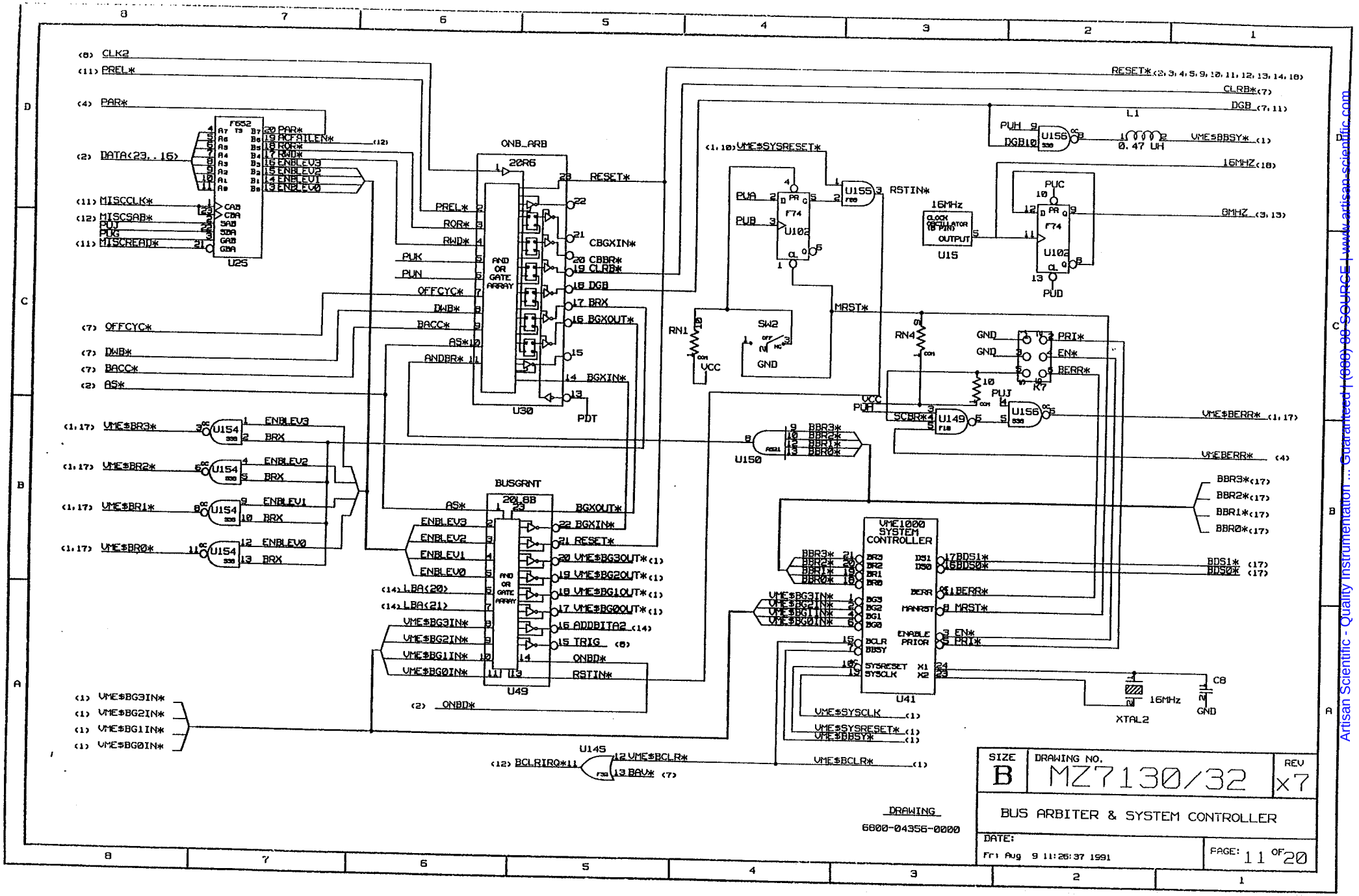
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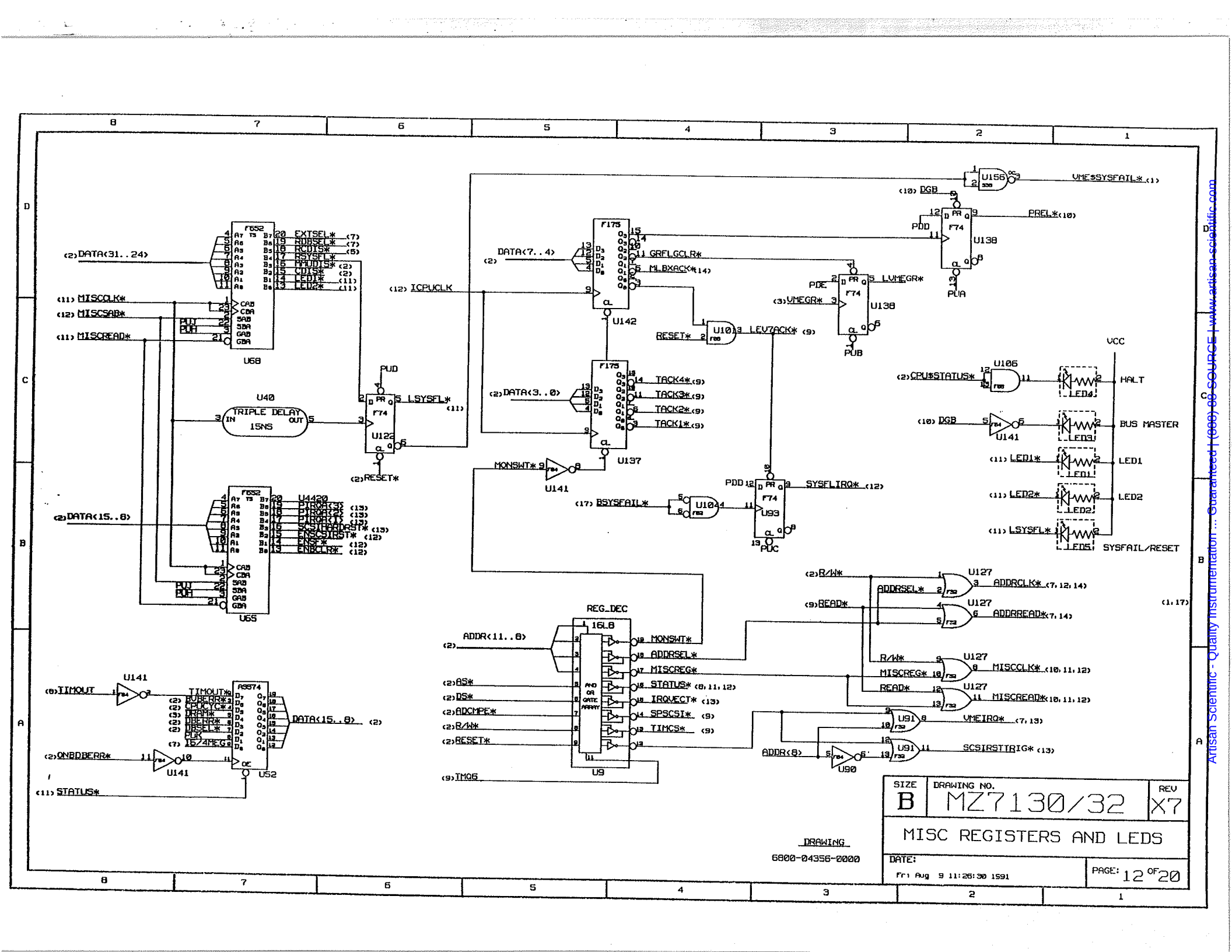
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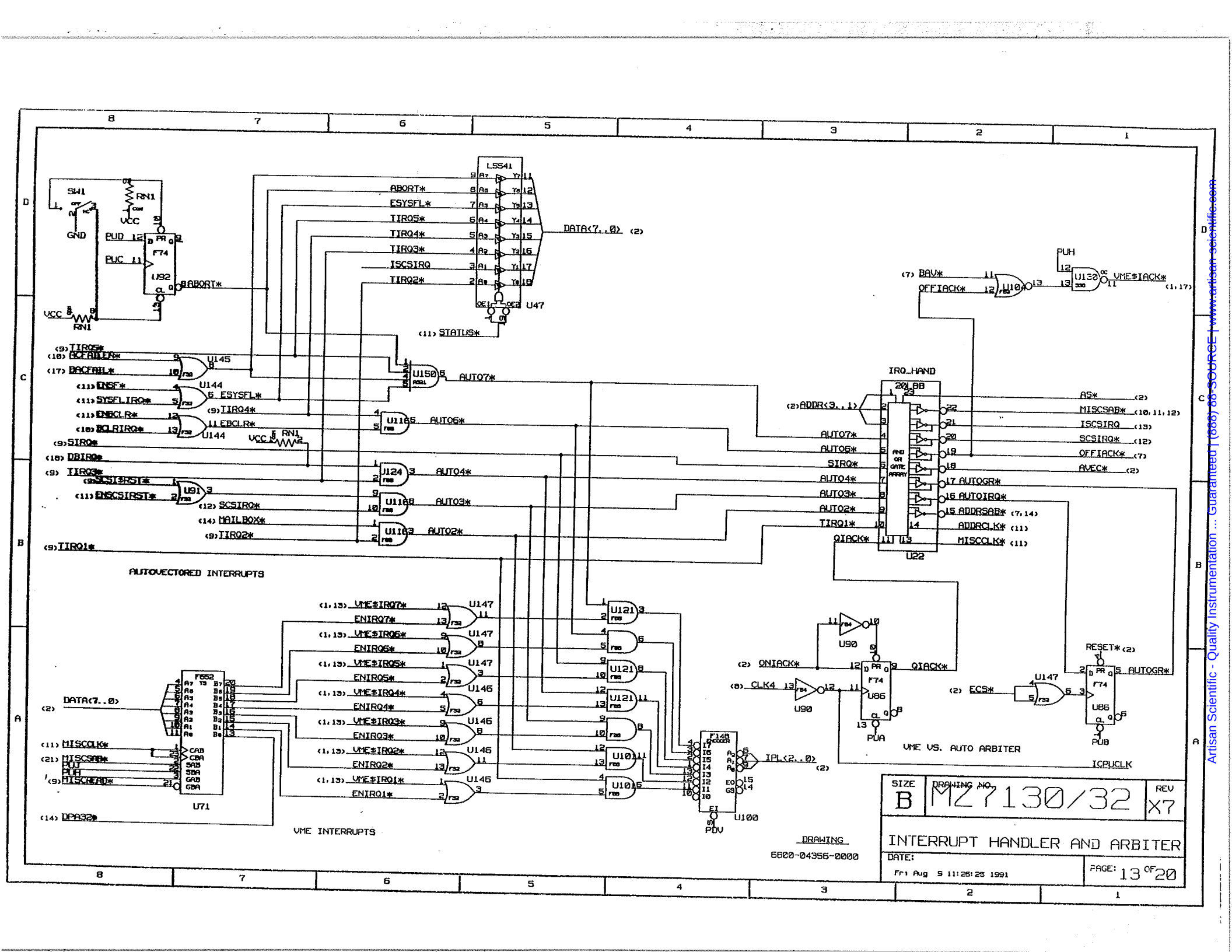
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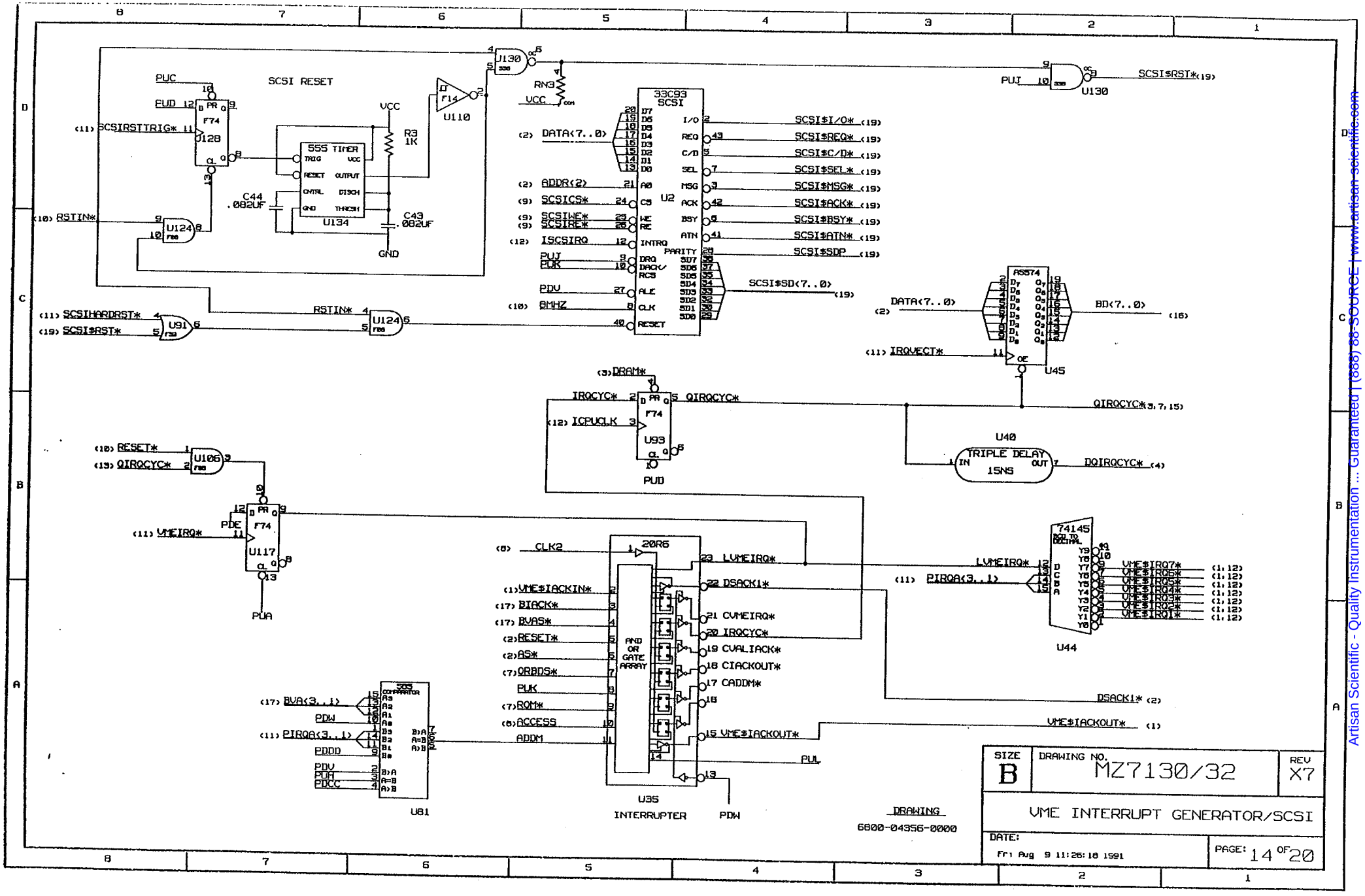
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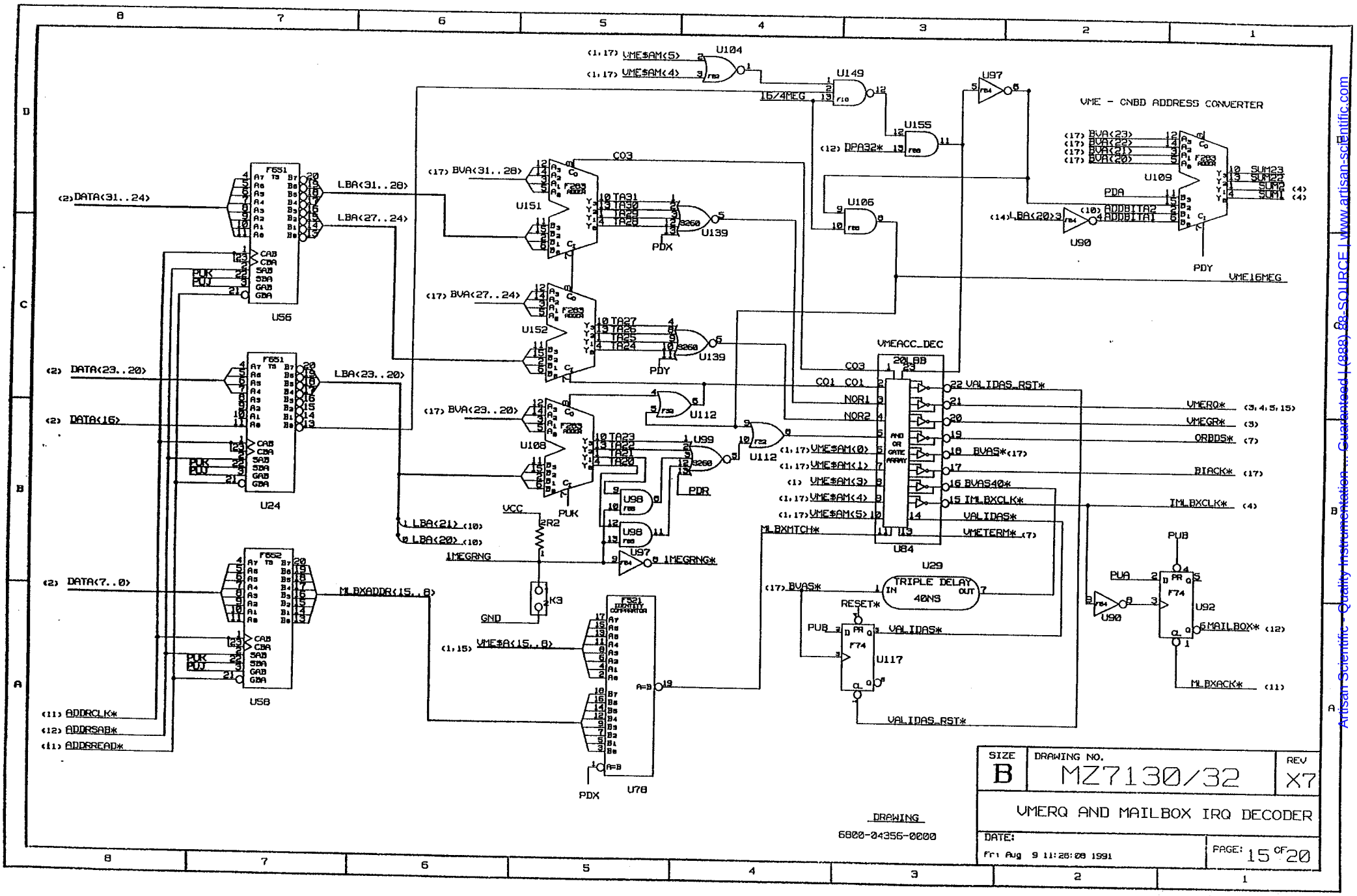
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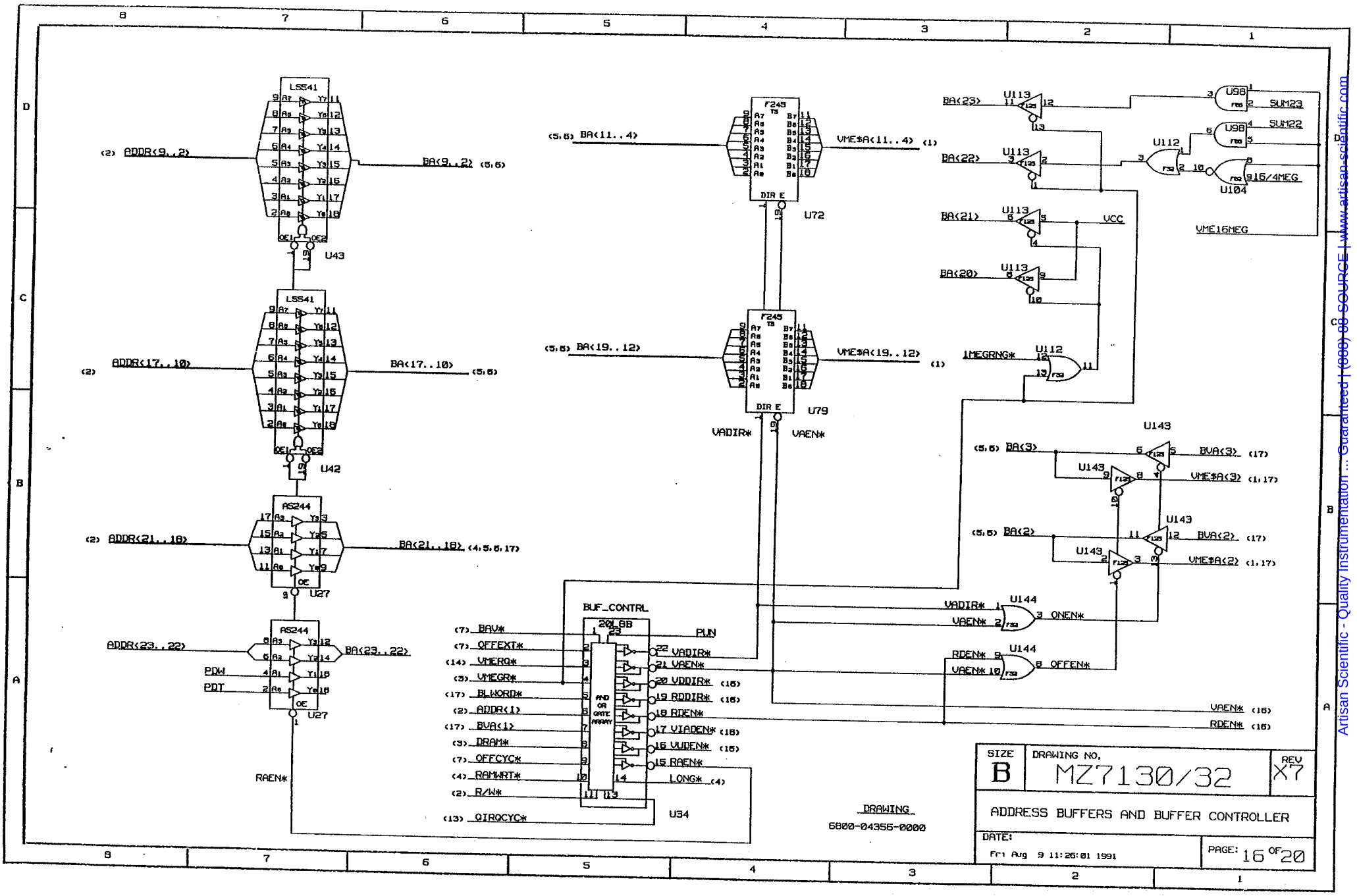
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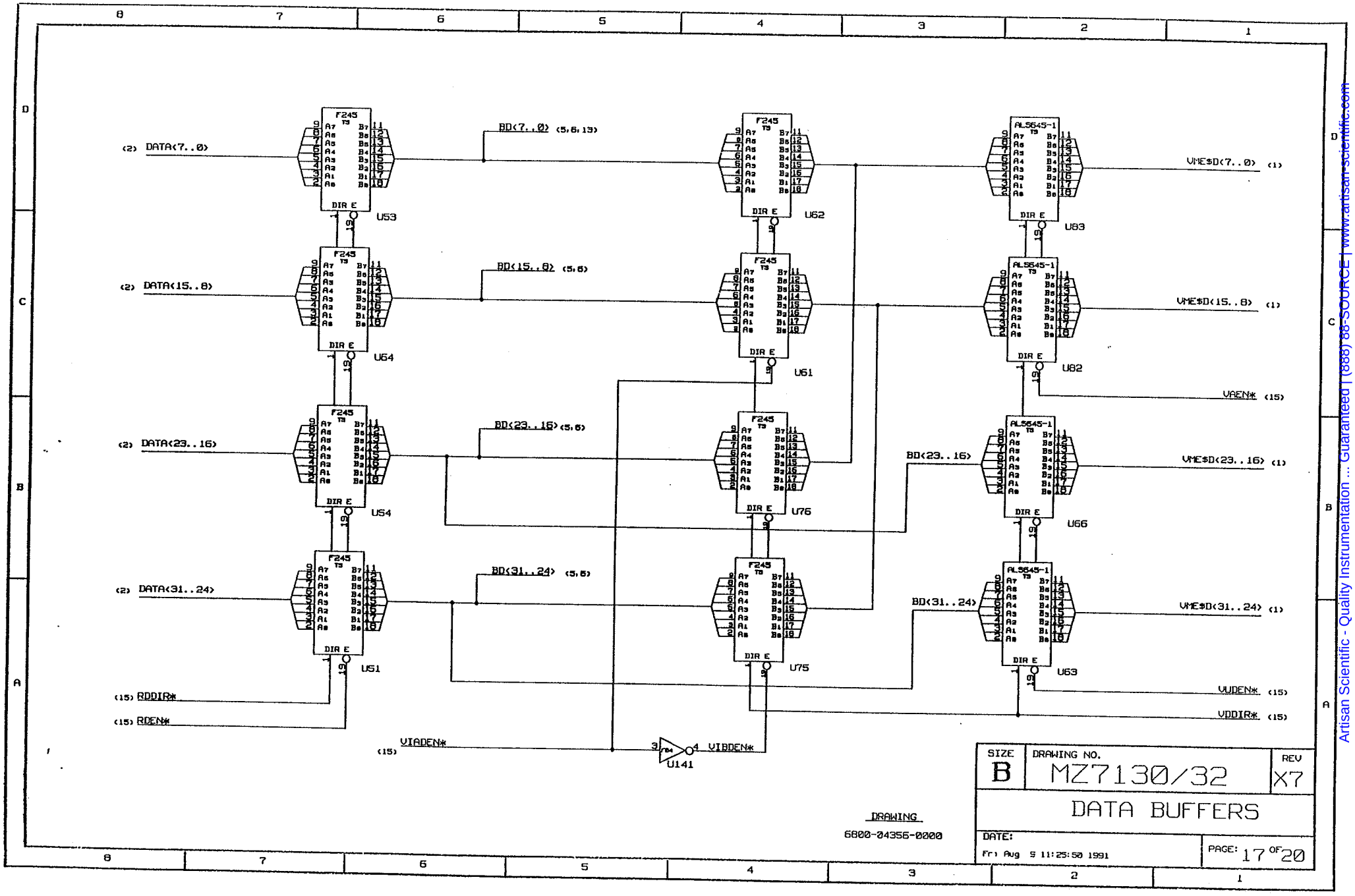
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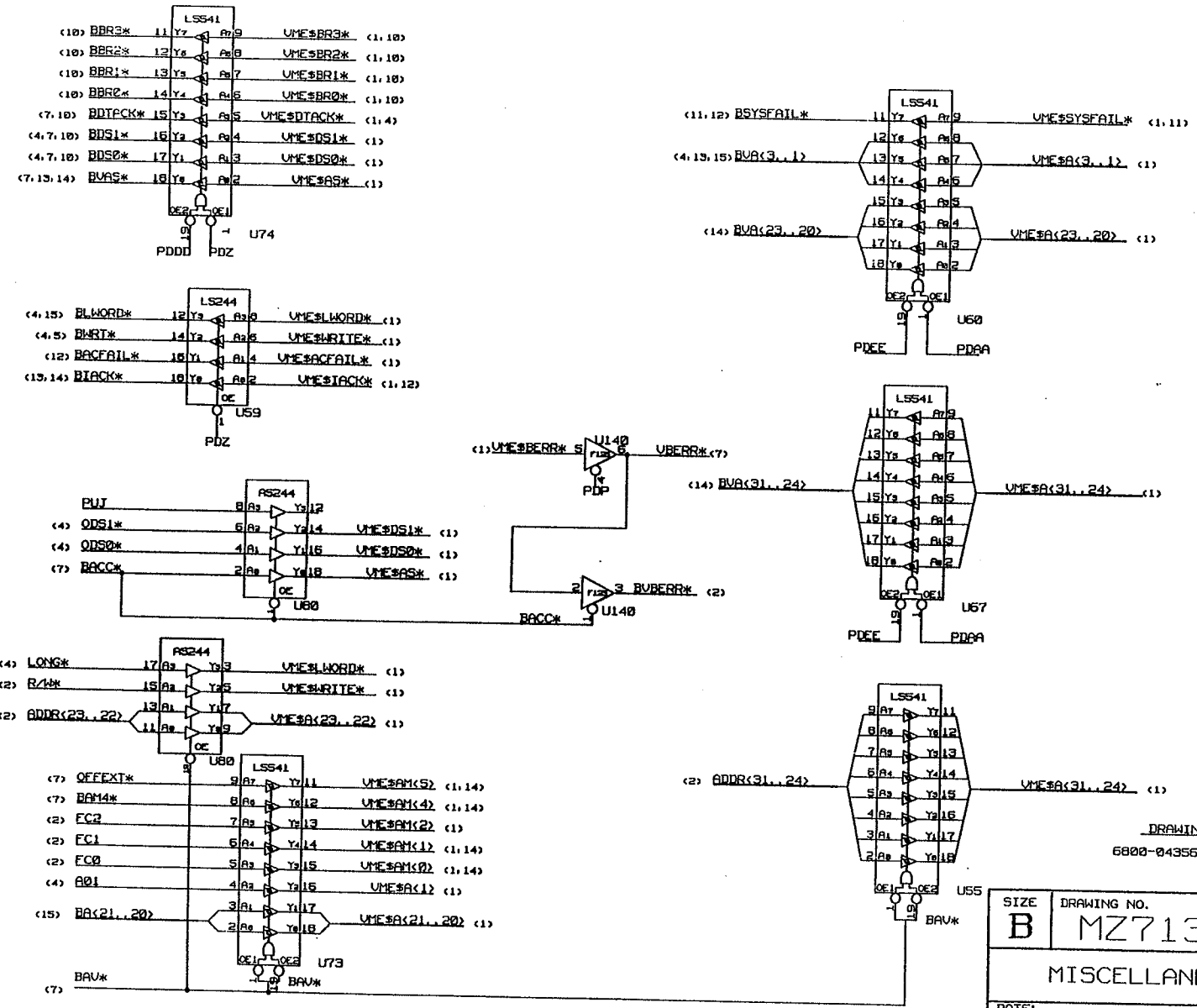
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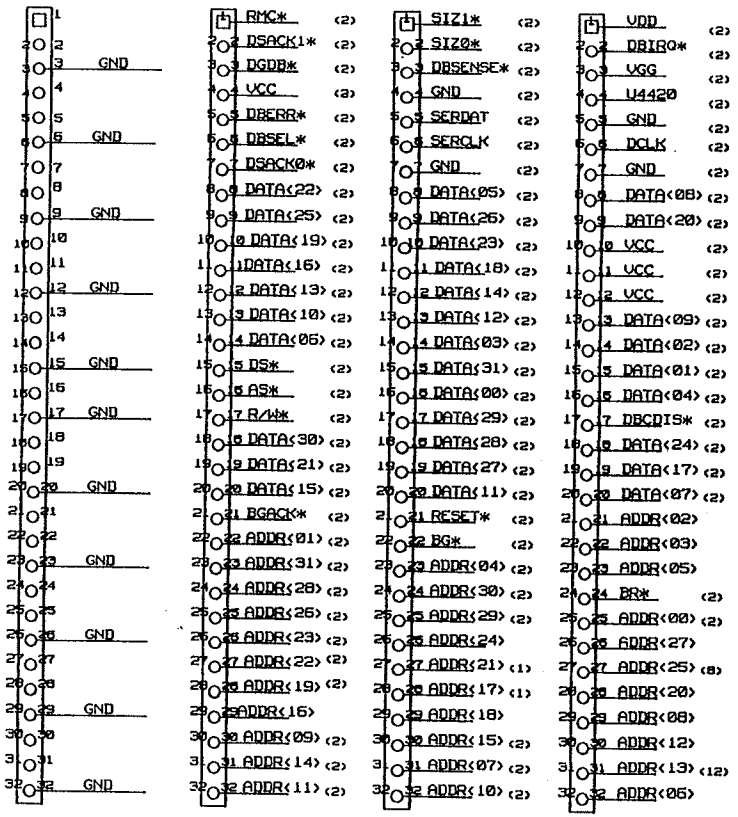
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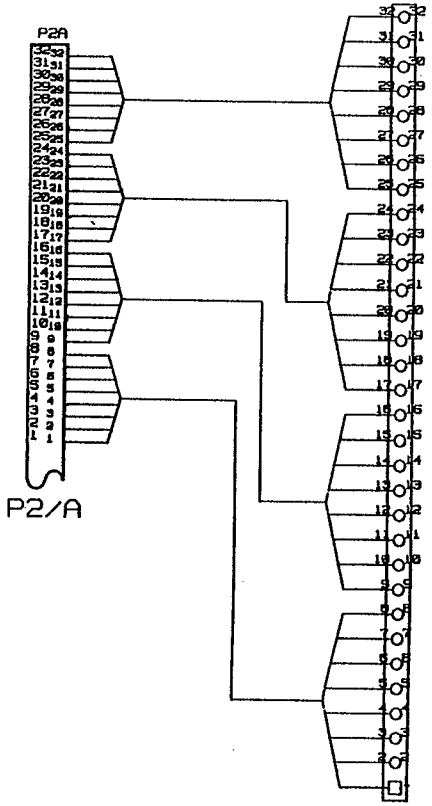


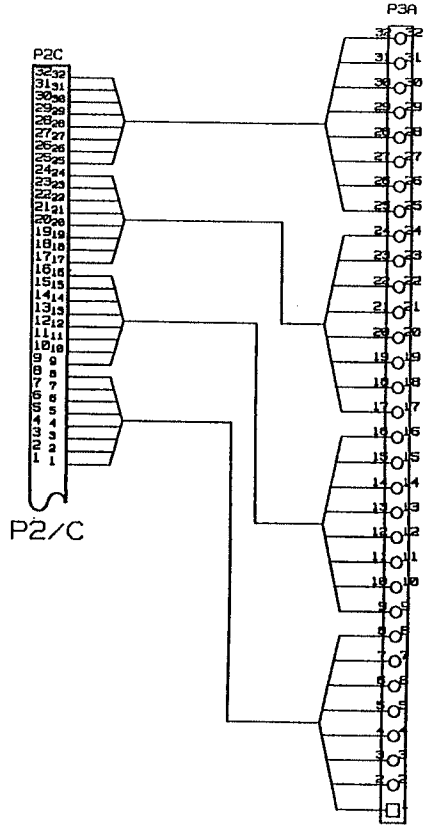
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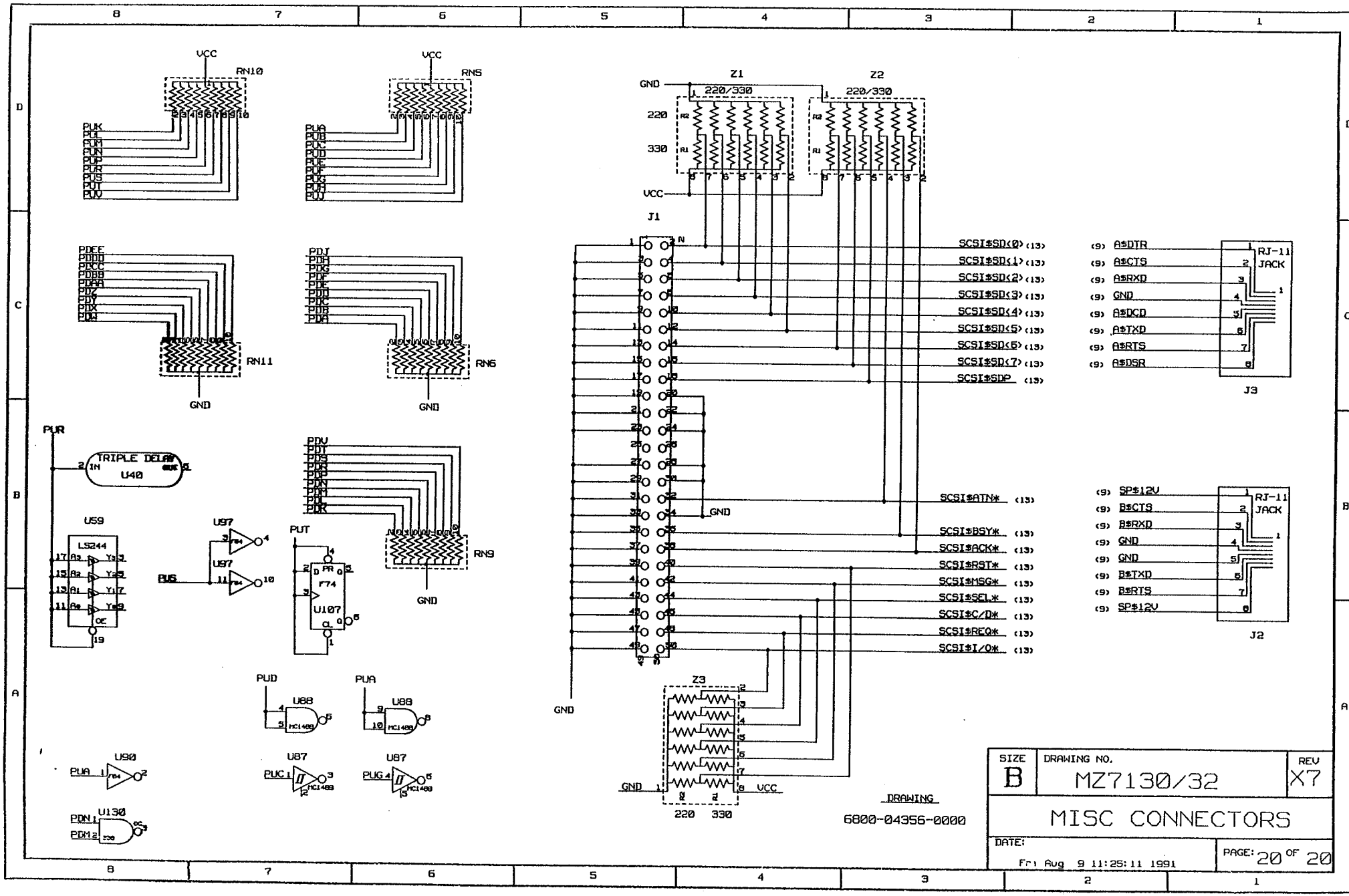
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DAUGHTERBOARD PINOUTS

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