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Schlumberger

July 12, 1999

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This is a description of changes to the operation of the DIP, Inc. CDN-291-1 (+5V version) Devicenet node. The changes involve the latching of the input signals and storing the state information in registors. These changes will be incorporated utilizing the node's internal logical registers and CCO software commands.

There is one input signal (EOT) that acts as a clock (rising edge) and 17 input signals whose state needs to be registered at the rising edge of the clock pulse. The state of the clock pulse (a TTL low) also needs to be registered and mapped. This is highlighted in the following table.

Inputs

BIT #	SIGNAL	DIRECTION	NODE PIN NUMBER	COMMENTS
8	EOT	Input	M-1	This input signal acts as the clock pulse, is received on pin #1, and is active low. Data is valid on rising edge. When pulse is received, a TTL low signal needs to be mapped for this bit location(BIT # 8). Once internal register receives 'CLEAR' pulse (discussed below in outputs), a TTL high signal is mapped to BIT 8.
9	Reprobe	Input	M-2	This input signal is received on pin #2, and is active low.
10	BIN_0	Input	M-3	This input signal is received on pin #3, and is active low.
11	BIN_1	Input	M-4	This input signal is received on pin #4, and is active low.
12	BIN_2	Input	M-5	This input signal is received on pin #5, and is active low.
13	BIN_3	Input	M-6	This input signal is received on pin #6, and is active low.
14	BIN_4	Input	M-7	This input signal is received on pin #7, and is active low.
15	BIN_5	Input	M-8	This input signal is received on pin #8, and is active low.
16	BIN_6	Input	M-9	This input signal is received on pin #9, and is active low.
17	BIN_7	Input	M-10	This input signal is received on pin #10, and is active low.
18	BIN_8	Input	M-11	This input signal is received on pin #11, and is active low.
19	BIN_9	Input	M-12	This input signal is received on pin #12, and is active low.
20	BIN_10	Input	M-13	This input signal is received on pin #13, and is active low.
21	BIN_11	Input	M-43	This input signal is received on pin #43, and is active low.
22	BIN_12	Input	M-44	This input signal is received on pin #44, and is active low.
23	BIN_13	Input	M-45	This input signal is received on pin #45, and is active low.
0	BIN_14	Input	M-14	This input signal is received on pin #14, and is active low.
1	BIN_15	Input	M-15	This input signal is received on pin #15, and is active low.

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Timing relationship of active low EOT pulse relative to BIN signals.



The register latched by EOT signal will be cleared by a bit mapped to the output. This bit will only be used internally by the internal registers. This signal is active low. Below is a table showing present output mapping and new 'CLEAR' signal location.

Outputs

BIT #	SIGNAL	DIRECTION	NODE PIN NUMBER	COMMENTS
2	SOT	Output	M-16	
3	DUT1	Output	M-17	
4	DUT2	Output	M-18	
5	DUT3	Output	M-19	
6	DUT4	Output	M-20	
7	CLEAR	Output (internal)	M-21	This signal is active low. This signal is used to clear the internal registers.

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