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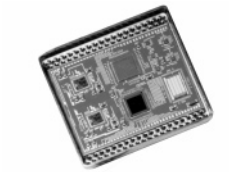
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MIL-STD-1553B NOTICE 2 ADVANCED INTEGRATED MUX HYBRIDS WITH ENHANCED RT FEATURES (AIM-HY'er)

DESCRIPTION

DDC's BUS-61559 series of Advanced Integrated Mux Hybrids with enhanced RT Features (AIM-HY'er) comprise a complete interface between a microprocessor and a MIL-STD-1553B Notice 2 bus, implementing Bus Controller (BC), Remote Terminal (RX, and Monitor Terminal (MT) modes. Packaged in a single 78-pin DIP or 82-pin flat package the BUS-61559 series contains dual low-power transceivers and encoder/decoders, complete BC/RT/MT protocol logic, memory management and interrupt logic, 8K x 16 of shared static RAM, and a direct, buffered interface to a host processor bus.

The BUS-61559 includes a number of advanced features in support of MIL-STD-1553B Notice 2 and STANAG 3838. Other salient features of the BUS-61559 serve to provide the benefits of reduced board space requirements enhanced software flexibility, and reduced host processor overhead

The BUS-61559 contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. Alternatively, the buffers may be operated in a fully transparent mode in order to interface to up to 64K words of external shared RAM and/or connect directly to a component set supporting the 20 MHz STANAG-3910 bus.

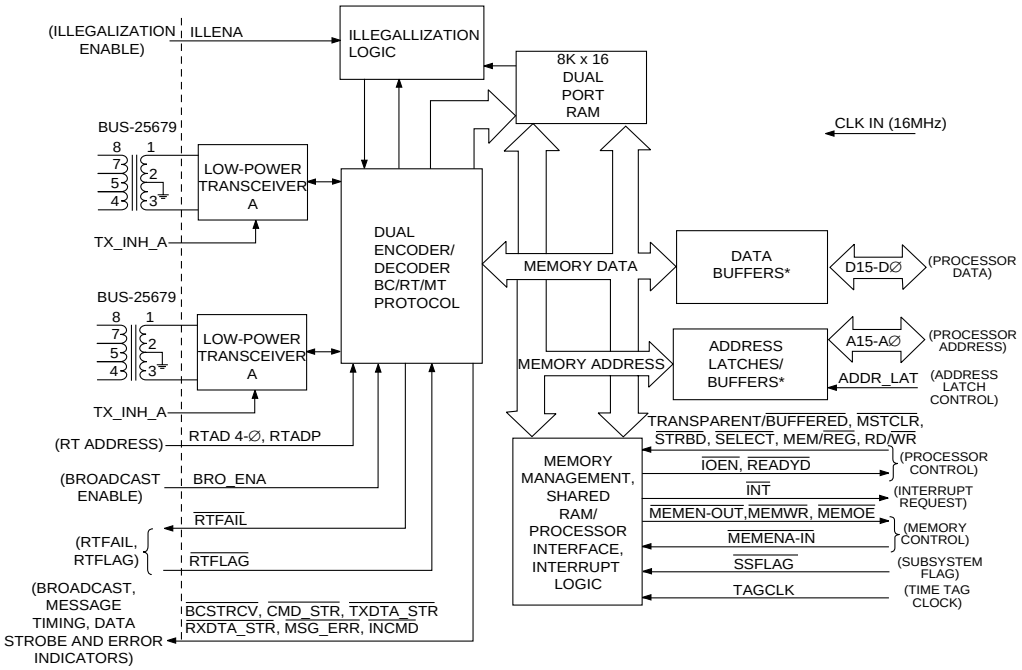
The memory management scheme for RT mode prevails an option for separation of broadcast data, in compliance with 1553B Notice 2. A circular buffer option for RT message data blocks offloads the host processor for bulk data transfer applications.

Another feature besides those listed to the right, is a transmitter inhibit control for the individual bus channels.

The BUS-61559 series hybrids operate over the full military temperature range of -55 to +125"C and MIL-PRF-38534 processing is available. The hybrids are ideal for demanding military and industrial microprocessor-to-1553 applications

FEATURES

- **Complete Integrated 1553B Notice 2 Interface Terminal**
- **Functlonal Superset of BUS-61553 AIM-HYSeries**
- **Internal Address and Data Buffers for Dlrect Interface to Processor Bus**
- **RT Subaddress Circular Buffers to Support Bulk Data Transfers**
- **Optlonal Separatlon of RT Broadcast Data**
- **Internal Interrupt Status and Time Tag Registers**
- **Internal ST Command Illegalization**
- **MIL-PRF-38534 Processing Available**



BU-61559 BLOCK DIAGRAM

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ORDERING INFORMATION

BUS-615XX- XX0X*

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See page xiii.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B**
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B** with PIND Testing
- 7 = B** with Solder Dip
- 8 = B** with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See page xiii.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Power Supply and Packaging
- 59 = +5 V/-15 V DDIP
- 60 = +5 V/-12 V DIP
- 69 = +5 V/-15 V Flat Pack
- 70 = +5 V/-12 V Flat Pack
- 71 = +5 V Flat Pack

*-601 version also available = MIL-STD-1760 compatible with fully compliant MIL-PRF-38534 Processing Available

NOTES

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

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