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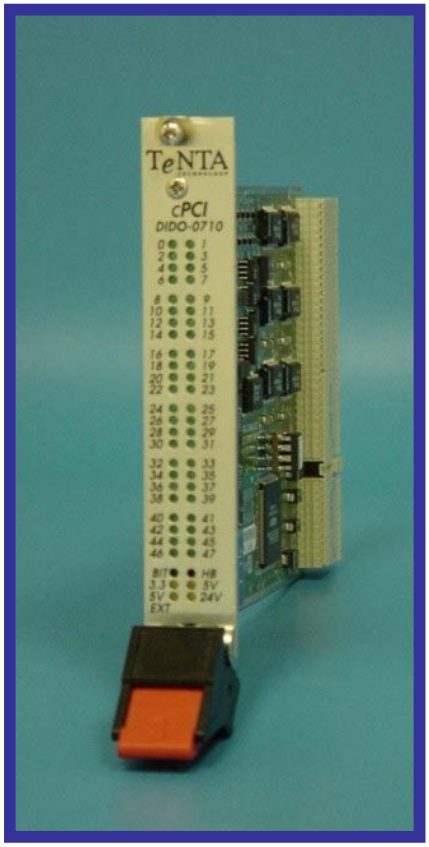
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DIDO-0710

3U CompactPCI Digital I/O Card

User Manual

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Document Revisions

Revision	Comment	BY	Date
E2.0	Release	LL, AF,RH	11/15/99
E2.3	Review and corrections	JR	03/10/00
E2.4	Added product revisions table, updated format	DG	06/04/01
E3.0	Updated format	TJ	01/03/02

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I. Introduction

This document describes the functionality of Tenta's DI/O board 3U CompactPCI form factor. This board design as general-purpose data acquisition, 48 Digital I/O pins, and each pin can be used as Digital input or Digital output. The I/O and power signals are distributed through J2 rear connector. The board form factor, physical dimension and BUS interface complies with CompactPCI Specification PICMG 2.0 R2.1. The board complies with Y2K requirement.

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II. Ordering Information

Part Number	Description
AS00710-01	Digital I/O board, 48 point, 3U cPCI, opto-isolated.

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III. Specifications

A. Physical Specifications

Criteria	Specifications
PCB Dimensions	100MM (3.9370”) Height X 160MM (6.2992”) Depth x 1.6MM (0.0629”) Thickness
Form Factor	Plug in Euro card, 3U Height, 8 HP Width (1 slot), IEEE (1101.1, 101.10 and P1101.11)
Connectors	Metric 2.0mm grid, female connector type A is used for J1 (cPCI BUS) and J2 (Signal distribution).
Front Panel	128.5mm Height X 20.32mm Depth X 2.5 mm Thickness.
Weight	200g

B. Environmental Specifications

Criteria	Specifications
Operating temperature	0-70 ºC
Storage	-40 to +85 ºC
Humidity	5 to 95% non-condensing

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C. Functional Specifications

Criteria	Specifications
BUS interface	Compact PCI, 32 bit (16 bit data transfer) 33MHz
Plug and Play	Support auto recognition of the board on power-on and plug-in includes device ID, Vendor ID and configuration
Front Panel Indicators:	RUN (HB), Power, In/Out Active 48 LEDs
Watchdog timer	Disable outputs (set all outputs to Inactive (+24V) on timeout.
Protection circuitry	2A fuse on each output driver and a suppression diode on each digital input/output port.

D. Power Specification

Criteria	Specifications
Digital Section Power Supply	+3.3VDC@ 20ma, +5VDC @ 220ma from J1
Output/input Section Power Supply	+24V from J2, +5V EXT@ generated on board

E. I/O Circuitry Specification

Criteria	Specifications
Number of I/O signals	48
I/O signal function	Each I/O can be used as Input OR Output. If used as output –output state can be read back.
Number of I/O front panel LEDs	48 green LEDs

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F. Digital Input Signals Specifications

Criteria	Specifications
Voltage Level	Current-sinking, active low
V_{IL}	<2V @ 8 mA sink, < 5V @ 15 mA
I_{MAX}	15 mA
$V_{WITHSTAND}$	5V min above actual voltage of 24V DIO power supply
Isolation	Min 100V
Active Input	Min 6mA (input channel to DIO_COM)
Inactive Input:	Open or Max 3mA from the input circuit.

G. Digital Output Signals Specifications

Criteria	Specifications
Voltage Level	Typical 24VDC, Min 18V DC,
Current	Max 200 mA @24V DC
Isolation	Min 100V
V_{OL}	1.1V max. @ -100mA (sinking), 2V @ -200 mA
V_{OC}	+18V
Current Limit	Max 500mA
Voltage Withstand	5V min above actual value of +24V DIO power supply
Off-state Leakage	100 µA max. @ 60V DC
Temperature Limit	Driver built in thermal shutdown over 165 ºC with 10ºC thermal shutdown Hysteresys
Fusing	2A fuse on each output driver.
Inactive state	24V

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H. Watchdog timer

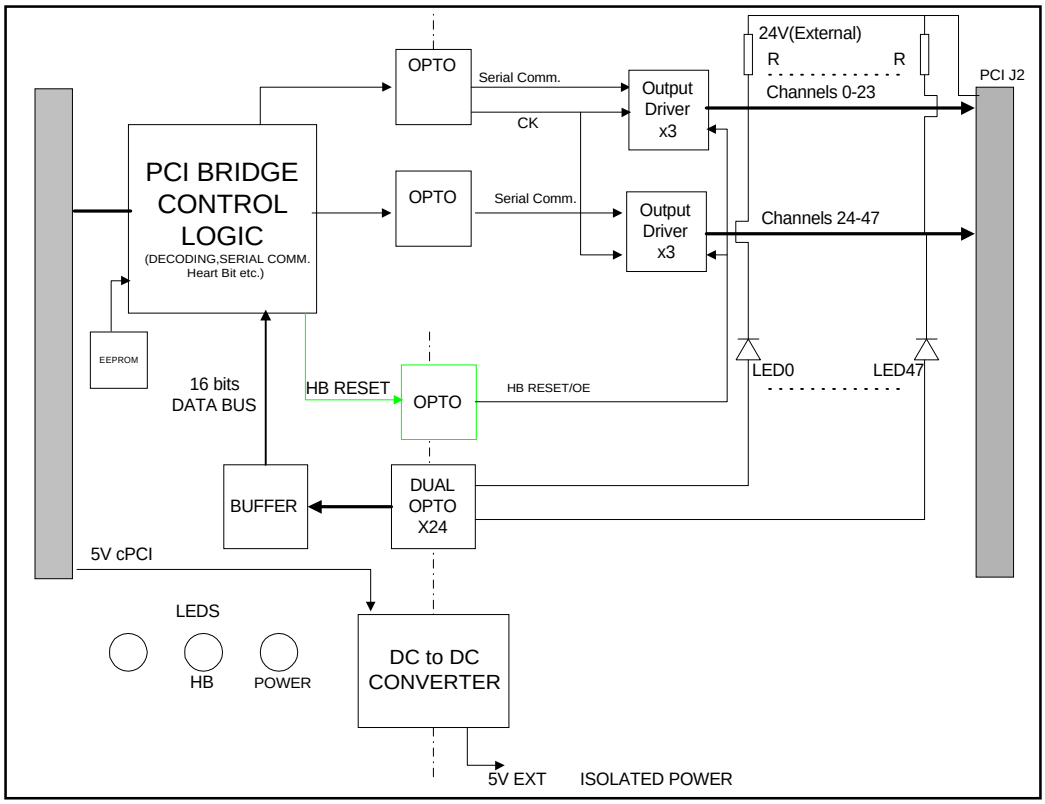
The Watchdog timer insures that cPCI bus communication with SBC is alive. The watchdog timer must be reset by the SBC every 100msec to avoid a time-out. If a time-out occurs, all digital outputs set to inactive state. On time-out the watchdog timer latch on “watchdog fail” until reinitialized by the SBC. On board jumper (JP3) allows to by-pass this feature.

I. J2 Signals Distribution

	Z	A	B	C	D	E	F
22	GND	Reserved	Reserved	Reserved	Reserved	Reserved	GND
21	GND	Reserved	Reserved	Reserved	Reserved	Reserved	GND
20	GND						GND
19	GND	DI/O 44	DI/O 45	DI/O 46	DI/O 47		GND
18	GND	DI/O 39	DI/O 40	DI/O 41	DI/O 42	DI/O 43	GND
17	GND	Dig Com	Dig Com	Dig Com	Dig Com	Dig Com	GND
16	GND	DI/O34	DI/O 35	DI/O 36	DI/O 37	DI/O 38	GND
15	GND	DI/O 29	DI/O 30	DI/O 31	DI/O 32	DI/O 33	GND
14	GND	DI/O 24	DI/O 25	DI/O 26	DI/O 27	DI/O 28	GND
13	GND	Dig Com	Dig Com	Dig Com	Dig Com	Dig Com	GND
12	GND						GND
11	GND						GND
10	GND	DI/O 20	DI/O 21	DI/O 22	DI/O 23		GND
9	GND	Dig Com	Dig Com	Dig Com	Dig Com	Dig Com	GND
8	GND	DI/O 15	DI/O 16	DI/O 17	DI/O 18	DI/O 19	GND
7	GND	DI/O 10	DI/O 11	DI/O 12	DI/O 13	DI/O 14	GND
6	GND	DI/O 5	DI/O 6	DI/O 7	DI/O 8	DI/O 9	GND
5	GND	DI/O 0	DI/O 1	DI/O 2	DI/O 3	DI/O4	GND
4	GND	24V	24Vret	24V	24Vret	Reserved	GND
3	GND	Reserved	Reserved	Reserved	Reserved	Reserved	GND
2	GND	Reserved	Reserved	Reserved	Reserved	Reserved	GND
1	GND	3.3V	3.3V	3.3V	5V	5V	GND

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IV. Block Diagram



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V. I/O Address Map

Board base address registers allocates 64 bytes within 32-bit memory space. On power-up or system reset, all on-board control registers are reset to 0. This sets all digital outputs to inactive state (high).

The following table defines the memory layout of the DIO710 relatively to its base address. Bit 0 is the LSB of a 32 bit long word. Bits not defined are considered don't-care.

Offset	Register Description	R/W	Bit	Bit Range Description
0	Reset	W	0-31	Reset By writing any value.
4	Write Digital Ports 0-23	W	0-23	Write Values, Output triggers refresh.
8	Write Digital Ports 24-47	W	0-23	Write Values, Output triggers refresh.
4	Read Digital Ports 0-23	R	0-23	Read Values
	Output (0-23) busy	R	24	Output refresh taking place. Busy = 0, Ready = 1
	BIT Failed	R	27	Hardware Built-In-Test failed indicator
	WD Enable	R	28	Watch dog enabled
	WD Interval	R	29-30	Watch dog Time-out interval.
	WD Reset	R	31	Reset Activated (Occurred = 0)
8	Read Digital Ports 24-47	R	0-23	Read Values
	Output (24-47) busy	R	24	Output refresh taking place. Busy = 0, Ready = 1
16	Watchdog Timer	W	0	Enable watchdog. Enable = 1
		W	4-5	Time-out interval. 100mS = 00 200mS = 01 400mS = 10 800mS = 11
		W	8	Report Reset Occurrence (Report = 1)
	BIT LED control	W	12	BIT LED
20	Interrupt Mask 0-23	W	0-23	Mask values. Interrupt enabled = 1
24	Interrupt Mask 24-47	W	0-23	Mask values. Interrupt enabled = 1

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VI. Interrupts

A. Interrupt Handling

This section is for future reference.
The application may register a change in the value of an input port that was masked as interrupt enabled. Once there was a change in digital input the board will force an interrupt over the PCI bus via INTA# signal.

B. Interrupt Mask

The driver should avoid enabling an interrupt to a port defined as output. Such definition is miss-configuration.

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VII. Test Procedure

The functionality of all digital outputs and digital inputs are examined by an automatic test procedure (ATP). DIO710 consists of 48 Digital I/O pins; each pin can be used as Digital input or Digital output. Software configurable, due to this fact each two consequent pins are connected together by an external loop-back connector and load (Iout=200mA) resistors. The ATP program checks validation of each digital output path and the consequent digital input that is connected to that digital output.

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VIII.Product Revision History

Rev	Changes	Reason
E1	Original	
B	Change C3 to 35VDC model	Capacitor has marginal voltage specification
C	Change EPROM to 710.30	2us spikes on DO lines during write operation

All boards of Rev. E1 should be discarded. All other boards under Rev. C can be returned to Tenta for upgrade.

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IX. Warranty

Tenta Technology warrants the original purchaser for two years from the date of delivery for any defect in the product, material or workmanship. Product should be used in suitable installation environment and for the purposes it was designed. Any damages caused by natural disasters such as: fire, flood, wind and lightning are not covered. For more information, please contact Tenta Technology customer support (see locations on front page). Tenta Technology hardware and software are not intended for use in any manner when human life or safety is at risk and not for use in life support equipment.

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