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Find the *Curtiss-Wright / VMETRO / Micro Memory MM6346D* at our website: *Click HERE*

MM-6346 Data Sheet

A 512 Mbyte, 40 Mbyte/sec Transfer Rate, Dual Port, VME/VSB Compatible DRAM Memory Module

FEATURES:

- **Capacity:** 16M, 32M, 64M, 128M, 256M, 512M bytes
- **Cycle/Access Time (nsec):** Read: 100/30 Write: 100/30 (Block Transfer-BLT, Page Mode)
- **Compatible with** VMEbus Rev C.1 and VSBbus Rev C with A32/A24/D16/D8 (UAT) for VME and A32/D32 for VSB
- **Block Transfer (BLT)** for sequential access for both ports
- **Parity** generation and checking for error detection on each byte
- **Module selection** on 1 Mbyte boundaries, switch-selective for lower and upper limits on each bus
- **VMEbus Control Status Register** (CSR) for parity reporting and control
- **Write-Wrong parity** for diagnostics
- **Lifetime Warranty**

DESCRIPTION:

A high-speed, dual-port, single card slot, high-density memory module, the MM-6346D provides up to 512 Mbytes for VME/VSB systems. It is intended for high performance applications employing Page Mode and Block Transfer at data rates greater than 40 Mbytes/sec. It also supports sequential access (BLT) of 256 bytes on the VME and VSB bus.

The Control Status Register (CSR), located in the short I/O address space, stores and reads byte-wide parity errors detected on the VME/VSB buses. The other bits enable Write-Wrong parity for diagnostics, disable VME-port and determine whether the memory is CACHEable on the VSB bus. Parity generation and checking are provided for each byte: parity status is stored and transmitted via BERR*.

Reliability is ensured by burn-in and running memory diagnostics that check operation for 48 hours while temperature-cycling boards from 0 to 60 degrees (Celsius). Also, reliability is backed up by Micro Memory's **Lifetime Warranty.**

SPECIFICATIONS:

Capacity
16M, 32M, 64M, 128M, 256M, 512Mbytes

Cycle/Access Time (nsec)
Read: 100/30; Write: 100/30 (Block Transfer-BLT, Page Mode)

Address
32 bits for VMEbus
32 bits multiplexed with 32 data bits for the VSBbus

Data In/Data Out
8, 16, 32 bits (UAT) for VMEbus
32 bit slave for VSBbus

Sequential Access
Block Transfer (BLT) of 256 bytes on the VMEbus
256 bytes on VSBbus

Address Modifiers
AM0-AM5 are decoded by a socketed PLD with the following codes:
A24: 39, 3A, 3D and 3E
A32: 09, 0A, 0D and 0E
A24 with 8K BLT: 10
A24 with BLT: 38, 3F
A32 with BLT: 0B, 0F
A32 with 8K BLT: 17

Parity Checking
Byte-wide parity generation and checking; parity output stored and transmitted via CSR. Write-Wrong parity for diagnostics

Control Status Register (CSR)
Read/Write, 8 bits wide, jumper-selectable, in VME short I/O space (A16) with VMEbus low limit address tracking

CSR Format
D0 Enable Parity Out
D1 Write-Wrong Parity
D2 Memory CACHEable for VSB
D6 VMEbus Disable
D7 Parity Error
Others: Don't Care

Interface
VME Rev C.1 and VSB Rev C

Modes of Operation
Read, write, read-modify-write, page mode in BLT, and refresh

Memory Selection
Two independent memory ports, switch-selectable on 1M byte (100000H) boundaries for each port by setting the upper and lower limits

Operating Temperature
0 to +60 degrees (Celsius)

Storage Temperature
-40 to +85 degrees (Celsius)

Relative Humidity
Up to 95% without condensation

Power Requirements
5V @ 5.5A

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