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MANUAL, AXOCLAMP-2A MICROELECTRODE CLAMP THEORY AND OPERATION

2500-000 REV C

February 1990

AXOCLAMP-2A MICROELECTRODE CLAMP

THEORY AND OPERATION

Written for Axon Instruments, Inc.
by Alan Finkel, Ph.D.

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Illustrations of the rear-panel view of the AXOCLAMP-2A are shown on the fold-out page at the rear of the manual.

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INTRODUCTION

The AXOCLAMP-2A Microelectrode Clamp can be used as a dual channel microelectrode probe, or as a microelectrode voltage clamp.

Voltage clamping is a powerful technique for the control of membrane potential and for the investigation of processes affecting membrane conductance. Voltage clamping has traditionally been performed using two intracellular microelectrodes and the AXOCLAMP-2A can be used for this purpose.

The AXOCLAMP-2A can also be used for discontinuous single-electrode voltage clamping (dSEVC) and for continuous single-electrode voltage clamping (cSEVC). A single-electrode voltage clamp (SEVC) is more convenient to use than a two-electrode voltage clamp (TEVC) in very small cells and cells which cannot be visualized. A particular advantage of a dSEVC is that the voltage drop due to current flow through the series component of cell membrane resistance (R_s) is not clamped. In addition, for both types of SEVC instabilities due to coupling capacitance and coupling resistance between two microelectrodes do not arise.

The disadvantages of a dSEVC compared with a TEVC are that the response speed is slower, the maximum achievable gain is lower, and the noise in the current and voltage records is greater. The design of the AXOCLAMP-2A reduces these disadvantages towards their theoretical minimums, thereby allowing single-electrode voltage clamping to be performed in the many situations where conventional voltage clamping is not suitable.

A cSEVC is as low in noise as a TEVC but has a severe disadvantage in that the voltage drop across the microelectrode is clamped unless compensation is made. Since the required compensation is never perfect, the cSEVC can only be used when the electrode resistance is very small compared with the cell input resistance. These favorable conditions can often be achieved by the whole-cell patch technique.

Because of the AXOCLAMP-2A's advanced design, it itself does not limit the achievable performance. **Instead, the dominant factor affecting SEVC performance is the microelectrode.** Users of the AXOCLAMP-2A in either of the SEVC modes should be quick to question, then adjust, the microelectrode and its placement.

The AXOCLAMP-2A is a sophisticated instrument. Even experienced researchers are advised to read this manual thoroughly and to familiarize themselves with the instrument using model electrodes (i.e. resistors) and cells (e.g. parallel RC) before attempting experiments with real microelectrodes and cells.

We will be pleased to answer any questions regarding the theory and use of the AXOCLAMP-2A. Any comments and suggestions on the use and design of the AXOCLAMP-2A will be much appreciated.

We would be most grateful for reprints of papers describing work performed with the AXOCLAMP-2A. Keeping abreast of research performed helps us to design our instruments to be of maximum usefulness to you who use them.

Axon Instruments, Inc.

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FEATURES

The AXOCLAMP-2A is a complete microelectrode current and voltage clamp for intracellular investigations. It combines state-of-the-art single-electrode voltage clamping, two-electrode voltage clamping, and two complete bridge amplifiers into one instrument. Precision command voltages, meters, filters, offsets and many other features are built in to give you unprecedented flexibility.

- ♦ discontinuous single-electrode voltage clamping
- ♦ continuous single-electrode voltage clamping
- ♦ two-electrode voltages clamping
- ♦ discontinuous current clamping
- ♦ two complete bridge amplifiers
- ♦ high-speed headstages
- ♦ low-noise low-hum operation
- ♦ push-button selection of operating mode
- ♦ computer selection of operating mode
- ♦ two digital meters for voltage display
- ♦ digital counter for display of sample rate
- ♦ 3-input digital meter for current display
- ♦ separate current-measurement circuits for each microelectrode
- ♦ virtual-ground current measurement
- ♦ bath potential measurement and compensation
- ♦ internally generated precision command voltages
- ♦ automatic clamping at resting membrane potential
- ♦ offset compensation
- ♦ rejection of stimulus artifacts
- ♦ output bandwidth selection
- ♦ calbration signal on outputs
- ♦ electrode buzz
- ♦ electrode clear
- ♦ hands-free operation of buzz and clear
- ♦ anti-alias filter
- ♦ phase control
- ♦ sampling clock synchronization
- ♦ model cell

VOLTAGE CLAMPING

Voltage clamp with **one or two** microelectrodes -- your choice is dictated by the needs of your investigation; the AXOCLAMP-2A does both. **Discontinuous Single-Electrode Voltage Clamping (dSEVC)** is based on the technique of sampling the membrane potential while zero current flows and then retaining this sampled value while current is injected into the cell. This procedure is rapidly repeated to produce a smooth response. **Continuous Single-Electrode Voltage Clamping** uses a low resistance electrode to continuously record membrane potential and inject current. The error caused by voltage drop across the electrode resistance can be partially reduced by series resistance compensation. With **Two-Electrode Voltage Clamping** (TEVC) one microelectrode is used to continuously record membrane potential while the other is used to inject current.

Gain of the voltage-clamp amplifier is quickly set on a smooth-acting nonlinear control. The phase response of the amplifier is altered from lead to lag by a **Phase Shift** potentiometer with a **Center Frequency** switch to select the range.

A unique variable **Anti-Alias Filter** helps reduce noise towards the theoretical minimum during dSEVC by slowing the response of the sampling circuit to suit the sample rate and the microelectrode response. The **Sample Rate** can be continuously altered from a low value of 500 Hz to a high of 50 kHz. This enables you to take advantage of the decrease in noise and response times occurring when faster sampling rates are used.

The **sample clocks** of two AXOCLAMP-2A's can be **synchronized** in a "Master-Slave" configuration. This is useful in experiments in which two cells in the same preparations are independently voltage clamped using dSEVC. Linking the two clocks prevents the generation of spurious signals which would otherwise appear at harmonics of the difference in the two clocks frequencies.

Output compliance in TEVC mode is **±30 V.** This reduces the chance of saturation while the membrane capacitance is charging after a step change in voltage. To further minimize the chance of saturation during TEVC a relay-switched headstage (HS-4) is available to automatically bypass the current-sensing resistor inside the headstage. The HS-4 headstage must therefore be used in conjunction with a virtual-ground current monitor (VG-2). The HS-4 headstage is recommended only when large, ultra-fast voltage steps in big cells must be established.

Another unique control is a **Resting Membrane Potential (RMP) Balance Indicator** which enables you to preset the clamp offset so that when you switch into voltage-clamp mode the cell membrane will automatically be clamped at its resting value, irrespective of the clamp gain.

A remarkable **"BLANK"** facility can be used to force the voltage clamp system to ignore stimulus artifacts that would otherwise be picked up by the voltage-recording circuit and result in large current artifacts which could damage the cell under clamp.

A **"Monitor"** output enables the input to the sampling circuit to be observed. It is essential to observe this signal during dSEVC to ensure that the microelectrode voltage due to current passing has time to adequately decay at the end of each cycle. An oscilloscope trigger signal at the sample rate is provided for use with the Monitor signal.

The AXOCLAMP-2A allows **very fast** discontinuous single-electrode voltage clamping. In a test cell (see specifications) the 10% to 90% rise time is only 100 μs. In a real setup the response speed is limited by the microelectrode characteristics, but membrane potential rise times (without overshoot) of less than 1 ms have been regularly achieved in a variety of cell types. Two-electrode voltage clamping is much faster.

CURRENT CLAMPING

Two controls for each microelectrode are devoted to clearing blocked microelectrode tips and assisting cell penetration. One is a **"Clear"** switch which can be used to force large hyperpolarizing or depolarizing currents through the microelectrode. The other is a **"BUZZ"** switch which causes the mocroelectrode voltage to oscillate. Depending on the microelectrode and the preparation, one of these two methods will often succeed in lowering the resistance of blocked microelectrode tips. When used while the tip of the microelectrode is pressing against the membrane, Buzz and Clear may also cause the microelectrode to penetrate the cell.

HEADSTAGES

Unity-voltage-gain HS-2 headstages are available in **several current gains.** These cover the range of cell input impedances from less than 1 MΩ to greater than 1 GΩ. Ultrahigh-input impedance versions are also available for ion-sensitive electrodes.

High speed and low noise are achieved by using **bootstrapped power supplies** for the input circuit of each headstage. These bootstrapped power supplies are derived from special high-voltage circuits so that the headstages will not be saturated by the large voltages that may occur during the passage of current through high-resistance microelectrodes. **Capacitance Neutralization** is also derived from high-voltage circuits so that fast responses are not degraded during large input signals.

Current in each microelectrode is continuously measured during both voltage clamp and current clamp. This measurement does not include currents from sources other than the microelectrode (e.g. hum, ionophoresis, the other microelectrode) and indicates zero if the microelectrode blocks.

Headstages have a gold-plated 2 mm (0.08") input socket to directly accept standard microelectrode holders. 2 mm plugs are supplied with the headstages to connect wire leads, if used.

COMMAND GENERATORS

In any mode, level and step commands can be generated internally. **Level Commands** (one for voltage clamp and one for each microelectrode for a total of 3) are set on precision ten-turn potentiometers. The **Step Command** is set on a 3½-digit thumbwheel switch and can be directed to either one of the microelectrodes or to the voltage clamp. An indicator light for each microelectrode illuminates during current commands. External command sources can be used simultaneously with the internal command sources.

OUTPUTS

Two dedicated **Digital Voltmeters** continuously display the microelectrode voltages while a third displays the current in the selected microelectrode or in a virtual-ground circuit, if used. Front-panel controls for each microelectrode and the virtual ground set the scaling of the current meter to suit the gain of your headstage.

A **Digital Counter** lets you know precisely what sampling rate you are using during single-electrode voltage clamp or discontinuous current clamp.

Offset Controls are provided for each microelectrode, and a variable **Lowpass Filter** is provided for the microelectrode used in single-electrode voltage clamping. As well, an internally generated **Calibration Signal** can be superimposed onto each of the outputs. Hence, the output signals in many cases can be wholly conditioned within the AXOCLAMP-2A to suit your recording apparatus.

Six outputs are conveniently located at the front panel for connecting to your oscilloscope. These outputs are repeated at the rear panel, where the other outputs, the inputs and the headstage connectors are also located.

REMOTE CONTROL

Hands-free operation of Buzz is possible using the footswitches supplied with every AXOCLAMP-2A. Selection of the operating mode can be made remotely for **computer sequencing** of experiments.

All AXOCLAMP-2As have a Buzz oscillator to assist in cell penetration. The duration of the Buzz oscillation is normally equal to the time that the front-panel switch is pressed. Practically, the shortest duration that this switch can be pressed is about 100 ms. For small cells, 100 ms Buzz oscillation sometimes damages the cells immediately after penetration.

The **Remote Buzz Duration Control** supplied with the AXOCLAMP-2A is a hand held control that contains a trigger switch to buzz either electrode, and a duration control for setting the Buzz duration in the range 1-50 ms. An appropriate duration can be found for most cells that is sufficiently long to allow penetration of the membrane but short enough that the cell is not damaged after penetration.

MODEL CELL

Every AXOCLAMP-2A is supplied with a CLAMP-1 model cell. This model cell plugs directly into the input sockets of the headstages. A switch allows the CLAMP-1 model cell to be configured as (a) BATH mode -- two 50 MΩ electrodes to ground, or (b) CELL mode -- two electrodes connected to a 50 MΩ // 500 pF cell.

The CLAMP-1 model cell can be used to test and practice using bridge current clamp, discontinuous current clamp, single-electrode voltage clamp and two-electrode voltage clamp. It is a useful tool to use while learning the operation of the AXOCLAMP-2A and subsequently to verify the correct operation of the AXOCLAMP-2A and the recording pathway.

GENERAL

A third HS-2 headstage can be used **extracellularly** to record bath potential. The bath potential is then subtracted from the potentials recorded by the two intracellular microelectrodes to compensate for shifts in bath potential due to changing of solutions or temperature.

A **VG-2 Virtual-Ground** headstage may be used to measure total bath current. Generally, the built-in current monitors are more useful since they yield the microelectrode currents separately without any interfering currents (e.g. from ionophoresis). Since both microelectrode amplifiers are complete, one microelectrode can be used for ionophoresis while the

other is used intracellularly. Internally generated hum due to the built-in power supply has been prevented by using a specially constructed low-radiation transformer, by placing the supply well away from the rest of the circuitry, and by using internal shielding. The incoming power is filtered to remove radio-frequency interference (RFI).

QUALITY

The excellence of the components and construction will be obvious to you from the high quality of the cabinet and controls. Precision ten-turn potentiometers and reliable switches abound. But the high quality is more than "skin deep" gold plated connectors are used throughout, ultralow-drift operational amplifiers are used in all critical positions, I.C.s are socketed for easy maintenance, and the circuit designs and operation have been well tested in laboratories throughout the world. All this adds up to low-noise, low-drift, reliable and accurate operation. And the excellence does not stop with the hardware. We also provide a detailed operator's manual that serves as a handbook of procedures for microelectrode users. A separate service manual is also supplied.

FURTHER INFORMATION AND ORDERING

The AXOCLAMP specification sheet contains complete technical details and ordering information. Please call the factory for answers to any questions you may have.

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GLOSSARY

AXOCLAMP and AXOCLAMP-2A are used interchangeably.

C_{in}	Total input capacitance of the headstage due mainly to the microelectrode and any connecting cable
C_m	Input capacitance of cell
cSEVC	Continuous single-electrode voltage clamp
DCC	Discontinuous current clamp
dSEVC	Discontinuous single-electrode voltage clamp
f_s	Sampling rate; rate for switching from current passing to voltage recording in DCC and dSEVC modes
G	The average gain during dSEVC
G_T	The instantaneous gain of the controlled current source during dSEVC
H	Headstage current gain
I_1	Continuous current flow in microelectrode 1
I_2	Current flow in microelectrode 2
I_m	Membrane current flow
Lag	High-frequency cut
Lead	High-frequency boost
ME1	Microelectrode 1
ME2	Microelectrode 2
R_e	Electrode resistance
R_s	Resistance in series with membrane
RMP	Resting membrane potential
R_m,R_{in}	Input resistance of cell membrane
SEVC	Single-electrode voltage clamp
TEVC	Two-electrode voltage clamp
V_1	Continuous voltage recorded by microelectrode 1
V_2	Voltage recorded by microelectrode 2
VC	Voltage Clamp
VG	Virtual-ground output attenuation
V_m	Membrane potential recorded by microelectrode 1
V_{mon}	Voltage at the input of the sample-and-hold amplifier (SH1)

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QUICK GUIDE TO OPERATIONS

The controls and operation of the AXOCLAMP-2A are very briefly described in this section. Detailed explanations are given in the alphabetically organized Section E of this manual.

D1. HEADSTAGES

(1) HS-2 Series

HS-2 series headstages are standard. Two supplied with AXOCLAMP-2A.

All HS-2 headstages record voltage at unity gain.

Available in several headstage current gains (H). Front-panel controls read directly in indicated units when H = x1. All H values are powers of 10. Small H values used with high-resistance cells and electrodes. Large H values used to pass large currents.

H = x10, x1, x0.1, x0.01 for recording and clamping. H = 0.0001 for ion-sensitive electrodes.

Headstages normally supplied in L version (low-noise, low capacitance-neutralization range). M version can be supplied to compensate large capacitance of grounded shield.

Red connector: Microelectrode input
Gold Connector: Driven shield; case
Yellow connector: Ground output

(2) HS-4 Series

Optional for current-passing electrode (ME2) in two-electrode voltage clamp. (Requires VG-2 for current measurement.) Bypasses internal current-setting resistor during two-electrode voltage clamp so output voltage applied directly to electrode.

Supplied in L or M versions only.

When AXOCLAMP-2A is not in two-electrode voltage clamp mode HS-4 operates same as HS-2.

(3) VG-2 Series

Optional virtual-ground headstage measures total bath current. Not required for normal operation. Required in two-electrode voltage clamp if HS-4 headstage used. Virtual Ground output attenuation (VG) specifies the sensitivity. Smaller VG is more sensitive; used for low currents.

D2. MODE GROUP

Illuminated pushbuttons reconfigure AXOCLAMP-2A for different operating modes.

BRIDGE: Two conventional microelectrode amplifiers.

DCC: Discontinuous current clamp on microelectrode 1.

SEVC: Single-electrode voltage clamp on microelectrode 1.

Discontinuous SEVC (dSEVC) uses time-sharing technique (electrode switches repetitively from voltage recording to current-passing).

Continuous SEVC (cSEVC) is analogous to whole-cell patch clamp (electrode simultaneously does voltage recording and current passing).

TEVC: Two-electrode voltage clamp. Microelectrode 1 does voltage recording. Microelectrode 2 does current passing.

Cont./Discont.: Switch and lamps operate only in SEVC mode.

D3. MICROELECTRODE 1 (ME1) GROUP

Complete intracellular/extracellular electrometer.

Capacitance Neutralization: Neutralizes electrode input capacitance. Clockwise rotation reduces effective input capacitance and speeds response. Overutilization oscillates headstage.

Buzz: Deliberate overutilization of capacitance neutralization. Oscillation helps cell penetration. Footswitches supplied as standard accessories.

Bridge: Compensates electrode voltage drop during current passing. Resistance (scaled by H) read on ten-turn dial. Range automatically reduced tenfold during cSEVC.

Input Offset: Adds $\pm$500 mV DC to electrode voltage at early stage. Use to zero electrode voltage while extracellular.

DC Current Command: For injection of constant current. Magnitude set on ten-turn dial. Polarity set on switch. LED indicates when current injection activated.

Clear: Passes large hyperpolarizing and depolarizing current to clear blocked electrodes or help cell impalement.

Voltmeter: Indicates membrane potential (V_m) in mV.

D4. MICROELECTRODE 2 (ME2) GROUP

An independent intracellular/extracellular electrometer similar to ME1. Differences are:

Potential is labelled V_2.

Output offset adds $\pm$500 mV to electrode voltage in output stage.

D5. VOLTAGE-CLAMP GROUP

Gain:	Sets open-loop gain during voltage clamp. In SEVC modes output is current source. Therefore gain is nA/mV. In TEVC mode output is voltage source. Therefore gain is V/V.
Holding Position:	Sets holding potential during voltage clamp. Range ±200 mV.
RMP Balance Lamps:	Null during Bridge or DCC so that when activated, voltage clamp will be at resting membrane potential.
Phase shift:	Modifies frequency response of voltage-clamp amplifier. Compensates for nonideal phase shifts of membrane. Potentiometer adds phase advance (lead) or phase delay (lag). Switch selects range.
Anti-Alias Filter:	Used in DCC or dSEVC modes to reduce noise of electrodes that have fast and slow settling characteristics.

D6. STEP-COMMAND GROUP

Uses D/A converter to generate precision command voltage.

Destination Switch:	Selects voltage clamp or either microelectrode as target for command. Commands are mV or nA respectively.
Thumbwheel Switch:	Sets magnitude with 0.05% resolution.
Ext./Cont./Off Switch:	Cont. position activates step command. Ext. position thumbwheel switch is off unless logic level HIGH applied to rear-panel Step Activate input. Off position overrides logic input.
Indication:	When destination is a microelectrode and step command is activated, lamp in microelectrode DC Current Command Section illuminates.

D7. RATE GROUP

Counter indicates sampling rate (cycling rate) in DCC and dSEVC modes.

Potentiometer adjusts rate from 500 Hz to 50 kHz.

D8. INPUTS AND OUTPUTS

V_m, I_m Output Bandwidth switch selects -3 dB frequency of single-pole lowpass on I_m and $10.V_m$ outputs.

Current (I) voltmeter displays DC current from either microelectrode or virtual ground if used. Switch used to select meter input. Decimal point set on H_1, H_2 or VG switches.

All BNC inputs and outputs located on rear panel. Frequently used outputs repeated on front panel.

I_m output:	Membrane current recorded by ME1.
I_1 Cont. Output:	ME1 current (equals I_m in Bridge, cSEVC and TEVC modes).
I_2 output:	ME2 current.
I_{VIRT} output:	Virtual-ground current.
$10.V_m$ output:	Membrane potential recorded by ME1; gain of 10.
V_1 Cont. output:	Instantaneous ME1 potential. No Bridge Balance.
Monitor output:	Input of sample-and-hold amplifier. Should be observed on second oscilloscope during DCC and dSEVC modes.
V_2 output:	ME2 potential. Includes Bridge Balance.
Sample Clock output:	Logic-level pulses at the sample rate; used to trigger monitor oscilloscope.
V_{BATH} output:	Potential recorded by bath electrode.
Cal. Activate input:	Logic HIGH on this input puts calibration voltage proportional to thumbwheel setting onto voltage and current outputs.
Step Activate input:	Logic HIGH activates Step Command.
Blank Activate input:	Logic HIGH activates Blank. During Blank, V_m prevented from updating. Thus stimulus artifacts are rejected.
Ext. VC Command input:	Voltage on this input converted into voltage-clamp command.
Ext. ME1 Command input:	Voltage on this input converted into ME1 current command.
Ext. ME2 Command input:	Voltage on this input converted into ME2 current command.
R_s Comp. input:	Used to compensate voltage drop across membrane R_s during TEVC. Not normally required. See service manual for suggested circuit.
V_{BATH} IN input:	Bath potential recorded by other equipment subtracted from V_1 and V_2 if connected to this input.

D9. REMOTE

Allows certain functions to be remotely activated by computer or switches. These are Mode, Buzz and Clear.

D10. CLOCK LINK-UP

Allows sampling clocks from two AXOCLAMP-2As to be synchronized. This eliminates electrode cross-talk when two AXOCLAMP-2As in dSEVC mode used to clamp two cells in same preparation. Requires LU-1 link-up cable.

DETAILED GUIDE TO OPERATIONS

ANTI-ALIAS FILTER

A property of all digital sampling systems is that noise in the input signal at frequencies greater than 0.5 of the sample rate (f_s) is folded down to appear as extra noise in the bandwidth from zero to 0.5 of f_s (see section on noise). This phenomenon is known as aliasing.

Aliasing can be overcome by filtering the input signal before sampling, thereby reducing the high-frequency noise content. However, this filtering procedure degrades the dynamic response of the input signal and when used with an ideal microelectrode worsens the clamp performance.

The voltage across a real microelectrode often has a two-phase decay after the end of a current pulse, either because of redistribution of ions in the tip, or because of the distributed nature of the capacitance through the wall of the microelectrode (see Fig. 1). The final stages of the decay may often be so slow that additional delay introduced by a filter used to prevent aliasing (an Anti-Alias Filter) causes insignificant worsening of the dynamic response. The Anti-Alias Filter can be used by the experimenter to trade off the noise recorded in DCC and dSEVC modes against the dynamic response. That is, increasing the Anti-Alias Filter setting decreases the noise but can lead to instability in dSEVC and can make it more difficult in DCC to balance the response to a current step.

The Anti-Alias Filter also has an effect in the continuous modes. It acts as a lowpass filter on the voltage recorded by ME1. Thus the effects during TEVC and cSEVC are the same as those due to a slow voltage-recording microelectrode. **Using the Anti-Alias Filter in these modes is not recommended.**

Rotating the Anti-Alias Filter control clockwise logarithmically increases the amount of filtering. In the fully counterclockwise position the filter time constant is 0.2 μs and the discontinuous clamp responses are unaffected. In the fully clockwise position the filter time constant is 100 μs. There is a maximal reduction in noise but the maximum sampling rate which can be achieved is severely limited (to about 1 kHz or less).

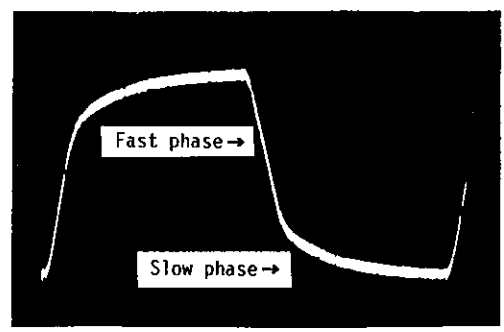


FIGURE 1 - TWO-PHASE MICROELECTRODE DECAY

BATH PROBE

Bath Potential Measurement

In certain experimental circumstances it is desirable to make all voltage measurements relative to a reference point in the bathing solution rather than relative to ground. (These conditions may include precision measurements during changes of temperature or ion content of the saline, or cases of restricted access from the extracellular space to the grounding point.)

All measurements are normally made relative to the system ground. However, if an HS-2 headstage is plugged into the rear-panel Bath Probe connector, measurements by both ME1 and ME2 are automatically made relative to the potential recorded by this headstage. For optimum voltage-clamp performance, the bandwidth of the bath potential is limited to 300 Hz before it is subtracted from the potentials recorded by ME1 and ME2 (see Finkel & Gage, 1985). The bath microelectrode cannot be used for current passing.

The full-bandwidth voltage recorded by the bath microelectrode is available at the V_{BATH} OUT connector.

If there is no HS-2 headstage plugged into the Bath Probe connector, a reference potential from an external amplifier can be subtracted by connecting a reference source to the V_{BATH} IN connector.

Grounding

It is quite uncommon to measure the bath potential. Irrespective of whether or not the bath potential is measured, the preparation bath should be grounded by directly connecting it to the yellow ground connector on the back of the ME1 headstage (or to a virtual-ground headstage if used).

BLANKING

A common problem when using stimulating electrodes is that some of the stimulus is directly coupled into the recording microelectrode. This can saturate subsequent high-gain amplifiers and the coupling capacitors of AC circuits. The saturation effects may take tens or hundreds of milliseconds to subside. The best way to minimize or even eliminate this artifact is at the source, by using small stimuli, isolated stimulators, placing an grounded shield between the stimulating electrodes and the microelectrodes, etc. Often, though, it is not possible to reduce the artifact to manageable levels.

The AXOCLAMP-2A can circumvent the effects of the stimulus artifact by Blanking. At the moment the logic level of the Blank Activate input goes HIGH the value of V_m is sampled and saved. For the duration of the HIGH signal, this saved value is used instead of the actual potential.

In voltage-clamp modes the voltage-clamp current during the Blanking period will be held at the level which existed at the start of the period. A small deviation from the command potential may develop during the Blanking period as a result of comparing the command to the sampled value of V_m instead of the instantaneous value of V_m. This deviation will only be seen when the Blanking period ends. Usually this deviation is preferable to the situation that can occur if Blanking is not used. If Blanking is not used the artifact picked up by ME1 is treated by the voltage-clamp circuit as an attempt by the cell to change its potential. Therefore, the voltage-clamp circuit causes a current to be passed into the cell to clamp this presumed membrane potential change. If the stimulus artifact is large, the consequent current artifact can be large enough to damage the cell.

The width of the Blanking period should be no longer than the minimum width required to cover the period of the stimulus artifact. It is important not to Blank for longer than necessary since during Blanking no updating of V_m is allowed. Even when Blanking is used, attempts should still be made to minimize the artifact at the source.

BRIDGE MODE

Description

In Bridge mode the microelectrode voltages are monitored continuously, and continuous currents can be injected down ME1 or ME2.

Associated with the current flow (I) in a microelectrode is a voltage drop across the microelectrode which depends on the product of the current and the microelectrode resistance (R_e). This unwanted IR voltage drop adds to the recorded potential. The Bridge Balance control can be used to balance out this voltage drop so that only membrane potential is recorded. The term "Bridge" refers to the original Wheatstone Bridge circuit used to balance the IR voltage drop and is retained by convention even though the circuitry has been replaced by operational amplifier techniques.

The particular setting required to balance the Bridge is a measure of the microelectrode resistance.

In cSEVC mode the Bridge potentiometer compensates electrode IR voltage drop at one-tenth sensitivity.

Suggested Use

Set the Destination switch to ME1/2 and externally trigger the Step Command generator so that pulses of current are repetitively injected into ME1/2. (Alternatively, derive the command for injecting current pulses by connecting a signal source to the Ext. ME1/2 Command input.) Start with the Bridge Balance control set to zero. Advance the dial until the fast voltage steps seen at the start and finish of the current step are just eliminated. The Bridge is correctly balanced. The residual transient at the start and finish of the current step is due to the finite response speed of the microelectrode. No attempt is made to balance this transient since it covers a very brief period only and it is a useful indication of the frequency response of the microelectrode. The transient can be minimized by correctly setting the Capacitance Neutralization.

The Bridge balancing procedure is illustrated in Fig. 2. The trace in A was recorded in a model cell when the Bridge Balance control was correctly set. In response to a positive current pulse the membrane potential began to charge up. Before the membrane potential reached its final value the current pulse was terminated and the membrane potential exponentially decayed to its final value.

The traces in B were recorded at a sweep speed which was fast compared with the membrane time constant, hence the membrane responses look like straight lines. The top trace shows the voltage recorded when no Bridge Balance was used. The response was dominated by the IR voltage drop across the electrode. In the middle trace the Bridge Balance was optimum and in the bottom trace it was slightly overused.

When the Bridge is correctly balanced the resistance of the microelectrode can be read directly from the dial. The sensitivity is $10 \div H$ MΩ per turn.

The Bridge Balance controls operate on the $10.V_m$ output and on the V_2 output. On the $10.V_m$ output the Bridge Balance control saturates when the IR voltage drop exceeds ± 600 mV referred to the input.

Intracellular Balancing

The traces in Fig 2. were all recorded with the electrode inside the cell. Since the electrode response and the oscilloscope sweep speed were fast compared with the membrane time constant (as in Fig. 2B), the correct Bridge Balance setting was easy to see, even through the electrode was inside the cell.

It is sometimes useful to inject a brief small current pulse at the start of each oscilloscope sweep in order to continually check the Bridge Balance setting during the course of an experiment.

Figure 2

Illustration of Bridge balancing technique. All traces were recorded from the $10.V_m$ output. The model cell was 10 MΩ//1 nF. R_e was 10 MΩ.

Recording bandwidth: 30 kHz.

Vertical calibration: 20 mV referred to V_m.

A. Response to +5 nA 10 ms current pulse. Bridge correctly balanced. Trace is membrane response only.

Cal. bar: 20 ms.

B. Response to +5 nA 1 ms pulse.

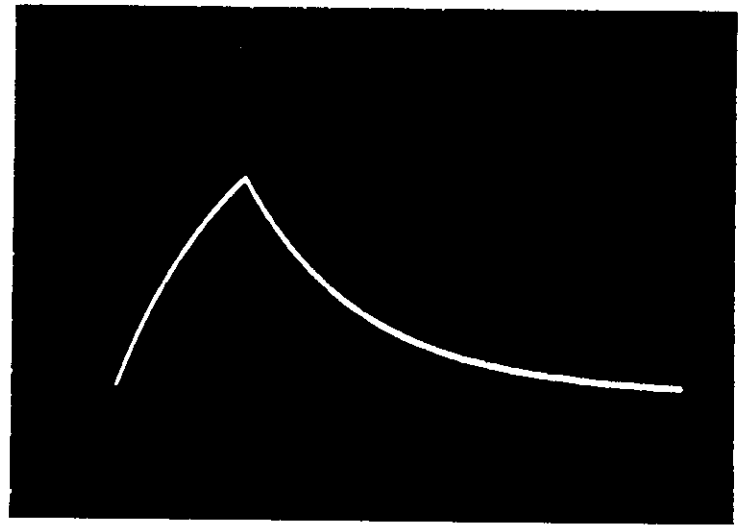
Cal. bar: 1 ms.

Top trace: No Bridge balance used. Fast voltage steps at start and finish of the current pulse are the electrode IR voltage drop.

Middle trace: Bridge correctly balanced. Trace is membrane response only. Transient electrode response remains.

Bottom trace: Bridge balance overused. Negative going step is introduced by the Bridge Balance circuit.

A



B

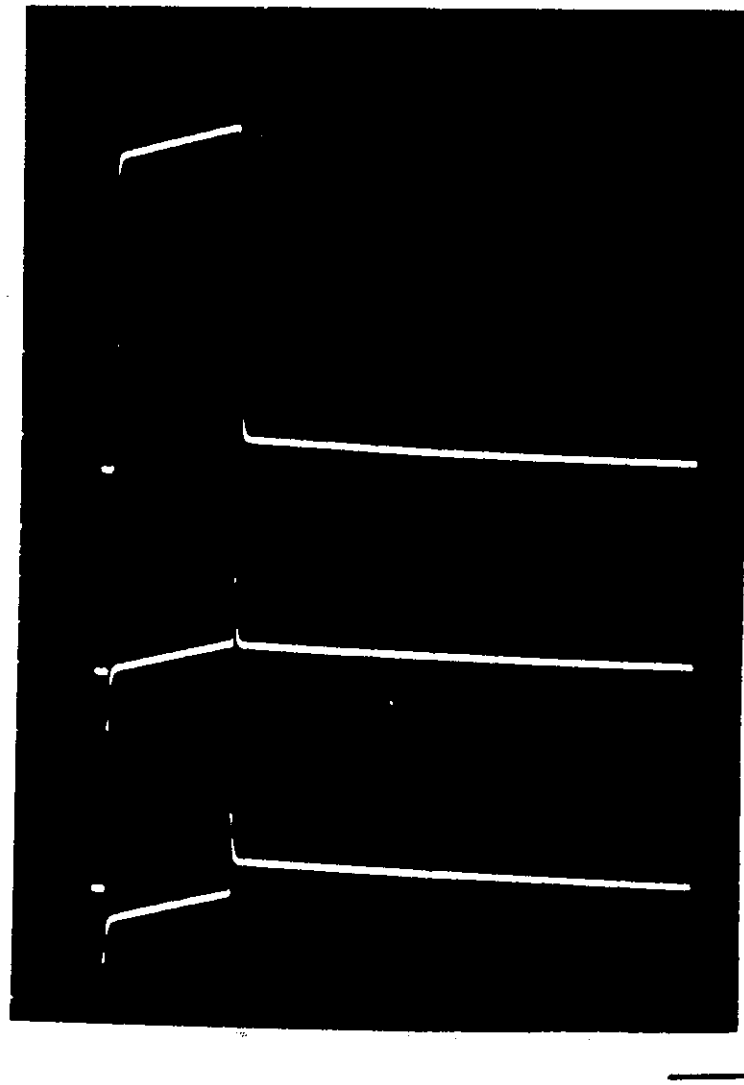


FIGURE 2 - BRIDGE BALANCING PROCEDURE

BUZZ

When the Buzz switch or the footswitch is depressed, the amount of Capacitance Neutralization is increased. If the Capacitance Neutralization control is within a few turns of optimum, this extra compensation causes the headstage to go into high-frequency oscillation. If this is done while the tip of the microelectrode is pressing against the cell membrane the oscillation will often help the microelectrode impale the cell. The exact mechanism is unknown, but it may involve attraction between the charge at the tip of the microelectrode and bound charges on the inside of the membrane.

To use the FS-3 footswitches, plug them into the 4 mm jacks on the back panel. The red jack labelled "+5 V" is shared by the two footswitches. There is one violet jack for each of the two footswitches.

Precise control of the duration of Buzz can be achieved by connecting a pulse generator to pin 15 of the Remote connector (see Remote Section). For some small cells a long duration Buzz can be deadly. In this case it may be helpful to use an external pulse generator connected to pin 15 of the Remote connector to gate the Buzz oscillation so that it is on for just a few milliseconds. The hand-held Remote Buzz generator (see next page) is designed to allow you to conveniently generate Buzz durations between 1 and 50 ms.

It is difficult to interpret the operation of Buzz by watching the $10.V_m$ trace. This is because the x10 gain and lowpass filter on the $10.V_m$ output strongly affect the amount of headstage oscillation seen. As a quick guide, if the $10.V_m$ trace is unaffected then Buzz did not succeed (so increase the Capacitance Neutralization setting). If the $10.V_m$ trace jumps then Buzz was successful.

The Buzz oscillation can be clearly observed on the V_1 Cont. output.

If a grounded shield adds a lot of capacitance to ME2 the Capacitance Neutralization range may be insufficient when an HS-2L headstage is used. In this case it will be necessary to use an HS-2M headstage (see Headstage Section).

Remote Buzz

Installation: Plug the Buzz control into the rear-panel `remote' connector of the Axoclamp.

If you want to use some of the pins on the rear-panel remote connector to remotely select the operating mode or activate the Clear currents, you will have to remove the cover from the plug on the Remote Buzz unit and solder your inputs to the appropriate spare pins on this plug.

Use: Set the desired Buzz duration on the Duration control of the Remote Buzz unit. Press the button corresponding to the electrode you want to buzz. Note that the Duration control is shared by the two electrodes.

For Buzz durations greater than 50 ms, use the buttons on the front panel of the Axoclamp. Neither the buttons on the front panel of the Axoclamp nor the footswitches use the duration set on the Remote Buzz unit.

CALIBRATION SIGNAL

A calibration signal can be simultaneously superimposed on all of the voltage and current outputs (except I_{VIRT}.) for the duration of a HIGH signal on the Cal. Activate input.

For voltage outputs, the magnitude of the Cal. signal is directly equal to the setting of the Step Command thumbwheel switch. For example, +123.4 will put +123.4 mV on the voltage outputs.

For current outputs, the magnitude of the Cal. Signal is 10x the setting of the Step Command thumbwheel switch. For example, -019.6 will put -196 mV on the current outputs. The equivalent current depends on H. In this example, the Cal. signal of -196 mV would correspond to -19.6 nA for H = x1, -1.96 nA for H = x0.1 etc.

Suggested Use

At the start of a recording sequence, briefly activate Cal. After a short interval, activate the Step Command. The Cal signal will be a permanent record of the command voltage or current.

CAPACITANCE NEUTRALIZATION AND INPUT CAPACITANCE

The Capacitance (C_{in}) at the input of the headstage amplifier is due to the capacitance of the amplifier input itself (C_{in1}) plus the capacitance to ground of the microelectrode and any connecting lead (C_{in2}). C_{in} combined with the microelectrode resistance (R_e) acts as a lowpass filter for signals recorded at the tip of the microelectrode. Two techniques may be used to increase the recording bandwidth.

Primary

A special technique is used in the headstages to keep the contribution to C_{in} from the input amplifier as small as possible. This consists of adding the input signal voltage to the power-supply voltages used by the input stages. This technique, known as bootstrapping, fixes the voltage drop across C_{in1} to a constant value thereby preventing current flow through C_{in1}. The effective value of C_{in1} is thus reduced to well below its real value.

Secondary

A commonly used technique known as capacitance neutralization is used to negate C_{in2} and the effective remnant of C_{in1}. The capacitance neutralization circuit attempts to inject into the headstage input a current which it anticipates will be required to charge and discharge C_{in} during signal changes. To use the capacitance neutralization circuit the voltage response to a current step should be observed on an oscilloscope. Advance the capacitance neutralization control as far as is possible without introducing overshoot in the step response. This setting is optimal for current passing and is also optimal for recording potentials at the tip of the microelectrode.

It is important to recognize that the capacitance neutralization circuit is not more than 90% effective even for ideal microelectrodes. This is because of the finite frequency responses of the headstage amplifiers

and the capacitance neutralization circuit, and also because C_{in} does not behave ideally as a linear lumped capacitor. Consequently, the amount of C_{in} that the circuit must neutralize should be kept as small as possible. To this end, **avoid using long lengths of shielded cable to connect the microelectrode to the input. If possible, plug the microelectrode holder directly into the input. Use shallow bathing solutions. Avoid having grounded objects near the electrode. Do not ground the headstage case.**

If metal objects (such as the microscope) must be very near the electrode, they may be disconnected from ground and connected to the gold shield socket in the headstage. This technique can improve the microelectrode response speed. However, it may be that in DCC and dSEVC modes there will be an increase in the amount of switching noise picked up by independent recording electrodes, if used.

See also the section titled Microelectrodes for Fast Settling.

CLEAR

There is one Clear switch for each microelectrode. It is used to pass up to ± 600 x H nA down the microelectrode. "+" and "-" correspond to depolarizing and hyperpolarizing currents respectively. The Clear switch is used for two purposes:

(1) When the microelectrode tip resistance goes high this condition can often be cleared by rapidly toggling the Clear switch from + to -. Because of the large current passed this should only be done extracellularly.

(2) Sometimes microelectrode tips press against the cell membrane but fail to penetrate. A quick flick of the Clear switch will often force the microelectrode to penetrate. Whether to use a hyperpolarizing or depolarizing current depends on the preparation and must be determined by trial and error. Like Buzz, the mechanism for impalement is unknown.

COMMAND GENERATORS

Command levels for voltage clamp or current clamp can be obtained from the internal step command generator, from the internal DC command generators, and from external sources.

Step Command Generator

The Step Command generator can be used either as a current-clamp or voltage-clamp command depending on the position of the Destination switch. If the Destination switch is used to select VC then the magnitude on the thumbwheel switch represents voltage-clamp potential in mV's irrespective of the headstage current gain (H). If the Destination switch is used to select ME1 or ME2 then the magnitude on the thumbwheel switch represents the number of nA of current to be injected down ME1 or ME2 respectively. The current range is scaled by the H. The maximum magnitude on the thumbwheel switch is 199.9. "+" corresponds to depolarizing voltage shifts and currents. "-" corresponds to hyperpolarizing voltage shifts and currents.

The duration for which the Step Command is activated can be made continuous by switching the Ext./Cont./Off toggle to "Cont." or externally determined by a logic HIGH level on the rear-panel Step Activate input. When rotating the thumbwheel switch in continuous mode, be decisive. If the switch is rotated slowly the output will momentarily fall to zero because the switching contacts will pass through an open-circuit state.

DC Command Generators

Separate DC command generators are provided for VC, ME1 and ME2.

The DC command for VC is called "Holding Position." It allows the membrane potential holding position during voltage clamp to be shifted to a value in the range ± 200 mV. It is always operative during voltage clamp. Before the voltage clamp mode is selected, the Holding Position potentiometer is used to set the RMP Balance (see the RMP Balance section). The Holding Position potentiometer is deliberately not calibrated because the exact setting depends on the adequacy of the clamp gain. Instead, the holding position should be read directly from the digital voltmeter displaying V_m. A ten-turn locking dial is used so that once set, the Holding Position potentiometer can be locked to prevent accidental changes.

The ME1 and ME2 DC commands are called "DC Current Command." Each is controlled by a precision ten-turn dial and can be switched by a toggle switch from depolarizing (+) to hyperpolarizing (-) or off (OFF). An LED illuminates whenever the toggle switch is in the + or - position. It also illuminates if the Destination switch is turned to the microelectrode in question and the Step Command generator is activated either by the Ext./Cont. switch or by a logic HIGH level on the Step Activate input. The current is scaled by the H. If the Step Command and the DC Current Command are used simultaneously, the total command is their sum.

External Command Inputs

Three external command inputs are provided. These are for setting the voltage-clamp command (Ext. VC Command), the current-clamp command in ME1 (Ext. ME1 Command), and the current-clamp command in ME2 (Ext. ME2 Command). These inputs are active simultaneously with the internal command generators and do not depend on the position of the Destination switch. The sensitivity of Ext. VC Command is 20 mV/V. The sensitivity of the Ext. ME1/ME2 Command is 10 x H nA/V.

The external command inputs are DC connected. Therefore, when using the Ext. ME1 and ME2 Command inputs any deviation from zero volts of the external signal source while it is in its "off" state will cause a DC current to flow in the electrode.

This can be avoided by using:

(1) A very high-quality external source which puts out a true zero voltage level in its off state or which can be trimmed to do so.

(2) An isolated external source.

Mixing Commands

Complex command waveforms can be generated by appropriately mixing the Step Command, the DC Command and the Ext. Command. For example, the command waveform in Fig. 3 can be used to establish the current injected into ME1 by setting the Destination switch to the ME1 position and using the ME1 DC Command and the Ext. ME1 Command input.

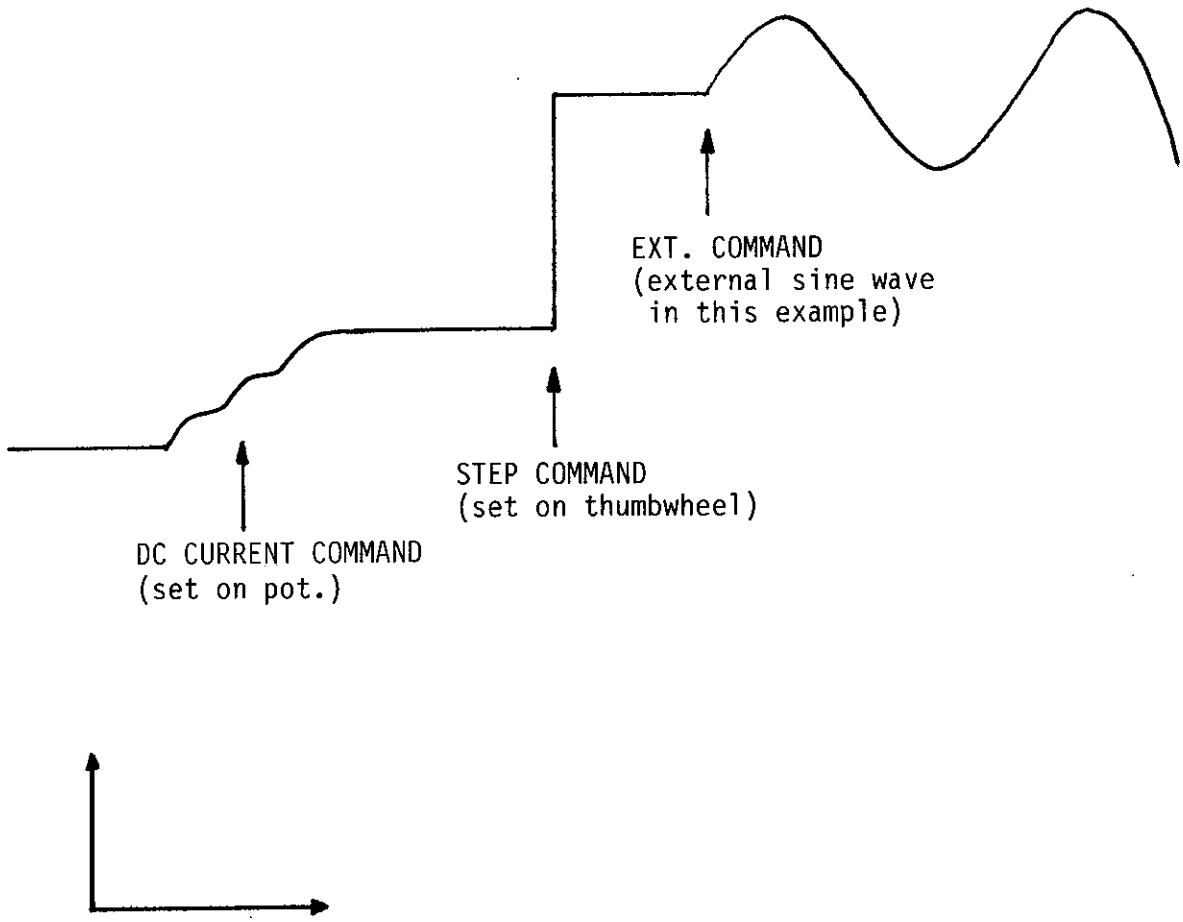


FIGURE 3 - SUMMATION OF COMMANDS

This figure shows the command potential that would result if all command sources were switched on one at a time and left on.

CURRENT MEASUREMENT

The current injected down each microelectrode is independently measured. The measurement is true. Thus if the electrode blocks the measured current falls to zero even though a current command may exist.

Two current outputs apply to ME1. I_m is the membrane current while I_1 Cont. is the instantaneous current in ME1. In continuous modes (Bridge, cSEVC and even TEVC) I_m and I_1 Cont. are identical. However, in discontinuous modes (i.e. DCC and dSEVC) I_m and I_1 Cont. are different. I_1 Cont. switches from zero to some finite value at the sample rate. This is because for 30% of each period ME1 is used for passing current while for the remaining 70% of each period no current is passed and the IR drop due to the previous current is allowed to passively decay (see DCC and cSEVC sections). On the other hand, I_m is the true membrane current. It is recovered from the instantaneous electrode current by a circuit which samples the current pulses, retains the samples during the passive-decay period, then scales the samples to yield the average current for the whole period. The I_m output is smoothed by the output filter (see the Output Filter section).

The current in ME2 is labelled I_2.

The gain of the current measurement circuits depends on the headstage current gain (H). It is $10 \div H$ mV/nA.

The whole current into the bath can be separately measured using a virtual-ground headstage. (See the Virtual Ground section.)

DCC MODE

Description

In Discontinuous Current Clamp (DCC) mode ME1 is cyclically used to pass current. The voltage recorded at the tip of ME1 is memorized by a sample-and-hold circuit inbetween each current-passing period after all transient voltages due to current passing have decayed. Thus the membrane potential can be recorded independently of IR voltage drops across the electrode. The advantage of DCC mode compared with Bridge mode is that it is tolerant of small changes in microelectrode resistance. The disadvantage is that DCC mode is noisier than Bridge mode. During DCC mode ME2 can be used for continuous current passing.

The principles of operation are outlined in the block diagram and timing diagram of Fig. 4, and in the following discussion.

The voltage recorded by the microelectrode (V_1) is buffered by a unity-gain head stage (A1). To begin the discussion assume that V_1 is exactly equal to the instantaneous membrane potential (V_m). Switch S2 briefly closes thereby enabling the voltage on the holding capacitor (C_H) to charge up to the value of V_m. S2 opens again after the "sample" period and V_m is held by C_H. A buffer amplifier (A2) interfaces C_H to the recording apparatus. This switch, capacitor and buffer amplifier arrangement constitute an analog memory known as a sample-and-hold amplifier.

Immediately after the sample period, the current injection period begins when switch S1 changes over from the 0 volts position to the current-command voltage (V_c) position. This connects V_c to a differential amplifier (A4) arranged so that its output is $V_1 + V_c$. The voltage appearing across R_o is exactly equal to V_c thereby forcing the current (I_o) into the microelectrode to be equal to V_c/R_o. Amplifiers A4 and A1 and resistor R_o constitute a controlled-current source (CCS) which injects a current into the microelectrode directly proportional to the voltage at the input of the CCS irrespective of the resistance of the microelectrode or the voltage at its tip.

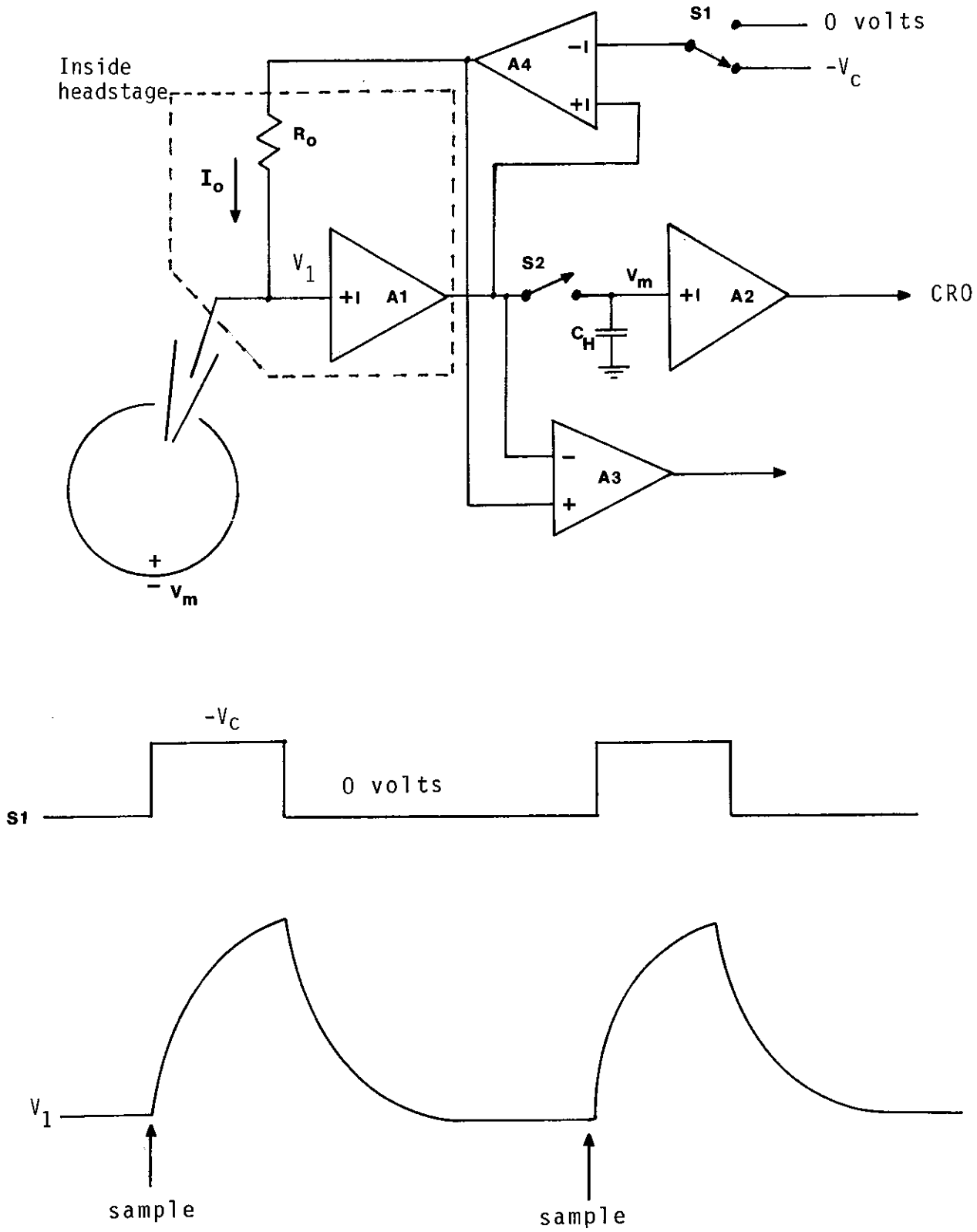


FIGURE 4 - DCC MODE BLOCK DIAGRAM AND TIMING DIAGRAM

During the current-injection period a square pulse of current proportional to V_c is injected into the electrode. Because of this current V_1 rises. The rate of rise of V_1 is limited by the parasitic effects of capacitance through the wall of the glass microelectrode to the solution, and capacitance at the input of the buffer amplifier. The final value of V_1 reached consists mostly of the IR voltage drop across the micro-electrode resistance. Only a tiny fraction of V_1 consists of the membrane potential recorded at the tip.

After 30% of one cycle has elapsed, the voltage-recording period begins when S1 changes over to the 0 volts position. Passive decay occurs because the input of the CCS is 0 volts and thus its output current is zero. Sufficient time must be allowed during the voltage-recording period for V_1 to decay to within a millivolt or less of V_m. At the end of the passive decay period S2 is again briefly closed and a new sample of V_m is taken to begin a new cycle.

The actual voltage used for recording purposes is the sampled voltage. The sampled membrane potential is connected to the $10.V_m$ output. The V_1 Cont. output is the instantaneous electrode voltage.

The instantaneous current into the microelectrode is monitored by a differential amplifier (A3). The output of A3 is taken to an averager (not shown) which samples, smooths and scales the current pulses and connects the average value to the I_m output.

During DCC mode the input to the CCS and the output of the ME1 current monitor are automatically scaled so that they represent the true membrane current even though the instantaneous current flows for only 30% of the time.

The cycling (sampling) rate must be chosen so that there are ten or more cycles per membrane time constant. This enables the membrane capacitance to smooth the membrane voltage response to the current pulses.

Suggested Use

Turn the Anti-Alias Filter to the minimum value and switch to DCC mode. Set the Destination switch to ME1 and set up a repetitive square current command. Observe I_m and $10.V_m$ on the main oscilloscope. Observe the voltage at the Monitor output on a second oscilloscope (which need not be a high quality type) with the gain at 100 mV/div (= 10 mV/div input referred). Trigger this oscilloscope from the Sample Clock output on the rear panel.

Proceed to adjust the Capacitance Neutralization in one of two 1

A. For acceptable but not optimum Capacitance Neutralization, advance the Capacitance Neutralization control until the square step at the leading edge of the $10.V_m$ response is first eliminated.

B. For optimum Capacitance Neutralization, switch the Step Command generator to continuous. Advance the Capacitance Neutralization control until the Monitor waveform decays most rapidly to a horizontal baseline, but without any overshoot.

These techniques are illustrated in Fig. 5. The traces in Fig. 5A show that poorly adjusted Capacitance Neutralization during DCC mode is similar to poorly adjusted Bridge Balance during Bridge mode.

If the square step cannot be eliminated (without overshoot on the Monitor waveform), decrease the sample rate (f_s).

Set the Output Bandwidth to 1/5 or less of f_s.

Reduce the noise on the $10.V_m$ and I_m traces either by advancing the Anti-Alias Filter or by increasing f_s, adjusting the capacitance neutralization where necessary.

Figure 5

Illustration of Capacitance Neutralization adjustment during DCC. All traces were recorded with a model cell
10 MΩ//1 nF. R_e was 10 MΩ. Cycling rate was 25 kHz.

A. 10.V_m output. Response to a 10 nA 1 ms current pulse.
Vertical calibration: 20 mV referred to V_m.
Horizontal calibration: 1 ms.

B. V_{mon} output during the 10 nA current pulse.
Vertical calibration: 40 mV referred to V_m.
Horizontal calibration: 10 μs.

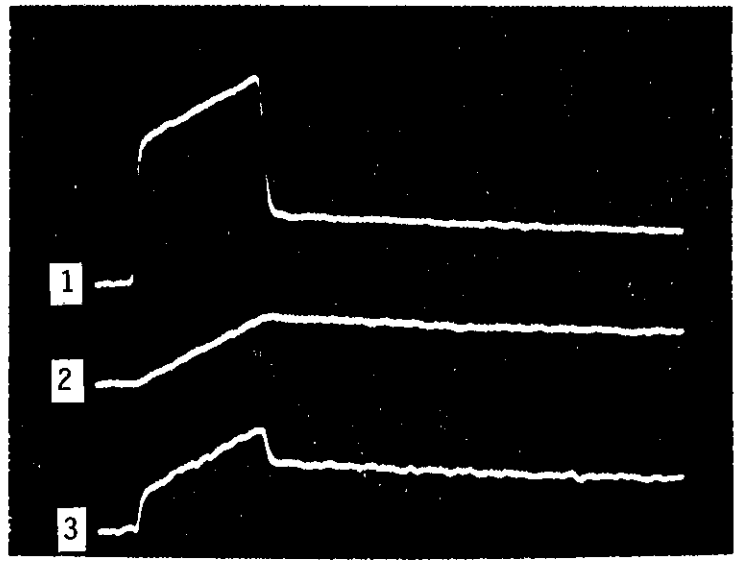
There are three pairs of corresponding traces.

Traces 1: Capacitance neutralization underutilized. There was a fast step in V_m at the start and finish of the current pulse because V_{mon} decayed too slowly to reach its final value.

Traces 2: Capacitance neutralization optimum. V_m shows the membrane response only. V_{mon} decay was fast with no overshoot and easily reached the final value.

Traces 3: Capacitance neutralization overutilized. The fast steps in V_m reappeared, this time because of overshoot and ringing in V_{mon}. Note that unlike a Bridge circuit, the effect of two much compensation can put either a positive or a negative step on V_m (positive in this example) depending on which cycle of the ringing in V_{mon} is sampled.

A



B

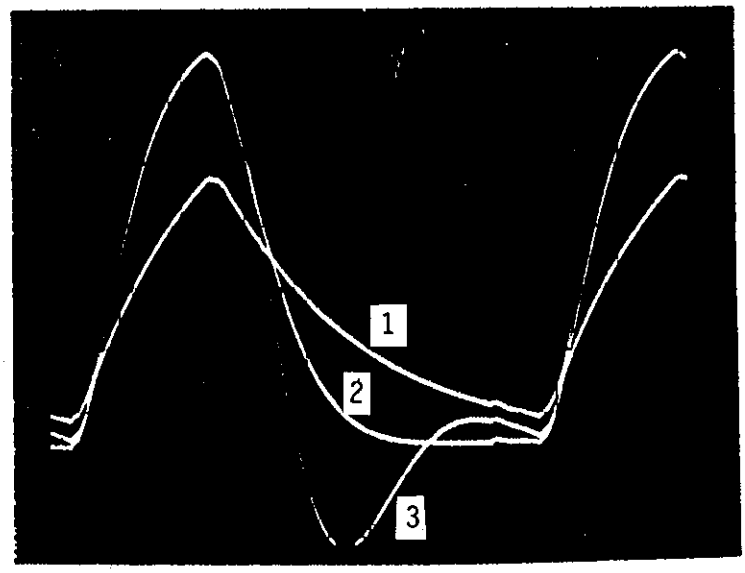


FIGURE 5 - HOW TO SET THE CAPACITANCE NEUTRALIZATION DURING DCC MODE

GROUNDING AND HUM

A perennial bane of electrophysiology is line-frequency pickup (noise), often referred to as hum. Hum can occur not only at the mains frequency but also at multiples of it.

The AXOCLAMP-2A has inherently low hum levels (less than 20 μV peak-to-peak). To take advantage of these low levels great care must be taken when integrating the AXOCLAMP-2A into a complete recording system. The following procedures should be followed.

(1) **Only ground the preparation bath by directly connecting it to the yellow ground connector on the back of the ME1 headstage (or to a virtual-ground headstage if used).**

(2) Place the AXOCLAMP-2A in a position in the rack where transformers in adjacent equipment are unlikely to radiate into its electronics. The most sensitive part of the electronics is the right hand side looking from the front. A thick sheet of steel placed between the AXOCLAMP-2A and the radiating equipment can effectively reduce the induced hum.

(3) Initially make only one connection to the AXOCLAMP-2A. This should be to the oscilloscope from the V_1 or $10.V_m$ outputs. Ground the ME1 headstage input through a 1 MΩ resistor to the yellow ground connector. After verifying that the hum levels are low, start increasing the complexity of the connections one lead at a time. Leads should not be draped near transformers which are inside other equipment. In desperate circumstances the continuity of the shield on an offending coaxial cable can be broken.

(4) Try grounding auxiliary equipment from a ground distribution buss. This buss should be connected to the AXOCLAMP-2A via the yellow 0.16 inch (4 mm) socket on the rear panel. This socket is connected to the AXOCLAMP-2A's signal ground (i.e. the outer conductors of all the BNC connectors). The signal ground in the AXOCLAMP-2A is isolated from the chassis and power ground.

(5) If more than one headstage is used, all the headstage cables should run from the AXOCLAMP-2A to the preparation in a bundle. The bundle can be formed either by gently twisting the cables together or by loosely tying them together.

(6) Experiment. While hum can be explained in theory (e.g. direct pickup, earth loops), in practice the ultimate theory is the end result. Following the rules above is the best start. The final hum level can often be kept to less than 100 μV peak-to-peak referred to V_m. One technique that should **not** be used to reduce the hum is the delicate placement of cables so that a number of competing hum sources cancel out. Such a procedure is too prone to accidental alteration.

HEADSTAGES

The HS-2 unity gain headstage buffers the high impedance of the microelectrode, making the potential recorded by the microelectrode available to the rest of the circuitry. It also provides the means for injecting current into the microelectrode and for neutralizing the input capacitance.

The Meaning Of H

A precision resistor (Ro in Fig.4) inside the headstage sets the headstage current gain (H). Choosing the H depends on the cell to be clamped (see below). The particular value of H used affects the Bridge Balance range, the sensitivity to current commands, the sensitivity of the current monitors and the gain in SEVC mode. The effects are clearly marked on the front and rear panels, and since they always appear in multiples of 10 they are easy to calculate. For your convenience, Table 1 summarizes these effects. Note that voltage commands during voltage clamp are not affected.

Which Headstage To Use

The H value required depends on the typical input resistances (R_{in}) of your cells. The recommended values are in Table 2.

TABLE 1

How H affects control and measurement ranges

H[1]	x10	x1	x0.1
R_o	1 MΩ	10 MΩ	100 MΩ
Max. Bridge Balance	10 MΩ	100 MΩ	1000 MΩ
Max. Step Command	±1999 nA	±199.9 nA	±19.99 nA
Max. DC Current Command	±1000 nA	±100 nA	±10 nA
Ext. Command	100 nA	10 nA/V	1 nA/V
Max Total Current[2]	6000 nA	600 nA	60 nA
I Output	1 mV/nA	10 mV/nA	100 mV/nA
Max. Gain in dSEVC	1000 nA/mV	100 nA/mV	10 nA/mV
Max. Gain in cSEVC	10000 nA/mV	1000 nA/mV	100 nA/mV
Max. Gain in TEVC	10000	10000	10000

(1) For H = x0.01 replace MΩ by GΩ, nA by pA in x10 column
For H = x0.0001 replace MΩ by GΩ, nA by pA in x0.1 column
For H = x100 replace MΩ by kΩ, nA by μA in x0.1 column

(2) Measured with electrode resistance $R_e = R_o$

TABLE 2

Recommended H values for various cell input resistances

H	=	x10	for	300 kΩ <	R_{in}	<	3 MΩ
H	=	x1	for	3 MΩ <	R_{in}	<	30 MΩ
H	=	x0.1	for	30 MΩ <	R_{in}	<	300 MΩ
H	=	x0.01	for		R_{in}	>	300 MΩ
H	=	x0.0001	for		ion-sensitive electrodes		

Some overlap in these recommendations is allowable. The guiding principles are these:

(1) For maximum sampling rates in dSEVC and DCC modes use the **largest** feasible H value. (This is because the current-passing response is best with **low** values of R_o.)

(2) A limitation on using large H values is that as R_o becomes smaller the input leakage current of the headstage becomes more prone to increase with time and temperature (see Input Leakage Current discussion later in this section).

(3) A further limitation on using large H values is that if R_o (see Table 1) is less than the microelectrode resistance (R_e) the high-frequency noise is worse.

(4) The H sets the current-passing sensitivity in Bridge and DCC modes and the Gain in SEVC modes. Hence it should be chosen for sensitivities suitable for your cell. These sensitivities are listed in Table 1 above.

(5) If $R_e >> R_{in}$ a smaller H value should be favored.

Capacitance Neutralization Range

HS-2 Series headstages are available with L or M suffixes representing low and medium ranges respectively of Capacitance Neutralization (see Table 3). The increased Capacitance Neutralization range is a trade-off against microelectrode noise. The HS-2L has the lowest noise close to the theoretically predicted thermal noise of the electrode. The HS-2M has about 25% extra noise.

TABLE 3

	HS-2L	HS-2M
Cap Neut Range:		
in ME1 Slot	-1 to 4 pF	-2 to 12 pF
in ME2 Slot	-1 to 11 pF	-2 to 35 pF

Headstage Connectors

There are three teflon-insulated 2 mm (0.08 inch) sockets in the headstage (see diagram). These are standard-diameter sockets.

1. Microelectrode Input Connector

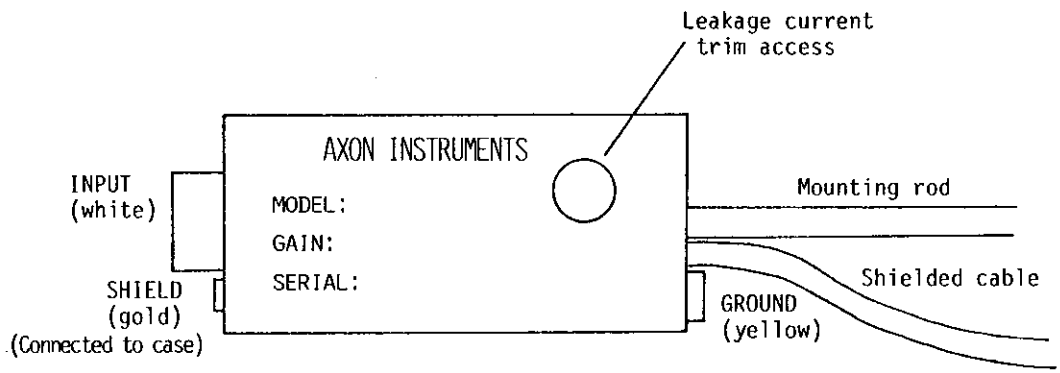
The red socket is the microelectrode input. The connection between the microelectrode and this socket should be kept as short as possible. Some excellent methods are:

(i) Solder a silver/silver-chloride wire directly to one of the 2 mm plugs supplied. Use the wire to connect to the microelectrode which can be supported on a separate mounting.

(ii) For greater mechanical stability, use an HL-2 series microelectrode holder from Axon Instruments.

(iii) Plug a standard microelectrode holder (2 mm plug) directly into the input socket. The teflon input socket should allow enough clearance for most standard holders.

(iv) Use a BNC-type microelectrode holder. This requires an HLB-2 adaptor from Axon Instruments.



Notes

"Model" may be HS-2L, HS-2M or HS-4M

"Gain" refers to headstage current gain (H)

HS-2 and HS-4 HEADSTAGE CONNECTION DIAGRAM

2. Shield Drive Connector

The Shield drive is connected to the gold-plated guard socket and to the case of the HS-2 x1L, x0.1L, x0.01M and x0.0001M headstages. This drive is protected against continuous short circuits, however for best frequency response **the case must not be grounded.** In general, this necessitates using an insulated mounting for the headstage (such as the rod provided).

The shield connection is provided primarily for driving the shield of microelectrodes prepared for deep immersion (see notes in Microelectrodes for Fast Settling section). It may also be used for driving metal objects near the input, or even the hutch in which the preparation is housed. It can be used for driving the shield of a coaxial cable used to connect the microelectrode to the input, although it is not recommended that the microelectrode be connected in this way. If not used, the shield socket is simply left unconnected.

There are two reasons why we do not recommend using shielded cable to connect the microelectrode to the headstage. (1) The leakage resistance of shielded cable can degrade the input resistance when used with ion-sensitive and other high-impedance electrodes. If shielded cable is used it should have teflon as the insulating material separating the shield and the inner conductor. (2) Shielded cables add significant input capacitance. The shield drive circuit mostly removes the effect of this capacitance on electrode response speed. However, from a noise point of view the capacitance remains and causes an increase in high-frequency electrode noise.

To optimize the response speed of low and medium impedance electrodes (up to approx. 300 MΩ) when a driven shield is used, the shield of headstages with H = x0.1 and larger is driven from the capacitance neutralization circuit. To optimize the headstage input resistance when a driven shield is used, the shield of headstages with H = x0.01 and smaller is driven from the output of the unity gain buffer inside the headstage.

If a shielded cable is being used and unusual electrode responses are observed, try disconnecting the shield.

No shield drive is provided on the HS-2 x1MG, x10MG and the HS-4 x1MG. On these headstages the case is grounded. This is because they are primarily used for current passing in a two-electrode voltage clamp (TEVC). In TEVC, it is essential to minimize the amount of coupling capacitance between the voltage-recording electrode and the current-passing electrode. This coupling can be minimized most conveniently if the case of the current-passing headstage is grounded.

3. Ground Output Connector

The yellow ground socket of the ME1 headstage is used for grounding the preparation. Using this connection as the preparation ground minimizes hum.

Tip Potentials - Detection

During the passage of current the tip potentials of many electrodes change. Changes in tip potential are indistinguishable from the membrane potential and can therefore represent a serious source of error. To prevent this error the following checks should be made.

(1) While the microelectrode is outside the cell, set the offset to zero. In bridge or DCC mode pass a constant current into the bath for about 10 seconds. The current magnitude should be the same as the maximum sustained current likely to be passed during the experiment. When the current is switched off the recorded potential should return to zero within a few milliseconds at most. Some electrodes either return very slowly to zero potential, or not at all. These electrodes should be discarded.

(2) Once the experiment is in progress occasionally check the resistance of the microelectrode. Changes in tip potential are usually accompanied by changes in electrode resistance.

Note that the tip potential changes described in this section are happening with a slower time course than the ones described in the Anti-Aliasing section. The causes of these slow changes in tip potential are unknown.

Tip Potentials - Prevention

Not much can be done to prevent tip potentials from changing but the following may be helpful.

(1) Sometimes the slow changes in tip potentials are worse when standard microelectrode holders with an embedded AgCl pellet are used instead of an Ag/AgCl wire. Some holders are all right while other ostensibly identical holders are not. Therefore holders should be tested and selected.

The variability of the tip potentials may in some way be related to pressure developed when the microelectrode is pressed into the holder. A narrow hole drilled into the side of the holder to relieve pressure might help.

(2) Using filling solutions with low pH, or adding small concentrations of polyvalent cations like Th^{4+}, may reduce the size of the tip potential (Purves, 1981) and therefore the magnitude of any changes.

Interchangeability

Any unity-gain headstage in the HS-2 series can be used for ME1 or ME2. The equipment will not be damaged if headstages are exchanged while the AXOCLAMP-2A is switched on.

Cleaning

To clean salt spills from the input connectors wipe with a damp cloth. Avoid spilling liquids on the headstage.

Input Leakage Current And How To Trim It To Zero

All DC-connected systems suffer from the problem of drift. With changes in temperature and the passage of time the DC transfer functions of all semiconductor devices can drift by many millivolts away from their initial values. The major worry in a microelectrode system is that the cumulative effects of drift in various parts of the circuit may lead to the development of a DC offset across the resistor (R_o) used to set the H. As a result, an undesirable DC leakage current is injected into the microelectrode.

Careful consideration to this problem has been applied throughout the design of the AXOCLAMP-2A and the overall DC offset has been made as insensitive as possible to the drift in the integrated circuits. As well, special low-drift integrated circuits have been used in all critical positions. The magnitude of the DC leakage current increases with increases in H. This normally introduces no greater error in the DC offset voltage developed across the microelectrode or the cell membrane because larger Hs are usually used with lower-resistance cells and microelectrodes.

Before leaving the factory, the DC offset voltage of each HS-2 headstage is trimmed so that the input leakage current is no more than:

100	pA	for	H	=	x10
10	pA	for	H	=	x1
1	pA	for	H	=	x0.1
1	pA	for	H	=	x0.01
10	fA	for	H	=	x0.0001

These input current levels are very low and cause negligible shifts in the cell membrane potential when the headstages are used with the recommended ranges of cell input resistances (see Table 2). (The shift in V_m is calculated from input current x R_{in}.)

If you ever suspect that the input current has grown to a level where V_m is significantly affected, it can be re-adjusted by the following procedure.

(1) Switch off all current commands and disconnect any external current commands.

(2) Remove the plastic cap from the access hole in the headstage cover.

(3) Ground the headstage input via a resistor equal to $R_o \div 10$ (where R_o is given in Table 1). On an oscilloscope at 2 mV/div observe the $10V_m$ output through the filter set to 100 Hz. Use the Offset control to center the trace on the screen.

(4) Now ground the headstage input via a resistor equal to R_o(1) in Table 1. Observe the shift of the oscilloscope trace.

(5) Repetitively swap from grounding via $R_o \div 10$ to grounding via R_o. Adjust the trim pot inside the headstage until there is no shift.

Note 1. For values of 1 GΩ or more it is important to clean the surface of the resistor thoroughly to remove leakage pathways.

Depending on the reason for a trim being necessary, the trim procedure may have to be repeated if the headstage is changed.

Warning

If an external source is connected to the Ext. ME1 and ME2 Command input, any time the source is non-zero a proportional current will flow in the microelectrode. Many external sources do not put out a true zero voltage when in the "off" state, thus there may be an unwanted electrode current due to the fact that an external source is connected. To avoid this, use an external source in which you can adjust the off-state voltage, or use an isolated external source.

DC Removal

One potential source of a small but variable input leakage current is due to DC current flow through the dielectric of the capacitor (C_n) used for capacitance neutralization. For example, the electrode potential might be 200 mV (though the experimenter does not see this potential because of the offset compensation). To compensate several pF of input capacitance the gain of the capacitance neutralization circuit might be 2. Thus 400 mV would be fed back to C_n resulting in 200 mV across it. If the dielectric resistance of C_n were 10^{11} Ω (the guaranteed minimum of high-quality capacitors) there would be 2 pA flowing through the capacitor.

To eliminate this source of leakage current a DC removal circuit removes the DC voltage from across C_n. The DC removal circuit operates with a 1 s or 10 s time constant. There may be a transient shift in the electrode voltage while the Capacitance Neutralization control is being adjusted. The DC voltage is also removed from the shield drive.

Input Resistance

The input resistance of the headstages is predommantly related to R_o. A circuit inside the AXOCLAMP called a constant current source (CCS) controls the voltage across R_o. Ideally, the voltage across R_o is independent of the electrode voltage. The accuracy of the CCS in controlling the voltage across R_o is preset at the factory. Extremely stable components are used in the CCS so that the accuracy will not deteriorate with time. In general the CCS is effective to one part in 10^4 so that the input resistance is 10^4R_o.

Other possible factors which would decrease the input resistance are minimized. For example, the field effect transistor (FET) input of the headstage is referenced to the input voltage rather than to ground. This technique is known as bootstrapping. Thus the effective resistance of the input is much greater than the already high resistance of the FET. Leakage current and resistive loading through the insulation of the input socket are minimized by using Teflon insulation and by driving the case with the DC input voltage.

HOLDERS

Features

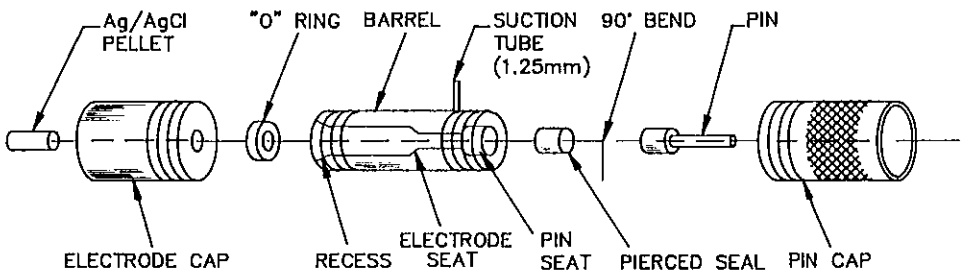
The HL-2 series holders have been designed for low-noise mechanically stable microelectrode recordings with or without suction. The body of the holders are made out of polycarbonate for lowest noise and easy cleaning. Maintenance is simple because the holder can be fully disassembled for cleaning and parts replacement.

Mechanical stability of the electrode is assured several ways. For example, as the electrode cap is closed, the 'O' ring is forced into a special recess and pulls the electrode firmly back into the holder so that its end presses tightly against the electrode seat. The holder mates firmly with the special teflon connectors on the HS-2, HS-4 and VG-2 series headstages. A 2 mm diameter pin is used for the electrical connection.

The holders are designed to emerge along the long axis of the headstage. A right-angle adapter can be purchased if it is necessary for the holder to emerge at 90° from the headstage. A BNC-to-Axon adaptor (HLB-2) can be purchased if you wish to use third-pary BNC-style holders.

Parts

The various parts of the holders are shown in the exploded view:



Five spare 'O' rings and one spare pierced seal are provided with each holder. Additional 'O' rings, pierced seals, pins and Ag/AgCl pellet assemblies can be purchased from Axon Instruments.

HL-2-12 holders use a plain Ag wire and 'O' rings with a 1.2 mm hole. HL-2-17 holders use a Ag/AgCl pellet assembly and 'O' rings with a 1.7 mm hole.

To replace the silver wire, insert the nonchlorided end through the hole of the pierced seal and bend the last 1 mm over to an angle of 90°. Press the pierced seal and the wire into the pin seat. Push the large end of the pin down onto the bent-over wire and into the pin seat. This assures good electrical contact. Screw the pin cap down firmly but without excessive force.

Use

Insertion of electrode

Make sure the electrode cap is loosened so that pressure on the 'O' ring is relieved, but do not remove the electrode cap. Push the back end of the electrode through the electrode cap and `O' ring until it presses against the electrode seat. Gently tighten the electrode cap so that the electrode is gripped firmly.

To minimize cutting of the 'O' ring by the sharp back end of the electrode, you can smooth the electrode edges by rotating the back end of the electrode in a bunsen burner flame.

Cleaning

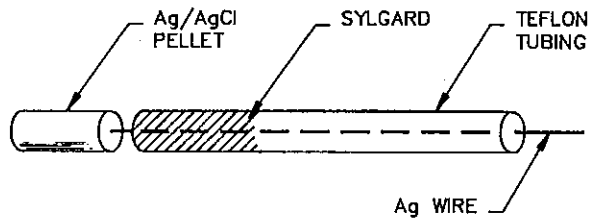
For lowest noise, keep the holder clean. Frequently rinse the holder with distilled water. If heavier cleaning is required, briefly wash in ethanol or mild soapy water. Never use methanol or strong solvents.

Filling electrodes

Only the taper and a few millimeters of the shaft of the electrode should be filled with solution. The chlorided tip of the wire should be inserted into this solution. Avoid wetting the holder since this will increase the noise.

Silver Chloriding

The HL-2-17 holders are supplied with a Ag/AgCl pellet that should give you many months of DC-stable recordings. The silver wire is surrounded by a Sylgard-sealed teflon tube. This ensures that the electrode solution only contacts the Ag/AgCl pellet.



It is not practical to make a pellet small enough to fit inside the shaft of the narrow glass electrodes used in the and HL-2-12 holders, therefore these holders are supplied with a piece of 0.25 mm silver wire. It is up to you to chloride the end of this wire as required. Chloriding procedures are contained in many electrophysiology texts (e.g. Purves, 1981). Typically the chlorided wire will need to be replaced every few weeks.

Heat smoothing the back end of the electrode extends the life of the chloride coating by minimizing the amount of scratch damage. Another way to protect the AgCl coating is to slip a perforated teflon tube over the chlorided region.

The chlorided region should be long enough so that the electrode solution does not come in contact with the bare silver wire.

Glass Dimensions

Use the HL-2-12 holders for glass from 1.0 to 1.2 mm outside diameter (OD). The optimal dimensions are 1.15 mm OD and >0.5 mm ID.

Use the HL-2-17 holders for glass from 1.5 to 1.7 mm outside diameter (OD). The optimal dimensions are 1.65 mm OD and >1.1 mm ID.

For other glass dimensions you can drill out the bore of the HL-2-12 holder.

IONOPHORESIS

When ME2 is not used for intracellular penetrations it can be used for ionophoresis. To set the retaining and pulse currents:

(1) Set the desired retaining current on the ME2 DC Current Command control.

(2) Switch the Destination switch to ME2. Set the Step Command equal to the desired pulse current **minus** the retaining current.

or Connect a pulse generator to the Ext. ME2 Command input to set the desired pulse current **minus** the retaining current.

e.g. For retaining current = -5 nA, ejection current = 40 nA.
Set ME2 DC Current Command = -5 nA, Step Command (or Ext. ME2 Command) = 45 nA.

Use a headstage with the appropriate H. x1 is generally useful.

LINK-UP

When the AXOCLAMP-2A is used in dSEVC and DCC modes the voltage across the microelectrode rapidly switches up and down. To an extent which depends on proximity, a second microelectrode used in the same preparation will pick up some switching noise.

If the second electrode is used in a continuous mode the picked up noise can usually be removed by a lowpass filter.

If the second electrode is also used in a discontinuous mode (e.g. when two interconnected cells in the same preparation are placed under dSEVC) the pick-up from one to the other can become a problem. The two switching signals mix and a beat frequency signal appears at the difference frequency. When both electrodes are switched at similar frequencies the beat frequency signal appears at a low frequency which cannot be filtered out. Worse, in an effort to clamp out the beat signal the clamping circuit passes beat-frequency currents into the cell.

There are two ways to avoid this problem.

(1) Place an extensive grounded shield between the two electrodes. This method has disadvantages. The shield may be physically difficult to arrange, and it may introduce sufficient capacitance at the headstage inputs to worsen the electrode performances.

(2) Use the Clock Link-Up facility provided with each AXOCLAMP-2A to synchronize their sampling clocks. A 15-pin connector on the rear panel enables the sampling clock circuits of two AXOCLAMP-2As to be linked by a cable. One AXOCLAMP-2A becomes the Master and the other the Slave (which is which is determined by the orientation of the cable).

After Link-up, whenever both AXOCLAMP-2As are in DCC or dSEVC modes, the Slave's sampling clock is overridden by the Master's. In all other combinations of operating modes the two AXOCLAMP-2As remain fully independent. For example, if the Slave is in DCC or dSEVC modes but the Master is in neither, the Slave's sampling clock is re-enabled.

By forcing both AXOCLAMP-2As to sample synchronously the beat frequency problem is eliminated. At the instant that both AXOCLAMP-2As sample their electrode voltages there will be no pick-up from one electrode to the other because the voltages across both electrodes must have decayed to near zero in order for the clamps to operate.

Clock Link-Up only affects the sampling clocks. All other functions of the two AXOCLAMP-2As remain fully independent.

MICROELECTRODES FOR FAST SETTLING

The key to discontinuous voltage and current clamping with a single microelectrode is the character of the microelectrode itself. The microelectrode voltage must settle rapidly after a current pulse, and the microelectrode must be able to pass current without large changes in resistance.

Microelectrode Capacitance

To get fast settling it is essential to minimize the transmural capacitance (C_t) from the inside of the microelectrode to the external solution. C_t is usually 1-2 pF per mm of immersion. Two applications requiring different approaches are discussed here.

Target Cell Near Surface Of Solution.

In an isolated preparation, C_t can be reduced by lowering the surface of the solution as far as possible (see note below). Precautions must be taken to prevent surface tension effects from drawing a thin layer of solution up the outer wall of the microelectrode. If this film of saline is allowed to develop, C_t will be much worse that otherwise. Because the film of saline has axial resistance the contribution to C_t will be very nonlinear, and the voltage decay after a current pulse will either be biphasic (as in Fig. 1), or if it is monophasic it will not be very fast even when capacitance neutralization is used. To prevent the saline film from developing, the electrode should be coated with a hydrophobic material. This can be done just before use by dipping the **filled** microelectrode into a fluid such as silicone oil or mineral oil. Another method is to coat the electrode with Sylgard (Hamill et al., 1981).

Sylgard or Q-dope (airplane glue) can also be used to build up the wall thickness of the electrode thereby reducing C_t. The selected material should be painted onto the electrode to within 100 μm of the tip.

Note: For a long slender microelectrode we regard 200 μm or less as a low solution level. 500 μm is tolerable. 1 mm or more is regarded as deep. For a microelectrode which tapers steeply (i.e. a stubby microelectrode) deeper solutions can be used with less loss of performance. When working with very low solution levels there is a risk of evaporation exposing the cells to the air unless a continuous flow of solution is provided across or through the preparation. If evaporation is a problem one way to overcome it is to float a layer of mineral oil on the surface of the solution. If used, this layer of oil will have the additional advantage of automatically coating the electrode as it is lowered into the solution.

Target Cell Deep In Solution.

In some preparations, e.g., in vivo CNS, the target cell is several millimeters below the surface of the solution. In this case the more difficult procedure of guarding the electrodes may have to be used. This involves coating the outside of the microelectrode with a metal layer and connecting this layer to the case socket of the unity-gain headstage. Depending upon H the case socket is either connected to the capacitance neutralization circuit or to the unity-gain output. The guarding procedure does not reduce C_t. Instead, it reduces the effect of C_t by controlling the voltage across it. The metal guard layer must be insulated from the preparation solution. For different approaches to this method see Schwartz & House (1970), Suzuki, Rohliçek & Fròmter (1978), Sachs & McGarrigle (1980) and Finkel & Redman (1983).

Shielding the electrode introduces high-frequency noise therefore it should only be done when absolutely necessary. The amount of added noise is proportional to the amount of shield capacitance, so only the minimum necessary length of microelectrode should be shielded.

Because of the distributed nature of the axial resistance of the microelectrode, of the axial resistance of the metal layer, and of C_t, the shielding technique is not perfect. In practice, the effect of these nonidealities is to cause the step response of the microelectrode to overshoot even when the Capacitance Neutralization gain is unity. For this reason, the Capacitance Neutralization circuit has a minimum less than unity.

Microelectrode Resistance

Another important aspect of the microelectrode is the tip resistance (R_e). This should be as low as possible consistent with good impalements of the cell. There are two advantages associated with low values of R_e:

Settling Time

The decay time constant for the microelectrode voltage after a current pulse depends strongly on R_e. Hence, lower R_e values produce faster settling times. As well, high R_e values are sometimes associated with a slow final decay even after C_t has been eliminated.

Stability

R_e of most microelectrodes changes with time and with current passing. R_e is affected not only by the magnitude of the current but also by its polarity. In general, microelectrodes of lower resistance are more stable during current passing than microelectrodes of higher resistance.

Filling Solutions

The best filling solution to use depends on the preparation under investigation and the experience of the investigator. Although KCl gives one of the lowest tip resistances for a given tip diameter it is not necessarily the fastest to settle after a current pulse. K-citrate is sometimes faster.

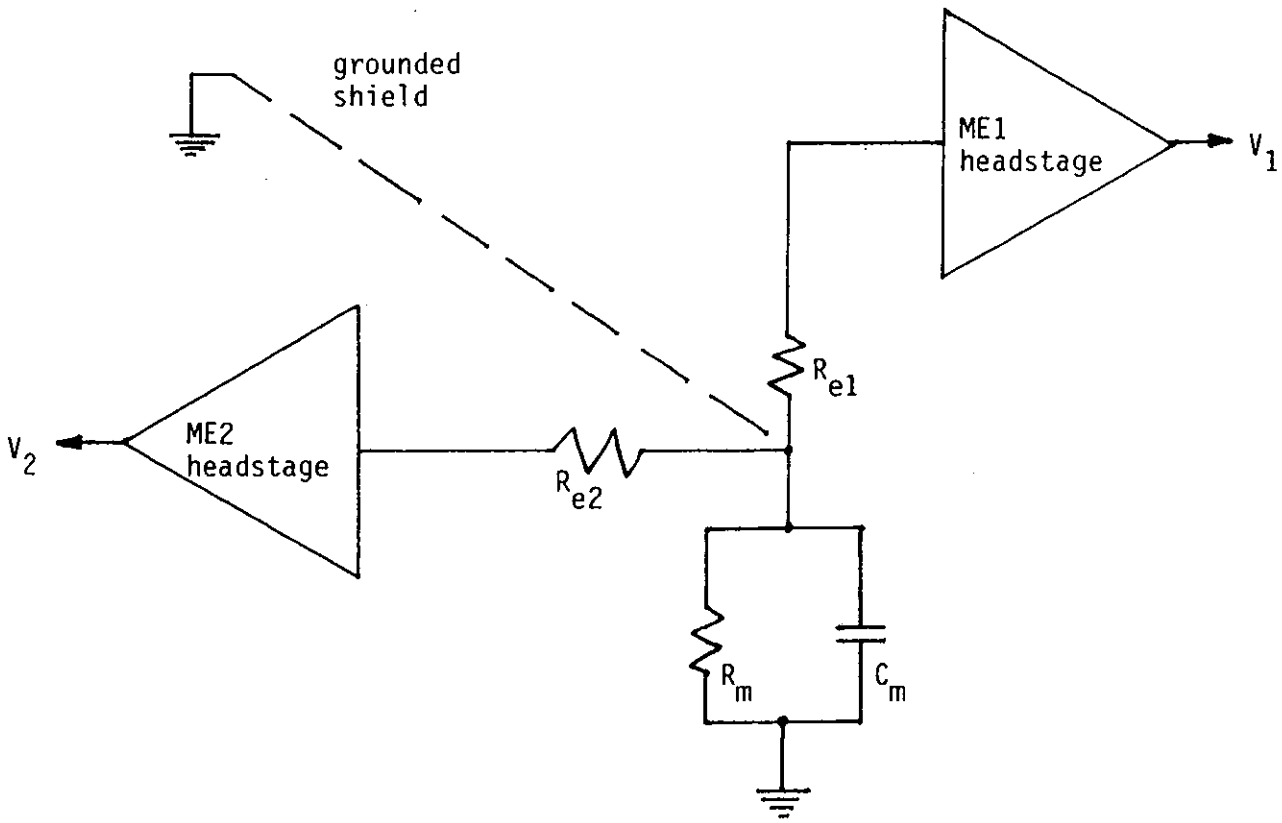
It is important to be aware that during current-passing large amounts of ions from inside the microelectrode can be ionophoresed into the cell. For example, if current is passed by the flow of ion species A from the microelectrode into the cell, then after 50 seconds of current at 1 nA (or 1 second of current at 50 nA) the change in concentration of A inside a cell 100 μm in diameter is 1 mM. If A is an impermeant ion, the cell may swell due to the inflow of water to balance the osmotic pressure.

Recommended Reading

A small book by Purves (1981) serves as an excellent general reference for microelectrode techniques.

MODEL CELLS

We recommend that you practice using the AXOCLAMP-2A on an RC cell model. The resistor provided with each headstage can be conveniently used to simulate the microelectrode and the RC cell model can be soldered directly to the free end (see Fig. 6). If two-electrode voltage clamping is being practiced it is important to place a grounded shield between the model electrodes and between the headstages.



Notes:
1. R_{e1} and R_{e2} are resistors to simulate the microelectrodes.
2. R_m and C_m are a resistor and capacitor to simulate the cell.

FIGURE 6A - SUGGESTED CELL MODEL

The CLAMP-1 Model Cell

If you do not need to model your cell exactly, the CLAMP-1 Model Cell shipped with your AXOCLAMP-2A is a convenient model to work with. The cell and electrode components simulate a small-to-medium sized cell having an input resistance of 50 MΩ, a membrane time constant of 25 ms and electrode resistances of 50 MΩ. See Figure 6B. The case of the model cell is connected to ground. Shielding between the two electrode resistors is effected by the body of the switch.

Install the model cell by plugging it into one or both of your headstages. Connect the gold-plated ground jack to the **yellow** jack on the back of the ME1 headstage using the cable provided. Do not make any connection to the gold-plated jack on the front of the HS-2 headstage -- this is connected to the headstage case which is driven to the electrode potential.

When the switch is in the BATH position, both electrode resistors are connected to ground. This is a convenient position for practicing bridge balancing techniques and offset adjustment.

When the switch is in the CELL position, both electrode resistors are effectively intracellular. In Bridge or DCC mode you should see exponential voltage responses to steps of current. In dSEVC mode you should be able to clamp the cell at gains of up to 0.8 nA/mV using an HS-2 x0.1 headstage, at sampling rates up to 8 kHz. In TEVC mode, use one of the following electrode combinations: 1) two x0.1 headstages, two x1 headstages, or a x1 headstage for ME2 and a x0.1 headstage for ME1. The electrode resistances in this model cell are too large for you to practice cSEVC.

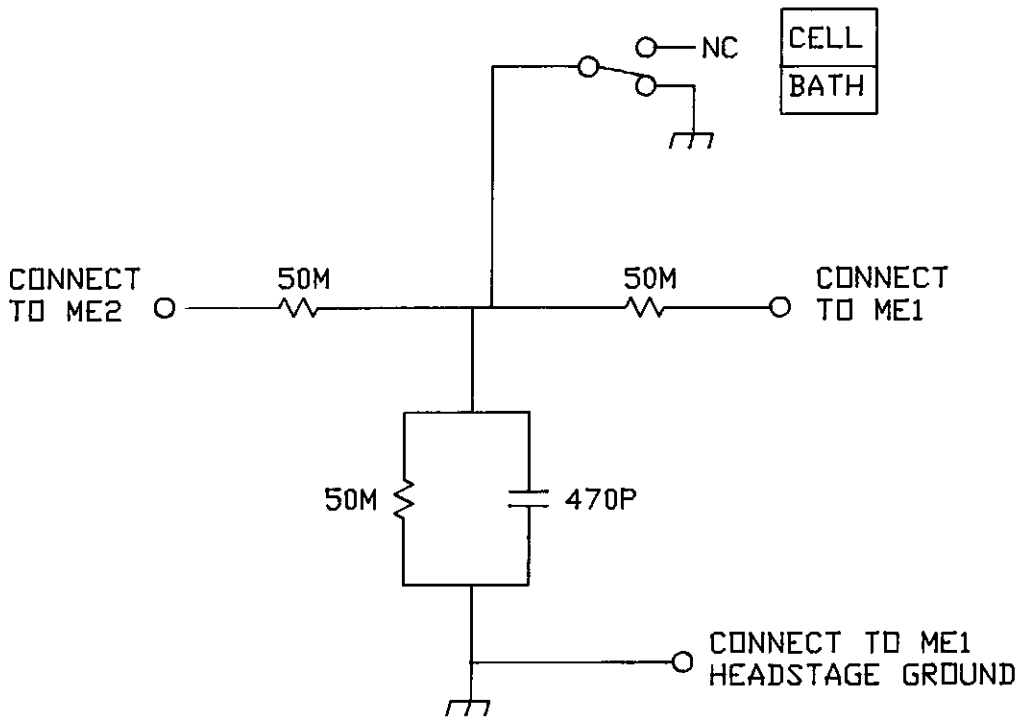


FIGURE 6B - CLAMP-1 MODEL CELL

MONITOR

The Monitor output is used to check the settling characteristics of the voltage at the input to the sample-and-hold device. This is advisable during DCC and dSEVC and the notes on these two modes should be consulted for details.

The Monitor signal is derived from V_1 (see Fig. 7). After amplification by 10, V_1 is filtered by the Anti-Alias Filter. The output of the Anti-Alias Filter is the input of the sample-and-hold device and the signal provided to the Monitor output.

A baseline correction circuit compensates for shifts in V_1 so that V_{mon} always decays to zero. This prevents V_{mon} from moving off the oscilloscope screen when the holding potential is shifted during voltage clamp.

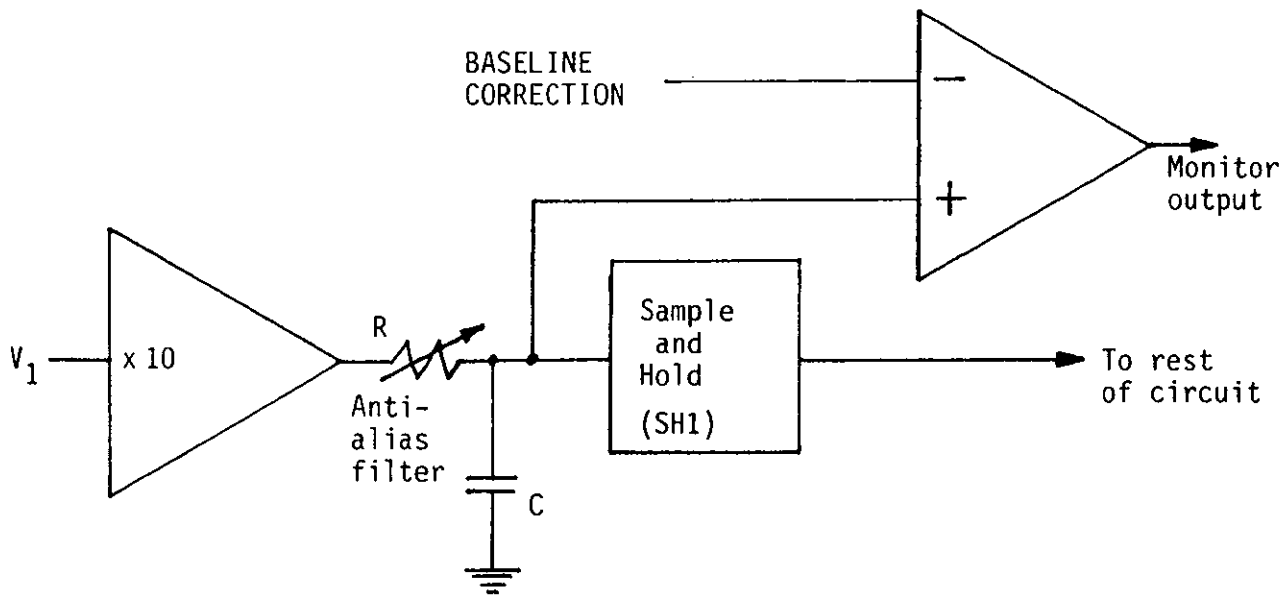


FIGURE 7 - ANTI-ALIAS FILTER & MONITOR CIRCUIT

NOISE IN DCC AND dSEVC MODES

The noise inherent in discontinuous microelectrode clamps (discontinuous current clamp or discontinuous single-electrode voltage clamp) is four or more times worse than the noise in continuous microelectrode clamps (bridge current clamp or two-electrode voltage clamp) when the discontinuous microelectrode clamps are adjusted for the same dynamic response and accuracy as the continuous microelectrode clamps.

There are two major reasons for this inherent deterioration in noise performance.

The first is to do with capacitance neutralization. A fundamental property of all capacitance neutralization circuits is that they introduce noise in excess of what is contributed by the thermal noise of the recording microelectrode and the input noise of the buffer amplifier. The excess noise becomes progressively larger as the microelectrode time constant is reduced. In discontinuous systems the microelectrode time constant must be reduced more than in continuous systems so that after a current pulse the microelectrode voltage will decay to V_m within the time allotted for passive recording. The excess noise due to optimizing the capacitance neutralization can vary from a factor of about two in a system where primary efforts have been taken to keep the input capacitance low, to much larger factors in systems where large amounts of capacitance-to-earth and capacitance-to-shield are tolerated.

The second major reason for the deterioration in noise performance of discontinuous microelectrode clamps has to do with the sampling process. As discussed in the section on the Anti-Alias Filter, sampling processes alias the noise in the input signal spectrum into a larger-magnitude spectrum confined to a bandwidth equal to half of the sampling rate (f_s). The normal procedure used in digitizing systems to avoid aliasing is to reduce the bandwidth of the input signal to $f_s/2$ or below. This is not possible in discontinuous microelectrode clamping because reducing the bandwidth of the microelectrode increases the time constant and therefore prevents adequate settling. The amount of aliased noise depends in part on the current duty cycle used in the discontinuous clamp. The 30% duty cycle used in the AXOCLAMP-2A has been chosen to give a good compromise between aliased noise and dynamic performance (Finkel & Redman, 1984b). With this duty cycle the increase in noise due to aliasing is a factor of about two.

The two contributions to noise discussed above lead to a factor of four or more deterioration in noise. To keep the deterioration as small as this the experimenter should aim to do the following.

(1) Keep the real value of C_{in} as small as possible so that only minimal capacitance neutralization must be used. (Avoid using coaxial cable to connect the microelectrode to the headstage.)

(2) Either increase the Anti-Alias Filter setting at a given cycle rate, or increase the cycle rate at a given setting of the Anti-Alias Filter, so that the amount of aliased noise is minimized.

Finally, the amount of noise recorded can be reduced to some extent by using as much output filtering as possible. However, the output filtering should never be increased to the extent that dynamic information (e.g. rise time) is lost. Usually, output filtering at $f_s/10$ is a good compromise. The best way of reducing noise in the records is by averaging repetitive signals. This well-known procedure reduces the noise by the square root of the number of averages without affecting the time course of the signal.

Notwithstanding the comparatively poor noise performance of discontinuous single-electrode voltage clamps compared with two-electrode voltage clamps, the single-electrode technique is extremely rewarding because it allows voltage-clamps to be performed in preparations where two-electrode voltage clamping is just not feasible. As well, the signal-to-noise ratio in many preparations during discontinuous single-electrode voltage clamp is, despite the above considerations, adequate for data to be analyzed without averaging.

OFFSET CONTROLS

The Offset controls compensate for the junction potentials in the experimental setup.

The offset compensation for the V_2 output works by adding a DC voltage to the output. Therefore, it is called the "Output" Offset control.

The offset compensation for the $10.V_m$ and V_1 outputs is performed in the first stage of the recording circuit. This is necessary so that after amplification of the input signal the full range of the sample-and-hold circuitry can be utilized. The ME1 offset compensation should **not** be altered during voltage clamp because the voltage-clamp circuitry will interpret the change in the offset setting as a change in V_m. To remind you of this important characteristic the control is called the "Input" Offset.

For both controls, the compensation range is ± 500 mV. The no-compensation point is in the middle of the range of the multi-turn dials. Each turn of the dials is approximately 100 mV. The dials can be locked after setting. The dial markings are not meaningful. Calibrated dials are used for these controls because they have brakes to prevent accidental movement.

The normal procedure for using the Offset controls is to zero the voltmeter readings when the microelectrode is outside the cell. All subsequent readings are then with respect to the potential of the extracellular solution.

OUTPUT FILTER

Built-in filters are provided to smooth the $10.V_m$ and I_m outputs. These are single-pole lowpass filters. Six -3 dB frequencies (f_L) can be selected.

As well as reducing the noise, a filter also slows the rise time of the filtered signal. A single-pole filter converts a step into an exponential. There is no overshoot. The time constant of the exponential is

$$\tau = (2\pi f_L)_{-1}$$

The 10% - 90% rise time of the exponential is

$$t_r = 2.2\tau.$$

The six available f_L's and the corresponding τ's and t_r's are given in Table 3.

TABLE 3

f_L (kHz)	0.1	0.3	1	3	10	30
τ (μs)	1600	530	160	53	16	5.3
t_r (μs)	3500	1200	350	120	35	12

High-Order Lowpass Filters For Low-Noise Recordings

The "order" of a filter refers to the number of poles (RC sections). For example, a third-order filter has three poles. Each pole attenuates the high-frequency noise at 20 db/decade.

During TEVC the current noise increases at +20 db/decade above a frequency determined by the membrane time constant (Finkel & Gage, 1984). To adequately limit this noise the filter used for data display and storage should be at least 2nd order and preferably 3rd or 4th order.

Rise Time Of High-Order Filters

As a rule of thumb it can be noted that for lowpass multiple-pole filters having less than 10% overshoot, the 10-90% rise time is within a few percent of t in a single-pole filter having the same -3 dB frequency.

However, the frequency specified for many multiple-pole lowpass filters is the -3 dB frequency of the component lower-order filters instead of being the -3 dB frequency of the complete filter. Before using these filters it is advisable to check the 10-90% rise time of a step signal applied to the input.

Note On Ultimate Rise Time

When a signal with 10-90% rise time t_1 is passed through a filter with 10-90% rise time t_2 the rise time of the output signal is approximately

$$t_r = \sqrt{(t_1^2 + t_2^2)}$$

OUTPUT IMPEDANCE AND PROTECTION

All outputs are protected by 560 Ω output resistors.

All outputs can withstand a continuous short circuit to ground or any voltage in the ±15 V range. However, in keeping with normal practice, such short circuits should be avoided.

PANEL METERS

Three digital panel meters (DPMs) are provided to continuously display the DC level of some of the important outputs. These displays are.

V_m (mV)

This DPM indicates the membrane potential in all modes. It is derived from the $10.V_m$ output. The maximum displayed value is approximately ±600 mV, which is the value which will typically be seen when the ME1 headstage input is open circuit.

V_2 (mV)

This DPM indicates V_2 in all modes. The maximum displayed value is $\pm$1999 mV. Out-of-range signals are indicated by a partially blanked display, and + or - to indicate polarity.

I (nA)

This DPM can display one of the following currents: I_m, I_2 or I_{VIRT}. The current to be displayed is chosen using the I-Display Select switch.

Three small switches are used to change the decimal point location so that the display can be read directly in nA for the headstage being used. The HCG_1 switch is active when the I-Display Select switch is in the I_m position; the HCG_2 switch is active when I_2 is selected; the VG switch is active when I_{VIRT} is selected. To use, turn the switch to the gain of your headstage.

PHASE

A voltage-clamp is a negative-feedback circuit and as such it requires a 90° phase shift within the circuit. Ideally this phase shift is supplied by the capacitance of the membrane. In practice, membranes introduce significantly less than 90° phase shift (see discussion by Finkel & Gage, 1984).

The frequency response of the voltage-clamp circuit can be modified by the Phase controls. The voltage-clamp circuit can thereby be adjusted to compensate for the nonideal phase response of real membranes.

The controls are in two parts; a potentiometer to shift from lead to lag, and a 4-position switch to set the time constant.

Phase lead **boosts** the high-frequency gain of the voltage-clamp circuit. In some preparations this can be used to sharpen the step response and improve the voltage clamping of fast conductance changes. On the debit side, use of phase lead increases the noise and can also cause high-frequency oscillations. To reduce the risk of oscillations the phase-control circuit is arranged to always introduce some phase lag with the phase lead. The added phase lag restricts the maximum increase in the high-frequency gain to a factor of 2, achieved when the potentiometer control is turned to the extreme lead position.

Phase lag **cuts** the high-frequency gain of the voltage-clamp circuit. This can be used to reduce the noise but at the same time it slows the response and introduces ringing. In the extreme lag position the phase-control circuit introduces pure lag.

The action of the Phase Shift potentiometer can be summarized as follows. In the extreme lead position a combination of phase lead and lag is introduced such that the high-frequency gain is doubled. The amount of phase lead is gradually reduced by counterclockwise rotation of the potentiometer and falls to zero at the extreme lag position. At the same time the amount of phase lag cutting the high-frequency gain is increased by counterclockwise rotation of the potentiometer. At the center position of the potentiometer the net change to the frequency characteristics of the voltage-clamp circuit is nil.

The Time Constant switch changes the maximum lag and lead values as listed in the Specifications. In some preparations no phase lag or lead is required. If this is so, the Time Constant switch should be switched to the Off position.

With an RC cell model the best voltage-clamp will be achieved when no Phase shift is used.

Use

The Phase controls can be used during voltage clamp to compensate for the frequency characteristics of membranes which are not well modeled by a parallel resistance and capacitance. Both the membrane voltage and current step responses should be improved by using the Phase controls. If only the membrane voltage step response is improved it is likely that there is a resistance (R_s) in series with the membrane. See the Series Resistance Section for a discussion of this problem.

In some cases using some phase lag will reduce the current noise during voltage clamp. See the Sections on each type of voltage clamp for more details.

POWER-SUPPLY GLITCHES

The AXOCLAMP-2A has been designed to minimize the effects of power supply transients (glitches). This is achieved by:

1) taking the incoming power through a radio frequency interference (RFI) filter and

2) capacitively isolating the transformer primaries and secondaries.

Nevertheless, some power-supply glitches do get through. These can cause transients to appear on the voltage and current outputs which may corrupt high-sensitivity recordings (for example, during fluctuation analysis).

The only completely effective way to gain immunity from mains glitches is to eliminate them at the source. Most glitches are due to the switching on and off of other equipment and lights on the same power-supply circuit. Precautions to be taken include:

(1) Avoid switching equipment and lights on or off while recordings are being made.

(2) Water baths, heaters, coolers etc. should operate from zero-crossing relays.

(3) RFI filters should be installed in glitch-producing equipment.

In most circumstances occasional transients on the outputs are inconsequential and therefore no precautions have to be taken.

POWER SUPPLY VOLTAGE SELECTION & FUSE CHANGING

Supply Voltage

The AXOCLAMP-2A can work from all international supply voltages. The two input ranges are:

(1) 115 V : For 100 V_{ac} to 125 V_{ac} operation.

(2) 230 V : For 200 V_{ac} to 250 V_{ac} operation.

To change the supply voltage setting:

(1) **Disconnect the power cord**

(2) Remove the top cover

(3) Locate the slide switch labeled "S2" at the back of the power supply board. The power supply board is the small horizontal board in the left side of the instrument.

(4) For 115 V operation slide S2 to the left towards the label "115". For 230 V operation slide S2 to the right towards the label "230".

(5) Replace the top cover.

(6) Re-connect the power cord.

(7) Mark the new operating voltage on the identification plate on the rear of the instrument.

Changing The Fuse

The AXOCLAMP-2A uses a 0.5 A 250 V slow acting 5 x 20 mm fuse on both voltage ranges. Before changing the fuse investigate the reason for its failure.

To change the fuse:

(1) **Disconnect the power cord.**

(2) Use a screwdriver or something similar to lever out the fuse holder.

(3) Discard the fuse from the active slot, i.e. the slot which places the fuse closest to the inside of the instrument.

(4) Shift the spare fuse from the spare slot (i.e. the slot which places the fuse towards the outside of the instrument) to the active slot.

(5) Re-connect the power cord.

REMOTE

Some of the front-panel functions can be activated via the Remote connector at the rear of the Clamp. These are Mode selection, Buzz, and Clear. Possible uses of this facility include using a computer to select the Modes, and using hand-operated or foot-operated switches for Buzz and Clear so that these functions can be used by the experimenter without moving from the microscope.

The selected functions are activated by HIGH logic levels applied to the appropriate pin. New Modes are selected and kept after a HIGH level of 1 μs or more in duration. Buzz and Clear are activated for the duration of the HIGH level. Using the Remote facility does not disable the front-panel switches.

The pin connections for the Remote connector are as follows:

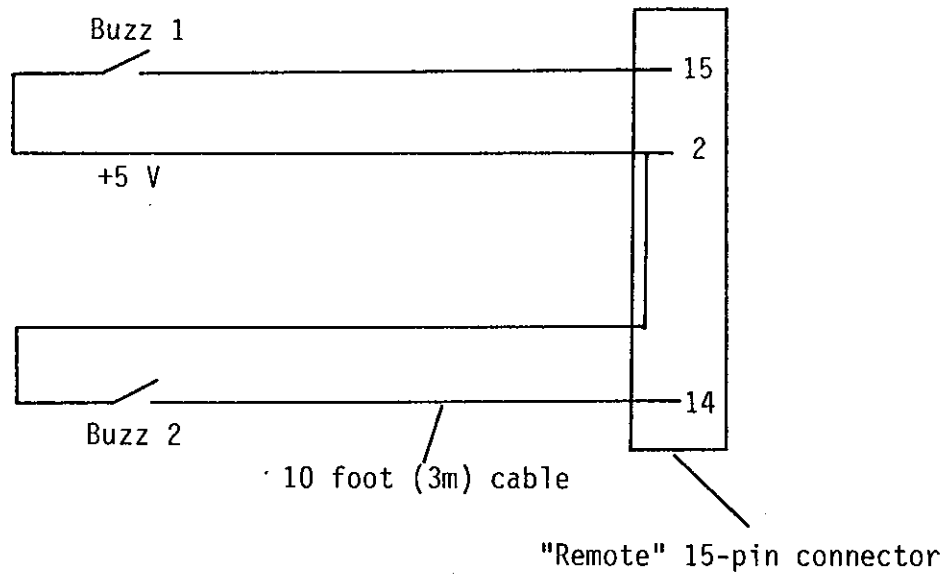
1. DIGITAL Ground
2. +5 V output
3. BRIDGE mode
4. DCC mode
5. SEVC mode
6. TEVC mode
7. CLEAR ME1 "+"
8. CLEAR ME1 "-"
9. Not used
10. Not used
11. Not used
12. CLEAR ME2 "+"
13. CLEAR ME2 "-"
14. BUZZ ME2
15. BUZZ ME1

To use the Remote controls, the external control signals can be wired to a 15-pin D-type connector which can then be plugged into the Remote connector on the rear panel.

+5 V is provided for wiring up any remote switches you may use. **Do not short circuit this supply.** The Mode-Select inputs (pins 3-6) have 50 kΩ input resistances; the other inputs (pins 7, 8, 12-15) have 7 kΩ input resistances.

The FS-3 footswitches provided with the AXOCLAMP-2A consist of a pair of normally open switches for activating Buzz of each electrode. If footswitches are not convenient you can easily connect your preferred switches by following the wiring diagram below.

For remote operation of microelectrode 1 Buzz and microelectrode 2 Buzz.



EXTERNAL SWITCH WIRING DIAGRAM

RMP BALANCE

The two indicator lights for monitoring resting membrane potential (RMP) are used in two ways.

Before switching into a voltage-clamp mode the Holding Position potentiometer is adjusted until the two lamps are equally dim (nulled). This ensures that when a voltage-clamp mode is selected the membrane potential will be held within a few millivolts of RMP. When adjusting the Holding Position control before voltage clamping the sensitivity of the null point is affected by the Gain.

During voltage clamp the RMP Balance lights provide a quick indication of when the cell is being held at its resting level. That is, the RMP Balance lights are nulled at this point.

SERIES RESISTANCE

Origin

A resistance (R_s) in series with the membrane can arise a number of different ways. In cSEVC, R_s would mainly be due to the resistance of the suction electrode. In dSEVC, R_s would be due to a slow microelectrode response. In TEVC, R_s would be due to the tissue, the bathing solution and the grounding electrode.

Problem

The voltage-recording microelectrode (ME_1) records the voltage across R_s and R_m, thus the recorded membrane potential is in error due to the IR voltage drop across R_s. In addition, R_s limits the maximum rate at which the membrane capacitance can be charged.

Solutions

There are no perfect solutions for these two problems. As always, the best solution is to take steps to minimize R_s in the first place. These include:

(1) In cSEVC arrange for the electrode resistance (R_e) to be extremely small, since $R_s \approx R_e$.

(2) In dSEVC eliminate R_s altogether by watching the Monitor output to make sure the transient decays completely before the next sample is taken.

(3) In TEVC keep the resistance of the grounding path low. This includes the solution resistance, the grounding electrode, and a virtual ground if used. Usually R_s is only a problem in TEVC if very large currents are passed.

Secondary solutions are the following:

(1) In cSEVC electronically subtract from the command voltage a voltage equal to the product of the membrane current and the presumed series resistance (see cSEVC section). This technique can begin to cope with both the error and the limited charging rate. Unfortunately, the compensation can rarely exceed 70% before introducing instabilities.

(2) The high-frequency current noise is proportional to the gain, but the clamp speed is limited by R_s. Since the membrane potential step response time is slow anyway, it turns out that using some phase lag can significantly lessen the current noise without worsening the response speed. This is illustrated in Fig. 8. Note that even though the recorded potential is made faster by using the Phase controls, the true membrane potential and current are not speeded up.

(3) In TEVC electronically subtract from the command voltage a voltage equal to the product of the membrane current and the presumed series resistance. To do this you would need to use an external potentiometer to find a fraction of I_2, and feed it into the rear-panel R_s COMP input.

What is the True Membrane Potential Time Course?

For an isopotential cell, the time course of the true membrane potential is the same as that of the recorded membrane current. The recorded potential, which includes the voltage drop across R_s, may be much faster. See Fig. 8 for an illustration of this effect.

In a non-isopotential cell, for example a neuron with an axon and dendrites, the true membrane potential recorded at the tip of the voltage-recording electrode will in fact settle faster in response to a step voltage command than will the membrane current. In this situation the presence of a series resistance will exaggerate the difference in time courses.

Fig. 8

Membrane potential and current during TEVC.

Cell model was R_m = 10 MΩ, C_m = 1 nF, R_s = 300 kΩ, R_{el} = R_c = 10 MΩ. For all traces recording bandwidth was 30 kHz. Gain was 700 V/V. Vertical calibration: 10 mV/div. Horizontal calibration: 1 ms/div.

Upper trace is true membrane potential recorded by a third independent electrode.

Middle trace is membrane potential recorded by ME1 and clamped by the voltage-clamp circuit.

Bottom trace is the membrane current.

A. No added phase shift.

B. Phase control set to Center Frequency time constant of 0.2 ms, Phase shift on -4. The true membrane potential response is unaffected, but the membrane current noise is greatly reduced, to a level consistent with the slow membrane potential response.

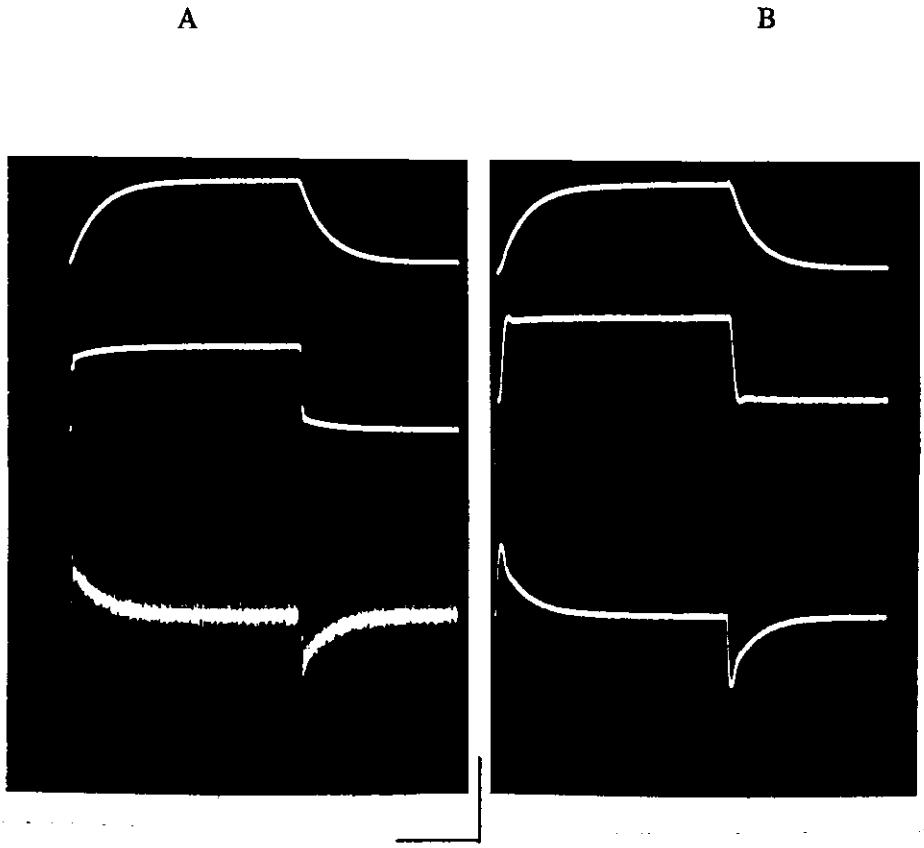


FIGURE 8 - HOW SERIES RESISTANCE (R_s) AFFECTS VOLTAGE CLAMP PERFORMANCE

SEVC MODE - CONTINUOUS

Continuous single-electrode voltage clamping (cSEVC) is one of two single-electrode voltage clamp modes. In cSEVC current passing and voltage recording are performed simultaneously as shown in the block diagram of Fig. 9. The voltage (V_1) recorded by the microelectrode buffer (A1) is compared in a high-gain differential amplifier (A2) to a command potential (V_c). The output of A2 acts to keep the difference at its input (ϵ_1) very small. Hence, V_1 is clamped equal to V_c.

The circuit clamps the voltage across the microelectrode (ME1) as well as the membrane potential (V_m). The voltage across ME1 is non-zero because of the current (I_m) which flows through it. This voltage drop is equal to the product of I_m and the resistance (R_{e1}) of ME1.

To keep the error due to $I_m R_{e1}$ small it is necessary that R_{e1} be much smaller than the membrane resistance (R_m). Thus a 3 MΩ microelectrode would be appropriate for use with a 300 MΩ cell.

The voltage across ME1 can be partially compensated by using the Bridge potentiometer. Note that the range of the Bridge potentiometer is ten times less in cSEVC mode than in Bridge mode. The reduced range is indicated by a small LED. It is not normally possible to compensate more than about 70% of the electrode resistance without introducing oscillations.

During cSEVC, R_{e1} has the nature of a series resistance (R_s). R_s is discussed in the Series Resistance Section.

Important Note - Anti-Alias Filter

The Anti-Alias Filter is not recommended for use in cSEVC mode. The reasons why are the same as those given in the TEVC Section.

Suggested Use

In Bridge mode set the Capacitance Neutralization control for the best step response.

Set the Gain and Anti-Alias Filter to minimum values. Switch the Phase control off. Switch off all current commands.

Use the Holding Position control to yield equal brightness in each of the two RMP Balance lights. At this setting the command potential during voltage clamp will be equal to the resting membrane potential (RMP). Lock the Holding Position control if desired.

Switch into cSEVC mode. Set up a repetitive step command. Monitor $10.V_m$ and I_m. For maximum stability switch the Phase Time Constant to 20 or 200 ms. Increase the Gain for the best response on both V_m and I_m. Sometimes lower current noise can be achieved for the same step response with the Phase Time Constant on 0.2 or 2 ms. Before switching to these values reduce the Gain since the stability margin is lower for smaller values of the Time Constant. Advance the Bridge potentiometer to speed up the current and voltage settling times.

An example of a cSEVC set up in a cell model is shown in Fig. 10. The cell model was 300 MΩ//33 pF and the electrode was modeled by a 3 MΩ resistor. Because of R_e there was a limit to how fast the membrane capacitance could be charged. This can be seen from the duration of the capacitance transient in the upper trace. The clamping electrode (ME1) records the true membrane potential as well as the IR drop across itself, thus the step response of the recorded voltage (middle trace) is faster than the true membrane potential (lower trace) recorded by an independent electrode. As discussed in the Series Resistance section, the time course of the true membrane potential corresponds to the time course of the membrane current.

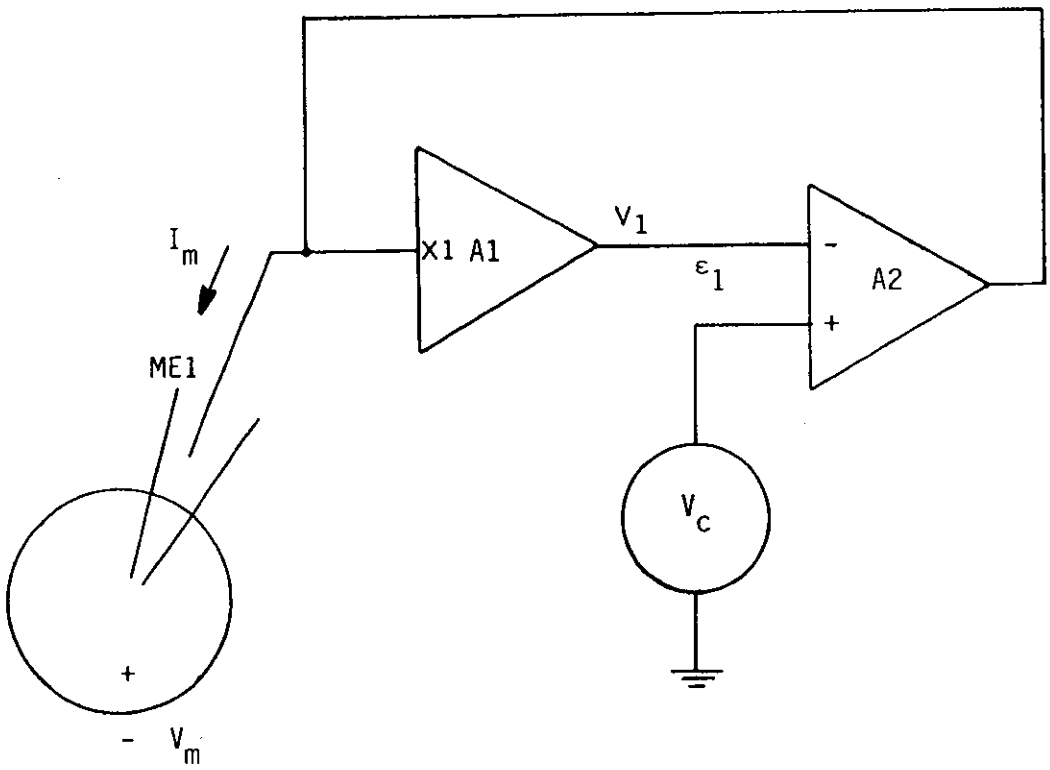


FIGURE 9 - SIMPLIFIED SCHEMATIC OF cSEVC

cSEVC Compared With Whole-Cell Patch Clamp

The simplified schematic in Fig. 9 shows that cSEVC is similar to whole-cell clamping using the patch-clamp technique. However the implementation is very different.

In the patch-clamp technique the voltage-clamp is established by a specialized headstage containing a virtual-ground circuit. In the cSEVC technique the headstage is a general-purpose unity-gain buffer and the voltage-clamp circuit is located in the main unit.

This difference is significant. In the dedicated virtual-ground headstage much less circuitry is involved and thus nonidealities of the electronics have much less effect. Thus for fast events the patch-clamp technique is considerably better than cSEVC. On the other hand for slow and moderate events the techniques become comparable.

Fig. 10

Current and potential recorded during cSEVC. Cell model was 300 MΩ//33 pf. Electrode was 3 MΩ. Bandwidth was 3 kHz for all traces. H of HS-2L headstage was x0.1. Clamp gain was 3.3 nA/mV. Voltage command was a 10 mV step. Phase Time Constant was 0.2 ms. Phase Shift was full lag. A-A Filter was off. Capacitance Neutralization was minimum.

Upper trace: Membrane current. Charging time was limited by R_e.

Middle trace: Potential recorded by clamping electrode (ME1) and available at the $10.V_m$ output. Includes IR drop across ME1.

Lower trace: True membrane potential recorded by an independent electrode. Time course is the same as that of the membrane current.

Noise: The current noise in the 3 kHz bandwidth was 55 pA peak-to-peak. If the gain was reduced so that the capacitance transient took 1.5 ms to settle the current noise fell to 12 pA peak-to-peak. The noise looks worse in the photo due to blooming of the photographed oscilloscope trace.

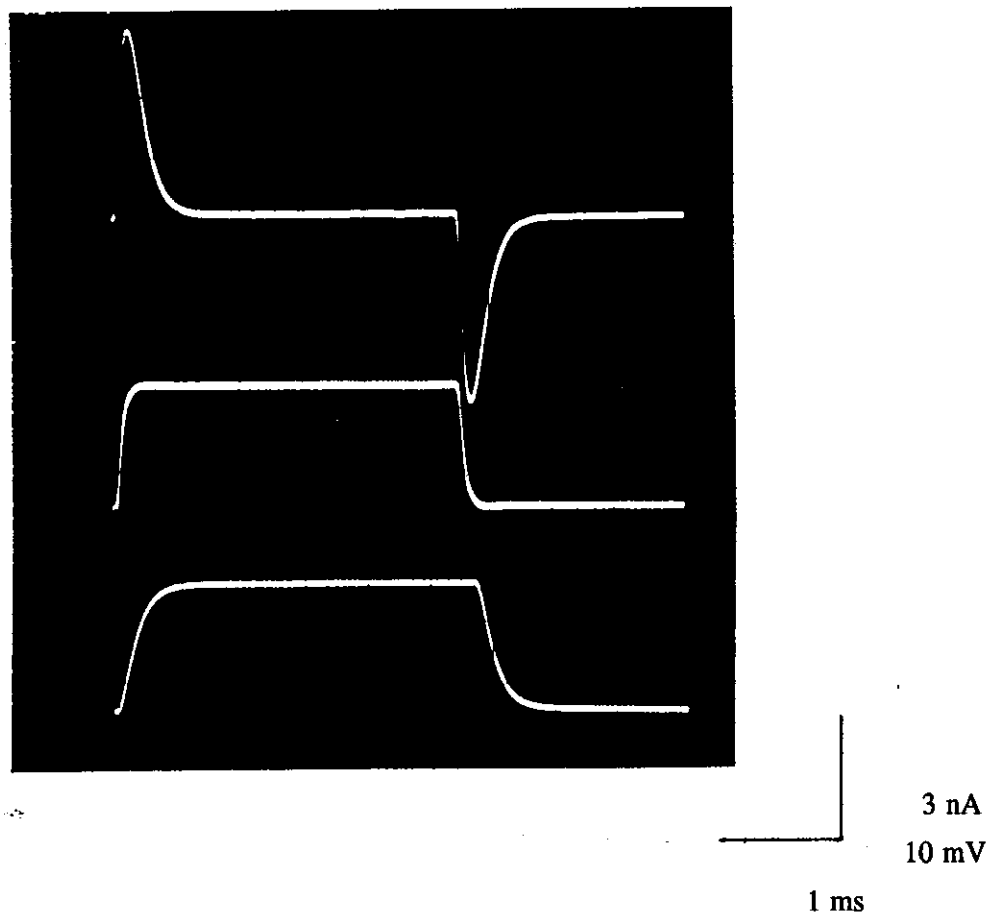


FIGURE 10 - CURRENT AND POTENTIAL RECORDING DURING cSEVC IN A CELL MODEL

SEVC MODE - DISCONTINUOUS

Description

In discontinuous single-electrode voltage clamp (dSEVC) mode the tasks of voltage-recording and current-passing are allocated to the same electrode. Time-sharing techniques are used to prevent interactions between the two tasks. The principles of operation have been published (Brenneke & Lindemannn, 1974; Wilson & Goldner, 1975; Finkel & Redman, 1984) and are outlined in the block diagram and timing diagram of Fig. 11, and in the following discussion.

A single microelectrode (ME1) penetrates the cell and the voltage recorded (V_1) is buffered by a unity-gain headstage (A1). To begin the discussion assume that at this moment V_1 is exactly equal to the instantaneous membrane potential (V_m). A sample-and-hold circuit (SH1) samples V_m and holds it for the rest of the cycle.

The sampled membrane potential is compared with a command voltage (V_c) in a differential amplifier (A2). The output of this amplifier becomes the input of a controlled-current source (CCS) if the switch S1 is in the current-passing position. The gain of the CCS is G_T.

The CCS injects a current into the microelectrode which is directly proportional to the voltage at the input of the CCS irrespective of the resistance of the microelectrode.

The period of current injection is illustrated at the start of the timing waveform. S1 is shown in the current-passing position during which a square pulse of current is injected into the microelectrode. Because of this current V_1 rises.

The rate of rise is limited by the parasitic effects of the capacitance through the wall of the glass microelectrode to the solution, and the capacitance at the input of the buffer amplifier. The final value of V_1 mostly consists of the IR voltage drop across the microelectrode due to the passage of current I_o through the microelectrode resistance R_e. Only a tiny fraction of V_1 consists of the membrane potential recorded at the tip.

S1 then switches to the voltage-recording position. When the input of the CCS is 0 volts, its output current is zero and V_1 passively decays. During the voltage-recording period V_1 decays asymptotically towards V_m. Sufficient time must be allowed for V_1 to reach within a millivolt or less of V_m. This requires a period of up to 9 electrodes time constants (τ_e). At the end of the voltage-recording period a new sample of V_m is taken and a new cycle begins.

The actual voltage used for recording purposes is the sampled voltage. As illustrated in the bottom timing waveform the sampled value of V_m moves in small increments about the average value. The difference between V_m(ave) and V_c is the steady-state error (ϵ_1) of the clamp which arises because the gain (G_T) of the CCS is finite. The error becomes progressively smaller as G_T is increased.

The duty cycle used in dSEVC is current passing for 30% of each cycle, and voltage recording for 70% of each cycle.

The cycling rate (sample rate) must be chosen so that there are ten or more cycles per membrane time constant. This enables the membrane capacitance to smooth the membrane voltage response to the current pulses.

When optimally adjusted, the circuit enables the first steady-state measurement of voltage to be taken 1 to 2 cycle periods after the onset of a membrane conductance change or a change in the command voltage.

Two controls not shown in the Figure are the Anti-Alias Filter and the Phase control. The Anti-Alias Filter is a single-pole filter between the output of the unity-gain headstage (A1) and SH1 (see Fig. 7). It can be used to reduce noise at a given sampling frequency. The output of the Anti-Alias Filter can be observed on the Monitor output. In practice it is this voltage, not V_1, which has to decay to V_m before a sample is taken. The Phase control alters the frequency response of the differential amplifier (A2). It can be used to compensate for the complicated frequency characteristics of a real cell.

The Gain control alters G_T. Refer to the Specifications for its operating range.

While ME1 is occupied by the dSEVC it is still possible to independently use ME2. For example, ME2 could be used for recording from and stimulating other cells which make connections to the cell being voltage-clamped.

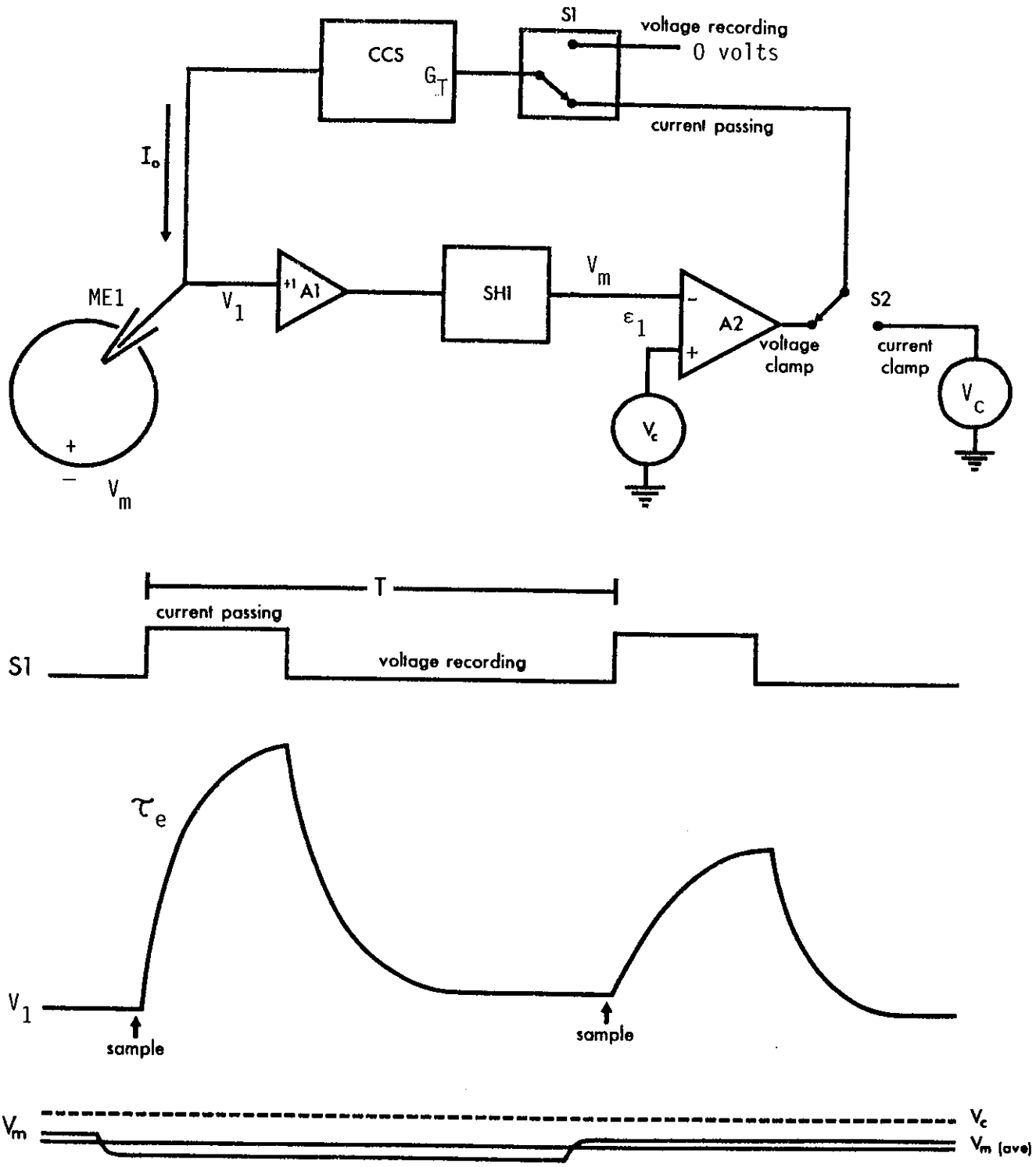


FIGURE 11 - SEVC BLOCK DIAGRAM AND TIMING WAVEFORMS

Suggested Use

Use two oscilloscopes. To the main one connect the $10.V_m$ and I_m outputs. Trigger this oscilloscope from the source used to time the command signals. To the second one (which need not be a high-quality type) connect the Monitor output. Set the gain to 100 mV/div (= 10 mV/div input referred). Trigger this oscilloscope from the SAMPLE CLOCK output on the rear panel.

Set up a repetitive current pulse in Bridge Mode. Balance the electrode voltage drop as shown in Fig. 2 in the Bridge Section.

Set Gain and Anti-Alias to minimum. Switch Phase Shift off (i.e. set Center Frequency to OFF).

Switch to DCC mode.

Proceed to **optimally** set the Capacitance Neutralization as described in the DCC Section, method B, and illustrated in Fig. 5.

Set the Output Bandwidth to 1/5 or less of f_s.

Switch off the current pulse. Use the Holding Position control to achieve equal brightness in each of the two RMP Balance lights.

Switch to SEVC.

Set up a repetitive 10 mV step command.

Increase the Gain as far as possible without causing overshoot or instability in the step response. Reduce the Gain slightly below the maximum value to get a safety margin.

Introduce Phase lag or lead if by doing so the step response of both the current and the voltage can be improved.

Increase the Anti-Alias Filter while checking the settling characteristics on the monitor waveform. The noise on V_m and I_m may be reduced by this procedure. Only use as much Anti-Alias as is consistent with stability.

Set the Anti-Alias Filter back to minimum before using a new electrode.

An example of a correctly set up dSEVC is shown in Fig. 12.

Fig. 12
An example of a correctly set up dSEVC in a cell model. R_m was 100 MΩ. C_m was 33 pF. R_{el} was 100 MΩ. Gain was 1 nA/mV. HS-2L headstage; H = x0.1. Sampling rate was 7 kHz. Voltage command was a 10 mV step. No Phase Shift or A-A Filter. Capacitance Neutralization was optimum. Recording bandwidth in A was 1 kHz.

A. Top trace: Membrane current. Cal: 4 nA, 1 ms

Middle trace: Sampled membrane potential (available at the 10.V_m output).
Cal: 10 mV, 1 ms.

Lower trace: True membrane potential recorded by an independent electrode.
Cal: 10 mV, 1 ms.

Note that the two voltage records are identical because the Capacitance Neutralization was correctly set.

B. Multiple sweeps of the Monitor waveform. This photo was taken with the cell held at rest. The current pulses vary from sweep to sweep because of the sampled voltage noise. The important feature is that the voltage transients decay completely by the time the samples are taken (arrow) even for the largest transients.

Cal: 20 mV, 40 μs.

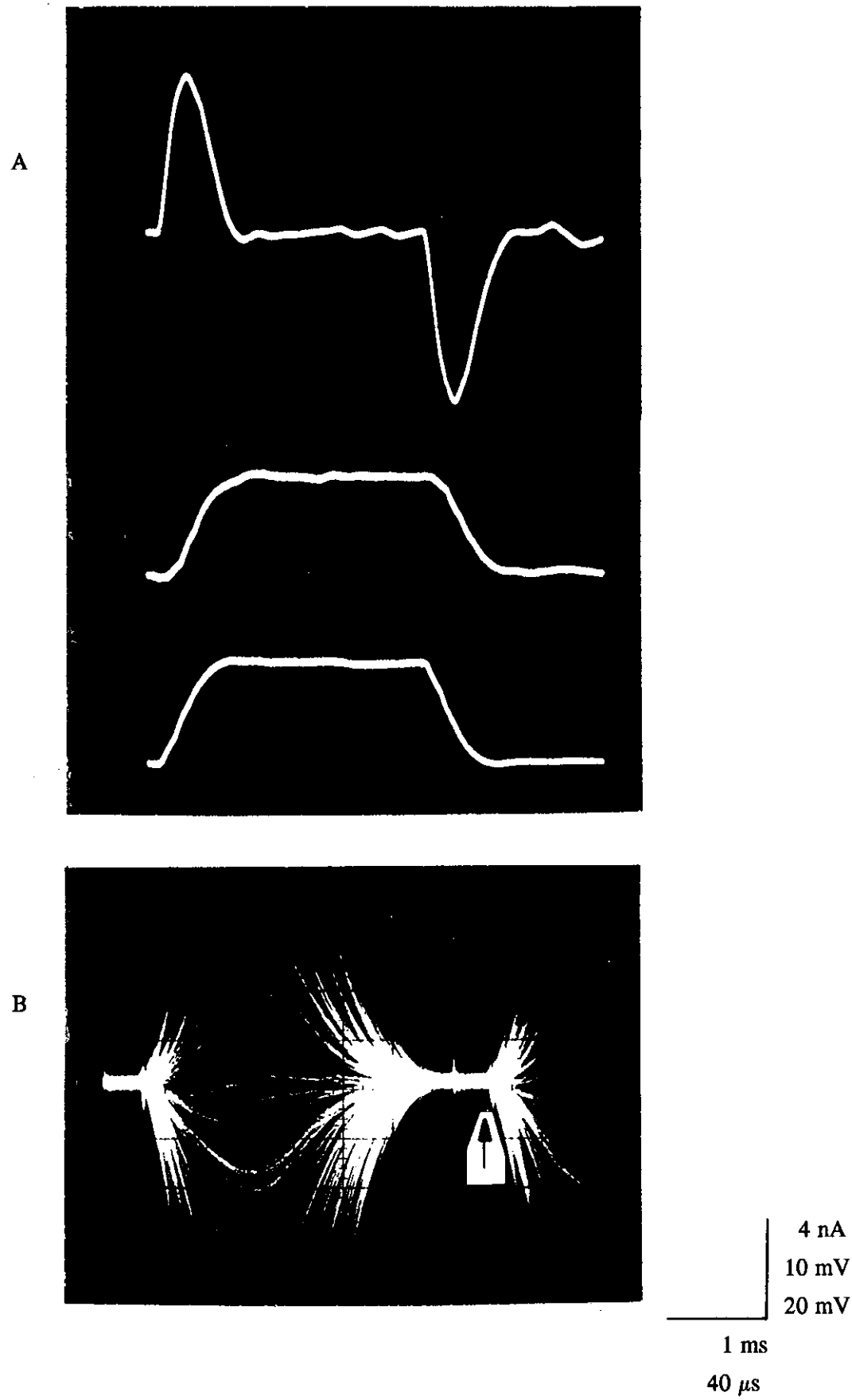


FIGURE 12 - CORRECTLY SET UP dSEVC IN A CELL MODEL

Important Note

If the Phase controls are used it is possible to find false settings of Capacitance Neutralization (or the Anti-Alias Filter) and Phase which together give a seemingly fast step response to V_m whereas in fact the step response in the cell is much slower.

This situation arises by underutilizing the Capacitance Neutralization (or overutilizing the Anti-Alias Filter) so that the Monitor waveform fails to decay adequately when the voltage sample is taken. The electrode voltage sampled has the nature of an IR drop across a series resistance (R_s; see Series Resistance Section). Normally this would make the clamp unstable, but by introducing phase lag stability can be re-imparted although without any reduction of the voltage error.

This false condition only arises if the Capacitance Neutralization setting is altered after the Phase control has been switched in. There are two ways to guarantee that this false condition will not occur.

1. Don't use the Phase controls.

2. If the Phase controls are used be sure to conscientiously observe the Monitor waveform to make sure that the decay to a horizontal baseline is complete at the end of each cycle.

An example of a false clamp is shown in Fig. 13.

The recorded value of I_m is always a true measure of the membrane current even during this false setting. Only the V_m record is erroneous. The danger of this false condition is that most of the presumed membrane potential is in fact voltage drop across the microelectrode.

Which SEVC to use with a Suction Electrode

In the previous section we discussed how a continuous SEVC can be implemented by taking advantage of the low resistance of a suction electrode.

The problem with the cSEVC technique is the error introduced by R_e which can only be partially overcome by series resistance compensation. This problem can be completely avoided by using the dSEVC mode.

It turns out that the conditions when a suction electrode is used are ideal for dSEVC. That is , because R_e is very small the electrode time constant is fast. In addition, the magnitude of the voltage transient across the electrode for a given current is proportional to R_e and therefore small when R_e is small. This double advantage of low R_e values means that the dSEVC can be cycled very rapidly without introducing a sampling error.

Fig. 14 shows the result of a dSEVC in exactly the same cell model that was used in the cSEVC shown in Fig. 0. The most significant difference in the set-up besides the clamping mode used was the fact that no phase shift was used in the dSEVC.

Since the IR drop across the electrode was not sampled, the recorded potential during dSEVC had the same time course as the membrane current and the true membrane potential recorded by an independent electrode (not shown).

The disadvantage of the dSEVC mode was the additional current noise.

Fig. 13

An example of an incorrectly set up dSEVC (i.e. a "false" clamp) in a cell model. R_m, C_m, R_{el}, Gain, H, sampling rate, recording bandwidth and A-A Filter were the same as in Fig. 12. Phase Shift was at maximum lag, Time Constant was 2 ms. Capacitance Neutralization was under-utilized.

A. Top trace: Membrane current.
Cal: 1 nA, 4 ms.

Note that this membrane current is much smaller and slower than the one in Fig. 12.

Middle trace: Sampled membrane potential (available at the $10.V_m$ output).

Cal: 10 mV, 4 ms.

Lower trace: True membrane potential recorded by an independent electrode.

Cal: 10 mV, 4 ms.

Note that the two voltage records are not the same. The sampled membrane potential includes a large error due to the voltage across the microelectrode at the sampling time (see B below).

B. Multiple sweeps of the Monitor waveform. This photo was taken with the cell held at +50 mV from rest. (This was done because when the cell was held at rest with the considerable amount of phase lag used the noise current pulses were too small to allow the adequacy of the decay to be seen.) The voltage transients did not decay to a horizontal baseline at the times the samples were taken (arrow), therefore the samples included some of the IR voltage drop across the microelectrode.

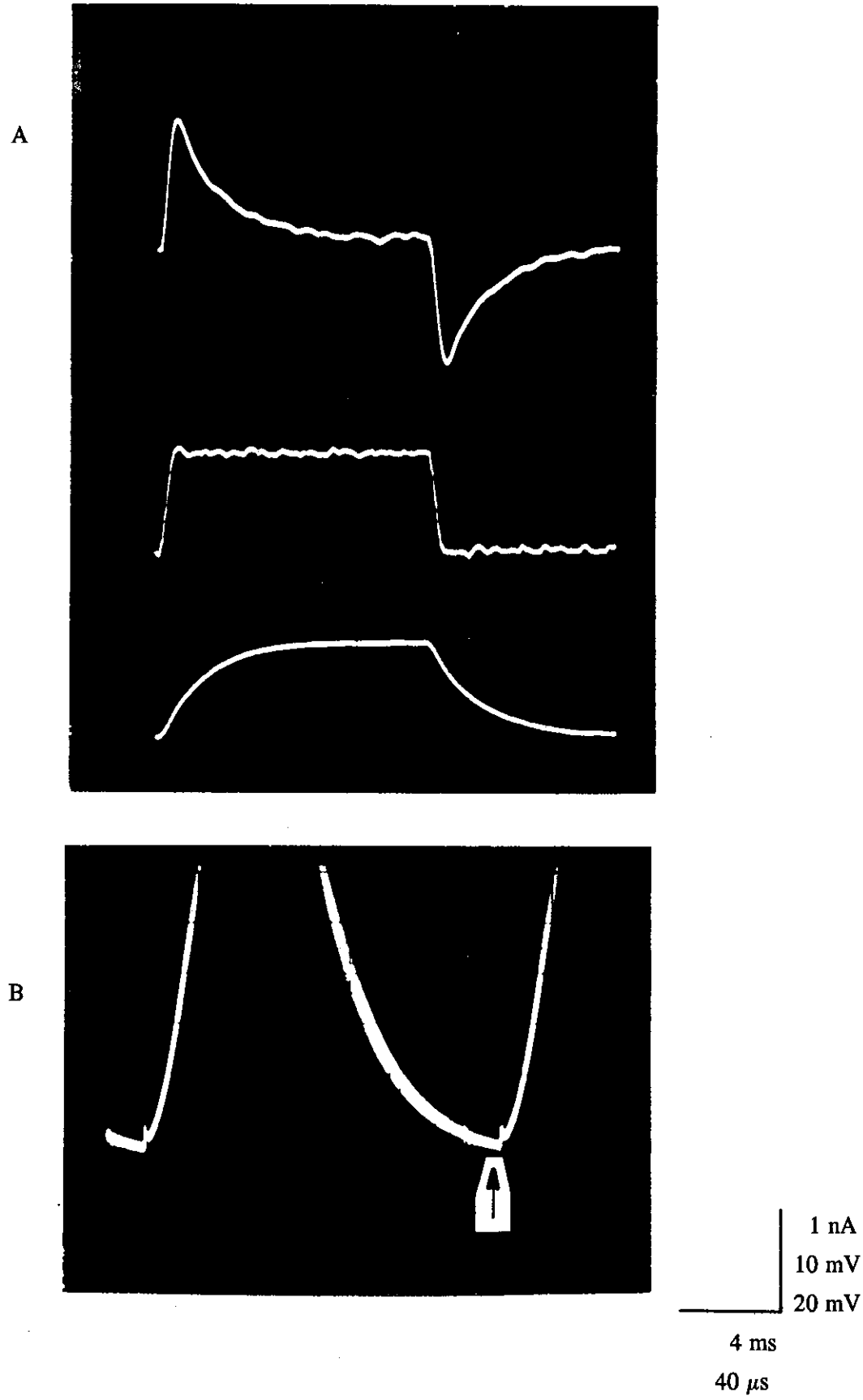


FIGURE 13 - INCORRECTLY SET UP dSEVC (i.e. "FALSE" CLAMP) IN A CELL MODEL

Fig. 14

Current and potential during dSEVC using the same suction electrode model used in Fig. 10.

Differences were: Gain was 0.7 nA/mV. Phase Shift and A-A Filter were both off. Sampling rate was 50 kHz.

Upper trace: Membrane current

Lower trace: Sampled membrane potential recorded from the 10.V_m output.

Noise: The current noise in the 3 kHz bandwidth was 80 pA peak-to-peak.

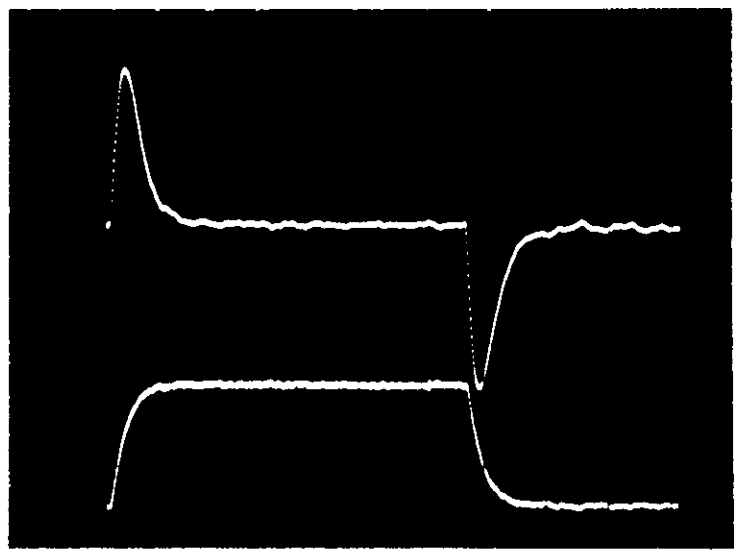


FIGURE 14 - CURRENT AND POTENTIAL RECORDING DURING dSEVC USING A SUCTION ELECTRODE MODEL

Minimum Sampling Rate and Maximum Gain

If the sampling rate is too slow the dSEVC will become unstable. This is because the long current-passing period allows the the membrane potential to charge right through and past the desired potential before the clamp has an opportunity to take a new sample of potential and adjust the current accordingly. The larger the cell membrane capacitance (C_m) the slower the sampling rate (f_s) which can be used for a given average gain (G). The stability criterion is (see Brenneke & Lindemann, 1974; Finkel & Redman, 1984)

$$0 < \frac{G}{C_m f_s} < 2$$

For critical damping we require

$$\frac{G}{C_m f_s} = 1$$

Thus for a given G, if C_m is small f_s must be large.

As an example, if G = 1 nA/mV and C_m = 100 pF, then f_s must be 10 kHz for critical damping. If f_s is less than 10 kHz in this example, the step response will overshoot and at 5 kHz the clamp will oscillate destructively.

If the sampling rate in this example cannot be as great as 10 kHz because the microelectrode response is too slow, then a lower value of G will have to be used to maintain stability.

Clamp Error

With finite gains in the voltage clamp circuit V_m does not quite follow V_c. The error is

$$\epsilon_1 = V_c - V_m$$

Similarly, if V_c is constant and the cell membrane conductance changes there is an error in the measurement of the current underlying the conductance change. This error is similar in percentage to the voltage error.

Usually the gain of the voltage clamp circuit can be increased so that ϵ_1 is 10% or less. The percentage error depends on the frequency of the command signal or of the conductance change. It is smallest for slow signals and DC, and largest for the fastest signals. Thus very fast transients (such as the rising phase of synaptic currents) will be clamped less well than slower transients (such as the decay phase of synaptic currents).

Gain

The clamp gain during dSEVC mode is given in nA/mV. This refers to how many nanoamps the output current will change by for each millivolt of difference between V_m (the membrane potential) and V_c (the command potential). The value indicated on the front panel is the average value. The average value depends upon the instantaneous gain during the current-passing period and upon the duty-cycle.

SPACE CLAMP

When interpreting the current measured during voltage clamp, due consideration should be given to the adequacy of the spatial extent of the membrane voltage control.

In general, measurements of currents generated more than 0.1 electrotonic lengths from the point of the voltage clamp electrode(s) will be subject to significant error. This problem is discussed in detail by Johnston and Brown (1983).

TEN-TURN POTENTIOMETERS

The ten-turn potentiometers used in the AXOCLAMP-2A are high-quality wirewound types.

An inherent problem of wirewound potentiometers is that the wire elements tend to oxidize. This condition is curable.

If a potentiometer becomes noisy, the potentiometer manufacturer recommends rapidly spinning the knob 20-30 times between full clockwise and full counterclockwise. This clears the oxide off the element and restores noise-free operation.

TEVC MODE

Description

In TEVC (Two-Electrode Voltage Clamp) mode the AXOCLAMP-2A acts as a conventional voltage clamp. ME1 is the voltage-recording electrode and ME2 is the current-passing electrode.

The output of the clamp is a voltage source (in contrast to SEVC modes in which the clamp output is a current source) which is connected to ME2. The voltage-clamp gain control is marked in units of V/V. This refers to how many volts the output will change by for each volt of difference between V_m (the membrane potential) and V_c (the command potential). For example, when the gain is at its maximum value of 10,000 V/V, a 100 μV difference between V_m and V_c would cause the output to shift by 1 V. If the resistance of ME2 was 10 MΩ there would be a current of 100 nA.

The best settings of the voltage-clamp parameters are found by setting up the best possible response to a step change in V_c. Usually, the ability of the voltage clamp to follow a step change in command is identical to the ability of the voltage clamp to follow a step change in membrane conductance (Finkel & Gage, 1985).

Factors affecting the voltage-clamp response are these:

The Gain control determines the steady-state accuracy and the response speed.

The Phase control introduces a combination of phase lag and phase lead (a zero) in the voltage-clamp amplifier.

The Holding Position control shifts the clamped membrane potential.

The Capacitance Neutralization setting of ME1 affects the voltage-clamp response. The Capacitance Neutralization setting of ME2 affects the current monitoring circuit at high frequencies and also has a small effect on the voltage-clamp response.

The Anti-Alais filter slows the microelectrode response and should not be used in TEVC mode.

Suggested Use

In Bridge mode set the Capacitance Neutralization of each microelectrode for the best step responses. This is important but not critical, and in order to be tolerant of changes in the microelectrodes' resistances which might occur during TEVC it is suggested that Capacitance Neutralization should be slightly underutilized.

Use a second-order or better lowpass filter to remove the high-frequency noise from I_2 (see Output Filter section).

Set the Gain and Anti-Alias Filter to minimum values. Switch the Phase control off. Switch off all current commands.

Use the Holding Position control to yield equal brightness in each of the two RMP Balance lamps. At this setting the command potential during voltage clamp will be equal to the resting membrane potential (RMP). Lock the Holding Position control if desired.

Switch into TEVC mode. Set up a repetitive step command. Monitor both $10.V_m$ and I_2. Increase the Gain as far as possible without causing overshoot in the step response. In cells whose membranes do not cause the same phase shift (90°) as a parallel RC cell model, the Phase control can be used to increase the maximum gain achievable. The Capacitance Neutralization setting of ME1 should not be altered during voltage clamp unless there is reason to believe the resistance of ME1 has altered.

Extremely Important Note - Coupling Capacitance

The most significant factor in achieving a good two-electrode voltage clamp is adequate prevention of interactions between the two electrodes. Coupling capacitance as low as 0.01 pF can destablize the response at high gain settings.

To minimize the coupling capacitance it is essential that a **grounded** shield be placed between the two microelectrodes and their headstages to prevent signals in ME2 being picked up by ME1. It should extend between the two electrodes to within a millimeter of the surface of the solution. It is possible to coat ME2 with a conductive paint which is then grounded. This procedure works well but has a minor disadvantage in that it vastly increases the capacitance at the input of the ME2 headstage, which may affect the high-frequency measurement of I_2 unless the capacitance neutralization of ME2 is properly set.

Fig. 15 shows the detrimental effects of only a small amount of coupling capacitance. The traces in Fig. 15A show the membrane current and voltage responses in a cell model when an extensive grounded shield was placed between the two electrodes. In Fig 15B a 2-3 mm wide gap in the shield caused high-frequency oscillations and noise. The back end of the electrodes were 40-50 mm apart. When the gap size was increased further the clamp went unstable.

Figure 15

The destabilizing effects of coupling capacitance. Traces were recorded in a cell model; R_m = 10 MΩ, C_m = 1 nF, $R_{e1} = R_{e2}$ = 10 MΩ, Gain = 1000 V/V, recording bandwidth = 10 kHz, Phase Shift and Anti-Alias Filter both off. 10 mV step command. Upper traces are I_2 (the membrane current). Lower traces are V_m. Electrodes were 40-50 mm apart.

A. Extensive grounded shielding between the two electrodes.

B. 2-3 mm gap in the grounded shield caused high-frequency oscillations.

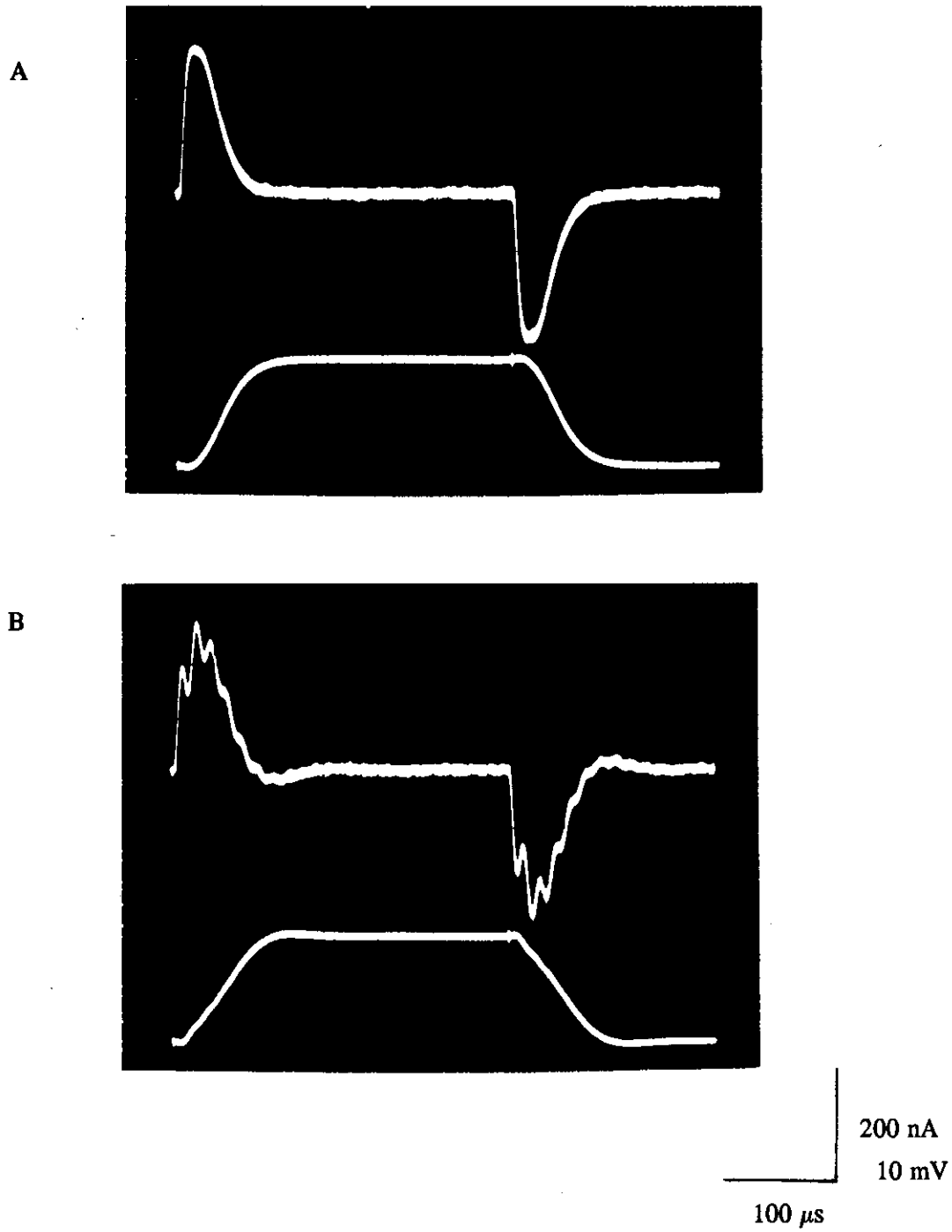


FIGURE 15 - AN EXAMPLE OF THE DESTABLIZING EFFECTS OF COUPLING CAPACITANCE

Saturation During The Capacitance Transient

The output voltage of the AXOCLAMP-2A main unit during TEVC is ± 30 V. This is usually sufficient to drive the current through ME2 required to charge the membrane capacitance during a step voltage change. However, for large steps in some cells the output may saturate and the time required to establish the step change will be longer than necessary.

Part of the reason for the saturation is that not all of the ± 30 V appears across the microelectrode. Some of it appears across the current-sensing resistor (R_o; see Fig. 4) in the headstage. If $R_e = R_o$ then ± 15 V appears across the microelectrode, but if $R_e < R_o$ the voltage across the microelectrode is even less.

To overcome this a headstage (designated HS-4) is available which has a relay inside it to automatically link out R_o whenever TEVC mode is selected. There are two advantages to using the HS-4 headstage. The first is that even in the linear operating region the time to establish a step voltage change is quicker, and the second is that larger step changes can be established without entering the nonlinear (i.e. saturating) region. The disadvantage is that the HS-4 headstage must be used in conjunction with a virtual-ground current-measurement headstage. This is because the normal built-in current monitors need R_o in order to operate.

Because it requires a virtual-ground headstage as well, we do not normally recommend the HS-4 headstage unless the experimental circumstances demand it. Contact Axon Instruments for more details.

Choosing the Microelectrode Resistances

If large currents must be passed, such as may occur during large depolarizations of excitable cells, then the resistance of ME2 should be as low as possible. If low-noise recordings are required, which would be necessary for resolving small transmitter-activated currents from the background noise, then the resistance of ME1 should be as low as possible.

If two headstages with different Hs are used, the one with the larger H (and therefore greater current-passing ability) should be used with ME2.

TRIGGERED CLAMPING

In some experiments it is desirable to switch into voltage clamp only when a specific event threshold is reached. For example, it may be desirable to switch into voltage clamp when the unclamped action potential goes above a predetermined level.

To do this an external device must be used to detect the event and signal its occurrence by putting out a logic HIGH. The logic HIGH is then applied to pin 5 or 6 of the Remote connector on the rear panel of the AXOCLAMP-2A. The AXOCLAMP-2A will then remain in voltage clamp mode until the logic HIGH is removed from pin 5 or 6 and a separate logic HIGH applied to pin 3 or 4 of the Remote connector.

TROUBLE SHOOTING

It has been our experience at Axon Instruments that the majority of troubles reported to us have been caused by faulty equipment connected to our instruments.

If you have a problem, please disconnect **all** instruments connected to the AXOCLAMP except for the oscilloscope and one headstage. Ground the headstage through the original test resistor supplied by Axon Instruments. If the problem persists, please call us for assistance.

UNITY-GAIN RECORDING - THIRD POINT

In normal operation both ME1 and ME2 can be used for unity-gain recording and current-passing. A third point in the preparation can be recorded from if virtual-ground current measurement is not being used. To do so, a unity-gain headstage (HS-2) is plugged into the Virtual-Ground connector on the rear panel. The voltage recorded appears on the IVIRT output. No current can be passed via the HS-2 headstage used in the Virtual-Ground connector. When plugged into the Virtual-Ground connector the input capacitance of the unity-gain headstage is 4 pF.

VIRTUAL-GROUND CURRENT MEASUREMENT

A Virtual-Ground headstage can be used to ground the preparation bath. All of the current flowing into the Virtual-Ground input is measured and a voltage proportional to the current is provided at the IVIRT output. The output gain is 10 mV/nA when the virtual-ground output attenuation (VG) is x1, 1 mV/nA when VG is x10, and 100 mV/nA when VG is x0.1

A Virtual-Ground headstage is not required for normal use of the AXOCLAMP-2A because built-in current-measurement circuits are provided for each microelectrode. However, in TEVC mode the current output of the Virtual-Ground headstage has slightly less high-frequency noise than the output of the built-in current-measurement circuit.

The Virtual-Ground circuit measures all currents into the preparation bath, hence special care must be taken to ensure that conducting connections to the preparation bath do not act as antennae which pick up hum. Saline-filled tubes act as excellent antennae. To prevent them carrying hum, long saline-filled tubes should have the saline pathway broken by an air-filled drip near the preparation.

More complete explanations and instructions are provided with the VG series of headstages.

10.V_m AND I_m OUTPUTS

The 10.V_m output is proportional to ten times the membrane potential (V_m). It is derived from the potential (V_1) recorded by ME1. Initially V_1 is amplified, then depending on the operating mode, one of two techniques is used to derive the 10.V_m signal from the amplified V_1 signal. In Bridge mode, the Bridge Balance technique is used to counter the effect of voltage drop (IR voltage drop) across ME1 during current passing so that only the membrane potential measured at the tip is passed to the 10.V_m output. In DCC or dSEVC mode samples of the amplified V_1 signal are taken after the IR voltage drop across ME1 due to the previous current pulse has completely decayed. Only the sampled values are passed to the 10.V_m output.

The maximum recording range of the 10.V_m output is $\pm$600 mV referred to the input. This range is centered on the zero value set by use of the Input Offset control. In Bridge mode this range includes the IR drop even though the IR drop may not be seen because the Bridge Balance is correctly set. The full $\pm$600 mV input-referred range is available in DCC and dSEVC modes irrespective of the current.

The I_m output is proportional to the membrane current. In Bridge, cSEVC and TEVC modes it is the continuous electrode current. In DCC and dSEVC modes, I_m is found by sampling the current during the current-passing period and multiplying by the duty cycle.

SPECIFICATIONS

MODES

Five main operating modes selectable by color-coded illuminated push buttons, or remotely. These are:

1. **Bridge**
2. **DCC:** Discontinuous Current Clamp
3. **dSEVC:** Discontinuous Single-Electrode Voltage Clamp
4. **cSEVC:** Continuous Single-Electrode Voltage Clamp
5. **TEVC:** Two-Electrode Voltage Clamp

MICROELECTRODE AMPLIFIERS (Two Channels)

Unity-Gain Headstages:

Standard is the HS-2L type. HS-2M types are the same except:
1) the noise is greater by about 20%
2) the capacitance neutralization range is extended.

HS-2MG types are similar to the HS-2M types except that the case is grounded instead of driven.

Hum (line-frequency pickup):

Less than 10 μV peak-to-peak, grounded input.

Headstage Current Gain (H):

Available in 5 values (specify two with order). Select on basis of cell input resistance (R_{in}) and maximum current capacity (I_{max}).

H = x0.0001 for ion-sensitive electrodes
H = x0.01 for R_{in} greater than about 300 MΩ
H = x0.1 for R_{in} about 30-300 MΩ
H = x 1 (standard) for R_{in} about 3-30 MΩ
H = x10 for R_{in} about 300 kΩ to 3 MΩ

These ranges are suggested for optimum performance. Some overlap is allowable.

Maximum Current:

I_{max} = 1000 x H nA.

Noise with grounded input:

5 μV rms measured with a 10 kHz single-pole filter in the measurement circuit.

Noise with a source resistance:

51 (47) μV rms measured with a 10(100) MΩ source resistance and capacitance neutralization adjusted for a 10(1) kHz bandwidth and with a 10 (1) kHz single-pole- filter in the measurement circuit. Values are for H = x1 (x0.1), HS-2L headstage.

1% Settling Time:

16(54) μs for a voltage step applied to the input via a 10(100) MΩ low-capacitance resistor and 16(60) μs for a current step into the same resistor. Capacitance neutralization adjusted for zero overshoot. Values are for H = x1 (x0.1).

Working Input Voltage Range: ±13 V for transients and steady state, protected to ±30 V.
Input Resistance: 10^{14}-10^{15} Ω, H = x 0.0001 (see note)*
10^{13} Ω, H = x .01
10^{12} Ω, H = x 0.1
10^{11} Ω, H = x 1
10^{10} Ω, H = x 10

*Note: For the x0.0001 headstage, the input resistance of each headstage is measured individually. The unique test results are supplied with each x0.0001 headstage.

Input Capacitance: Not relevant. See 1% settling time and noise specifications.

Input Leakage Current: Adjustable to zero.

Input Leakage Current vs. Temperature:

10	fA/	°C,	H = x0.0001
100	fA/	°C,	H = x0.01, x0.1
1	pA/	°C,	H = x1
10	pA/	°C,	H = x10

Offset Neutralization Range: ±500 mV. Ten-turn potentiometers.

Capacitance Neutralization Range:

HS-2L: -1 to 7 pF
HS-2M: -2 to 20 pF
HS-2MG: -4 to 18 pF

These values apply when headstage is used with microelectrode 1 amplifier. With microelectrode 2 amplifier the maximum values are doubled.

Buzz: Instantly increases capacitance neutralization to cause oscillation. Operated by spring-loaded pushbutton switch, footswitch or by Remote Buzz Duration control. The latter allows the Buzz duration to be set in the range 1-50 ms.

Buzz Duration: 1-50 ms when activated by the remote buzz control.

Clear: Forces $\pm I_{max}$ through the microelectrode. Spring-loaded toggle switch.

Bridge Balance Range: 10÷H MΩ/turn in Bridge mode. 1÷H MΩ/turn in cSEVC mode. Ten-turn potentiometers.

Digital Voltmeters:

Voltage Displays: ±1999mV. Separate meters for V_1 and V_2
Current Displays: ±19.99 pA, H = x 0.0001
±1.999 nA, H = x .01
±19.99 nA, H = x.0.1
±199.9 nA, H = x 1
±1.999 mA, H = x 10

Scaling is set by miniature panel switches. Display selections are I_1, I_2 and I_{virt}.

Currents exceeding the digital display range can be measured on the BNC outputs.

Outputs: $10 \cdot V_m$ and I_m are membrane voltage (gain = 10) and current recorded by microelectrode 1.
V_1 and I_1 are the continuous microelectrode 1 voltage and current.
V_2 and I_2 are microelectrode 2 voltage and current.
MONITOR is the output of the anti-alias filter (equals the input of the sampling device). Gain = 10. Baseline correction circuit automatically references Monitor trace to zero volts.

Gain of current outputs is 10 ÷ H mV/nA. Maximum output level is ±13V.

Current outputs indicate the **true** electrode current.

Output Lowpass Filter Cutoff:
0.1, 0.3, 1, 3, 10, 30 kHz.
Operates on V_m and I_m. Single-pole filter.

Output impedances are 500 Ω. ±10%

VOLTAGE CLAMP

10% - 90% Rise Time: The following values were measured using 10 MΩ and 1 nF in parallel to model the cell, 10 MΩ resistors to model the microelectrodes, and a 10 mV step command.

Rise Time in dSEVC mode = 100 μs.
Rise Time in TEVC mode = 30 μs.

Gain: Maximum in dSEVC mode is 100 x H nA/mV.
Maximum in cSEVC mode is 1000 x H nA/mV.
Maximum in TEVC mode is 10,000 mV/mV.
Range is 300:1, logarithmic scale.

Output compliance: ±25 V.

Phase Shift:

Time Constant (ms)	OFF	0.02	0.2	2	20	200
Lead range (ms)	0	0-0.04	0-0.4	0-4	0-40	0-400
Lag range (ms)	0	0-0.02	0-0.2	0-2	0-20	0-200

Anti-Alias Filter: Time constant range 0.2-100 μs

RMP Balance Indicators: Equal brightness indicates voltage clamping will be at resting membrane potential.

Blank: Stops clamp from responding to new inputs for the duration of a HIGH control signal on the BLANK ACTIVATE input. Used to reject stimulus artifacts.

Series Resistance Compensation:
Operates in cSEVC mode. Value set on Bridge potentiometer. External input at 100 mV/V can be used in TEVC mode.

SAMPLING CIRCUIT

Rate: 500 Hz to 50 kHz. Operates in DCC and dSEVC modes only.

Counter: 3-digit display to 99.9 kHz max. Blanked in continuous modes.

Sample Clock: Logic-level trigger output at the sampling rate.

Sample Acquisition Time: 1 μs (10 V step to 0.1%)

INTERNAL COMMANDS

Note: Commands from all sources sum linearly.

Voltage Clamp Step Command: $\pm$199.9 mV. Set on thumbwheel switch. Activated by a HIGH control signal on the STEP ACTIVATE input or by a front-panel switch.

Voltage Clamp Holding Position: Range $\pm$200 mV transmembrane potential. Ten-turn potentiometer.

Current Clamp Step Command: $\pm$199.9 x H nA. Set on thumbwheel as above.

DC Current Command: $\pm$100 x H nA. Ten-turn potentiometers.

EXTERNAL COMMANDS

Sensitivities:

Ext. VC command: 20 mV/V
Series resistance compensation: 100 mV/V
Ext. ME 1 (microelectrode 1) command: 10 x H nA/V
Ext. ME 2 (microelectrode 2) command: 10 x H nA/V
Input Impedance: 22 kΩ

Max. Input Voltages: $\pm$30 V for voltage-clamp commands
$\pm$60 V for current-clamp commands

CALIBRATION SIGNAL

A pulse equal in magnitude to the setting on the thumbwheel switch is superimposed on the voltage and current outputs for the duration of a HIGH control signal on the CAL ACTIVATE input.

BATH POTENTIAL COMPENSATION

Signal recorded by bath headstage or by an external amplifier is automatically subtracted from the intracellular measurements. If bath potential is not measured the system automatically reverts to using O V as the reference potential. Standard headstages (HS-2) work as bath headstages when plugged into the bath headstage connector.

VIRTUAL-GROUND CURRENT MEASUREMENT

A VG-2 virtual-ground headstage can be plugged into the connector provided. The current measured is the sum of all currents into the preparation. The correct operation of the AXOCLAMP is not affected by the use or nonuse of virtual-ground current measurement.

REMOTE

Logic HIGH control signals activate BUZZ and CLEAR of each microelectrode, and select between BRIDGE, DCC, SEVC and TEVC modes. 15-pin connector.

MODEL CELL

A model cell is provided with the AXOCLAMP-2A. Electrodes are 50 MΩ. The cell is 50 MΩ // 500 pF. A switch grounds the electrodes directly (BATH mode) or through the cell (CELL mode). Special plugs connect directly to the headstages.

GROUNDING

Signal ground is isolated from the chassis and power ground.

CONTROL INPUTS

Above 3 V is accepted as logic HIGH. Below 2 V is accepted as logic LOW. Inputs are protected to ±15 V.

HEADSTAGE DIMENSIONS

Case is 2.25 x 1.14 x 0.87" (57.2 x 29.0 x 22.1 mm). Mounting rod is 4" (102 mm) long. Available mounting rod diameters are 1/4, 5/16 or 3/8" (6.3, 7.0 or 9.5 mm). Specify required mounting rod diameter with order. Input sockets for the microelectrode, shield and ground are 0.08" (2 mm) diameter. Cable length is 10 feet (3 m).

CASE DIMENSIONS

7" (177 mm) high, 19" (483 mm) wide, 12.5" (317 mm) deep. Mounts in standard 19" rack. Handles are included. Net weight 18 lbs (8 kgs).

SUPPLY REQUIREMENTS

Line voltage:	100-125 V_{ac} or 200-250 V_{ac}. User selectable by an internal switch.
Line Frequency:	50-60 Hz.
Power:	20 W.
Fuse:	0.5 A slow. 5 x 20 mm.
Line Filter:	RFI filter is included.
Line Cord:	Shielded line cord is provided.

ACCESSORIES PROVIDED

Operator's & Service Manuals
2 mm plugs for use with headstages
Low-capacitance test resistor for each headstage.
Spare globes for Mode switches
Spare fuse
Footswitches to operate Buzz of both electrodes
Clamp-1 Model Cell
Remote Buzz Duration hand-held control

OPTIONAL ACCESSORIES (not required for normal operation)

HS-4 Relay-Switched Headstage.

Miniature relay inside headstage automatically bypasses the current-measuring resistor during two-electrode voltage clamp mode. In all other modes HS-4 headstage behaves like an HS-2MG headstage with H = x1. Must be used in conjunction with a VG-2 virtual-ground headstage.

VG-2 virtual-ground headstage.

Measures total bath current. The virtual-ground output attenuation (VG) is available in three values (specify with order): x 0.1, x1 (standard), and x10. The output (I_{virt}) is 10 ÷ VG mV/nA.

ORDERING INFORMATION

When ordering please specify:

1. Current gain (H) of two headstages provided
2. Gain and type of any extra headstages
3. Diameter (D) of headstage mounting rods.

Unless you specify otherwise the AXOCLAMP-2A will be supplied with one HS-2L x1 and one HS-2L x 0.1 headstage, each with D = $^5/_{16}$" (7.9 mm).

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