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# ClockGen

v1.1

Innovative Integration
... real time solutions!

## PMC Module with Precision Low Jitter Clock Generator and Four Channel Distribution Buffer

### FEATURES

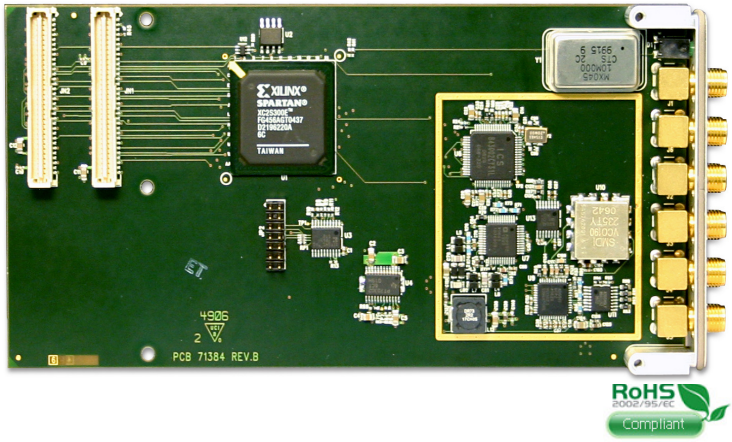
- Four Programmable Clock Outputs
- Output Ranges:
  100 KHz to 235 MHz
  (Optional) 100 KHz to 270 MHz
  (Optional) 100 KHz to 415 MHz
  (Optional) 100 KHz to 450 MHz
- 0.1 Hz resolution
- < 1 ps rms jitter in the VCO range (see description)
- External Reference Clock Input
- Lock to reference clock input from 2.3 kHz to 100 MHz
- Buffer and redistribute 1:4 an external clock input
- Optional high stability, 0.5 ppb reference clock
- Drives 50 ohm loads
- SMA connectors
- PCI Interface

### APPLICATIONS

- Sample rate generation
- System clock synchronization
- Frequency Translation
- Clock distribution

### SOFTWARE

- Turnkey virtual instrument application supplied, with source
- Windows/Linux drivers
- C++ libraries for integration into custom applications




### DESCRIPTION

The ClockGen is a precision clock generator on a PMC IO module for sample rate generation, system clock synchronization, and clock distribution. The four output clocks, external clock and reference clock inputs are front panel SMA connectors. Each output can drive a 50 ohm load.

For sample rate generation, the ClockGen PMC generates four clock outputs over a frequency range of 100 KHz to the maximum of the VCO. VCO options are available to support different frequency ranges. The clocks can be locked to a reference clock input or an optional Statum III (0.5 ppb) stable reference. The clock outputs have a tuning resolution of <1.0 Hz over the full output range.

In the clock distribution mode, the ClockGen PMC makes four low-skew copies of the input clock driven to the outputs. Clock rates for the distribution mode are DC to 350 MHz.

The ClockGen PMC generates output clocks that have jitter of less than 1 ps RMS, from the VCO minimum to the VCO maximum using integer divisors from 1 - 32. The even of these divisors resulting in symmetrical output signals and the odd divisors, asymmetrical outputs. These can be used as sample clocks for high frequency inputs and in under-sampling applications. For lower sample rates in the 100 KHz to 6.25 MHz range, jitter is <50 pS RMS.

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03/27/13

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# ClockGen

The application software for the ClockGen PMC allows complete configuration and control from its virtual instrumentation panel. Integration into system software is fully supported making the ClockGen a flexible solution to system clocking requirements.



This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| Product | Part Number | Description |
|---|---|---|
| ClockGen PMC Module | 80165-0 | PMC module with 4 programmable clock outputs, standard reference oscillator.<br>PLL Range 5.94-235 MHz |
| | 80165-1 | PMC module with 4 programmable clock outputs, 200 ppb Stratum III reference oscillator.<br>PLL Range 5.94-235 MHz |
| | 80165-2 | PMC module with 4 programmable clock outputs, standard reference oscillator.<br>PLL Range 11.72-415 MHz |
| | 80165-3 | PMC module with 4 programmable clock outputs, 200 ppb Stratum III reference oscillator.<br>PLL Range 11.72-415 MHz |
| | 80165-5 | PMC module with 4 programmable clock outputs, 200 ppb Stratum III reference oscillator.<br>PLL Range 11.56-450 MHz |
| SMA to BNC cable | 67048 | Coaxial cable (RG-179), 50 ohm, SMA to BNC, 1 meter |
| PMC - PCI Adapter | 80156 | PCI Carrier card for PMC modules |
| PMC - PCIe Adapter | 80166 | PCI Express Carrier card for PMC modules |

## ABSOLUTE MAXIMUM RATINGS

!Exposure to conditions exceeding these ratings may cause damage!

| Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|
| Supply Voltage, 3.3V to GND | +3.0 | +3.6 | V | |
| Operating Temperature | 0 | 70 | C | Non-condensing |
| Storage Temperature | -65 | +150 | C | |
| ESD Rating | - | 1k | V | Human Body Model |
| Vibration | - | 5 | g | 9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04) |
| Shock | - | 40 | g peak | Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04) |

| RECOMMENDED OPERATING CONDITIONS | | | | | |
|---|---|---|---|---|---|
| Parameter | Min | Typ | Max | Units | Conditions |
| Supply Voltage | +3.1<br>+4.5 | +3.3<br>+5.0 | +3.4<br>+5.5 | V | |
| Operating Temperature | 0 | | 60 | C | Non-condensing |

## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

| Parameter | | | Units | Notes |
|---|---|---|---|---|
| Input Voltage Thresholds (Ext Clock and Sync) | Vih (high) | 2.0 | V | min, 50 ohm terminated |
| | Vil (low) | 0.8 | V | max, 50 ohm terminated |
| Output Voltage Thresholds (output clocks) | Voh (high) | 2.6 | V | min, 50 ohm load |
| | Vol (low) | 0.5 | V | max, 50 ohm load |
| Output Skew | | 45 | ps | max, all 50 ohm loads |
| High Frequency Output Range | Frequency Range (other options available) | 5.94 | MHz | min, with standard VCO |
| | | 235 | MHz | max, with standard VCO |
| | Jitter | 1 | ps, RMS | max |
| Low Frequency Output Range | Frequency Range | 100 | KHz | min |
| | | 6.25 | MHz | Max recommend |
| | Jitter | 100 | ps, RMS | Max at 100 kHz output |
| | | 50 | ps, RMS | Max at 1 MHz output |
| Resolution | | 0.1 | Hz | All ranges |
| Frequency Error | | 0.001 | % | Phase Locked to Sync Input |
| Additive Jitter in Clock Distribution Mode | | 500 | fs | RMS additive noise when used in clock distribution mode. |
| | | | | |
| High Stability Reference Clock Option | Stability | 0.5 | ppb | 24 hours stability |
| | Warmup time | 2 | minutes | min |
| Power Consumption | | 4.5 | W | 3.3V supply @ 30 mA; 5V supply @ 880 mA |
| Mean time between failures (MTBF) | | | | 36975.24 hours |

# ClockGen

# ClockGen

## Standard Features

| Outputs | |
|---|---|
| Outputs | 4 |
| Connectors | SMA |
| Output Type | Single ended, LVCMOS |
| Output Impedance | 50 ohm |
| Clock Generation Range | 100 KHz to 235 MHz |
| Clock Generation Resolution | 0.1 Hz |
| Clock Distribution Frequency Range | DC to 350 MHz |

| External Clock Input | |
|---|---|
| Frequency Range | DC to 350 MHz |
| Connector | SMA |
| Input Type | Single ended, LVCMOS |
| Input Impedance | 50 ohm |

| Sync Input | |
|---|---|
| Frequency Range | 2.6 kHz to 100 MHz |
| Connector | SMA |
| Input Type | Single ended, LVCMOS |
| Input Impedance | 50 ohm |

| Host Interface | |
|---|---|
| Type | PCI, 2.1 |
| Compatibility | 32-bit, 66 MHz, 3V or 5V |
| Connectors | PMC Pn1 and Pn2 |

| Physicals | |
|---|---|
| Form Factor | Single width IEEE 1386 Mezzanine Card |
| Size | 75 x 150 mm |
| Spacing | 10 mm to host card |
| Weight | 80 grams |

# ClockGen

## Architecture and Features

The ClockGen PMC is used to provide clocks for high performance digitizing, communications and test equipment. Its function is the generation, synchronization and distribution of precision, low noise clocks that are typically used for digitizing, signal generation and communications.

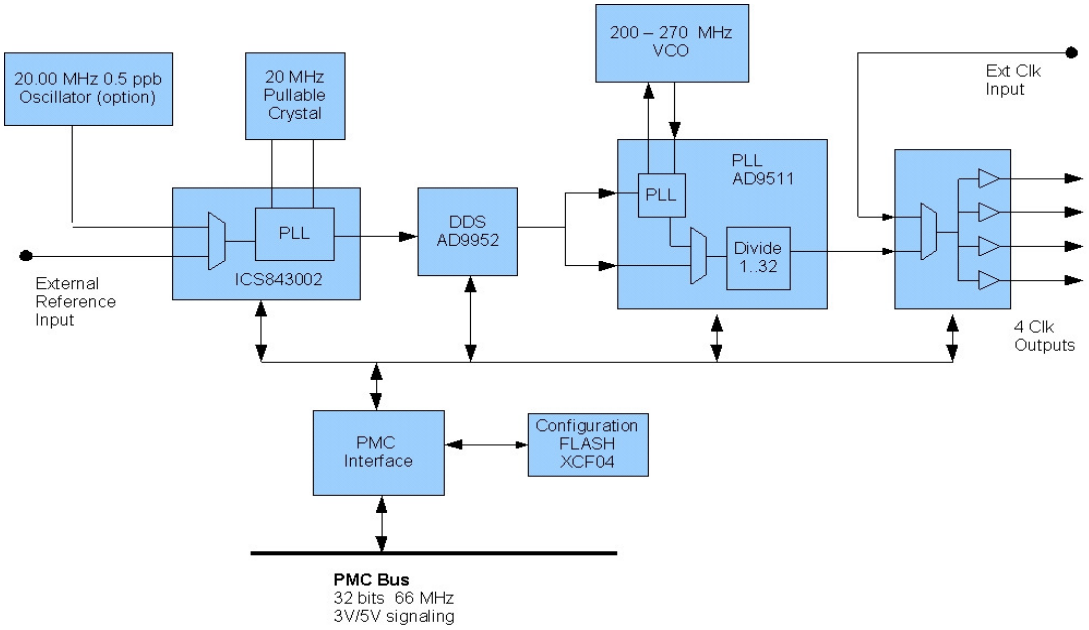



**Figure 1. ClockGen Block Diagram**

The ClockGen architecture combines a synchronization PLL, a high resolution DDS (Direct Digital Synthesizer) and a low noise PLL as shown in the block diagram. This allows the ClockGen to lock to a system reference clock then generate 4 identical output clocks that are low noise, programmable over the range of 100 KHz to 235 MHz. (Special ranges may be custom ordered.)

The ClockGen has two ranges: low range from 100 KHz to 6.25 MHz and high range from 5.94 MHz to 235 MHz. The low range uses the DDS output direct to the output drivers, while the high range uses the PLL output to the output drivers. The high range has the distinct advantage of typical jitter less than 1 ps RMS. In the low range, the clock jitter is typically 50 ps RMS over the 1 to 6.25 MHz range.

The flexibility of the ClockGen PMC is a result of the reference clocks that may be used by the PLL and DDS. In addition to an optional on-card reference, with a very stable 0.5 ppb option, the DDS can use an external sync input as its reference. This allows the DDS to generate clocks from 100 KHz to 20 MHz with 0.01 Hz resolution. The final PLL stage uses the DDS output as a reference clock, making it capable of a tuning range from 5.94 to 235 MHz with 0.10 Hz resolution. A final stage has a programmable divisor from 1 to 32 before the output driver.

Some of the useful operations that can be done with ClockGen PMC are

- Lock to a System Reference Clock

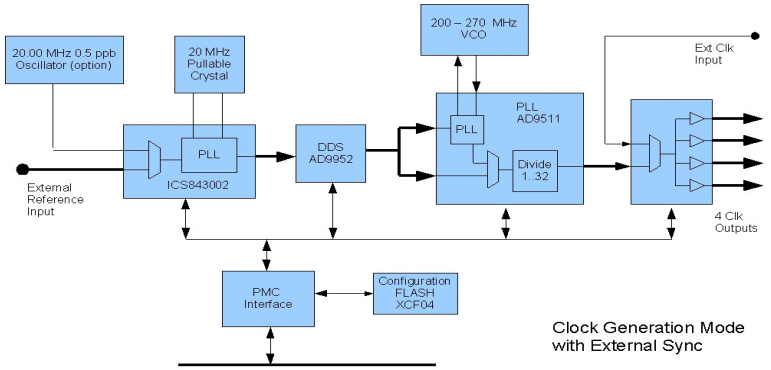
# ClockGen

- Phase lock to inputs from 2.3 kHz to 100 MHz

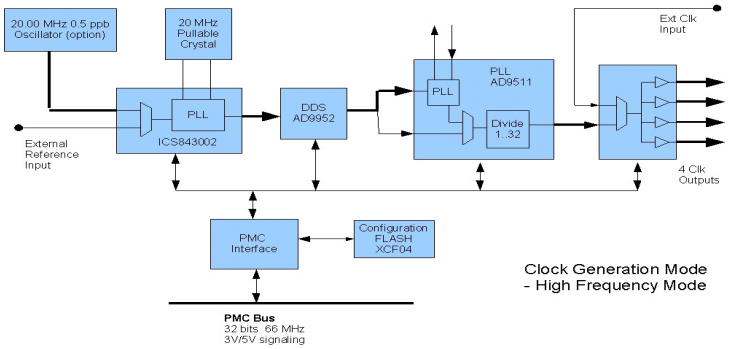
- Translate Clock Rates
  - Output clocks may be generated from any sync input (2.3k to 100 MHz) resulting in sample clocks from 100 KHz to 235 MHz.

- Generate Precision Clocks
  - Programmable clock generation with low jitter , typically less than 1 ps RMS.

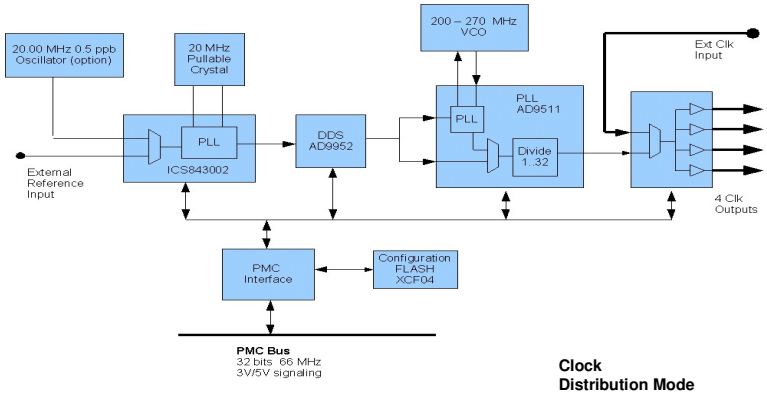
- Distribute Clocks
  - Distribute an input clock with 1:4 fanout and low skew.




Clock Generation Mode with External Sync




Clock Generation Mode - High Frequency Mode




**Clock Distribution Mode**

The clock synchronization function allows ClockGen to synchronize its clocks to an external reference such as a GPS time or system clock to eliminate sample skew and clock creep over time. The synchronization function also allows frequency translation for mixed clock rate systems. Many digitizing devices, such as Sigma-Delta converters, require clocks that are multiples of the sample rate. The ClockGen synchronization function allows it to lock to the input clock and generate a synchronous sample clock for these devices.

In the clock distribution mode, the ClockGen uses the output driver as a 1:4 fanout. The external clock input is driven to all outputs. Additive jitter is <0.45 ps RMS typical.

The ClockGen output drivers are capable of driving a 50 ohm load. SMA connectors on the front panel are used for all inputs and outputs.

# ClockGen

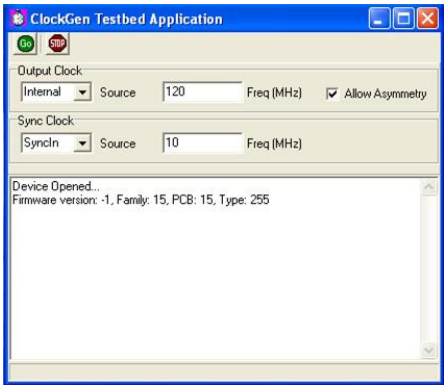



**Illustration 1: ClockGen Testbed Virtual Instrument**

## Software Tools

Virtual instrument software for the ClockGen PMC allows full configuration and control of the Clockgen features. This software application is provided with ClockGen.

Software development tools for the ClockGen PMC module provide comprehensive support including device drivers and card controls that allows developers to integrate ClockGen into instrumentation and test systems. Software classes provide C++ developers a powerful, high-level interface to the card that makes the card easier to integrate into applications than older techniques.

Support for MS Visual C++ and Borland (CodeGear) C++ is provided. Windows and Linux support is available.

## Features and Usage

The most-commonly used features of the ClockGen are exposed through four user-accessible methods of the ClockGen object within the Malibu board libraries. Manipulation of these basic methods are sufficient to address common timebase generation and routing requirements.

## Clock Source

The `Clockgen::OutputClock` method selects the source for the output clock produced by the board. If the source is set to `ClockGen::oExternal`, then a user-supplied LVCMOS clock signal injected into the Ext Clock connector (J6) is buffered and distributed to the output connectors J2, J3, J4 and J5. However. if the source is set to `ClockGen::oInternal`, then the clock signal produced by the onboard AD9511 PLL is buffered and driven to the output connectors on the board. This functionality is controlled by the *Output Clock* | *Source* combo box within the testbed application.

**Unusable Frequencies – Symmetrical Only**

| Lower (MHz) | Upper (MHz) |
|---|---|
| 117.5 | 190 |
| 58.75 | 95 |
| 39.17 | 45.7 |
| 29.3 | 31.67 |

**Unusable Frequencies -Asymmetry Allowed**

| Lower (MHz) | Upper (MHz) |
|---|---|
| 78 | 190 |
| 47 | 63 |

## Clock Frequency

When the clock source is `ClockGen::oInternal`, the frequency of the output clock is controlled via the `ClockGen::Frequency` method. For frequencies below 6.25 MHz, the AD9511 is configured for pass-through operation and the output clock is generated by the AD9952 DDS. In this mode, output jitter will be higher (approximately 50 pS), but frequency resolution is approximately 0.1 Hz.

For frequencies above 5.93 MHz, the output clock will be generated by the AD9511. In this mode, output jitter will be less than 1 pS, and frequency resolution will be < 1 Hz. However the frequencies listed in the tables cannot be generated, due to VCO operational restrictions. If operation in one of these bands is required, Innovative Integration can substitute alternative VCO devices which shift the range of unusable frequencies into an unimportant band.

This functionality is controlled by the *Output Clock* | *Frequency* edit box

within the testbed application.

When using the internal clock to generate frequencies above 5.93 MHz, the AD9511 is restricted to generation of frequencies within the operating range of the source VCO (190-235 MHz standard) post-divided by integers between 1 and 32. Use of even divisors will result in generation of a 50% duty cycle clock, whereas odd-divisors will create an asymmetric clock with a 33% duty cycle. The appropriate divisor based on the requested output frequency is automatically selected, but the `AllowAsymmetricDutyCycle` method may be used to control whether frequencies resulting in an asymmetric clock are permitted.

## Sync Clock

When the clock source is `ClockGen::oInternal`, the clock signal generated by the board is synchronous with the output of the onboard ICS843002 synchronization PLL. The synchronization PLL may be driven by a user-supplied reference clock injected into SMA connector J1, or by an onboard, low drift, 20 MHz TCXO crystal. Set the `ClockGen::SyncSource` method to `ClockGen::sSync` to use the reference clock supplied to connector J1 or to `ClockGen::sTcxo` to use the onboard TXCO oscillator as the reference clock. This functionality is controlled by the *Sync Clock | Source* combo box within the testbed application.

Since the sync reference clock may be supplied externally or a custom TCXO could be used, application code must explicitly specify the frequency of the sync reference clock via the `ClockGen::SyncFrequency` method. This is used internally to adjust the PLL within the ICS843002 to lock to the incoming reference clock. This functionality is controlled by the *Sync Clock | Frequency* edit box within the testbed application.

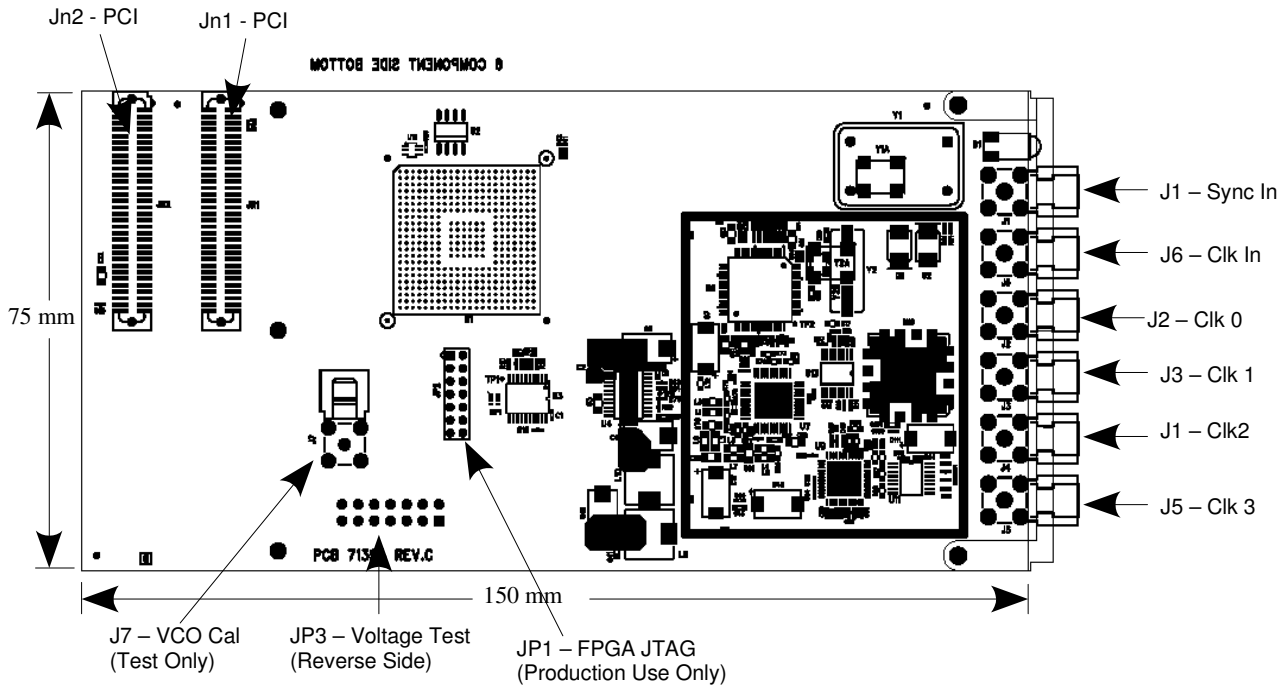
## Output Control

The outputs on connectors J2, J3, J4 and J5 may be programmed to clock normally, be driven into an active (`oActive`), continuous low state (`oLow`) or be placed into tri-state (`oTristate`) through use of the `ClockGen::OutputEnable` method. This facility is controlled by the Start and Stop buttons within the testbed application.

## Mechanicals

The ClockGen is a standard PMC module conforming to IEEE1384 specification.

# ClockGen




## Connectors

**Table 1. Connector Information**

| Reference | Type | Function | Mating Connector/Cable |
|---|---|---|---|
| J1 | SMA: Amphenol 132136 | Sync Input | Amphenol 132195 or equivalent<br>SMA to BNC Cable: II P/N 67048 |
| J2 | SMA: Amphenol 132136 | Clock Output 0 | Amphenol 132195 or equivalent<br>SMA to BNC Cable: II P/N 67048 |
| J3 | SMA: Amphenol 132136 | Clock Output 1 | Amphenol 132195 or equivalent<br>SMA to BNC Cable: II P/N 67048 |
| J4 | SMA: Amphenol 132136 | Clock Output 2 | Amphenol 132195 or equivalent<br>SMA to BNC Cable: II P/N 67048 |
| J5 | SMA: Amphenol 132136 | Clock Output 3 | Amphenol 132195 or equivalent<br>SMA to BNC Cable: II P/N 67048 |

| | | | |
|---|---|---|---|
| J6 | SMA: Amphenol 132136 | Clock Input | Amphenol 132195 or equivalent<br>SMA to BNC Cable: II P/N 67048 |
| J7 | SMB: AMP 414026-2 | VCO Calibration test output | SMB to BNC Cable: II P/N 67021 |
| Jn1, Jn2 | PMC: Molex 71436-2864 | PCI 32-bit | |

**PMC PCI Connector (JN1)**
JN1 is used for part of the PCI interface and power to the PMC.

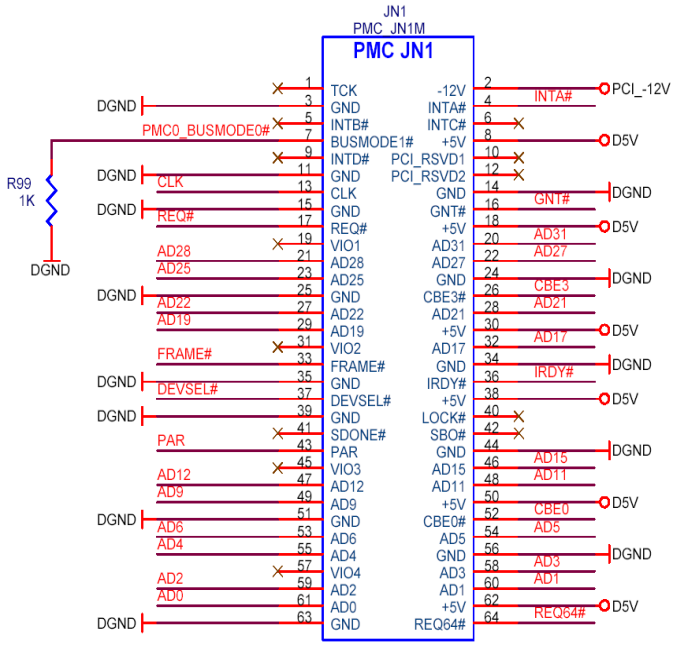



**Figure 1. PMC ClockGen JN1 Connector Schematic**

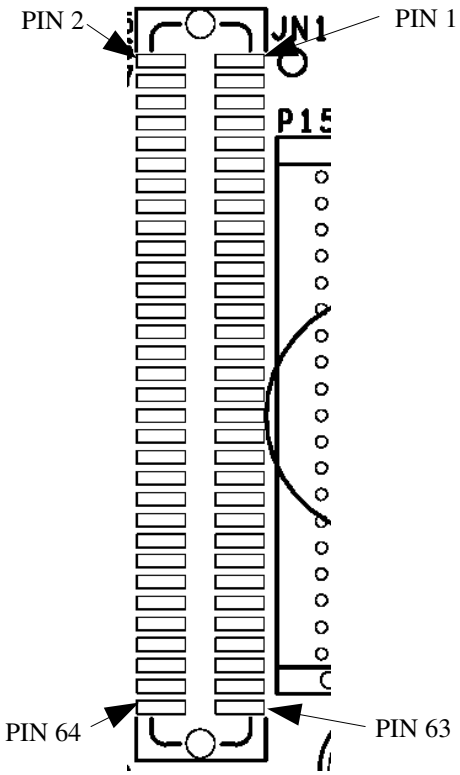



**Figure 2. PMC ClockGen JN1 Orientation (Bottom View)**

# ClockGen

**Table 2. PMC ClockGen JN1 Connector Pinout**

| Pin | Signal | Direction |
|---|---|---|
| 1 | No Connect | - |
| 2 | -12V from host | Power |
| 3 | Digital Ground | Power |
| 4 | INTA – interrupt to host | Out |
| 5 | No Connect | - |
| 6 | No Connect | - |
| 7 | PMC Busmode 1, configured as PCI | Out |
| 8 | 5V from host | Power |
| 9 | No Connect | - |
| 10 | No Connect | - |
| 11 | Digital Ground | Power |
| 12 | No Connect | - |
| 13 | PCI clock – 0-66 MHz | Input |
| 14 | No Connect | - |
| 15 | No Connect | - |
| 16 | GNT – PCI bus grant, active low | Input |
| 17 | REQ – PCI bus grant, active low | Output |
| 18 | 5V from host | Power |
| 19 | No Connect | - |
| 20 | AD31 | I/O |
| 21 | AD28 | I/O |
| 22 | AD27 | I/O |
| 23 | AD25 | I/O |
| 24 | Digital Ground | Power |
| 25 | Digital Ground | Power |
| 26 | CBE3 | I/O |
| 27 | AD22 | I/O |
| 28 | AD21 | I/O |

# ClockGen

| Pin | Signal | Direction |
|---|---|---|
| 29 | AD19 | I/O |
| 30 | 5V from host | Power |
| 31 | No Connect | - |
| 32 | AD17 | - |
| 33 | FRAME# | I/O |
| 34 | Digital Ground | Power |
| 35 | Digital Ground | Power |
| 36 | IRDY# | I/O |
| 37 | DEVSEL# | I/O |
| 38 | 5V from host | Power |
| 39 | Digital Ground | Power |
| 40 | No Connect | - |
| 41 | No Connect | - |
| 42 | No Connect | - |
| 43 | PAR | I/O |
| 44 | Digital Ground | Power |
| 45 | No Connect | - |
| 46 | AD15 | I/O |
| 47 | AD12 | I/O |
| 48 | AD11 | I/O |
| 49 | AD9 | I/O |
| 50 | 5V from host | Power |
| 51 | Digital Ground | Power |
| 52 | CBE0 | I/O |
| 53 | AD6 | I/O |
| 54 | AD5 | I/O |
| 55 | AD4 | I/O |
| 56 | Digital Ground | Power |
| 57 | No Connect | - |

# ClockGen

| Pin | Signal | Direction |
|---|---|---|
| 58 | AD3 | I/O |
| 59 | AD2 | I/O |
| 60 | AD1 | I/O |
| 61 | AD0 | I/O |
| 62 | 5V from host | Power |
| 63 | Digital Ground | Power |
| 64 | REQ64# | I/O |

# ClockGen

**PMC PCI Connector (JN2)**
JN2 is used for part of the PCI interface and power to the PMC.

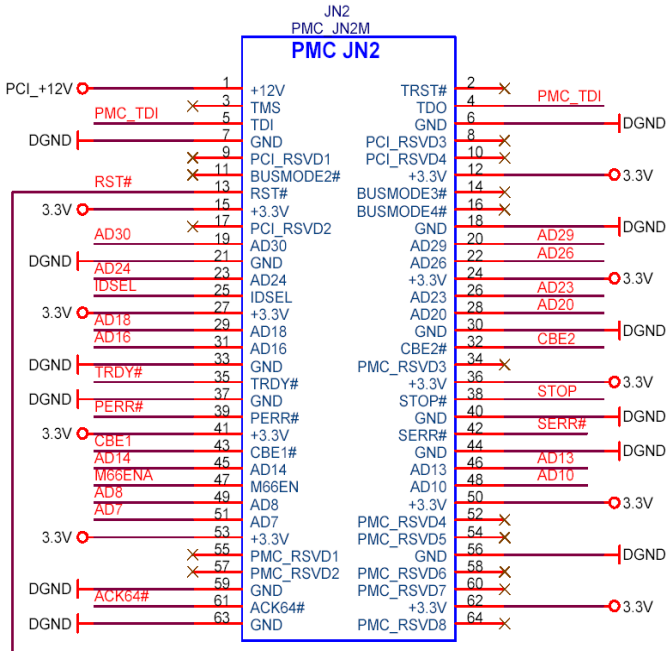



**Figure 3. PMC ClockGen JN1 Connector Schematic**

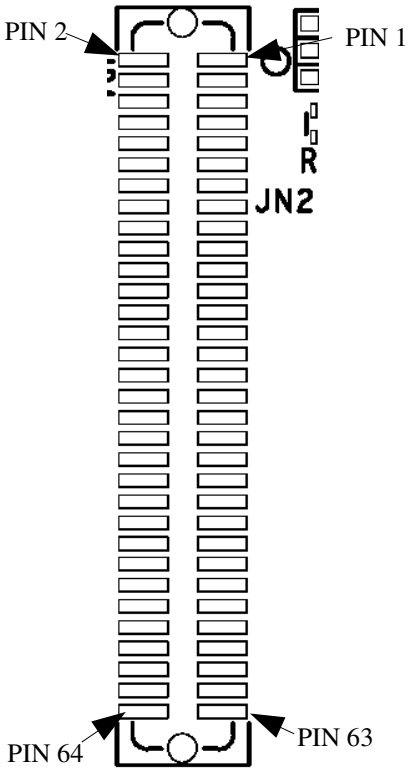



**Figure 4. PMC ClockGen JN1 Orientation (Bottom View)**

**Table 3. PMC ClockGen Jn2 Connector Pinout**

| Pin | Signal | Direction |
|---|---|---|
| 1 | +12 from host | Power |
| 2 | No Connect | - |
| 3 | No Connect | - |
| 4 | PMC JTAG TDO | I |
| 5 | PMC JTAG TDI | O |
| 6 | Digital Ground | Power |

# ClockGen

| Pin | Signal | Direction |
|---|---|---|
| 7 | Digital Ground | Power |
| 8 | No Connect | - |
| 9 | No Connect | - |
| 10 | No Connect | - |
| 11 | No Connect | - |
| 12 | 3.3V from host | Power |
| 13 | RST# | I |
| 14 | No Connect | - |
| 15 | 3.3V from host | Power |
| 16 | No Connect | - |
| 17 | No Connect | - |
| 18 | Digital Ground | Power |
| 19 | AD30 | I/O |
| 20 | AD29 | I/O |
| 21 | Digital Ground | Power |
| 22 | AD26 | I/O |
| 23 | AD24 | I/O |
| 24 | 3.3V from host | Power |
| 25 | IDSEL | I |
| 26 | AD23 | I/O |
| 27 | 3.3V from host | Power |
| 28 | AD20 | I/O |
| 29 | AD18 | I/O |
| 30 | Digital Ground | Power |
| 31 | AD16 | I/O |
| 32 | CBE2 | I/O |
| 33 | Digital Ground | Power |
| 34 | No Connect | - |
| 35 | TRDY# | I/O |

# ClockGen

| Pin | Signal | Direction |
|---|---|---|
| 36 | 3.3V from host | Power |
| 37 | Digital Ground | Power |
| 38 | STOP# | I/O |
| 39 | PERR | O |
| 40 | Digital Ground | Power |
| 41 | 3.3V from host | Power |
| 42 | SERR | O |
| 43 | CBE1 | I/O |
| 44 | Digital Ground | Power |
| 45 | AD14 | I/O |
| 46 | AD13 | I/O |
| 47 | M66EN | O |
| 48 | AD10 | I/O |
| 49 | AD8 | I/O |
| 50 | 3.3V from host | Power |
| 51 | AD7 | I/O |
| 52 | No Connect | - |
| 53 | 3.3V from host | Power |
| 54 | No Connect | - |
| 55 | No Connect | - |
| 56 | Digital Ground | Power |
| 57 | No Connect | - |
| 58 | No Connect | - |
| 59 | Digital Ground | Power |
| 60 | No Connect | - |
| 61 | ACK64# | I/O |
| 62 | 3.3V from host | Power |
| 63 | Digital Ground | Power |
| 64 | No Connect | - |

# ClockGen

## Applications Information

## Installation

The PMC ClockGen can be used on IEEE 1384 compatible PMC sites. The PCI interface supports 3.3V signaling with clock rates up to 66 Mhz and is 32-bit data path. The card is not compatible with 5V PCI signaling.

The power consumption of the module is about 4.5W total. The PMC requires 3.3 V and 5V from the bus for operation. The card may require forced air when ambient temperature exceeds 60C of about 5 CFM.

Each installation should be reviewed to verify that the operating temperature does not exceed 70 C on the card. The hottest point on the card is usually under the EMI shield. For accurate measurements, attach thermocouples to the underside of the card on the side opposite the EMI cover near the center of the card.

Excessive power supply noise can compromise the noise performance of the ClockGen. On-card power regulation provides clean power for most installations. Exceptionally noisy devices like fans and disk drives may cause spikes and should not share power or ground returns with the ClockGen.

## Standalone Operation

The ClockGen module has been designed to operate in a PCI system with the host software providing the configuration and controls. Software is provided to use the ClockGen as a virtual instrument in this environment.

Standalone operation can be provided as a customization to the module. In this mode, the FPGA is reconfigured so that it can configure the module to a specific operating mode. Contact Innovative sales for details on customization.

## Securing the Module

The card may be secured to the host card with two standoffs and four screws as shown. The Digikey number is provided (www.digikey.com) for convenience; many suppliers have these standardized screw and standoff sizes.

For high vibration applications, screws should be mounted with locking compound such as Loctite.

**Table 4. PMC Mounting Hardware**

| Description | Quantity | Digikey Part Number |
|---|---|---|
| Metric pan head screw, M3x5, 3mm x 5mm | 4 | H742-ND |
| Threaded Standoff, 10mm with 3mm thread | 2 | 4391K |

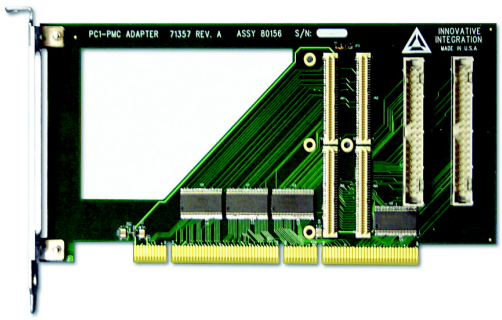
# ClockGen

## Cables

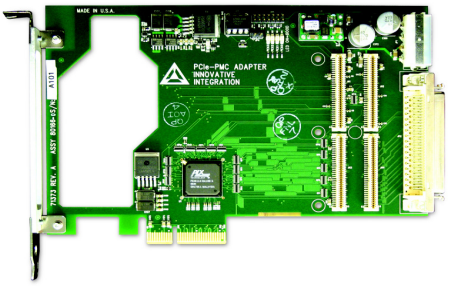
The ClockGen PMC uses SMA connectors for all input and output signals. Coaxial cables with 50 ohm characteristic impedance should be used with the ClockGen PMC. Innovative has a standard SMA to BNC cable, 1 meter in length (Innovative part number 67048).

## PMC Adapter Cards

The ClockGen PMC can be used in standard desktop systems by using a PMC to PCI adapter card (Innovative part number 80156) or a PMC to PCI Express adapter card (Innovative part number 80166).




**PMC to PCI Adapter (P/N 80156)**




**PCIe to PMC Adapter (P/N 80166)**

# ClockGen

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