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Ultrawideband PMC Hardware Manual

GENERAL

The PMC UWB is a member of the Velocia PMC family. These PMC modules have many common features such as the PCI interface, application logic attached to the IO, SelectMap application logic loading, local memories for data buffering and computation. The data moving architecture is built around a packet mechanism that is used to guide the data to/from devices in the system. J4 and XMC interfaces provide private, high-speed connections to the host system.

The PMC UWB has 2 channels of 210 MSPS A/D, an application FPGA and buffer memory. Module-specific clock mechanism allows two external input clocks that may be used by the A/D or divided and as a reference to the PLL.

Variants

None at this time. Possible variants include upgrades to the FPGA for size and/or speed. A VP30, VP40 (standard) or VP50 may be used on the module, but require unique logic images.

Interrupts

PMC Digital Receiver uses one interrupt on the PCI bus. This is always requested by the card at plug-n-play time.
Interrupt sources to the PCI bus are enabled in the PCI bus control register.

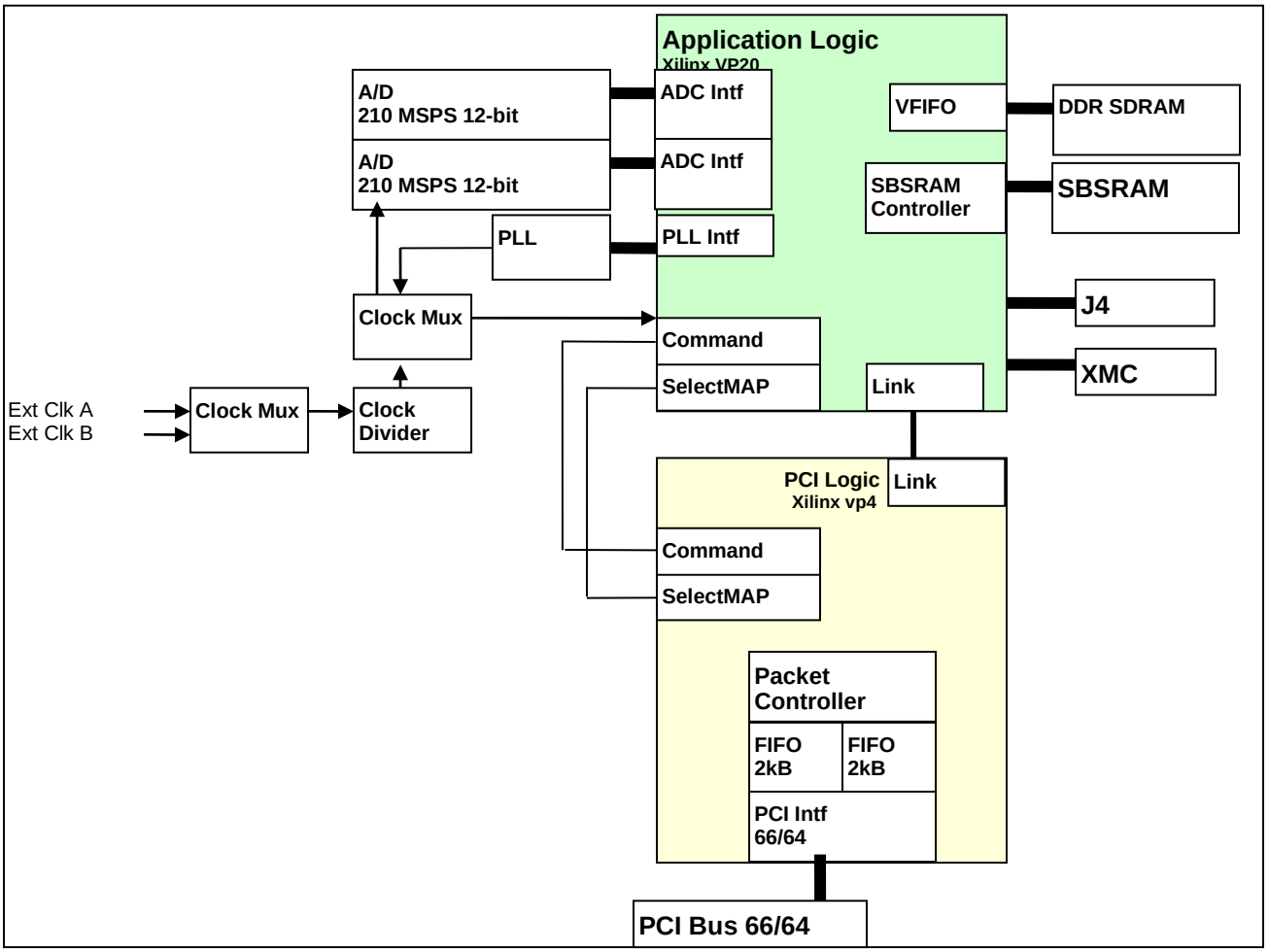
PCI bus Interface

Resource requirements

PMC UWB requires two BARs in memory space: BAR0 is the PCI registers, BAR1 are the application registers. One interrupt from the card has multiple functions and is reported using an interrupt status register. These resources are requested as part of the Plug-n-Play boot operation and are not programmable.

Failure to allocate these resources will cause erratic performance. Windows will NOT report the failure to allocate resources and the user should use care during installation that the resources are available and properly allocated.

Block Diagram



Functions of the PCI FPGA

PCI Interface

Flash Programming

USER FPGA Interface
- **Loading**
- **Reset**
- **Register Control**
- **Rocket I/O Payload Stream**

DSP (N/A for this board)
- **Loading (HPI Interface)**
- **Reset**

Calibration ROM

Security ROM

Functions of the USER FPGA

PCI FPGA Interface
- **Reset Input**
- **Register Control**
- **Rocket I/O Payload Stream**

Clock Source Control
- **External Clocks**
- **Synthesizer**
- **ADC's**

ADC Channel Operation
- **Shutdown**
- **Gain Selection (Programmable Gain Amps)**
- **Gain/Offset Correction**
- **Triggering**

DDR SDRAM

ZBT SRAM

XMC Interface

J4 Interface

PCI Interface Logic

The PCI Interface Logic is standardized across the PMC module products with the intention that all modules use the same FPGA logic image. This should reduce engineering support effort as a bug fix for PCI only needs to be implemented once in the one logic image that goes into all the PMC products.

Assumptions and Constraints:

All PMC modules must use the same pin out for the PCI FPGA.

Any added PCI features must use previously unused FPGA pins so that the new PCI logic will be backward compatible to previous modules.

It is OK to leave some features unused, as long as the pins for that feature are terminated (or left open) as appropriate for the FPGA logic.

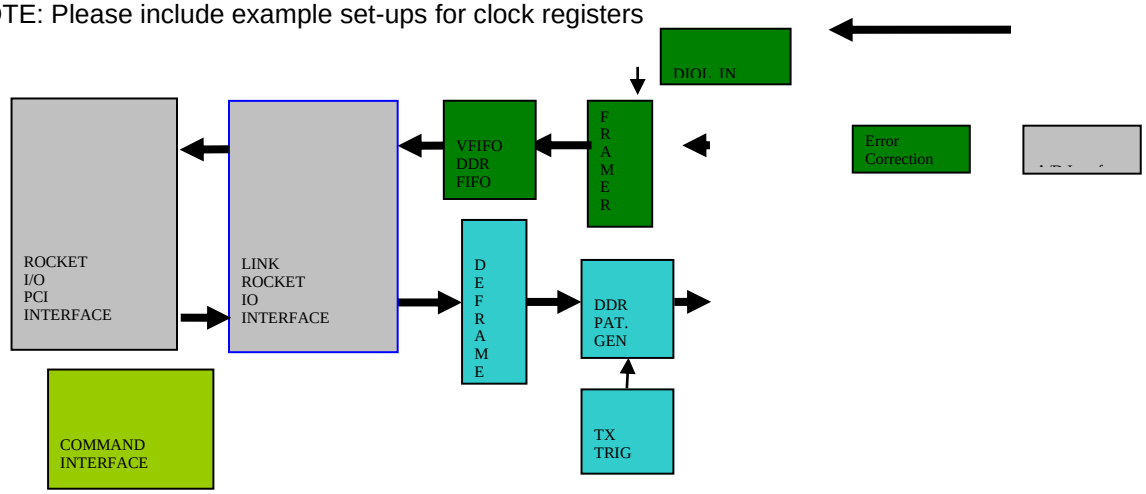
PCI Interface Documentation:

Because the interface is consistent across the PMC products, it is documented separately in one document called PCI_Manual, which is archived in SourceSafe under PMC Modules/Generic Items/Docs/Internal. This greatly simplifies maintenance of the documentation, avoiding redundant (and possibly conflicting) copies of the same information.

Application FPGA Logic

This section describes the Application FPGA which is specific to each board type, and may be custom programmed by customers. There are standardized modules for peripherals such as the memories and ADC's, but the interior modules may be varied according to customer needs.

NOTE: Please include example set-ups for clock registers



USER FPGA Register Map

Offset		Function
0x00	R	User FPGA code version
0x01	R/W	Control Reg 0
0x02	R/W	*test*
0x03	R/W	A/D Gain channel 0
0x04	R/W	A/D Gain channel 1
0x05	R/W	--
0x06	R/W	--
0x07	R/W	A/D Offset channel 0
0x08	R/W	A/D Offset channel 1
0x09	R/W	--
0x0A	R/W	--
0x0B	R/W	Packet Manager channel enables
0x0C	R/W	Packet Manager channel destinations
0x0D	R/W	*Matlab BSP*
0x0E	R/W	ZBT SRAM address
0x0F	R/W	ZBT SRAM data
0x10	R/W	Clocks & Frequency Synthesizer
0x11	R/W	A/D shutdown
0x12	R/W	Clock selects
0x13	R/W	J4 test register
0x14	R/W	*Matlab BSP*
0x15	R/W	*Matlab BSP*
0x16	R/W	*Matlab BSP*
0x17	R/W	Trigger Control A/D 0
0x18	R/W	Trigger Control A/D 1
0x19-- 0x1F	R/W	---
0x20	R/W	Packet Header channel A/D 0
0x21	R/W	Packet Header channel A/D 1
0x22 – 0xBF	R/W	*unused*
0xC0 – 0xC7	R	Status Locations
0xC8 – 0xFF		*unused*

USER FPGA Logic Version – 0x00 (read)

This register returns the version number for the USER FPGA. Each time the logic is modified, this value should be advanced. Allows verification that the proper logic is actually loaded into the FPGA. The values are hard coded in the logic to designate: which PMC board type, which hardware revision, and which hardware variant is appropriate for this logic. Example: if the logic shows hardware revision 3, it requires a board of hardware revision 3 or later to operate correctly. Multiple revisions and variants may work correctly for a particular logic image.

Bits	Function
31..24	PMC enumeration type
23..20	PMC hardware revision
19..16	PMC hardware variant
15..0	USER logic version

Control Register 0 – 0x01 (read)

Bits	Function
0	DCM lock '1' – DCM is locked
15..1	Not used
31..16	X"1303"

Control Register 0 – 0x01 (write)

Bits	Function
0	Software reset of User FPGA. '1' = reset
1	Run. Allows data capture. '1' = run
2	Not used
3	Mode: J4 or XMC, '0' = J4
4	Rocket I/O Loopback enabled
5	A/D 0 test counter, '1' = enabled
6	A/D 1 test counter, '1' = enabled
9 downto 7	--
10	trigger
(Others)	Not used

Gain and Offset Registers

These registers store the correction coefficients that are used by the FPGA to correct gain and offset in real time. There is a gain coefficient and offset coefficient for each ADC. When the board is calibrated, these values are stored in the non-volatile Calibration ROM (serial Flash) which is controlled by the PCI FPGA. Each time the board is powered up, the PCI host reads the values from the Calibration ROM and writes them into these registers in the USER FPGA.

Digital A/D Gain – 0x03, 0x04 (write)

Bits	Function
0..15	0x4000, channel A/D 0
0..15	0x4000, channel A/D 1

Digital A/D Offset – 0x07, 0x08 (write)

Bits	Function
0..14	0x0000, channel A/D 0
0..14	0x0000, channel A/D 1

Packet Manager channel enables – 0x0B (write)

Bits	Function
0	Enable channel A/D 0
1	Enable channel A/D 1
31..2	unused

Packet Manager channel destinations – 0x0C (write)

'0' = VFIFO/PCI, '1' = J4 or XMC (see Mode bit Ctl Reg 0 (3))

Bits	Function
0	Enable channel A/D 0
1	Enable channel A/D 1
31..2	unused

ZBT SRAM Address – 0x0E (write)

Bits	Function
19..0	Zbt address
31..20	unused

ZBT SRAM Data – 0x0F (write)

Bits	Function
15..0	Data
31..16	unused

Clocks & Frequency Synthesizer – 0x10 (write)

This register controls operation of the ICS8442 Synthesizer IC which can synthesize a frequency from one of the two external clock inputs, or from an on-board crystal reference. The selected external clock input passes through a divider IC controlled by the "Clocks, Input Divider" register before it reaches the synthesizer.

Bits	Function
8..0	PLL feedback divider ratio "M" (serial link)
13..12	Selects PLL output divider ratio "N" 0 => N=1; 1 => N=2; 2 => N=4; 3 => N=8 (serial link)
17..16	PLL Test Output Sel: Selects which synthesizer signal is applied to the Test Output. 0 = logic 0; 1 = Shift register output; 2 = Output of feedback divider; 3 = Output frequency (serial link)
20	VCO Sel: 1 = VCO (normal); 0 = bypass VCO '0' applies the VCO reference freq to the output divider. 'vco_sel'
24	Reference (XTAL) Sel: Selects the reference frequency for the VCO 1 = XTAL; 0 = external reference 'xtal_sel'
28	PLL Reset: '1' holds the synthesizer in reset 'pll_reset'
(Others)	Not used

Reference Frequency (Fr): 10 MHz to 25 MHz
VCO Frequency (Fvco): 250 MHz to 700 MHz
Fvco = Fr * M
Output Frequency = Fvco / N = Fr * M / N

Note: This register is almost identical to the Digital Receiver PMC with the following exceptions:

1. The reference frequency must be between 10 & 25 MHz (not 12 & 40 MHz)
2. N ranges from 1 to 8 (not 2 to 16)

ADC Shutdown – 0x11 (write)

The shutdown bit for each channel is in this register.

Bits	Function
15..0	Reserved for future use
16	Shutdown bit: 1 = shutdown ADC0
20	Shutdown bit: 1 = shutdown ADC1
(Others)	Not used

Clock Selects – 0x12

This register controls operation of a divider IC and selects clocks for the ADC's and other clock destinations. Three clock sources are available: two external clock inputs ACLK and BCLK, and one synthesizer. The synthesizer operates from a reference frequency which is generated by its on board 14.4 MHz crystal, or from a divided version of ACLK or BCLK.

Each ADC may be driven by any of the three clock sources.
Each ADC provides a copy of its sample rate clock to the USER FPGA.

The Sync Clock (available for use in the USER FPGA) may be driven by ACLK or BCLK.
The Divider (for the synthesizer) may be driven by ACLK or BCLK.

Bits	Function
1..0	ADC0 Clock Select: 0 = ACLK, 1 = BCLK, 2 = Synthesizer, 3 = Synthesizer
3..2	ADC1 Clock Select: same as above
8	Sync Clock Select: 0 = ACLK, 1 = BCLK
10	Divider Clock Select: same as above
13..12	Divider Ratio D: 0 => D=2, 1 => D=4, 2 => D=8, 3 => D=16
14	Divider Ratio: 0 => D=1, 1 => D is selected by bits 13..12
15	Divider Reset: 1 = reset
(others)	Not used

Packet Headers – 0x20, 0x21 (write)

Bits	Function
23..0	Number of dwords in packet, including 2 dword header
30..24	Peripheral ID number
31	Control/data packet, '0' = data packet

Triggering

Two trigger modes are supported for each A/D channel : unframed and framed. In unframed mode, the trigger output is true whenever the selected trigger source is true. In framed mode, the trigger output is true after a rising edge on the selected trigger source until the frame count number of sample clocks are counted. A point is counted on each rising edge of the sample clock input when sample enable is true. The trigger mode is selected with trig_sel input to be either framed or unframed, software or external trigger. The trigger sources are external or software. The external trigger must be enabled to use it, however the software trigger is always OR'd with the external trigger to allow it to be used anytime. For the framed mode, the number of points must be multiples of 256. This reduces the number of bits used for comparison and control for simplicity.

Trigger Controls – 0x17, 0x18

These registers set the trigger mode and enable the external trigger input.

Bits	Function
15..0	How many points to collect, in 256 blocks (total points = this number *256)
29..16	Not used
30	Trigger mode: 0 = unframed, 1 = framed
31	External trigger enable

END OF DOCUMENT

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