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X5-400M

V2.0 11/16/10

Innovative Integration
... real time solutions!

PCI Express XMC Module with Two 400 MSPS, 14-bit A/Ds and Two 500 MSPS, 16-bit DACs, Virtex5 FPGA and 512MB Memory

FEATURES

- Two 400 MSPS, 14-bit A/D channels
- Two 500 MSPS, 16-bit DAC channels
- Xilinx Virtex5, SX95T FPGA
- Internal or external clock and triggering
- 512MB DDR2 DRAM supporting 4 GB/s transfer rates
- 4MB QDR-II SRAM for computations
- 8 Rocket IO private links, 2.5 Gbps each
- >1 GB/s, 8-lane PCI Express Host Interface
- Conduction cooling and thermal monitoring
- PCI Express XMC Module (75x150 mm)
- Conduction cooled versions for wide temperature applications
- Extended vibration and shock capability available

APPLICATIONS

- Wireless IF Receiver and Transmitter
- RADAR
- Electronic Warfare
- High Speed Data Recording and Playback
- High speed servo controls
- IP development

SOFTWARE

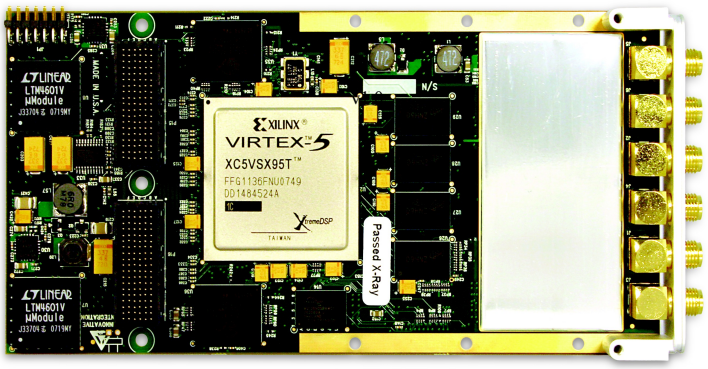
- MATLAB/VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ Host Tools

IP Cores

- Four fully independent DDC channels
- High density 128 channel receiver for mobile communications such as GSM
- PSK and FSK demodulation

MATLAB®

XILINX®



RoHS 2002/95/EC Compliant

X5 400m

DESCRIPTION

The X5-400M features two 14-bit, 400 MSPS TI ADS5474 A/Ds and two 16-bit 500 MSPS DAC channels with a Virtex5 FPGA computing core, DRAM and SRAM memory, and eight lane PCI Express host interface.

A Xilinx Virtex5 SX95T with 512MB DDR2 DRAM and 4MB QDR-II SRAM memory provide a very high performance DSP core that features 640 DSP MAC units in the FPGA along with ~11M gates of logic. The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates exceeding 150 GMACs per second.

The X5 modules couple Innovative's powerful Velocia architecture with a high performance, 8-lane PCI Express interface that provides over 1 GB/s sustained transfer rates to the host. Private links to host cards with > 1.6 GB/s capacity using P16 are provided for system integration.

The X5 family can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

The X5-400M can be purchased pre-configured with signal processing cores for receiver applications. Flexible cores offering up to 128 receiver channels with programmable tuning, gain and filters are available.

Software tools for host development include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features and use are provided.

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05/23/13

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X5-400M



This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X5-400M	80180-<CFG>-<ER>	PCI Express XMC module with two 400 MSPS TI ADS5474 A/Ds and 500 MSPS 16-bit DACs (EXT clock mode), Virtex5 LX155T FPGA, 4MB SRAM, 512MB DRAM <CFG> is configuration 0 - LX110T1 1 – SX95T1, External Clock Mode 2 – SX95T1, clk ext (PLL clock mode) 3 – LX155T1, clk ext (non interpolating) 5 – SX95T1, D/A clk: EXT, AC-coupled inputs 6 - SX95T1, D/A clk: EXT, AC-coupled inputs 9 - SX95T1, 1 A/D, D/A clk: ext 10 - SX95T1, 1 A/D, D/A clk: ext 12 - LX155-T2, ext D/A clk 13 - LX155-T2, PLL D/A clk 14 - SX95T2, D/A clk: EXT, AC-coupled inputs <ER> corresponds to -L0, -L1, -L2, -L3 or -L4 rating from Operating Environment Table below.
400M FrameWork Logic	55015	X5-400M FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters		
XMC-PCIe Adapter	80172-0	PCI Express carrier card for XMC PCI Express modules, x1 lanes
XMC-PCI Adapter	80167-0	PCI carrier card for XMC PCI Express modules, 64-bit PCI
XMC-PCIe Adapter	80173-0	PCI Express carrier card for XMC PCI Express modules, x8 lanes
XMC-compact PCI/PXI Adapter	80207	3U compact PCI carrier card for XMC PCI Express modules, 64-bit PCI. Support for PXI clock and trigger features (logic dependent).
XMC- Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
Embedded PC Host		
eInstrumentPC embedded PC XMC host	90200	Embedded PC with support for two XMC modules; Celeron, Core2Duo or Penryn CPU; Windows or Linux
eInstrumentPC-Atom low-power embedded PC XMC host	90201	Embedded PC with support for two XMC modules; Intel Atom or Penryn CPU; Windows or Linux

X5-400M

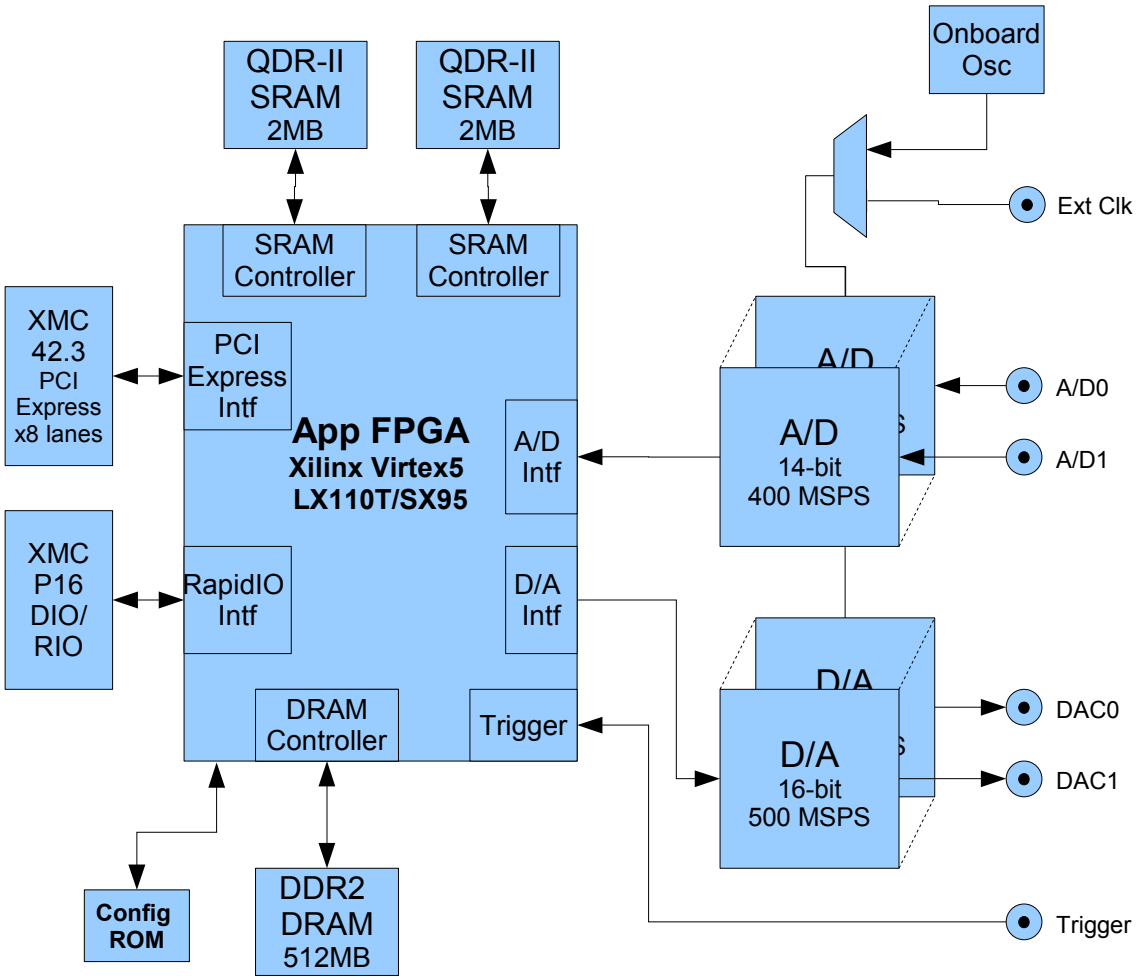
Operating Environment Ratings

X5 modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance. Click this link "Ruggedization Levels" to see the Ruggedization Levels available.

Contact sales support for pricing and availability.

X5-400M

X5-400M Block Diagram



X5-400M

Standard Features

Analog	
Inputs	2
Input Range	+/- 1V
Input Type	Single ended, AC or DC coupled
Max Safe Input Voltage	-5.7V to +5.7V
Input Impedance	50 ohm
A/D Device	Texas Instruments ADS5474
A/D Resolution	14-bit
A/D Sample Rate	20 MHz to 400 MHz (lower rates must use decimation in logic)
Outputs	2
Output Range	+/- 1V
Output Type	Single ended, DC coupled
Output Impedance	50 ohm
Max Output Current	95 mA
DAC Device	Texas Instruments DAC5687
DAC Resolution	16-bit
DAC Sample Rate	16 MHz to 500 MHz, depending on mode
DAC Interpolation	Programmable 2-8x
Data Format	2's complement, 16-bit integer
Connectors	SMA female
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

FPGA	
Device	Xilinx Virtex5 XC5VSX95T XC5VSX155T
Speed Grade	-1 or -2
Size	SX95T: ~9M gate equivalent LX155T: ~15M gate equivalent
Flip-Flops	SX95T : 58880 LX155T : 97280
Multipliers	SX95T: 640 LX155T: 128
Slices	SX95T: 17,280 LX155T: 24,320
18Kb Block RAMs	SX95T: 488 LX155T: 424
Rocket IO	16 lanes @ 2.5 Gbps
Configuration	SelectMAP from on-board flash EEPROM - JTAG during development
FPGA Usage (Framework Logic)	SX95T: LUT=23% FF=34% BR=29% DSP48E=2% LX155T: LUT=14% FF=20% BR=32% DSP48E=10%

Memories	
DRAM Size	512MB total 4 devices @ 64Mx16 each
DRAM Type	DDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	4.2 GB/s storage/retrieval rate sustained
SRAM Size	4 MB total 2 devices @ 512Kx32 each
SRAM Controller	Two independent SRAM controllers implemented in FPGA logic
SRAM Type	QDR-II
SRAM Rate	3.2 GB/s storage/retrieval max rate sustained

X5-400M

Host Interface	
Type	PCI Express; 8 lanes
Sustained Data Rate	1 GB/s each direction simultaneous
Protocol	PCI Express with Velocia packet system
Connector	XMC P15
Interface Standard	PCIe 1.0a; VITA 42.3
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Sources	On-board low jitter fixed oscillator, 400MHz default frequency
	External: Sine source 10 to 400 MHz, 0.3-3.3Vp-p (-6.47 to 14.3 dBm) AC-coupled, 50-ohm terminated
Jitter	Internal: 340 fs total
	External: 90 fs additive
Triggering	External or software; Continuous or N-sample frame
Ext Trigger	SMA female, LVTTL (0 to 3.3V max) DC-coupled, 50-ohm terminated.
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.

Acquisition Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

P16 Interfaces	
Rocket IO Channels	8
Rocket IO data rate	2.5 Gbps/lane (2 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	33
Signal Standard	LVTTL (0 to 3.3V max)
Drive	+/-12 mA (adjustable in FPGA)
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g (includes bracket)
Hazardous Materials	Lead-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Supply Voltage, VPWR to GND	+4.5	+16	V	
Analog Input Voltage, Vin+ or Vin- to GND	-6	+6	V	
Operating Temperature	0	70	C	Cooling is required for operation. Convection cooling must be non-condensing.
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	See Environmental Ratings Table			
Shock	See Environmental Ratings Table			

RECOMMENDED OPERATING CONDITIONS

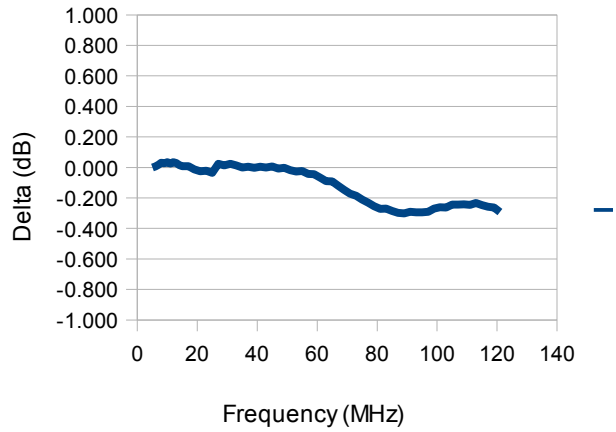
Parameter	Min
Supply Voltage (3.3V)	+3.15
Supply Voltage (VPWR)	+11
Operating Temperature	0
Forced Air Cooling	2**

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

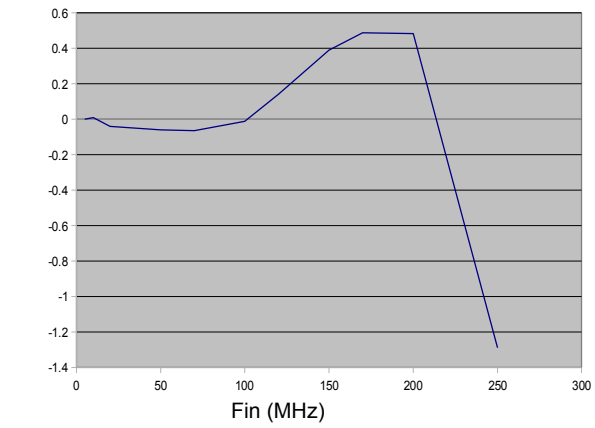
Parameter		Typ	Units	Notes
A/D Channels				
	Analog Input Bandwidth	260	MHz	-3dB, AC or DC coupled inputs
	Analog Input Passband Flatness	2	dB	0 to 200 MHz, DC-coupled
		1	dB	0 to 100 MHz, DC-coupled
		0.35	dB	5 to 120 MHz, AC-coupled
	Broadband SFDR	67.9	dB	Fin = 70 MHz, 850 mVRMS filtered sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC Coupled
		78.5	dB	Fin = 70.1 MHz, 850 mVRMS filtered sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC Coupled
	SFDR, 70 MHz carrier +/-5 MHz band	90	dB	Fin = 70 MHz, 850 mVRMS filtered sine sampled at 400 MSPS; 65 to 75 MHz band, DC-Coupled
		92	dB	Fin = 70.1 MHz, 850 mVRMS filtered sine sampled at 400 MSPS; 65 to 75 MHz band, AC-Coupled
	Harmonic Distortion	-65.1	dB	70 MHz, 850 mVRMS filtered sine sampled at 400 MSPS, DC-200 MHz, DC-coupled
		-92.8	dB	70.1 MHz, 850 mVRMS filtered sine sampled at 400 MSPS, DC-200 MHz, AC-coupled
	ENOB	10.1	bits	70MHz, 850 mVRMS filtered sine sampled at 400 MSPS, DC-200 MHz, DC-coupled
		10.3	bits	70.1 MHz, 850 mVRMS filtered sine sampled at 400 MSPS, DC-200 MHz, AC-coupled
	SNR	73.6	dB	70 MHz, 850 mVRMS filtered sine sampled at 400 MSPS, DC-200 MHz, DC-coupled, 64K point FFT
		64	dB	70.1 MHz, 850 mVRMS filtered sine sampled at 400 MSPS, DC-200 MHz, AC-coupled, 64K point FFT
	Crosstalk	-87	dB	Measured channel grounded with a 70.5 MHz, 850 mVRMS filtered sine input on other channel
	Noise	350	µV	Typical for grounded input, 1 standard deviation.
	Noise Floor	-95	dB	Grounded input, sampled at 250 MSPS.
	Offset Error	700	µV	Factory calibration, average of 64K samples after warmup.
	Gain Error	0.02	%	Factory calibration after warmup.
DAC Channels				

	SFDR	68	dB	Fout = 7.8 MHz sine, Sample rate at 125 MSPS, 4x interpolation resulting in 500 MSPS update rate
	Intermodulation Distortion	-58	dB	Dual tone output with Fout = 69 MHz + 71 MHz, updatye rate at 200 MSPS, 2x interpolation resulting in 400 MSPS update rate.
	DAC Channel Crosstalk	-68	dBm	50 MHz square wave at 95% FS on adjacent channel, 200 MSPS update rate
Power Consumption		28	W	FPGA system clock @ 250 MHz, all A/D channels sampling at 400 MSPS, 24C ambient; specific applications may be may vary from 20 to 35W (12V @ 0.6A) (3.3V @ 5.9A)
Mean Time Between Failures (MTBF)				16391 hours

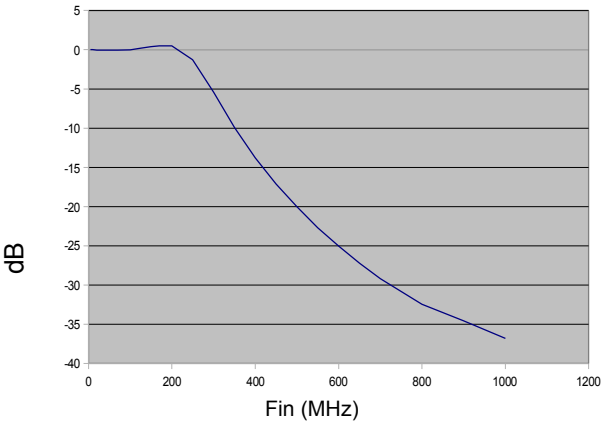


Fs=400MHz

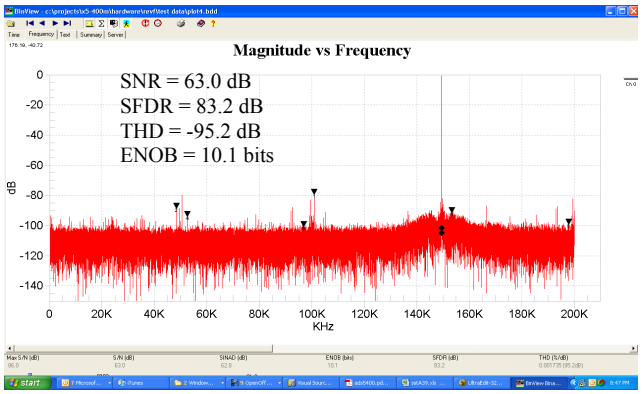
Amplitude Variation, AC-Coupled input



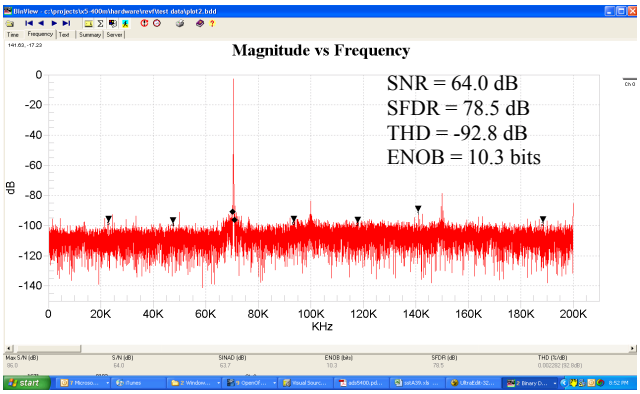
Amplitude Variation, DC-Coupled



Amplitude Variation, DC-Coupled

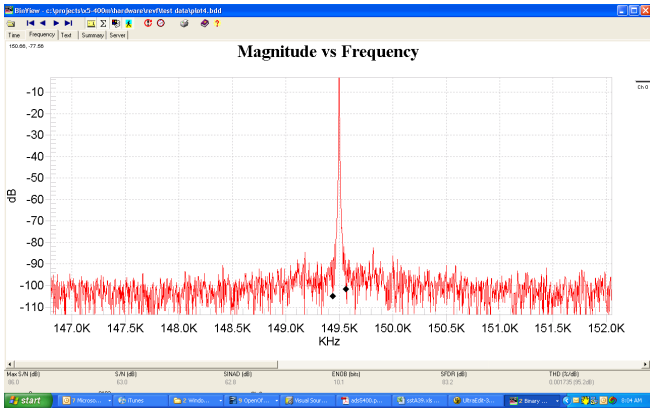


Wideband Signal Quality, AC-Coupled Input, Fin =250.5MHz, 850 mVp-p, Fs =400MHz

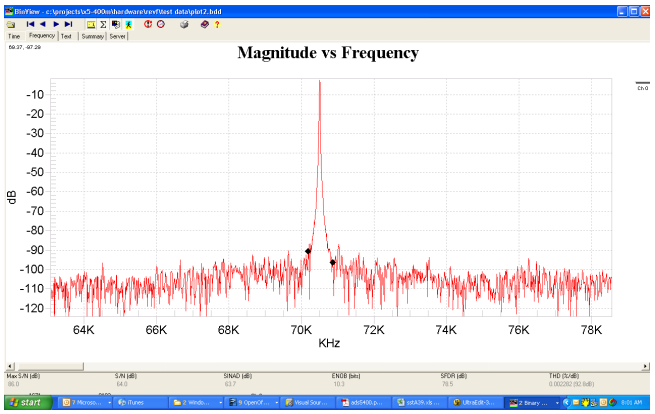


Wideband Signal Quality, AC-Coupled Input, Fin =70.5MHz, 850 mVp-p, Fs =400MHz

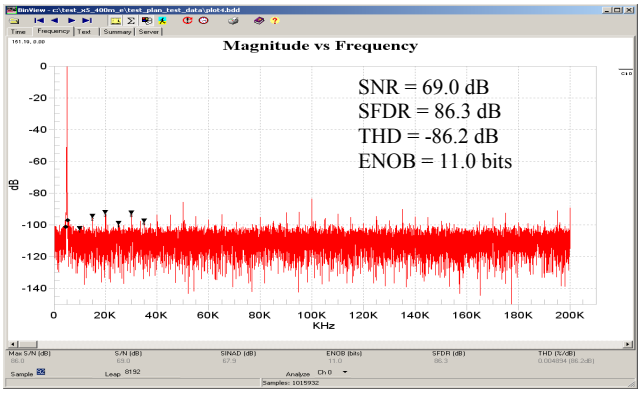
X5-400M



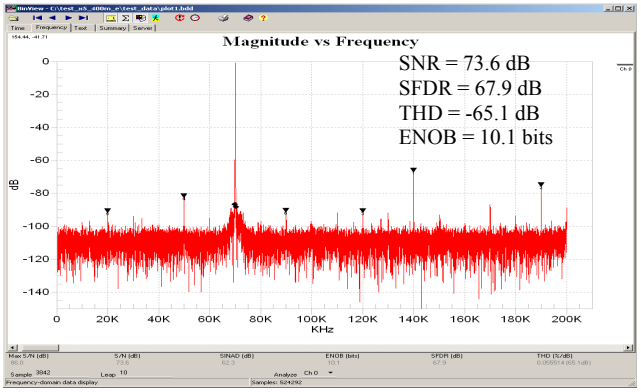
Narrowband Signal Quality, AC-Coupled Input, Fin =250.5MHz, 850 mVp-p, Fs =400MHz



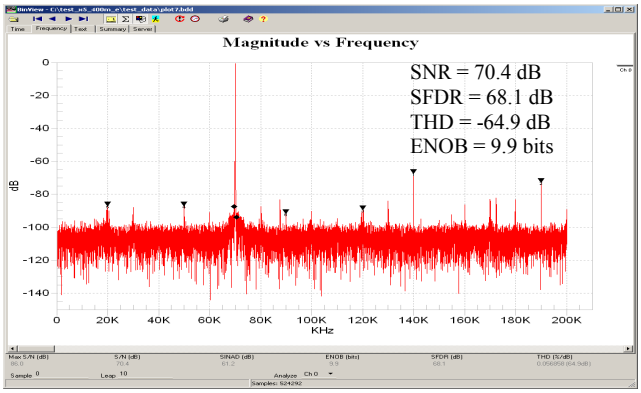
Narrowband Signal Quality, AC-Coupled Input, Fin =70.5MHz, 850 mVp-p, Fs =400MHz



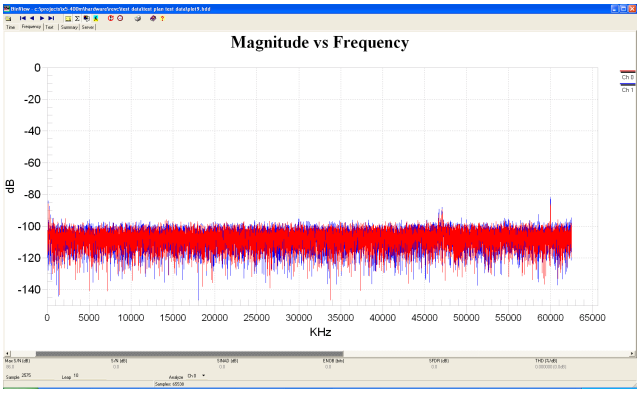
Wideband Signal Quality, DC-Coupled Input, Fin =5.0MHz, 850 mVp-p, Fs =400MHz



Wideband Signal Quality, DC-Coupled Input, Fin =70.0MHz, 850 mVp-p, Fs =400MHz

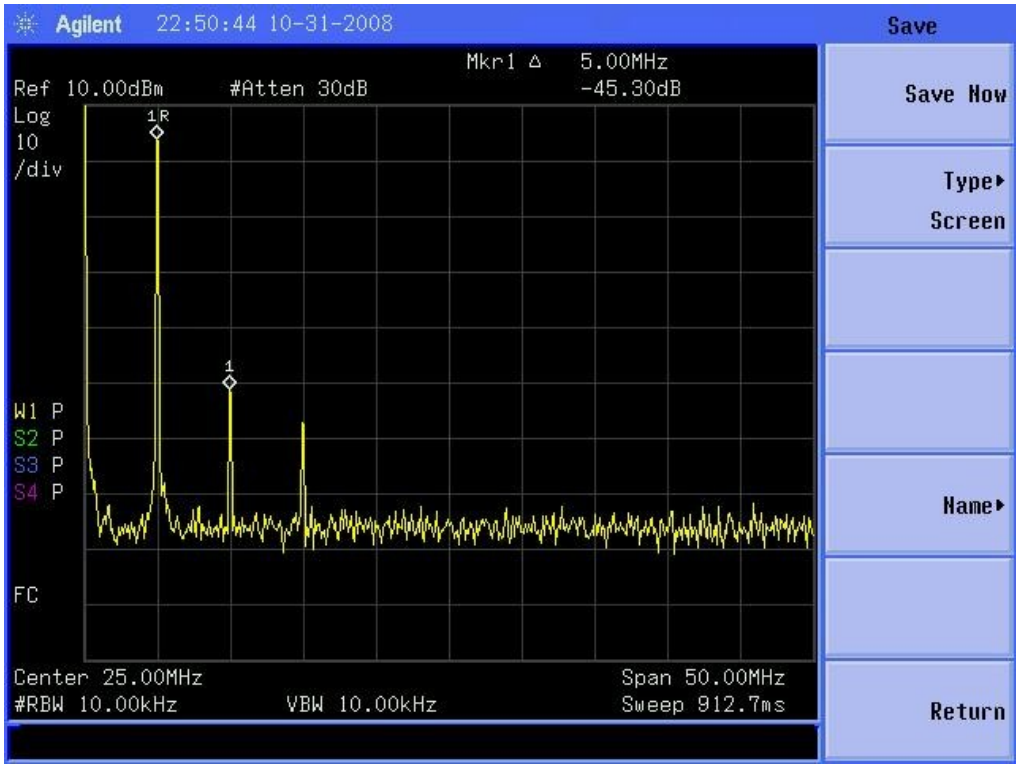


Wideband Signal Quality, DC-Coupled Input, Fin =70.0MHz, 850 mVp-p, Fs =400MHz external clock

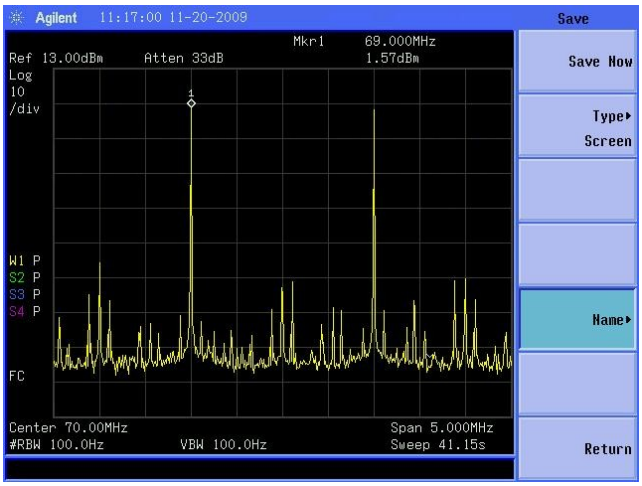


Noise Floor, DC-Coupled Input, Fs =250MHz external clock

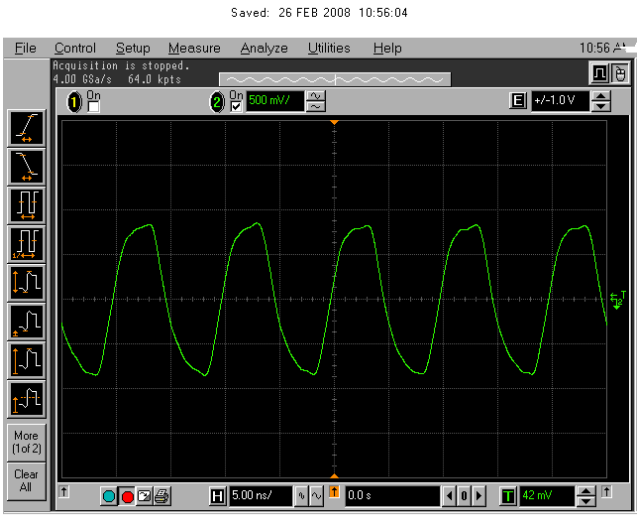
X5-400M



D/A output, update rate = 400 MHz (x2 interpolation of 200MHz clock), analyzer adding approximately 15dB to harmonics



Dual tone test: 69.0 and 71.0 MHz sine waves, fs = 200, interpolation =2, internal clock.

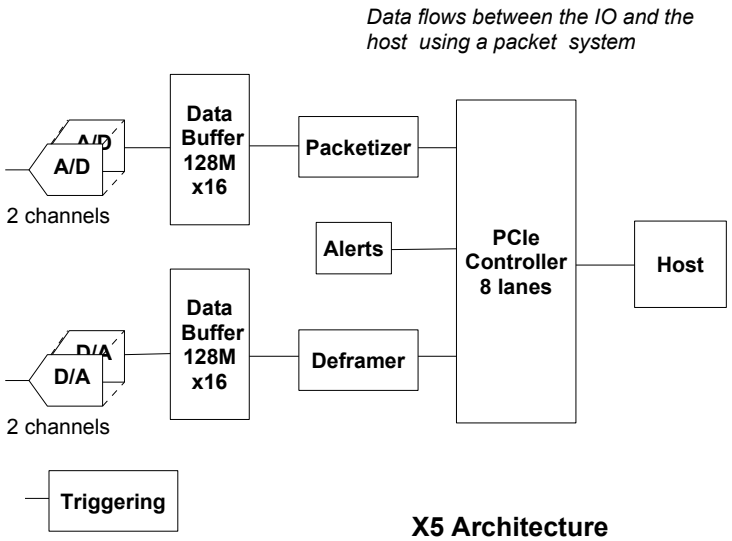


DAC Settling time for 100 MHz square ware using DAC sample rate at 200 MSPS, no interpolation, external clock mode with 95% FS amplitude

X5-400M

Architecture and Features

The X5-400M module architecture integrates analog IO with an FPGA computing core, memories and PCI Express host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates making it ideal for demanding applications in wireless IF processing, RADAR and electronic warfare applications.



X5 Architecture

Analog IO

The analog front end of the X5-400M module has two simultaneously sampling channels of 14-bit, 400 MSPS A/D input (TI ADS5474) and two channels of 500 MSPS, 16-bit D/A converter. The A/D inputs have an analog input bandwidth of 1 GHz for wideband and direct sampling applications. The DAC outputs have an output bandwidth of 250 MHz (may be customized). The A/Ds and DACs are directly connected to the FPGA for minimum data latency. In the standard logic, the A/D and DACs have an interface component that receives the data, provides digital error correction, and a FIFO. The digital error correction is used to compensate for gain and offset errors providing long term stability and accuracy. This method is more stable than analog adjustments and typically sacrifices less than 1% of the analog range. A non-volatile ROM on the card is used to store the calibration coefficients for the analog and is programmed during factory test.

The A/D and DAC channels operate synchronously for simultaneously sampling systems using the external clock input. Controls for triggering allow precise control over the collection of data and are integrated into the FPGA logic. Trigger modes include frames of programmable size, external and software. Multiple cards can sample simultaneously by using external trigger inputs. The trigger component in the logic can be customized in the logic to accommodate a variety of triggering requirements.

The DAC 5687 used on the X5-400M XMC module employs an up-sampling architecture in which the rate of digital-to-analog conversion (*update rate*) may differ from the rate at which data is supplied to its digital bus interface (*data rate*). The rate differences are a function of the device's interpolation and clock mode settings. Since the A/D and D/A devices on the module share a common clock, the rate restrictions of the D/A converters limit the usable sample rates for the module as shown below.

I/O Configuration	D/A				A/D
	Clock Mode	Interpolation Mode	Maximum Rate (MSPS)		Maximum Rate (MSPS)
			Update	Data	Update & Data
Simultaneous A/D and D/A operation	EXT	1x 2x	200 400	200 200	200 400
	PLL	1x 2x	160 320	160 160	160 160
D/A channels only	EXT	1x 2x	250 500	250 250	
	PLL	1x 2x 4x	160 320 500	160 160 125	
A/D channels only					400

Update Rate: Rate at which samples are converted between digital and analog domain
Data Rate: Rate at which digital sample values are transferred between FPGA and analog converter device
EXT: On-board X5-400M fixed-frequency oscillator OR an sinus source driven into the X5-400M external clock input
PLL: Internal DAC 5687 PLL output using EXT as a reference clock.

A surface mount resister controls the configuration of the D/A clock mode. Specify the desired factory configuration by ordering the appropriate part number from the table below.

Part Number	D/A Clock Mode
80180-1 or 80180-3	EXT
80180-2or 80180-4	PLL

FPGA Core

The X5 Module family has a Virtex5 FPGA and memory at its core for DSP and control. The Virtex5 FPGA is capable of >300x10^9 MACs (SX95T operating at 500 MHz internally), about 20x faster than competing DSPs. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to 512 MB of DDR2 DRAM capable of >4 GB/s data transfer rate and 4 MB or QDR II SRAM capable of 4GB/s data rate. The QDR memory is composed of two independent banks of 2 MB (512Kx32). These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The X5 module family uses the Virtex5 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the dataflow, signal processing,

controls and host interfaces, allowing complete customization of the X5 module functionality.

PCI Express Host Interface

The X5 architecture delivers over 1 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds or DACs, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex5 FPGA using 8 Rocket IO ports, for a maximum bit rate of over 20 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 200 MB/s per lane. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

Private Data Links

The X5 module family has private data links on the P16 connector that can be used for system integration. The P16 connector has 8 Rocket IO links, each capable of 2.5 Gbps, and 16 sideband signals. The 8 RIO lanes can be used to provide low-latency, high rate data to the system in addition to the PCI Express interface. Maximum data rates, with deterministic performance can be implemented in performance-driven systems using little or no protocol. For more complex systems, protocols such as Rapid IO or Aurora can be used.

Module Management

The data acquisition process can be monitored using the X5 alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the X5 cards easier to integrate into larger systems.

FPGA Configuration

The X5 modules have a 128Mb FLASH that holds the FPGA application image. The FLASH can be reprogrammed in-system using a software applet for field upgrades. Two application images are stored: the application logic and backup version. In case of the application logic is corrupted or malfunctions, the back logic can be used to restore the card to operation.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB or Parallel IV cable.

Thermal Monitoring and Cooling

The X5-400M logic provides FPGA temperature monitoring that is used to prevent overheating. If the temperature exceeds the maximum safe operating temperature (85C for commercial temperature range devices), then the module power supplies are turned off to prevent damage. The temperature can also be read by software for system health monitoring.

Conductive cooling for the module is provided through two cooling bar attachment areas along the edges. These cooling bar areas are connected to a thermal plane in the PCB that spreads heat and conducts from the devices to the bars. For convection

cooling, the thermal plane provides a larger surface area and also spreads heat to the bracket for better cooling.

Software Tools

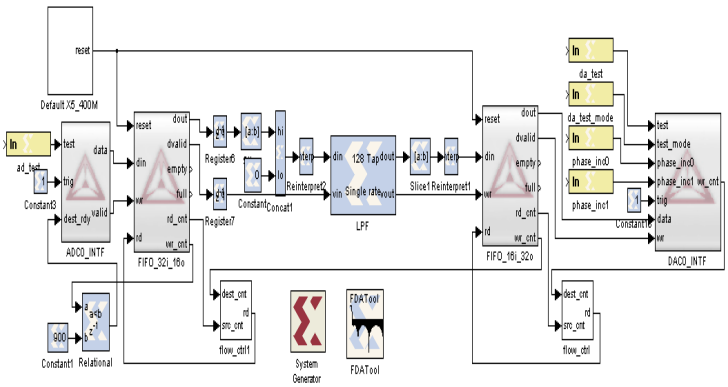
Software development tools for the X5 modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every X5 module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the X5 performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the X5 modules by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designers can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functions and providing a starting point for your application.



Using MATLAB Simulink for X5 Logic Design

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

IP for X5 Modules

Innovative provides a range of down-conversion channelizer logic cores for wideband and narrowband receiver applications for the X5 family. When fitted with these cores, the X5 modules provide powerful receiver functionality integrated for IF processing.

The DDC channelizers are offered in channel densities from 4 to 128. The four channel DDC offers complete flexibility and independence in the channels, while the 128 channel core offers higher density for uniform channel width applications. The DDC cores are highly configurable and include programmable channel filters, decimation rates, tuning and gain controls. An

integrated power meter allows the DDC to measure any channel power for AGC controls.

Each IP core is provided with a MATLAB simulation model that shows bit-true, cycle-true functionality. Signal processing designers can then use this model for channel design and performance studies. Filter coefficients and other parameters from the MATLAB simulation can be directly loaded to the hardware for verification.

Part Number	IP Core	Channels	Tuning	Decimation	Max Bandwidth	Channel Filter
58014	IP-MDDC4	4	Fs/2^32	16 to 32768	Fs/16	Programmable 100 tap filter
58015	IP-MDDC128	128	Fs/2^32	512 to 16384	Fs/512	Programmable 100 tap filter

Additional IP cores are offered for IF processing and baseband demodulation.

Part Number	IP Core	Features
58001	PSK Demodulation	N=2,4,8,PI/4. Integrated carrier tracking and bit decision.
58002	FSK Demodulation	Programmable discrimination filters, bit decision logic.
58003	TinyDDS	Tiny DDS, 1/3 to ½ size of Xilinx DDS with equal SFDR, clock rates to 400 MHz with flow control
58011	XLFFT	IP core for 64K to 1M FFTs with windowing functions.
58012	Windowing	IP core for Hann, Blackman and uniform data windowing functions.
58013	CORDIC	IP core for sine/cosine generation using CORDIC method, resulting in 1/3 logic size of standard DDS cores.

Applications Information

Cables

The X5-400M module uses coaxial cable assemblies for the analog IO. The mating cable should have an SMA male connector and 50 ohm characteristic impedance for best signal quality. Innovative offers SMA to BNC cables (P/N 67048) for quick connection to test equipment.

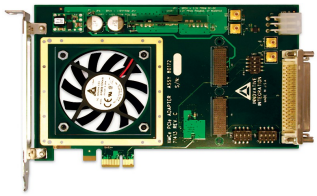
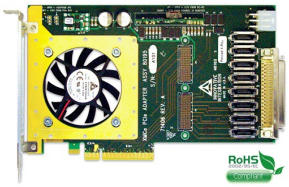
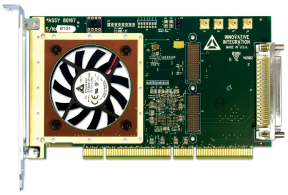
XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The X5 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with 16 LVTTL signals provide support for data transfer rates up to 1.6 GB/s sustained, as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed Rocket IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80173 is suitable for high speed P16 applications.

X5-400M

PCIe-XMC Adapter (80172) x1 PCIe to XMC Clock and trigger inputs 	**PCIe-XMC Adapter x8 lane (80173)** x8 PCIe to XMC x8 RIO ports supported on P16 	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC 	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support 

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X5 modules.

X5-400M

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201)

Windows/Linux embedded PC
Intel Core2Duo or low power Atom available
8x USB, GbE, cable PCIe, VGA
High speed x8 interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
100 MB/s, 400 GB datalogger
9-18VDC operation



eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion
Up to 7 meter cable
electrically isolated from host computer
software transparent
Supports standalone operation for X5 modules



X5-400M

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