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SST-DN3-104-1 and SST-DN3-104-2

Hardware Reference Guide

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This document applies to the SST-DN3-104-1 and SST-DN3-104-2 interface cards.

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Preface

Preface Sections:

- Purpose of this Guide
- Using this Guide
- Conventions

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Purpose of this Guide

This guide contains technical and product-related information on the SST-DN3-104-1 and SST-DN3-104-2 network interface cards.

The SST-DN3-104-1 consists of a single DeviceNet network interface (or *channel*), and the SST-DN3-104-2 comprises two independent interfaces, controlled by independent CPUs. Each CPU executes downloadable application firmware modules, which enable application-level product behavior. For more details, refer to relevant firmware documentation.



Note

An application running on one channel does not affect the performance of other channels, as it does not share memory or processor resources with them.



Note

In this manual, the SST-DN3-104-1 and SST-DN3-104-2 will be referred to as the *card*, except where product differences apply.

Using this Guide

If you are running a 3rd party application or writing your own application using the card's DLL calls, the sections of interest in this guide will be "Card Overview", "Installation" and potentially "Troubleshooting". If you are writing your own application in a non-Windows environment (interfacing directly with the card's memory registers), we recommend that you read the whole guide.

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Conventions

This guide uses stylistic conventions, special terms, and special notation to help enhance your understanding.

Style

The following stylistic conventions are used throughout this guide:

Bold	indicates field names, button names, tab names, and options or selections
Italics	indicates keywords (indexed) or instances of new terms and/or specialized words that need emphasis
CAPS	indicates a specific key selection, such as ENTER, TAB, CTRL, ALT, DELETE
`Code Font`	indicates command line entries or text that you'd type into a field
Underlining	indicates a hyperlink
">" delimiter	indicates how to navigate through a hierarchy of menu selections/options
"0x"	indicates a hexadecimal value

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Terminology

The following special terms are used throughout this guide:

Card	the SST-DN3-104-1 or SST-DN3-104-2 network interface card
Channel	a DeviceNet network interface on the card
Firmware Module	the embedded software module that gets loaded to the card's memory and runs on the card. This is the operating system of the card, enabling it to respond to commands from the host and manage network communications.
Host	the computer system in which the card is installed
.bin	an unencrypted firmware module for the card
.ss3	an encrypted firmware module for the card

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Special Notation

The following special notations are used throughout this guide:



Warning

Warning messages alert the reader to situations where personal injury may result. Warnings are accompanied by the symbol shown, and precede the topic to which they refer.



Caution

Caution messages alert the reader to situations where equipment damage may result. Cautions are accompanied by the symbol shown, and precede the topic to which they refer.



Note

A note provides additional information, emphasizes a point, or gives a tip for easier operation. Notes are accompanied by the symbol shown, and follow the text to which they refer.

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1
Card Overview

Chapter Sections:

- Warnings and Cautions
- Card Features
- Hardware Description

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1.1 Warnings and Cautions

The card is an electrical component and must be treated with the following precautions:



Warning

Only qualified electrical personnel familiar with the construction/ operation of this equipment and the hazards involved should install, adjust, operate, and/or service this equipment. Read and understand this guide in its entirety before proceeding. Failure to observe this precaution could result in severe bodily injury or, in extreme cases, loss of life.



Warning

You must provide an external, hard-wired emergency stop circuit outside the programmable controller circuitry. This circuit must disable the system in case of improper operation. Uncontrolled machine motion may result if this procedure is not followed. Failure to observe this precaution could result in bodily injury.



Caution

The card contains static-sensitive components. Careless handling may severely damage the card. Do not touch any of the connectors or pins on the card. When not in use, the card should be stored in an anti-static bag. Failure to observe this precaution could result in damage to or destruction of the equipment.

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1.2 Card Features

The card is a PC/104 interface for communication with DeviceNet and other CAN-based networks. The main features of each channel are:

- 16-bit PC/104 interface (compliant with PC/104, specification 2.4). 16 bits is the width of the data bus and does not restrict the card from being used in a 32-bit operating system.
- 66 MHz ColdFire Processor
- 256 KB of shared RAM
- DeviceNet-compliant 5-pin CAN connector
- Data rate of up to 1 Mbaud for CAN, and 125K, 250K and 500K for DeviceNet
- Bi-color LEDs showing card status
- Isolated physical layer

1.3 Byte Ordering

The card uses Intel-style (little endian) byte ordering for multi-byte entities LSB-low address and MSB-high address. If your host system uses Motorola (big endian) byte ordering (MSB-low address and LSB-high address), you must compensate for byte ordering in software.

The following language macro will compensate for byte ordering in a 16-bit data entity:

```
#define SWAP_WORD (WordData) ((WordData<<8) | (WordData>>8))
```

1.4 DN3 Compatibility

For a comparison of DN3 with DNP, refer to Section D.2, Reference Documents.

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1.5 Hardware Description

The main features of the card are described in more detail in the following sections. For information on card dimensions, refer to Section B.1, Technical Specifications.

Figure 1: SST-DN3-104-1 & 2 Interface Card

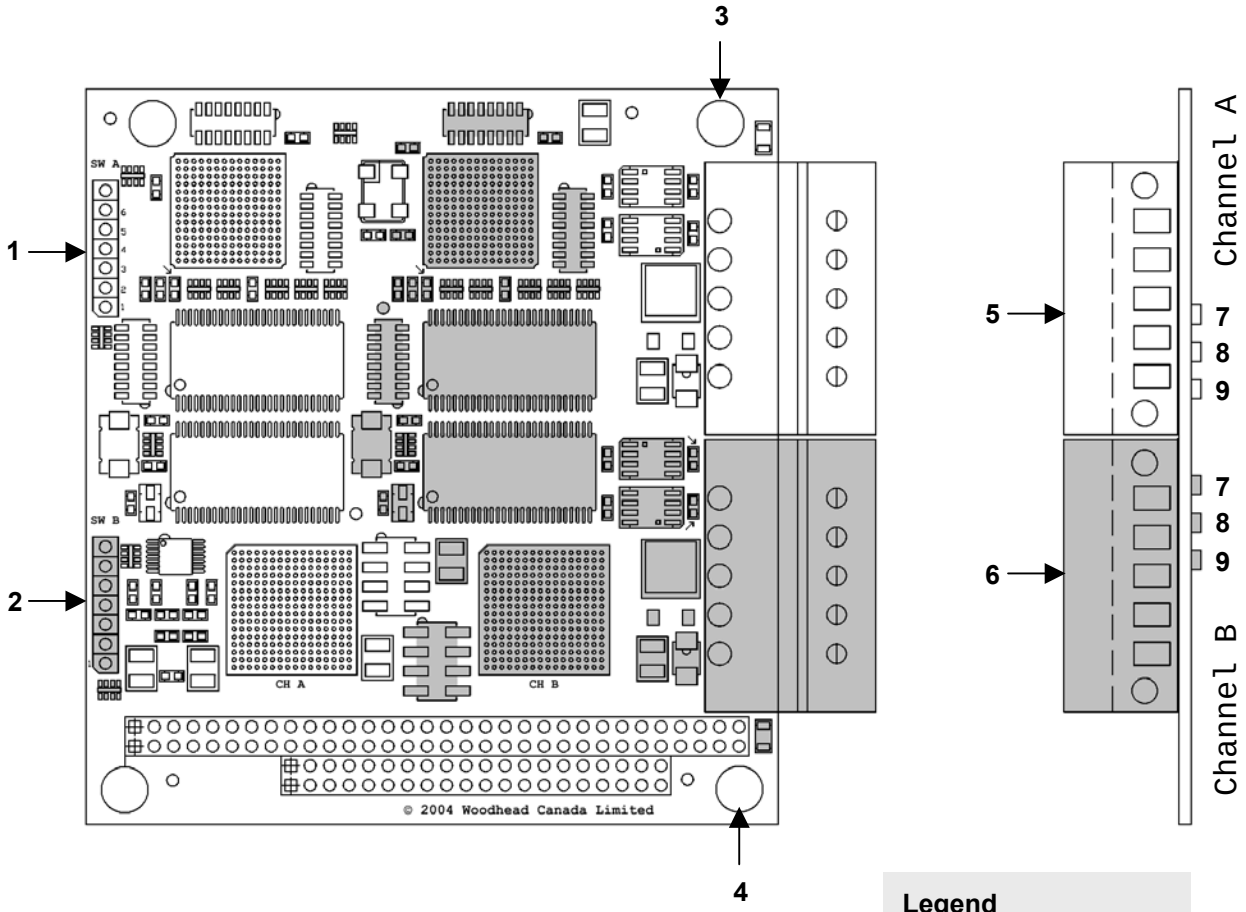


Table 1: Card Features

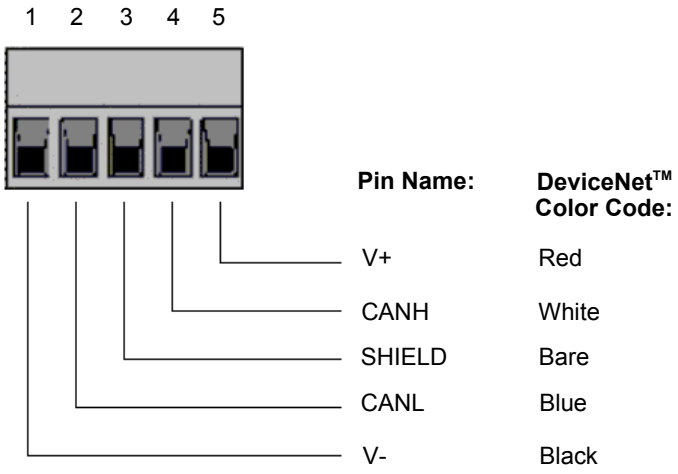
Feature	Description
1	Channel A Switch
2	Channel B Switch
3	Connector Hole (H1)
4	Connector Hole (H2)
5	Channel A CAN Connector (J101)
6	Channel B CAN Connector (J201)
7	PWR LED
8	HLTH LED
9	COMM LED

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1.5.1 CAN Connector

The 5-pin connector is a removable connector that conforms to the standard DeviceNet pinout. Pin numbers, names and color codes are identified in the figure below.

Figure 2: 5-Pin CAN Connector



1.5.1.1 V+, V-

These terminals provide power to the isolated section of the network interface, and must be connected and powered for the card to communicate on the network. On DeviceNet networks, they connect directly to the red (V+) and black (V-) wires of the DeviceNet cable. On non-powered CAN networks, they must be connected to an external 24VDC supply.

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1.5.1.2 CANH, CANL

These are the CAN communication bus signal terminals. Use only shielded twisted pair cable. When using the card on DeviceNet with DeviceNet approved cabling, these wires will already be a twisted pair with the proper DeviceNet impedance.

1.5.1.3 SHIELD

This is the shield connector. This terminal is “snubbed” to the PC/104 chassis ground via a 1M-ohm resistor, through the PC/104 standoffs connected to holes H1 and H2.



Note

The shield should be connected directly to earth ground at only one point in the network.

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1.5.2 LEDs

There are three LEDs per channel: Power (PWR), Health (HLTH) and Communications (COMM).



Note

For information on troubleshooting using LEDs, refer to Section 4.1, HLTH or PWR LED is Red.

1.5.2.1 PWR LED

The PWR LED is an indicator that represents whether or not power is applied to the CAN connector. The PWR LED's behavior is described in the following table:

Table 2: PWR LED Behavior

Color	Status
Green	CAN bus power present
Red	CAN bus power not present
Off	PC/104 power not present

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1.5.2.2 HLTH LED

The HLTH LED indicates the channel's health status. The HLTH LED's behavior is described in the following table:

Table 3: HLTH LED Behavior

Color	Status
Off	Card initialization failed or the card is not powered
Green	The firmware is running
Red	The card has halted or there is a firmware run-time error
Amber	Startup self-test complete, no firmware loaded. The firmware must be reloaded (refer to Section 4.1, HEALTH or PWR LED is Red).



Note

If the HLTH LED is flashing, there may have been a startup failure. For more details, refer to Section A.3, Fatal Hardware Self-Test Flash Codes.

1.5.2.3 COMM LED

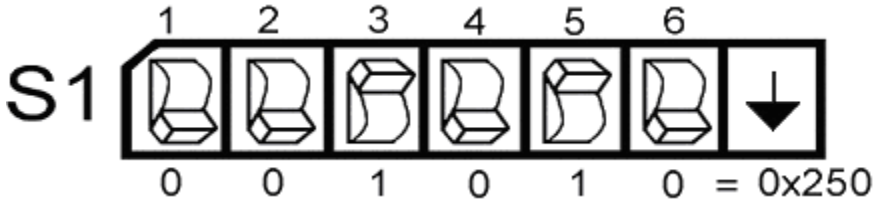
The COMM LED indicates the network status. This LED's meaning and behavior are determined by the currently loaded firmware module. Refer to the module's reference guide for more details.

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1.5.3 Switches

Each channel's I/O base address is set via a 6-position switch.

Figure 3: Switch Positions



Note

Keep in mind that each channel uses 8 I/O addresses. For example, on the 2-channel card, selecting I/O addresses 228 and 250 actually uses 228 through 22F and 250 through 257.

Note

Switches 1-6 represent the channel's I/O base address.

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Table 4: Switch Settings

A “1” in the following table indicates that a switch is *on* (or UP), and a “0” indicates that a switch is *off* (or DOWN). The arrow on the switch (refer to Figure 3: Switch Positions) points to the *off* position.

Channel Base Address Hex	1	2	3	4	5	6	Remarks
0x200	0	0	0	0	0	0	game port
0x208	0	0	0	0	0	1	
0x210	0	0	0	0	1	0	
0x218	0	0	0	0	1	1	
0x220	0	0	0	1	0	0	sound card
0x228	0	0	0	1	0	1	
0x230	0	0	0	1	1	0	
0x238	0	0	0	1	1	1	
0x240	0	0	1	0	0	0	
0x248	0	0	1	0	0	1	
0x250	0	0	1	0	1	0	Default for Channel A
0x258	0	0	1	0	1	1	Default for Channel B
0x260	0	0	1	1	0	0	
0x268	0	0	1	1	0	1	
0x270	0	0	1	1	1	0	
0x278	0	0	1	1	1	1	LPT2
0x280	0	1	0	0	0	0	
0x288	0	1	0	0	0	1	
0x290	0	1	0	0	1	0	
0x298	0	1	0	0	1	1	
0x2A0	0	1	0	1	0	0	
0x2A8	0	1	0	1	0	1	
0x2B0	0	1	0	1	1	0	
0x2B8	0	1	0	1	1	1	
0x2C0	0	1	1	0	0	0	
0x2C8	0	1	1	0	0	1	
0x2D0	0	1	1	0	1	0	
0x2D8	0	1	1	0	1	1	
0x2E0	0	1	1	1	0	0	
0x2E8	0	1	1	1	0	1	COM4
0x2F0	0	1	1	1	1	0	
0x2F8	0	1	1	1	1	1	COM2
0x600	1	0	0	0	0	0	Game port
0x608	1	0	0	0	0	1	
0x610	1	0	0	0	1	0	
0x618	1	0	0	0	1	1	

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Channel Base Address Hex	1	2	3	4	5	6	Remarks
0x620	1	0	0	1	0	0	
0x628	1	0	0	1	0	1	
0x630	1	0	0	1	1	0	
0x638	1	0	0	1	1	1	
0x640	1	0	1	0	0	0	
0x648	1	0	1	0	0	1	
0x650	1	0	1	0	1	0	
0x658	1	0	1	0	1	1	
0x660	1	0	1	1	0	0	
0x668	1	0	1	1	0	1	
0x670	1	0	1	1	1	0	
0x678	1	0	1	1	1	1	LPT2
0x680	1	1	0	0	0	0	
0x688	1	1	0	0	0	1	
0x690	1	1	0	0	1	0	
0x698	1	1	0	0	1	1	
0x6A0	1	1	0	1	0	0	
0x6A8	1	1	0	1	0	1	
0x6B0	1	1	0	1	1	0	
0x6B8	1	1	0	1	1	1	
0x6C0	1	1	1	0	0	0	
0x6C8	1	1	1	0	0	1	
0x6D0	1	1	1	0	1	0	
0x6D8	1	1	1	0	1	1	
0x6E0	1	1	1	1	0	0	
0x6E8	1	1	1	1	0	1	COM4
0x6F0	1	1	1	1	1	0	
0x6F8	1	1	1	1	1	1	COM2

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2
Installation

Chapter Sections:

- System Requirements
- Handling Precautions
- Installing the Card
- Connecting to a DeviceNet Network
- Connecting to a CAN Network

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2.1 System Requirements

To install and operate the card, the following system requirements must be met:

- Minimum 8K window in host memory map (default is 16K)
- An available PC/104 slot
- If interrupts are required, you will need a physical interrupt for each channel on which they will be enabled.



Note

As each channel operates independently, you do not need to enable interrupts on one channel to make them work on the other.

2.2 Handling Precautions

The card contains components that are sensitive to electrostatic discharge (ESD). Do not touch it without following these precautions:



Caution

- Always follow correct ESD procedures before handling the card. We strongly recommend the use of a grounding wrist strap as a standard handling practice.
- Never touch any of the card's connectors or pins. Handle the card by its edges or bracket.
- When the card is not in your computer, always store it in its protective anti-static bag.

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2.3 Installing the Card

To install the card in your computer:

1. Ensure that all power to the computer is off.
2. Adequately ground yourself, as cautioned in Section 2.2, Handling Precautions.
3. Unplug the power cord, modem (if applicable), and any network cables.
4. Remove the computer cover. Consult your computer user's guide for information on installing add-in boards.
5. Remove the card from its shipping container and anti-static bag, being careful not to touch any of the connectors or pins.
6. Set each switch to the selected I/O address (refer to Section 1.5.3, Switches, for details).
7. Firmly press the card on to the PC/104 connector.
8. Secure the card using the standoffs provided. Re-connect any items unplugged in Step 3.
9. Connect the card to the DeviceNet network, as explained in the following section.
10. Replace the computer cover and power up the machine.

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2.4 Connecting to a Network

This section consists of two parts: connecting to a DeviceNet network, and connecting to a CAN network.

2.4.1 Connecting to a DeviceNet Network

Connect either a DeviceNet Trunk or Drop cable to the 5-pin connector according to the color code in Section 1.5.1, CAN Connector. Make sure that all strands of wire go into the connector, as bent strands may cause shorts to the adjacent terminal.

Directly connecting DeviceNet Trunk cable is not recommended due to the mechanical stress placed on the connector by the heavy trunk cable. If you must attach trunk cable, secure it so no undue stress is placed on the 5-pin screw terminal connector.

2.4.1.1 Termination

The card does not have a built-in termination resistor. Each network must have two termination resistors—one at each end. Always refer to the DeviceNet Specification (see Section D.2, Reference Documents) for proper network termination and wiring directions.

2.4.1.2 Power

Refer to http://www.odva.org/ for basic network guidelines, and to the DeviceNet Specification for proper powering directions.

2.4.1.3 Grounding

The network shield should be connected directly to earth ground at a single point in the network. Refer to http://www.odva.org/ for basic network guidelines, and to the DeviceNet Specification for proper grounding directions.

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2.4.2 Connecting to a CAN Network

Connect the CAN cable to the 5-pin connector and tighten all screws. Make sure that all strands of wire go into the connector as bent strands may cause shorts to an adjacent terminal.

2.4.2.1 Termination

The card does not have a built-in termination resistor. You must add termination in accordance with the requirements of the target CAN network.

2.4.2.2 Power

If the CAN Network does not supply 24 VDC power, connect an external power supply to the V+ and V- pins on the connector.

2.4.2.3 Grounding

Refer to the CAN network documentation for grounding directions.

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3
Hardware Registers

Chapter Sections:

- DN3 Card Configuration Registers

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3.1 DN3 Card Configuration Registers

This section provides hardware register details for the card.

3.1.1 Host Register Layout

Each channel has its own set of registers, located in I/O space. The base I/O address is set via the switch.



Note

Upon card power up, or after a physical reset from the system, it typically takes 1 second for the channel to initialize (though it is recommended that applications wait up to 2 seconds). Initialization can be confirmed by monitoring the LEDs or by reading the FamilyID register, as described in Section C.1.1, Verify Card Presence.

Table 5: Host Register Layout

The following “offsets” are offsets from the base address.

Offset	Register Name	Bit Name							
		7	6	5	4	3	2	1	0
0	Control	CardRun	MemEn	IntEn	WdTout	HostIrq1	HostIrq0	CardIrq1	CardIrq0
1	AddrMatch	AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12
2	BankAddress	BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12
3	WinSize	WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12
4	HostIrq	Reserved				IrqLevel			
5(rd)	LedReg	Reserved		PwrRed	PwrGrn	HealthRed	HealthGrn	CommRed	CommGrn
6	Reserved, 00h								
7(rd)	FamilyId	DN3 = 40h							

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3.1.2 Control Register

This register is a group of control and status bits.

Table 6: Control Register Settings

Bit	7	6	5	4	3	2	1	0
Name	CardRun	MemEn	IntEn	WdTout	HostIrq1	HostIrq0	CardIrq1	CardIrq0
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Each channel has four interrupt flags, two for use in each direction. Setting CardIrq1 or CardIrq0 generates an interrupt to the card with the relevant flag set. When HostIrq1 OR HostIrq0 is '1' and IntEn is '1', the card drives the IRQ pin (as set by IrqLevel) high.

One flag could be used for a command interface, and another for changing I/O data.
The firmware module dictates how these flags are used. If the module uses only one flag, it will be Flag 0.

Table 7: Control Register Bit Descriptions

Bit Name	Description
CardRun	This bit controls and indicates whether or not the channel's processor is running. It also affects the Health LED. • When this bit is 0, the processor is halted, and the LED is RED • When this bit is 1, the processor is running normally, and the LED is under channel processor control • When this bit is 1, and watchdog has timed out, processor is halted, and the LED is RED • This bit must remain low for at least 50 μs to guarantee proper reset.
MemEn	This bit indicates and controls whether or not the channel's shared memory will respond to host memory accesses. This may be used to multiplex several SST-DN3-104-1 or SST-DN3-104-2 cards or channels at the same base address by enabling the memory on one channel at a time. MemEn high ('1') enables shared memory decoding of addresses in this board's range.
IntEn	• Writing 1 enables interrupts • Writing 0 disables interrupts (the HostIrq flags still function as described)
WdTout	WdTout high ('1') indicates that a watchdog timeout has occurred, or that the channel's processor has been held in RESET by some other means. To restore this bit to 0, clear CardRun.

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Bit Name	Description
HostIrq1	• This bit is used by the channel's processor to send interrupts to interrupt flag 1 of the host. • Writing 1 acknowledges the interrupt and clears it • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
HostIrq0	• This bit is used by the channel's processor to send interrupts to interrupt flag 0 of the host. • Writing 1 acknowledges the interrupt and clears it • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
CardIrq1	This bit is used by the host to send interrupts to interrupt flag 1 of the channel's processor. • Writing 1 generates an interrupt • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
CardIrq0	This bit is used by the host to send interrupts to interrupt flag 0 of the channel's processor. • Writing 1 generates an interrupt • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete

3.1.3 AddrMatch Register

This register controls the base memory address of the channel in host memory space.

Each channel may be at a different address. If two channels are used at the same address, use MemEn to turn on one channel at a time.



Caution

Setting two channels or two cards to the same address and enabling the channels could damage the card permanently.

Table 8: AddrMatch Register Settings

Bit	7	6	5	4	3	2	1	0
Name	AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	1	0	0	0	0	0	0	0

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Table 9: AddrMatch Register Values

Bit and Value								Hex	Address
AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12		
1	0	0	0	0	0	0	0	0x80	0x80000
1	0	0	0	0	0	1	0	0x82	0x82000
1	0	0	0	0	1	0	0	0x84	0x84000
1	0	0	0	0	1	1	0	0x86	0x86000
1	0	0	0	1	0	0	0	0x88	0x88000
1	0	0	0	1	0	1	0	0x8A	0x8A000
1	0	0	0	1	1	0	0	0x8C	0x8C000
1	0	0	0	1	1	1	0	0x8E	0x8E000
1	0	0	1	0	0	0	0	0x90	0x90000
1	0	0	1	0	0	1	0	0x92	0x92000
1	0	0	1	0	1	0	0	0x94	0x94000
1	0	0	1	0	1	1	0	0x96	0x96000
1	0	0	1	1	0	0	0	0x98	0x98000
1	0	0	1	1	0	1	0	0x9A	0x9A000
1	0	0	1	1	1	0	0	0x9C	0x9C000
1	0	0	1	1	1	1	0	0x9E	0x9E000
1	0	1	0	0	0	0	0	0xA0	0xA0000
1	0	1	0	0	0	1	0	0xA2	0xA2000
1	0	1	0	0	1	0	0	0xA4	0xA4000
1	0	1	0	0	1	1	0	0xA6	0xA6000
1	0	1	0	1	0	0	0	0xA8	0xA8000
1	0	1	0	1	0	1	0	0xAA	0xAA000
1	0	1	0	1	1	0	0	0xAC	0xAC000
1	0	1	0	1	1	1	0	0xAE	0xAE000
1	0	1	1	0	0	0	0	0xB0	0xB0000
1	0	1	1	0	0	1	0	0xB2	0xB2000
1	0	1	1	0	1	0	0	0xB4	0xB4000
1	0	1	1	0	1	1	0	0xB6	0xB6000
1	0	1	1	1	0	0	0	0xB8	0xB8000
1	0	1	1	1	0	1	0	0xBA	0xBA000
1	0	1	1	1	1	0	0	0xBC	0xBC000
1	0	1	1	1	1	1	0	0xBE	0xBE000
1	1	0	0	0	0	0	0	0xC0	0xC0000
1	1	0	0	0	0	1	0	0xC2	0xC2000
1	1	0	0	0	1	0	0	0xC4	0xC4000
1	1	0	0	0	1	1	0	0xC6	0xC6000
1	1	0	0	1	0	0	0	0xC8	0xC8000
1	1	0	0	1	0	1	0	0xCA	0xCA000
1	1	0	0	1	1	0	0	0xCC	0xCC000

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Bit and Value								Hex	Address
AM19	AM18	AM17	AM16	AM15	AM14	AM13	AM12		
1	1	0	0	1	1	1	0	0xCE	0xCE000
1	1	0	1	0	0	0	0	0xD0	0xD0000
1	1	0	1	0	0	1	0	0xD2	0xD2000
1	1	0	1	0	1	0	0	0xD4	0xD4000
1	1	0	1	0	1	1	0	0xD6	0xD6000
1	1	0	1	1	0	0	0	0xD8	0xD8000
1	1	0	1	1	0	1	0	0xDA	0xDA000
1	1	0	1	1	1	0	0	0xDC	0xDC000
1	1	0	1	1	1	1	0	0xDE	0xDE000
1	1	1	0	0	0	0	0	0xE0	0xE0000
1	1	1	0	0	0	1	0	0xE2	0xE2000
1	1	1	0	0	1	0	0	0xE4	0xE4000
1	1	1	0	0	1	1	0	0xE6	0xE6000
1	1	1	0	1	0	0	0	0xE8	0xE8000
1	1	1	0	1	0	1	0	0xEA	0xEA000
1	1	1	0	1	1	0	0	0xEC	0xEC000
1	1	1	0	1	1	1	0	0xEE	0xEE000
1	1	1	1	0	0	0	0	0xF0	0xF0000
1	1	1	1	0	0	1	0	0xF2	0xF2000
1	1	1	1	0	1	0	0	0xF4	0xF4000
1	1	1	1	0	1	1	0	0xF6	0xF6000
1	1	1	1	1	0	0	0	0xF8	0xF8000
1	1	1	1	1	0	1	0	0xFA	0xFA000
1	1	1	1	1	1	0	0	0xFC	0xFC000
1	1	1	1	1	1	1	0	0xFE	0xFE000

Table 10: AddrMatch Register Bit Descriptions

Bit Name	Description
AM19 – AM12	AM19-AM12 represent the upper address match required to decode memory. These bits select the base memory address, from 0xA0000 to 0xFE000. For example, writing 0xD0 to this register selects 0xD0000 as the memory base address. Refer to Table 9: AddrMatch Register Values for more details. If a 16K window size is selected, AM13-AM12 are ignored and 16K boundaries are used for the memory address. As a result, only even-window boundaries may be chosen. The card could be set to 0xD0000 or 0xD4000 but 0xD2000 would be invalid. Refer to Table 12: WinSize Register Values for information on bit usage with other window sizes.

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3.1.4 WinSize Register

This register controls the window size by masking off the AM19-AM12 and BA19-12 bits in the AddrMatch and Bank Address registers. Table 12, WinSize Register Values, maps the WS bit values required for each valid window size.

Table 11: WinSize Register Settings

Bit	7	6	5	4	3	2	1	0
Name	WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	1	1

Table 12: WinSize Register Values

In this table, the default window values are highlighted.

Bit and Value								Window Size	Description
WS19	**WS18**	**WS17**	**WS16**	**WS15**	**WS14**	**WS13**	**WS12**		
0	0	0	0	0	0	0	1	8K	AM19-AM13 used, AM12 ignored BA19-BA13 used, BA12 ignored
0	0	0	0	0	0	1	1	16K	AM19-AM14 used, AM13-AM12 ignored BA19-BA14 used, BA13-BA12 ignored
0	0	0	0	0	1	1	1	32K	AM19-AM15 used, AM14-AM12 ignored BA19-BA15 used, BA14-BA12 ignored
0	0	0	0	1	1	1	1	64K	AM19-AM16 used, AM15-AM12 ignored BA19-BA16 used, BA15-BA12 ignored
0	0	0	1	1	1	1	1	128K	AM19-AM17 used, AM16-AM12 ignored BA19-BA17 used, BA16-BA12 ignored
0	0	1	1	1	1	1	1	256K	AM19-AM18 used, AM17-AM12 ignored BA19-BA18 used, BA17-BA12 ignored

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Table 13: WinSize Register Bit Descriptions

Bit Name	Description
WS19-WS12	WS19-WS12 represent the window size, according to Table 12: Winsize Register Values. • Writing any value other than those above has no effect The size of the memory window affects the number of banks required to access all memory. Refer to Table 15: Bank Address Register Values, for more information.

3.1.5 Bank Address Register

This register is used to switch banks of shared memory into host memory space.

Table 14: Bank Address Register Settings

Bit	7	6	5	4	3	2	1	0
Name	BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Table 15: Bank Address Register Values

In this table, the default window size is highlighted, and a value of "x" indicates "don't care".

Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	0	0	0	0	0	x	0	0	0	0	0	0
x	x	0	0	0	0	1	x	1	0	0	0	0	0
x	x	0	0	0	1	0	x	2	1	0	0	0	0
x	x	0	0	0	1	1	x	3	1	0	0	0	0
x	x	0	0	1	0	0	x	4	2	1	0	0	0
x	x	0	0	1	0	1	x	5	2	1	0	0	0
x	x	0	0	1	1	0	x	6	3	1	0	0	0
x	x	0	0	1	1	1	x	7	3	1	0	0	0
x	x	0	1	0	0	0	x	8	4	2	1	0	0
x	x	0	1	0	0	1	x	9	4	2	1	0	0
x	x	0	1	0	1	0	x	10	5	2	1	0	0
x	x	0	1	0	1	1	x	11	5	2	1	0	0
x	x	0	1	1	0	0	x	12	6	3	1	0	0
x	x	0	1	1	0	1	x	13	6	3	1	0	0

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Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	0	1	1	1	0	x	14	7	3	1	0	0
x	x	0	1	1	1	1	x	15	7	3	1	0	0
x	x	1	0	0	0	0	x	16	8	4	2	1	0
x	x	1	0	0	0	1	x	17	8	4	2	1	0
x	x	1	0	0	1	0	x	18	9	4	2	1	0
x	x	1	0	0	1	1	x	19	9	4	2	1	0
x	x	1	0	1	0	0	x	20	10	5	2	1	0
x	x	1	0	1	0	1	x	21	10	5	2	1	0
x	x	1	0	1	1	0	x	22	11	5	2	1	0
x	x	1	0	1	1	1	x	23	11	5	2	1	0
x	x	1	1	0	0	0	x	24	12	6	3	1	0
x	x	1	1	0	0	1	x	25	12	6	3	1	0
x	x	1	1	0	1	0	x	26	13	6	3	1	0
x	x	1	1	0	1	1	x	27	13	6	3	1	0
x	x	1	1	1	0	0	x	28	14	7	3	1	0
x	x	1	1	1	0	1	x	29	14	7	3	1	0
x	x	1	1	1	1	0	x	30	15	7	3	1	0
x	x	1	1	1	1	1	x	31	15	7	3	1	0

* x = don’t care

Table 16: Bank Address Register Bit Descriptions

Bit Name	Description
BA17-13	Each channel has 256k of memory accessible to the host. The Bank Address bits select which bank of memory the host can access. For example, in 16k mode, the bank number may be 0 through 15 (or 0x0 - 0xf). • The primary host interface window is located in bank 0 • BA17-BA13 represent the bank address, providing A17-A13 for shared RAM accesses • Bank numbers depend on the window size, selected using the WinSize bits. Refer to Table 12: WinSize Register Values, for more information.

To access any flat address of memory, “ADDR” in any window size, set the Bank Address bits to bits 19-12 of the address. In C, you would write:

```
outport( BankSelect, addr>>12);
offset= addr & ((inport( WinSize ) <<12 ) | 0x3FFF);
```


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3.1.6 HostIrq Register

This register controls how interrupts from the card are generated.

Table 17: HostIrq Register Settings

Bit	7	6	5	4	3	2	1	0
Name	Reserved				IrqLevel3	IrqLevel2	IrqLevel1	IrqLevel0
Read/Write	R	R	R	R	RW	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 18: HostIrq Register Bit Descriptions

Bit Name/ Value				Description
IrqLevel3-IrqLevel0				These bits determine the hardware interrupt level used when interrupts are enabled and an interrupt is generated by the channel's processor. Supported values are:
0	0	1	0	IRQ 2
0	1	0	1	IRQ 5
0	1	1	1	IRQ 7
1	0	0	1	IRQ 9
1	0	1	0	IRQ 10
1	0	1	1	IRQ 11
1	1	0	0	IRQ 12
1	1	1	1	IRQ 15
Any other value is not supported, and causes hardware interrupts to be disabled.				



Caution

On the 2-channel card, do not set Channel A's HostIrq to that of Channel B's, unless one or both channels are disabled.

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3.1.7 LedReg Register

This register reflects the state of the channel's LEDs, allowing host software to monitor the LEDs and display them on-screen.

Table 19: LedReg Register Settings

			PWR		HLTH		COMM	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		PwrRed	PwrGrn	HealthRed	HealthGrn	CommRed	CommGrn
Read/Write	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Table 20: LedReg Register Values

Bit Name/Value		Description
PwrRed	**PwrGrn**	These bits indicate the state of the channel's power LED.
0	0	Invalid
0	1	LED is green
1	0	LED is red
1	1	Invalid
HealthRed	**HealthGrn**	These bits indicate the state of the channel's health LED
0	0	LED is off
0	1	LED is green
1	0	LED is red
1	1	LED is amber
CommRed	**CommGrn**	These bits indicate the state of the channel's communications LED
0	0	LED is off
0	1	LED is green
1	0	LED is red
1	1	LED is amber

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3.1.8 Reserved Register

This register is reserved and must not be accessed by host applications.

3.1.9 FamilyId Register

This register identifies the product family of the card.

Table 21: FamilyId Register Settings

Bit	7	6	5	4	3	2	1	0
Name	FamilyId7	FamilyId6	FamilyId5	FamilyId4	FamilyId3	FamilyId2	FamilyId1	FamilyId0
Read/Write	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Run	0	1	0	0	0	0	0	0

Table 22: FamilyId Bit Descriptions

Bit/Reset Value								Description
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0	1	0	0	0	0	0	0	DN3 Family interface card
All other combinations								Reserved

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4
Troubleshooting

Chapter Sections:

- HLTH or PWR LED is Red
- Memory Conflict
- Card Not Found

For a list of hardware-related errors that can be generated by the card, refer to Appendix A, Error Messages.



Warning

Only qualified electrical personnel familiar with the construction and operation of this equipment and the hazards involved should install, adjust, operate, or service this equipment. Failure to observe this precaution could result in severe bodily injury or loss of life.

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4.1 HLTH or PWR LED is Red

This section describes strategies for troubleshooting, using a red HLTH or PWR LED.



Note

For information on LED flash codes, refer to Section A.3, Fatal Hardware Self-Test Flash Codes.

4.1.1 HLTH LED is Red

If the HLTH LED is red, the channel's processor is not running or there has been a firmware run-time error. Check the WdTout bit (refer to Table 7, Control Register Bit Descriptions) to determine whether or not there has been a watchdog timeout, and consult the appropriate firmware manual if necessary. If you continue to experience difficulties, please refer to Section 4.4, General Troubleshooting.



Note

The firmware must be reloaded to restart the processor.

4.1.2 PWR LED is Red

If the PWR LED is red, there is no power applied to the V+ and V- DeviceNet Network Power pins. Check the network power supply and network cable connectors.



Caution

Excessive voltage may damage the card permanently.

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4.2 Memory Conflict

If a memory conflict is detected, examine the resource allocations in the operating system. If the operating system does not manage resources, review the requirements of the other hardware installed in the machine to select a non-conflicting memory window. If you continue to experience difficulties, please refer to Section 4.4, General Troubleshooting.

4.3 Card Not Found

If a "card not found" message is displayed, double-check the switch settings and make sure they match up with the I/O driver, port address setting, in the host application software. Check for memory I/O and IRQ conflicts. If you continue to experience difficulties, refer to Section 4.4, General Troubleshooting.

4.4 General Troubleshooting

If you experience problems with the card:

1. Check the website at http://www.mysst.com/ for technical notes and DeviceNet release notes.

2. Check the FAQs found in the Technical Support section of the website at http://www.mysst.com/.

3. Refer to Section D.3, Technical Support.

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A

Error Messages

Appendix Sections:

- Introduction
- FamilyID Messages
- Fatal Hardware Self-Test Flash Codes

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A.1 Introduction

The following errors may be reported during the card's startup self-test. Error messages are posted in the Message Area (0x40) of the Host Interface Memory and can be displayed using one of the status applications, such as DNSTAT, provided with the card.

A.2 FamilyID Messages

If FamilyID reads anything other than 0x40, the card has not been found. To fix the problem, follow these steps:

1. Double-check the switch settings and make sure they match up with the I/O driver port address setting in the software application.
2. Make sure you have waited up to 2 seconds after the PC/104 RESET signal has been negated.
3. Check for an I/O conflict.
4. If you continue to experience difficulties, please refer to Section 4.4, General Troubleshooting.

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A.3 Fatal Hardware Self-Test Flash Codes

Fatal failures during startup are accompanied by an 8-bit fault code, flashed on the HLTH LED. The fault code will be output MSB first, with a 1 (one) bit shown as a green LED, and a zero (0) bit shown as a red LED. This will occur for a period of 900ms, followed by 100ms of off time. The LSB will be followed by an additional 1000ms of off time, after which the sequence will repeat.

The following table describes each possible fault code. If you see any of these codes, please contact Technical Support.

Table 23: LED Flash Codes

Value	Name	Description
0x01	BITTEST8	Bit test failure of an 8-bit memory range
0x02	BITTEST16	Bit test failure of a 16-bit memory range
0x03	BITTEST32	Bit test failure of a 32-bit memory range
0x04	ADDRTEST8	Address test failure of an 8-bit memory range
0x05	ADDRTEST16	Address test failure of a 16-bit memory range
0x06	ADDRTEST32	Address test failure of a 32-bit memory range
0x07-0x10	-	Reserved for future fatal start-up errors
0x11	JTAG_ UNKNOWN	JTAG programming error
0x12	JTAG_TDOMISMATCH	JTAG output data failed to match expected pattern
0x13	JTAG_MAXRETRIES	JTAG output data failed to match expected pattern after several attempts
0x14	JTAG_ILLEGALCMD	JTAG programming file contained an unknown/malformed command
0x15	JTAG_ILLEGALSTATE	JTAG programming file commanded an illegal TAP state transition
0x16	JTAG_DATAOVERFLOW	JTAG programming file contained a shift pattern in excess of MAX_LEN * 8 bits
0x20-0xFF	-	Reserved.

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B

Technical Specifications

Appendix Sections

- Technical Specifications

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B.1 Technical Specifications

The following tables list the technical specifications for the card.

Table 24: Environmental Specifications

Ambient Conditions	Storage temp:	-40°C to +85°C
	Operating temp:	0°C to 55°C
	Humidity:	5% to 95% non-condensing
	Ventilation	Airflow must be sufficient to ensure that card does not overheat.

Table 25: Network Specifications

Cable	Shielded twisted pair, compatible with target network
External Power	11-24 VDC, 50mA (typical)
Isolation	500V
Protocol	CAN 2.0 A/B
Data Rate	Up to 1 Mbaud

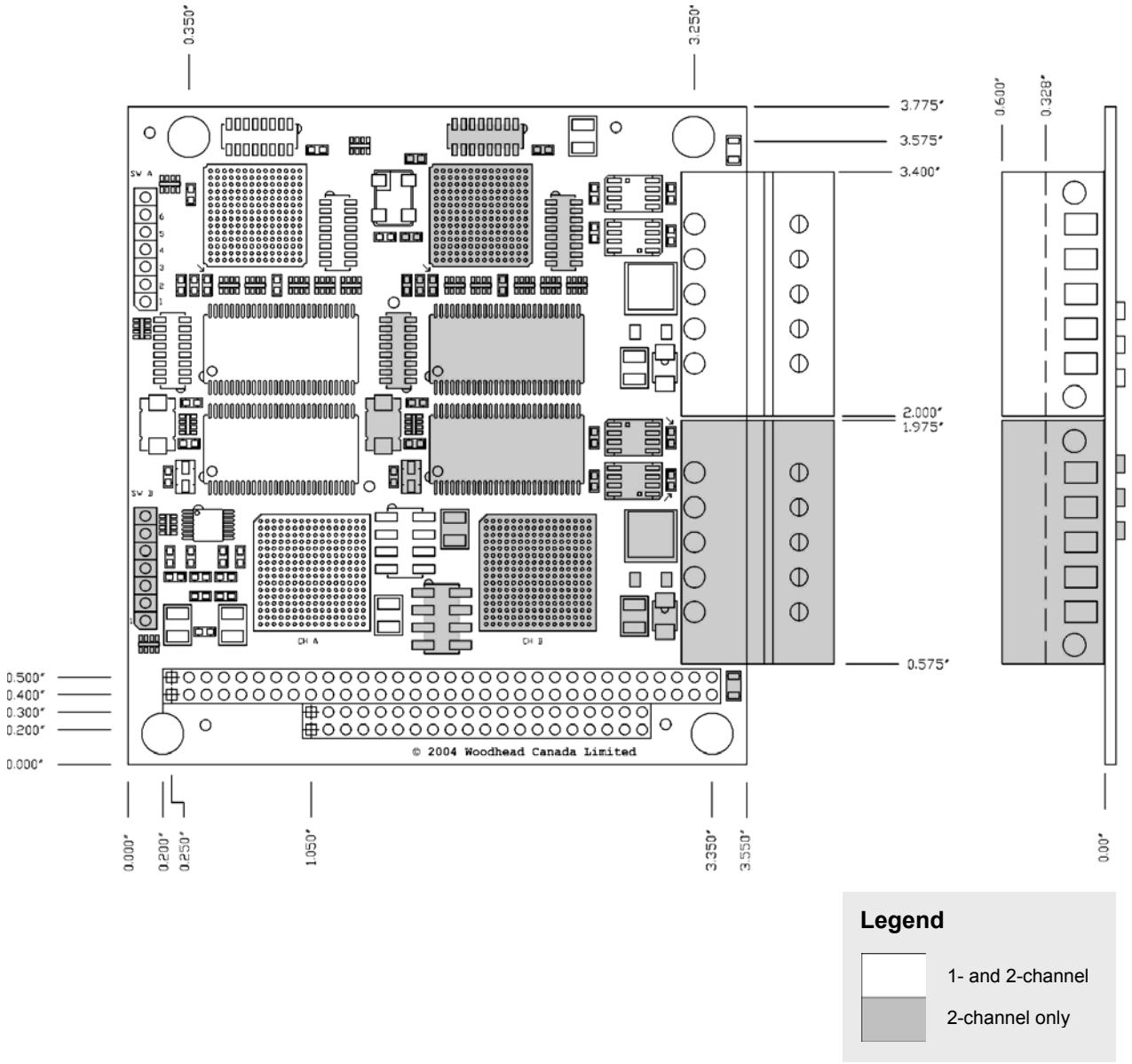
Table 26: PC/104 Bus Specifications

Dimensions (See Figure 4 for a detailed breakdown of dimensions)	General:	16-bit PC/104 2.3 or 2.4
	Height:	3.775 inches
	Width:	3.550 inches
Capabilities	Memory:	16-bit data, 20-bit address (1 MB upper limit)
	I/O:	8-bit data, 16-bit address
Addressing	Memory:	256K in a window of 8K, 16K, 32K, 64K, 128K, or 256K bytes on even window boundary between 512K and 1Mb
	I/O:	8 bytes on any even 8-bit boundary from 0x200 - 0x2F8 or 0x600 – 0x6F8
Interrupts		Software selectable level IRQ 2/9, 5, 7, 10, 11, 12, 15; standard TTL drive
Typical Current Draw		900mA
Voltage Requirements		5 volts

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The following figure provides a detailed breakdown of the card's dimensions.

Figure 4: SST-DN3-104-1 & 2 Interface Card Dimensions



For information on card components, refer to Section 1.5, Hardware Description.

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C
Loading Firmware

Appendix Sections:

- Loading Firmware



Note

This appendix describes how to load firmware to the card manually, or how to write your own loader. If you are using a Windows loader provided by Woodhead Software & Electronics, the following instructions are not required.

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C.1 Loading Firmware

Firmware modules for the card are supplied as .ss3 files, found on the software CD-ROM or on the website at http://www.mysst.com/.

If you are developing a driver for the card or producing a stand-alone embedded application, the following section describes the basic sequence of steps to load a module into the channel's memory.



Note

These procedures should be repeated for each channel of the card.



Note

For register descriptions, refer to Chapter 3, Hardware Registers.

C.1.1 Verify Card Presence

To verify the channel's presence, follow these steps:

1. Start up your computer.
2. Following release of the backplane reset, wait up to 2 seconds.
3. Verify a FamilyID Register value of 0x40.
4. If FamilyID reads anything other than 0x40, the card is still in Reset or has not been found. Double-check the switch settings and make sure they match up with the I/O port address setting. If you continue to experience difficulties, please refer to Section 4.4, General Troubleshooting.

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C.1.2 Check for Conflicting RAM

Before the channel's shared memory can be safely enabled, you must determine that no other system devices are using the intended memory address range.



Note

Any task switching, interrupts or processes should be disabled during this procedure.

To check for conflicting RAM, follow these steps:

1. Write zero (0x00) to the Control Register to disable the channel.
2. Read a word from the target memory window and save it.
3. Write 0xAA55 to the target address.
4. Read the target address. It should not contain 0xAA55.
5. If 0xAA55 is read, a conflict exists. Perform the following steps:
   - Restore the saved value to the target address
   - Abort the load procedure
   - Examine the resource allocations in your operating system. If your operating system does not manage resources, review the requirements of the other hardware installed in your machine to select a non-conflicting memory window. If you continue to experience difficulties, please refer to Section 4.4, General Troubleshooting.



Note

If you are unsure of the system's memory usage, you may want to do a full memory window verification to ensure that there are no memory conflicts.

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C.1.3 Test Channel RAM

To test a channel's RAM, follow these steps:

1. Write the upper byte of the desired 20-bit base address `(base address >> 12)` to the AddrMatch Register.
2. Write the desired window size to the WinSize register (refer to Section 3.1.4, WinSize Register, for details).
3. Write 0x40 (MemEn) to the Control Register.
4. Set the Bank Address Register (refer to Section 3.1.5, Bank Address Register, for details).
5. Fill the shared memory with a test pattern.



Note

Woodhead recommends a test pattern with a unique value for each word in a given bank. In C language this could be:

```
~offset + bank.
```

6. Repeat steps 4-5 for all memory banks.
7. Verify the test pattern.

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C.1.4 Load and Start the Firmware Module

To load and start the firmware module, follow these steps:

1. Write the contents of the entire firmware file into shared memory, starting at bank zero (0), offset zero (0).

2. If the application requires interrupts from the card, write the interrupt level to the HostIrq Register and bit-wise OR value 0x20 (IntEn) to the Control Register.

3. Bit-wise OR value 0x80 (CardRun) to the Control Register to start the firmware module.

4. Start a 2-second timeout timer and wait for value 0x04 (HostIrq0) in the Control Register to set.

5. If the timer expires, the firmware module failed to start. Write zero to the Control Register to disable the channel's processor. If this problem persists, contact Technical Support for assistance.

6. Check the load status, as per the firmware manual.

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D

Warranty and Support

Appendix Sections:

- Warranty
- Reference Documents
- Technical Support

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D.1 Warranty

For warranty information pertaining to the card, refer to http://www.mysst.com/warranty.asp.

D.2 Reference Documents

The following documents provide additional details on DeviceNet and/or the card:

DeviceNet Specification, Volumes I and II, V2.0, Errata 5
http://www.odva.org/

SST-DN3-104 and 5136-DNP-104 Comparison Technical Note
http://www.mysst.com/download/

D.3 Technical Support

Please ensure that you have the following information readily available before calling for technical support:

- Card model, type and serial number
- Computer's make, model, CPU speed and hardware configuration (other cards installed)
- Operating system type and version
- Details of the problem you are experiencing: application module type and version, target network and circumstances that may have caused the problem

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D.3.1 Getting Help

Technical support is available during regular business hours by telephone, fax or email from any Woodhead Software & Electronics office, or from http://www.woodhead.com/. Documentation and software updates are also available on the website.



Note

If you are using the card with a third-party application, refer to the documentation for that package for information on configuring software for the card.

North America

Canada:
Tel: 519-725-5136
Fax: 519-725-1515
Email: supportna@woodhead.com

Europe

France:
Tel: 33-2-32-96-04-20
Fax: 33-2-32-96-04-21
Email: supportfr@applicom-int.com

Germany:
Tel: 49-711-782374-0
Fax: 49-711-782374-11
Email: infode@applicom-int-com

Italy:
Tel: 30-9-10-59-30-77
Fax: 39-10-59-56-925
Email: imainfo@imaweb.it

United Kingdom:
Tel: 44-1495-35-04-36
Fax: 44-1495-35-08-77
Email: contact@wdhd.co.uk

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Japan:
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Fax: 81-3-5791-4688
Email: sst@woodhead.co.jp

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Tel: 65-261-6533
Fax: 65-265-6605
Email: info@woodhead.com.sg

For the most current contact details, please visit http://www.woodhead.com/.

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E

CE Compliance

Appendix Sections:

- CE Compliance

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E.1 CE Compliance

This device meets or exceeds the requirements of the following standard:

- EN 61326:1998 including amendments A1 and A2: - “Electrical equipment for measurement, control and laboratory use - EMC requirements.



Warning

This is a Class A product. In a domestic environment this product may cause radio interference in which case you may be required to take adequate measures.



Caution

This equipment is neither designed for, nor intended for operation in installations where it is subject to hazardous voltages and hazardous currents.

Marking of this equipment with the symbol CE indicates compliance with European Council Directive 89/336/EEC - The EMC Directive as amended by 92/31/EEC and 93/68/EEC.



Note

To maintain compliance with the limits and requirements of the EMC Directive, it is required to use quality interfacing cables and connectors when connecting to this device. Refer to the cable specifications in the Hardware Guide for selection of cable types.



Note

The backplane voltage supply for this equipment must be delivered as Separated Extra Low Voltage (SELV).

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