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SST-DN4-PCU

Hardware Reference Guide

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This document applies to the SST-DN4-PCU interface card.

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Preface

Preface Sections:

- Purpose of this Guide
- Using this Guide
- Conventions

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Purpose of this Guide

This guide contains technical and product-related information on the SST-DN4-PCU network interface card.

The SST-DN4-PCU consists of a single independent DeviceNet network interface (or *channel*), controlled by an embedded CPU. The CPU executes downloadable application firmware modules,
which enable application-level product behavior. For more details, refer to relevant firmware documentation.



Note

In this manual, the SST-DN4-PCU will be referred to as the *card.*

Using this Guide

If you are running a 3rd party application or writing your own application using the card's DLL calls, the sections of interest in this guide will be "Card Overview", "Installation" and potentially "Troubleshooting". If you are writing your own application in a non-Windows environment (interfacing directly with the card's memory registers), we recommend that you read the whole guide.

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Conventions

This guide uses stylistic conventions, special terms, and special notation to help enhance your understanding.

Style

The following stylistic conventions are used throughout this guide:

Bold	indicates field names, button names, tab names, and options or selections
Italics	indicates keywords (indexed) or instances of new terms and/or specialized words that need emphasis
CAPS	indicates a specific key selection, such as ENTER, TAB, CTRL, ALT, DELETE
`Code Font`	indicates command line entries or text that you would type into a field
Underlining	indicates a hyperlink
“>” delimiter	indicates how to navigate through a hierarchy of menu selections/options
“0x” or “-H”	indicates a hexadecimal value

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Terminology

The following special terms are used throughout this guide:

Card	the SST-DN4-PCU network interface card
Channel	a DeviceNet network interface on the card
Firmware Module	the embedded software module that gets loaded to the card's memory and runs on the card. This is the operating system of the card, enabling it to respond to commands from the host and manage network communications.
Host	the computer system in which the card is installed
.bin	an unencrypted firmware module for the card
.ss3	an encrypted firmware module for earlier designs that the card may emulate
.ss4	an encrypted firmware module for the card

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Special Notation

The following special notations are used throughout this guide:



Warning

Warning messages alert the reader to situations where personal injury may result. Warnings are accompanied by the symbol shown, and precede the topic to which they refer.



Caution

Caution messages alert the reader to situations where equipment damage may result. Cautions are accompanied by the symbol shown, and precede the topic to which they refer.



Note

A note provides additional information, emphasizes a point, or gives a tip for easier operation. Notes are accompanied by the symbol shown, and follow the text to which they refer.

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1
Card Overview

Chapter Sections:

- Warnings and Cautions
- Card Features
- Byte Ordering
- DN4 Compatibility Overview
- Hardware Description

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1.1 Warnings and Cautions

The card is an electrical component and must be treated with the following precautions:



Warning

Only qualified electrical personnel familiar with the construction/ operation of this equipment and the hazards involved should install, adjust, operate, and/or service this equipment. Read and understand this guide in its entirety before proceeding. Failure to observe this precaution could result in severe bodily injury or, in extreme cases, loss of life.



Warning

You must provide an external, hard-wired emergency stop circuit outside the programmable controller circuitry. This circuit must disable the system in case of improper operation. Uncontrolled machine motion may result if this procedure is not followed. Failure to observe this precaution could result in bodily injury.



Caution

The card contains static-sensitive components. Careless handling may severely damage the card. Do not touch any of the connectors or pins on the card. When not in use, the card should be stored in an anti-static bag. Failure to observe this precaution could result in damage to or destruction of the equipment.

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1.2 Card Features

The card is a PCI interface for communication with DeviceNet and other CAN-based networks. The main features of each channel are:

- 32-bit PCI interface (fully compatible with PCI v2.3)
- Half height short PCI card
- 64 MHz NIOS Processor
- 256 KB of shared RAM
- DeviceNet-compliant 5-pin CAN connector
- Data rate of up to 1M baud for CAN, and 125K, 250K and 500K for DeviceNet
- Bi-color LEDs showing card status
- Isolated CAN physical layer
- Compatible with CAN specification 2.0 part A and part B

1.3 Byte Ordering

The card uses Intel-style (little endian) byte ordering for multi-byte entities LSB-low address and MSB-high address. If your host system uses Motorola (big endian) byte ordering (MSB-low address and LSB-high address), you must compensate for byte ordering in software.

The following language macro will compensate for byte ordering in a 16-bit data entity:

```
#define SWAP_WORD (WordData) ((WordData<<8) | (WordData>>8))
```


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1.4 DN4 Compatibility Overview

For a comparison of DN4 with DN3 and DNP, refer to Section D.2, Reference Documents.

The following table outlines the requirements of different PCI revisions and the PCI requirements of the card.

Table 1: PCI Compatibility Table

PCI Specification Revision	Supply Voltage Provided by Motherboard		PCI I/O Signaling Voltage Level of Motherboard	
	3.3V	5V	3.3V	5V
2.1	[1]Optional	Required	Not supported	Supported
2.2	Required	Required	Supported	Supported
2.3	Required	Required	Supported	Not supported
SST Product				
SST-DN4-PCU	Optional	Required	[2]Supported	[2]Supported

[1] The card requires only 5V to be supplied by the motherboard. Because 3.3V supply voltage is optional in PCI specification revision 2.1, the card may not function in some PCI 2.1-compliant motherboards.

[2] The card will auto-detect the motherboard PCI I/O signaling level and adjust its signaling level accordingly, allowing it to function in PCI systems that support either 5V or 3.3V I/O signaling levels.

Summary

The card's compatibility can be summarized as follows:

- It will operate in PCI v2.2- and v2.3-compliant systems

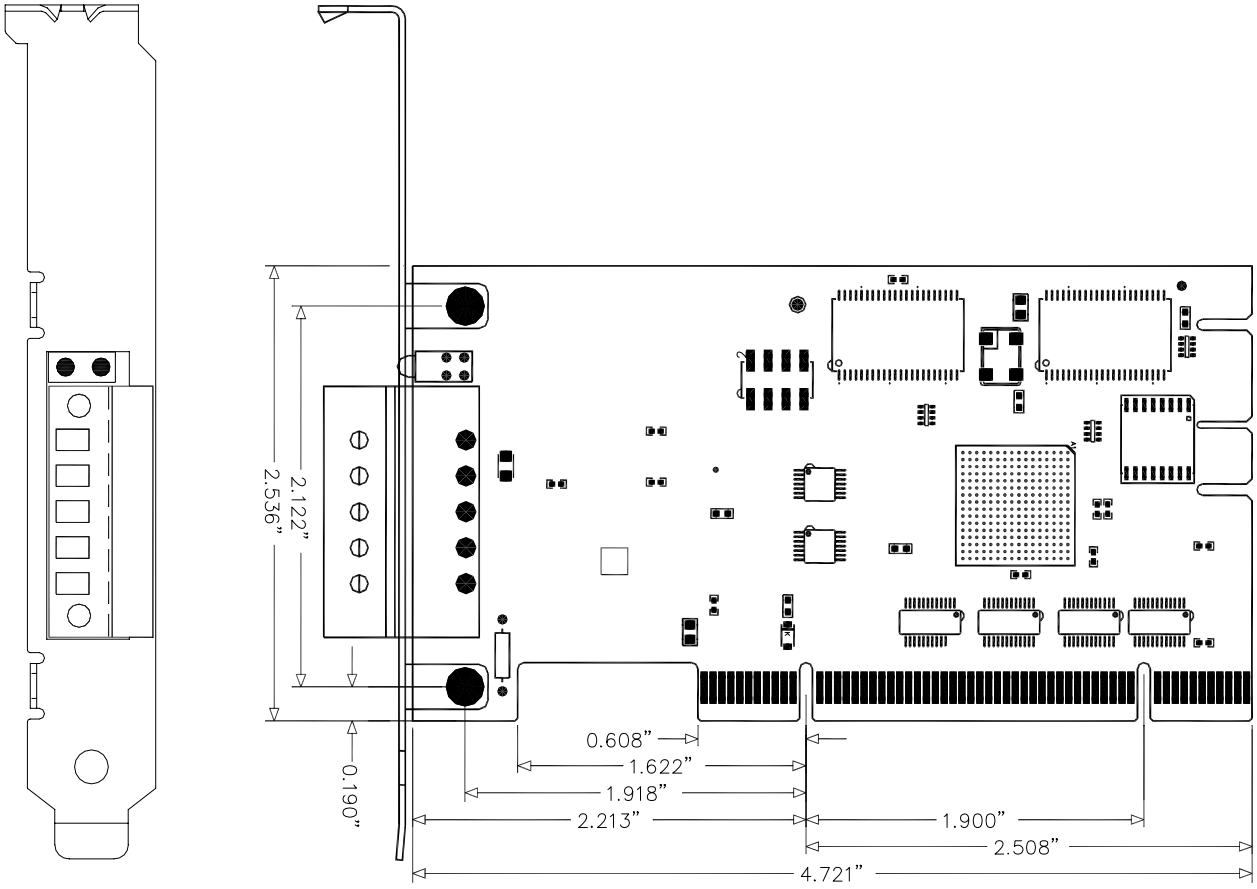
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1.5 Hardware Description

The main features of the card are described in more detail in the following sections. For information on card dimensions, refer to Section B.1, Technical Specifications.

Figure 1: The SST-DN4-PCU Interface Card



Card Components

Feature	Description
1	Channel A HLTH LED (top)
2	Channel A CAN Connector
3	Channel A COMM LED (bottom)

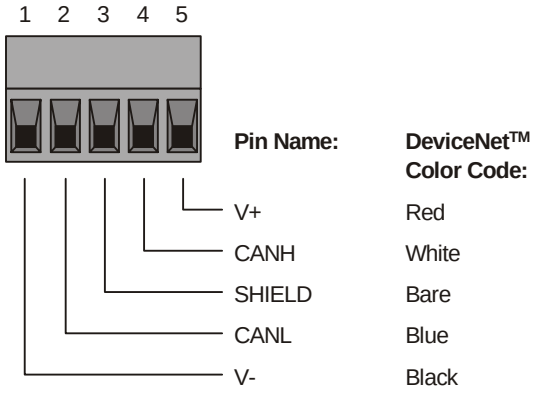
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1.5.1 CAN Connector

The 5-pin connector is a standard removable connector that conforms to the standard DeviceNet pinout. Pin numbers, names, and color codes are identified in the figure below.

Figure 2: 5-Pin CAN Connector



1.5.1.1 V+, V-

These terminals provide power to the isolated section of the network interface, and must be connected in order for the card to function. On DeviceNet networks, they connect directly to the red (V+) and black (V-) wires of the DeviceNet cable. On non-powered CAN networks, they must be connected to an external 11-24VDC supply.

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1.5.1.2 CANH, CANL

These are the CAN communication bus signal terminals. Use only shielded twisted pair cable.

1.5.1.3 SHIELD

This is the shield connector. This terminal is “snubbed” to the PC/PCI chassis ground via a 1M-ohm resistor.



Note

According to the DeviceNet specification, the snubber circuit can be omitted if the card has no local connection to ground.



Note

The shield should be connected directly to earth ground at only one point in the network. Refer to Section 2.4, Connecting to a Network, for more information.

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1.5.2 LEDs

There are two LEDs per channel: Health (HLTH) and Communications (COMM).

Note

For information on troubleshooting using LEDs, refer to Section 4.1, HLTH LED is Red.

Figure 3: Mounting Bracket, Front View

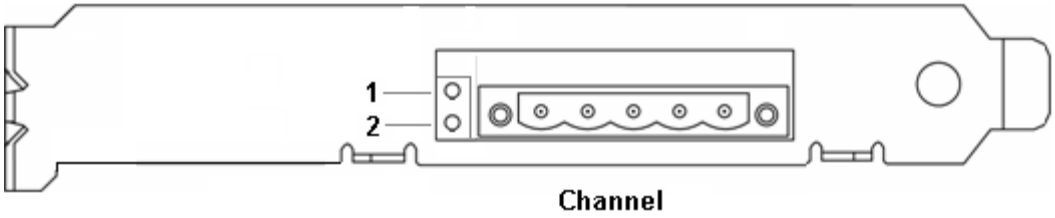


Table 2: LED Descriptions

Feature	Description
1	Channel A HLTH LED
2	Channel A COMM LED

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1.5.2.1 HLTH LED

The HLTH LED indicates the channel's health status. The HLTH LED's behavior is described in the following table.

Table 3: HLTH LED Behavior

Color	Status
Off	Card initialization failed or the card is not powered
Green	The firmware is loaded and running
Red	The card has not loaded, an error occurred during the load or there is a firmware run-time error
Amber	Startup self-test complete, no firmware loaded. The firmware must be reloaded (refer to Section 4.1, HLTH LED is Red).



Note

If the HEALTH LED is flashing, there may have been a startup failure. For more details, refer to Section A.3, Fatal Hardware Self-Test Flash Codes.

1.5.2.2 COMM LED

The COMM LED indicates the network status. This LED's meaning and behavior are determined by the currently loaded firmware module. Refer to the module's reference guide for more details.

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2
Installation

Chapter Sections:

- System Requirements
- Handling Precautions
- Installing the Card
- Connecting to a Network

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2.1 System Requirements

To install and operate the card, the following system requirements must be met:

- An available PC v2.2 or v2.3 slot. The card will also operate in some PCI v2.1-compliant systems. Refer to Section 1.4, DN4 Compatibility Overview, for more compatibility details.
- If interrupts are required, you will need a physical interrupt.

2.2 Handling Precautions

The card contains components that are sensitive to electrostatic discharge (ESD). Do not touch it without following these precautions:



Caution

- Always follow correct ESD procedures before handling the card. We strongly recommend the use of a grounding wrist strap as a standard handling practice.
- Never touch any of the card's connectors or pins. Handle the card by its edges or bracket.
- When the card is not in your computer, always store it in its protective anti-static bag.

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2.3 Installing the Card

To install the card in your computer:

1. Ensure that all power to your computer is off.
2. Adequately ground yourself, as cautioned in Section 2.2, Handling Precautions.
3. Unplug the power cord, modem (if applicable), and any network cables.
4. Remove the computer cover. Consult your computer user's guide for information on installing add-in boards.
5. Take the card out of its shipping container and anti-static bag, being careful not to touch any of the connectors or pins.
6. Firmly press the card into a compatible PCI-compliant connector.
7. Secure the card using the screws provided. Re-connect any items unplugged in Step 3.
8. Replace the computer cover and power up the machine.
9. Connect the card to the DeviceNet network, as explained in the following section.

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2.4 Connecting to a Network

This section is divided into two parts: connecting to a DeviceNet network, and connecting to a CAN network.

2.4.1 Connecting to a DeviceNet Network

Connect either a DeviceNet Trunk or Drop cable to the 5-pin connector according to the color code in Section 1.5.1, CAN Connector. Make sure that all strands of wire go into the connector, as bent strands may cause shorts to the adjacent terminal.

Directly connecting DeviceNet thick cable to the card is not recommended due to the mechanical stress that the cable places on the connector. If you must attach thick cable, secure it to prevent undue stress.

2.4.1.1 Termination

The card does not have a built-in termination resistor. Each network must have two termination resistors—one at each end of the trunk. Always refer to the DeviceNet Specification (see Section D.2, Reference Documents) for proper network termination and wiring directions.

2.4.1.2 Power

Refer to http://www.odva.org/ for basic network guidelines, and to the DeviceNet Specification for proper powering directions.

2.4.1.3 Grounding

The network shield should be connected directly to earth ground at a single point in the network. Refer to http://www.odva.org/ for basic network guidelines, and to the DeviceNet Specification for proper grounding directions.

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2.4.2 Connecting to a CAN Network

Connect the CAN cable to the 5-pin connector and tighten all screws. Make sure that all strands of wire go into the connector as bent strands may cause shorts to an adjacent terminal.

2.4.2.1 Termination

The card does not have a built-in termination resistor. You must add termination in accordance with the requirements of the target CAN network.

2.4.2.2 Power

If the CAN Network does not supply 11-24 VDC power, connect an external power supply to the V+ and V- pins on the connector.

2.4.2.3 Grounding

Refer to the CAN network documentation for grounding directions.

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3
Hardware Register Details

Chapter Sections:

- Introduction
- Card Configuration Space
- Card Configuration Registers

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3.1 Introduction

This section provides technical hardware information. The following information is intended for programmers familiar with hardware-level PC programming.

3.2 Card Configuration Space

This section provides card configuration details for the card.



Note

Refer to the PCI specification and your particular OS documentation for the function of all other PCI configuration space registers and their typical uses.



Note

Typically, the PCI configuration space registers do not need to be written to by the host system driver. A Plug & Play BIOS and/or host operating system will ensure there are no resource conflicts in the system.

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Table 4: Card Configuration Space

In this table, information relevant to the card is bolded.

PCI CFG Register Address	Register Function 32 24 23 16 15 8 7 0				PCI Writable
0000H	**Device ID 0x9030**		**Vendor ID 0x10B5**		N
0004H	Status 0x0000		Command 0x0000		Y
0008H	Class Code 0x0280000			Revision ID Factory set	N
000CH	BIST 0x00	Header ID 0x00	PCI Latency 0x00	CacheLineSize 0x00	Y[7:0]
0010H	PCI Base Address 0 for Memory-Mapped Config Registers				Y
0014H	PCI Base Address 1 for I/O-Mapped Config Registers				Y
0018H	**PCI Base Address 2 for Local Address Space 0 Shared RAM Access Window for all channels**				**Y**
001CH	**PCI Base Address 3 for Local Address Space 1 I/O Space Access Window for all channels**				**Y**
0020H	PCI Base Address 4 for Local Address Space 2				Y
0024H	PCI Base Address 5 for Local Address Space 3				Y
0028H	Cardbus CIS Pointer (Not supported)				N
002CH	**Subsystem Device ID 0x003A**		**Subsystem Vendor ID 0x133D**		**N**
0030H	PCI Base Address for Local Expansion ROM 0x00000000				Y
0034H	Reserved 0x00000000				N
0038H	Reserved 0x00000000				N
003CH	Max_Lat 0x00	Min_Gnt 0x00	Interrupt Pin 0x01	Interrupt Line 0x00	Y[7:0]

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3.3 Resource Allocation

Table 5: DN4-PCU Allocation

Resource	Total Allocated	Channel Allocation
Memory	256KB	256KB block
I/O	16-byte range Resource usage corresponds to the Host Register Layout.	16-byte block

3.4 DN4 Card Configuration Registers

This section provides hardware register details for the card.

3.4.1 Host Register Layout

The channel has its own set of registers, located in I/O space.



Note

Upon card power up, or after a physical reset from the system, it typically takes 1 second for the channel to initialize (though it is recommended that applications wait up to 2 seconds). Initialization can be confirmed by monitoring the LEDs or by reading the FamilyID register, as described in Section C.1.1, Verify Card Presence.

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Table 6: Host Register Layout

The following “offsets” are offsets from the base address. An “X” means that the bit is reserved (writing to it will result in undefined behavior).

Offset	Register Name	Bit Name							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	Control	CardRun (r/w)	MemEn (r/w)	IntEn (r/w)	WdTout (read)	0	HostIrq0 (r/w)	0	CardIrq0 (r/w)
01h (rd)	AddrMatch	1	X	X	X	X	X	X	0
02h	BankAddress	0	0	BA17	BA16	BA15	BA14	BA13	BA12
03h	BankSize	0	0	WS17	WS16	WS15	WS14	WS13	WS12
04h	HostIrq (r/w)	Platform	X	X	X	X	X	X	X
05(rd)	LedReg (read)	X	X	PwrRed	PwrGrn	HealthRed	HealthGrn	CommRed	CommGrn
06h	Debug (r/w)	X	X	X	X	X	X	X	X
07 (rd)	HDR (FamilyID)	HostDataReg (written by CPU) DN4 = 40h							

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3.4.2 Control Register

This register is a group of control and status bits.

Table 7: Control Register Settings

Bit	7	6	5	4	3	2	1	0
Name	CardRun	MemEn	IntEn	WdTout	0	HostIrq0	0	CardIrq0
Read/Write	R/W	R/W	R/W	R	R	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

The channel has two interrupt flags. Setting CardIrq0 generates an interrupt to the card with the relevant flag set. When HostIrq0 is '1' and IntEn is '1', the card drives the IRQ pin (as set by IrqLevel) high.

Table 8: Control Register Bit Descriptions

Bit Name	Description
CardRun	This bit controls and indicates whether or not the channel's processor is running. It also affects the Health LED. • When this bit is 0, the processor is halted, and the LED is RED • When this bit is 1, the processor is running normally, and the LED is under channel processor control • When this bit is 1, and watchdog has timed out, processor is halted, and the LED is RED • This bit must remain low for at least 50 μs to guarantee proper reset.
MemEn	This bit indicates and controls whether or not the channel's shared memory will respond to host memory accesses. This may be used to multiplex several SST-DN4-PCU cards or channels at the same base address by enabling the memory on one channel at a time. MemEn high ('1') enables shared memory decoding of addresses in this board's range.
IntEn	• Writing 1 enables interrupts • Writing 0 disables interrupts (the HostIrq flags still function as described)
WdTout	WdTout high ('1') indicates that a watchdog timeout has occurred, or that the channel's processor has been held in RESET by some other means. To restore this bit to 0, clear CardRun.
HostIrq0	• This bit is used by the channel's processor to indicate that the channel generated an interrupt. If IntEn is set to 1, this also means that the channel generated a physical interrupt on the PCI bus. • Writing 1 acknowledges the interrupt and clears it • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete
CardIrq0	This bit is used by the host to send interrupts to interrupt flag 0 of the channel's processor. • Writing 1 generates an interrupt • Writing 0 has no effect • Reading 1 indicates interrupt in progress • Reading 0 indicates interrupt complete

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3.4.3 AddrMatch Register

This register is reserved.

3.4.4 Bank Address Register

This register is used to switch banks of shared memory into host memory space.

Table 9: Bank Address Register Settings

Bit	7	6	5	4	3	2	1	0
Name	BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Table 10: Bank Address Register Values

In this table, the default window size is highlighted, and a value of “x” indicates “don’t care”.

Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	0	0	0	0	0	x	0	0	0	0	0	0
x	x	0	0	0	0	1	x	1	0	0	0	0	0
x	x	0	0	0	1	0	x	2	1	0	0	0	0
x	x	0	0	0	1	1	x	3	1	0	0	0	0
x	x	0	0	1	0	0	x	4	2	1	0	0	0
x	x	0	0	1	0	1	x	5	2	1	0	0	0
x	x	0	0	1	1	0	x	6	3	1	0	0	0
x	x	0	0	1	1	1	x	7	3	1	0	0	0
x	x	0	1	0	0	0	x	8	4	2	1	0	0
x	x	0	1	0	0	1	x	9	4	2	1	0	0
x	x	0	1	0	1	0	x	10	5	2	1	0	0
x	x	0	1	0	1	1	x	11	5	2	1	0	0
x	x	0	1	1	0	0	x	12	6	3	1	0	0
x	x	0	1	1	0	1	x	13	6	3	1	0	0
x	x	0	1	1	1	0	x	14	7	3	1	0	0
x	x	0	1	1	1	1	x	15	7	3	1	0	0
x	x	1	0	0	0	0	x	16	8	4	2	1	0
x	x	1	0	0	0	1	x	17	8	4	2	1	0
x	x	1	0	0	1	0	x	18	9	4	2	1	0
x	x	1	0	0	1	1	x	19	9	4	2	1	0

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Bit and Value								Window Size and Bank Number					
BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	8k	16k	32k	64k	128k	256k
x	x	1	0	1	0	0	x	20	10	5	2	1	0
x	x	1	0	1	0	1	x	21	10	5	2	1	0
x	x	1	0	1	1	0	x	22	11	5	2	1	0
x	x	1	0	1	1	1	x	23	11	5	2	1	0
x	x	1	1	0	0	0	x	24	12	6	3	1	0
x	x	1	1	0	0	1	x	25	12	6	3	1	0
x	x	1	1	0	1	0	x	26	13	6	3	1	0
x	x	1	1	0	1	1	x	27	13	6	3	1	0
x	x	1	1	1	0	0	x	28	14	7	3	1	0
x	x	1	1	1	0	1	x	29	14	7	3	1	0
x	x	1	1	1	1	0	x	30	15	7	3	1	0
x	x	1	1	1	1	1	x	31	15	7	3	1	0

* x = don’t care

Table 11: Bank Address Register Bit Descriptions

Bit Name	Description
BA17-13	The channel has 256k of memory accessible to the host. The Bank Address bits select which bank of memory the host can access. For example, in 16k mode, the bank number may be 0 through 15 (or 0x0 - 0xf). • BA17-BA13 represent the bank address • Bank numbers depend on the window size, selected using the WinSize bits. Refer to Table 15: BankSize Register Values, for more information.

To access any flat address of memory, “ADDR” in any window size, set the Bank Address bits to bits 19-12 of the address. In C, you would write:

```
outport( BankSelect, addr>>12);
offset= addr & ((inport( WinSize ) <<12 ) | 0x0FFF);
```


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3.4.5 BankSize Register

This register controls the window size by masking off bits BA19-BA12 in the Bank Address register. Table 13, BankSize Register Values, maps the WS values required for each valid window size.

Table 12: BankSize Register Settings

Bit	7	6	5	4	3	2	1	0
Name	WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	1	1

Table 13: BankSize Register Values

In this table, the default window values are highlighted.

Bit and Value								Window Size	Description
WS19	**WS18**	**WS17**	**WS16**	**WS15**	**WS14**	**WS13**	**WS12**		
0	0	0	0	0	0	0	1	8K	BA19-BA13 used, BA12 ignored
0	0	0	0	0	0	1	1	16K	BA19-BA14 used, BA13-BA12 ignored
0	0	0	0	0	1	1	1	32K	BA19-BA15 used, BA14-BA12 ignored
0	0	0	0	1	1	1	1	64K	BA19-BA16 used, BA15-BA12 ignored
0	0	0	1	1	1	1	1	128K	BA19-BA17 used, BA16-BA12 ignored
0	0	1	1	1	1	1	1	256K	BA19-BA18 used, BA17-BA12 ignored

Table 14: BankSize Register Bit Descriptions

Bit Name	Description
WS19-WS12	WS19-WS12 represent the window size, according to Table 15: BankSize Register Values. • Writing any value other than those above has no effect The size of the memory window affects the number of banks required to access all memory. Refer to Table 12: Bank Address Register Values, for more information.

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3.4.6 HostIrq Register

The Irq function is supported in the PCI interface so the Irq support in this register is reserved.

Table 15: HostIrq Register Settings

Bit	7	6	5	4	3	2	1	0
Name	Platform	Platform ID			reserved	reserved	reserved	reserved
Read/Write	R/W	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

The DN4 platform shall support DN3/DN4 hardware platform detection in the HostIrq register as follows:

1) Writing 1000b in bits 7-4 shall cause bits 7-4 to subsequently read a platform. This code shall only be non-zero for DN4 and above. The initial write of 1000b to bits 7-4 is to ensure old drivers will not see a value in these bits that it is not expecting, DN, DNP and DN3 expect 0000b and writing these bits did nothing.

2) DN4 platform shall read 0001b only if the previous access to the cards registers wrote "1" to the Platform bit. When the Platform is set then the next access, read or write, will clear the Platform bit.

3.4.7 LedReg Register

This register reflects the state of the channel's LEDs, allowing host software to monitor the LEDs and display them on-screen.

Table 16: LedReg Register Settings

			PWR		HLTH		COMM	
Bit	7	6	5	4	3	2	1	0
Name	Reserved		PwrRed	PwrGrn	HealthRed	HealthGrn	CommRed	CommGrn
Read/Write	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

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Note

Although the card does not have a physical power LED, the power status can be determined via the PWR bits. Refer to Section 1.5.2, LEDs, for more details.

Table 17: LedReg Register Values

Bit Name/Value		Description
PwrRed	**PwrGrn**	These bits indicate the channel's power state
0	0	Invalid
0	1	LED is green
1	0	LED is red
1	1	Invalid
HealthRed	**HealthGrn**	These bits indicate the channel's health LED state
0	0	LED is off
0	1	LED is green
1	0	LED is red
1	1	LED is amber
CommRed	**CommGrn**	These bits indicate the channel's communications LED state
0	0	LED is off
0	1	LED is green
1	0	LED is red
1	1	LED is amber

3.4.8 Debug Register

This register is reserved.

3.4.9 Host Data Register (FamilyID)

The Host Data register can be used to pass 1 byte of data from Card to Host. This register is written by the CPU and is read-only by the Host. Its use is determined by firmware/boot.

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4
Troubleshooting

Chapter Sections:

- HLTH LED is Red
- Memory Conflict
- Card Not Found
- General Troubleshooting

For a list of hardware-related errors that can be generated by the card, refer to Appendix A, Error Messages.



Warning

Only qualified electrical personnel familiar with the construction and operation of this equipment and the hazards involved should install, adjust, operate, or service this equipment. Failure to observe this precaution could result in severe bodily injury or loss of life.

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4.1 HLTH LED is Red

This section describes strategies for troubleshooting a red HLTH LED.



Note

For information on LED flash codes, refer to Section A.3, Fatal Hardware Self-Test Flash Codes.

If the HLTH LED is red, the channel is not running or there has been a firmware run-time error. Check the WdTout bit (refer to Table 10, Control Register Bit Descriptions) to determine whether or not there has been a watchdog timeout, and consult the appropriate firmware manual if necessary. If you continue to experience difficulties, refer to Section 4.4, General Troubleshooting.



Note

The firmware must be reloaded to restart the channel.

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4.2 Memory Conflict

If a memory conflict is detected, examine the resource allocations in the operating system. If the operating system does not manage resources, review the requirements of the other hardware installed in the machine to select a non-conflicting memory window. If you continue to experience difficulties, refer to Section 4.4, General Troubleshooting.

4.3 Card Not Found

If a “card not found” message is displayed, check for memory I/O and IRQ conflicts. If you continue to experience difficulties, refer to Section 4.4, General Troubleshooting.

4.4 General Troubleshooting

If you experience problems with the card:

1. Check the website at http://www.woodhead.com for technical notes and DeviceNet release notes.
2. Check the FAQs on the website.
3. Refer to Section D.3, Technical Support.

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A
Error Messages

Appendix Sections:

- Introduction
- FamilyID Messages
- Flashing LEDs

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A.1 Introduction

Error messages are posted in the Host Interface Memory's message area (0040h) and can be displayed using one of the status applications, such as DNSTAT, provided with the card. For details on the shared Host Interface Memory layout, refer to the Firmware Reference Guide.

A.2 FamilyID Messages

If FamilyID reads anything other than 0x40, the card has not been found. Check for memory and I/O conflicts. If you continue to experience difficulties, refer to Section 4.4, General Troubleshooting.

A.3 Fatal Hardware Self-Test Flash Codes

Fatal failures during startup are accompanied by an 8-bit fault code, flashed on the Health Led. The fault code will be output MSB first, with a 1 (one) bit shown as a green LED, and a zero (0) bit shown as a red LED. This will occur for a period of 900ms, followed by 100ms of off time. The LSB will be followed by an additional 1000ms of off time, after which the sequence will repeat.

The following table describes each possible fault code.

Table 18: LED Flash Codes

Value	Flash sequence Left->Right	Description
0x10	**R-R-R-G-R-R-R-R**	**Invalid/non-existent boot loader in Flash**
0x11	**R-R-R-G-R-R-R-G**	**Flash ID Invalid**
0x12	**R-R-R-G-R-R-G-R**	**Flash read error**
0x13	**R-R-R-G-R-R-G-G**	**Shared memory error**
0x14	**R-R-R-G-R-G-R-R**	**Local memory failure**
0x15-FF	-	Reserved for firmware-specific fatal errors

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B

Technical Specifications

Appendix Sections

- Technical Specifications

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B.1 Technical Specifications

The following tables list the technical specifications for the card.

Table 19: Environmental Specifications

Ambient Conditions	Storage temp:	-40°C to +85°C
	Operating temp:	0°C to 60°C
	Humidity:	5% to 95% non-condensing
Typical Current Draw		+5V, +/-5%, 0.3 A (1-channel)

Table 20: Network Specifications

Cable	Shielded twisted pair, compatible with target network
External Power	11-24 VDC, 50mA (typical)
Isolation	500V
Protocol	CAN 2.0 A/B
Data Rate	Up to 1M baud for CAN 125K, 250K and 500K baud for DeviceNet

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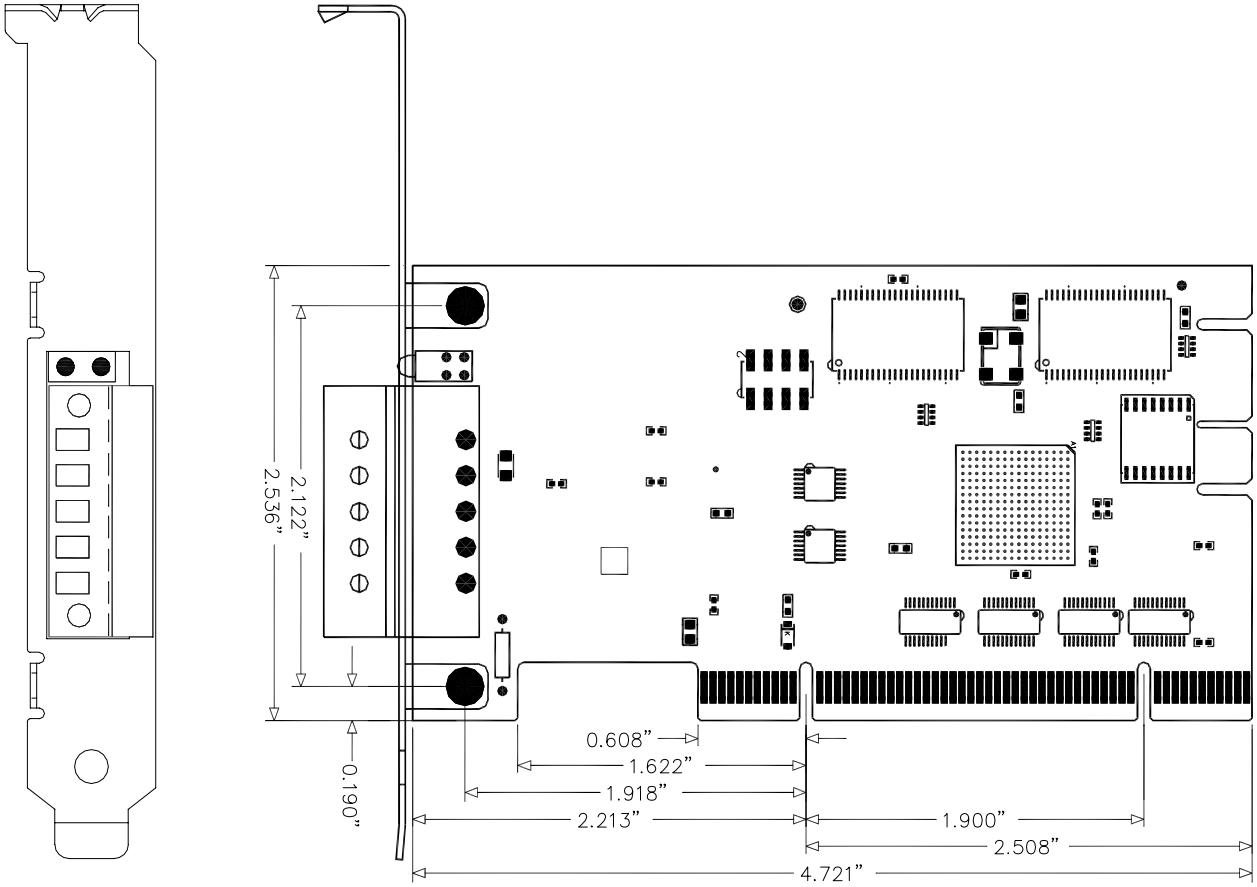
PCI Bus Specifications

Compliance	Compatible with PCI 2.2; will operate in 2.3 and some 2.1-compliant systems. Refer to Table 1: PCI Compatibility Table, for more information.
Size	Standard half-length, 32-bit, 33MHz, universal PCI card
Resources	(memory) 2K window for Card only (memory) 256KB window available to the host per channel (I/O) 16 bytes allocated for channel (I/O) 128 bytes for PCI configuration, per card

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Figure 4: Card Dimensions



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C
Loading Firmware

Appendix Sections:

- Loading Firmware



Note

This appendix describes how to load the card manually, or how to write your own loader. If you are using a Windows loader provided by Woodhead Software & Electronics, the following instructions are not required.

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C.1 Loading Firmware

Firmware modules for the card are supplied as .ss4 files, found on the software CD-ROM or on the website at http://www.woodhead.com.

If you are developing a driver for the card or producing a stand-alone embedded application, the following section describes the basic sequence of steps to load a module into the channel's memory.



Note

These procedures should be repeated for each channel.



Note

For register descriptions, refer to Chapter 3, Hardware Register Details.

C.1.1 Verify Card Presence

To verify the channel's presence, follow these steps:

1. Start up your computer.
2. Following release of the backplane reset, wait up to 2 seconds.
3. Verify a FamilyID Register value of 0x40.
4. If FamilyID reads anything other than 0x40, the card is still in Reset or has not been found. Refer to Section 4.4, General Troubleshooting.

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C.1.2 Check for Conflicting RAM

Before the channel's shared memory can be safely enabled, you must determine that no other system devices are using the intended memory address range.



Note

Any task switching, interrupts or processes should be disabled during this procedure.

To check for conflicting RAM, follow these steps:

1. Write zero (0) to the Control Register to disable the channel.
2. Read a word from the target memory window and save it.
3. Write 0xAA55 to the target address.
4. Read the target address. It should not contain 0xAA55.
5. If 0xAA55 is read, a conflict exists. Perform the following steps:
   - Restore the saved value to the target address
   - Abort the load procedure
   - Examine the resource allocations in your operating system. If your operating system does not manage resources, review the requirements of other hardware installed in your machine to select a non-conflicting memory window. If you continue to experience difficulties, please refer to Section 4.4, General Troubleshooting.



Note

If you are unsure of the system's memory usage, you may want to do a full memory window verification to ensure that there are no memory conflicts.

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C.1.3 Test Channel RAM

1. To test the channel's RAM, follow these steps:
2. Write the desired window size to the BankSize register (refer to Section 3.4.5, BankSize Register, for details).
3. Write 0x40 (MemEn) to the Control Register.
4. Set the Bank Address Register (refer to Section 3.4.4, Bank Address Register, for details).
5. Fill the shared memory with a test pattern.



Note

We recommend using a test pattern with a unique value for each word in a given bank. In C language this could be:

```
~offset + bank.
```

6. Repeat steps 3-4 for all memory banks.
7. Verify the test pattern.

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C.1.4 Load and Start the Firmware Module

To load and start the firmware module, follow these steps:

1. Write the contents of the entire firmware file into shared memory, starting at bank zero (0), offset zero (0).
2. If the application requires interrupts from the card, bit-wise OR value 0x20 (IntEn) to the Control Register.
3. Bit-wise OR value 0x80 (CardRun) to the Control Register to start the firmware module.
4. Start a 2-second timeout timer and wait for value 0x04 (HostIrq0) in the Control Register to set.
5. If the timer expires, the firmware module failed to start. Write zero to the Control Register to disable the channel's processor. If this problem persists, contact Technical Support for assistance.
6. Check the load status, as per the firmware manual.

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D

Warranty and Support

Appendix Sections:

- Warranty
- Reference Documents
- Technical Support

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D.1 Warranty

For warranty information pertaining to the card, refer to http://www.mysst.com/warranty.asp.

D.2 Reference Documents

DeviceNet Specification, CIP Library Volume 1 Ed 3.2 "Common Industrial Protocol:
CIP Library Volume 3 Ed 1.4 "DeviceNet Adaptation of CIP

ODVA Publication, March 2002
http://www.odva.org/

PCI Local Bus Specification v2.2
PCI Special Interest Group, December 1998

Molex User guides: 716-0019 DN3 vs DN4 comparison technical note

717-0037 DN4 Boot Code User Guide

D.3 Technical Support

Please ensure that you have the following information readily available before calling for technical support:

- Card model, type and serial number
- Computer's make, model, CPU speed and hardware configuration (other cards installed)
- Operating system type and version
- Details of the problem you are experiencing: application module type and version, target network, and circumstances that may have caused the problem

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D.3.1 Getting Help

Technical Support is available during regular business hours by telephone, fax or email from any Woodhead Software & Electronics office, or from http://www.woodhead.com. Documentation and software updates are also available on the website.

North America

Canada:
Tel: +1-519-725-5136
Fax: +1-519-725-1515
Email: WoodheadSupportNA@molex.com

Europe

France:
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E

CE Compliance

Appendix Sections:

- CE Compliance

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E.1 CE Compliance

This device meets or exceeds the requirements of the following standard:

- EN 61326:1998 including amendments A1 and A2: - “Electrical equipment for measurement, control and laboratory use - EMC requirements.



Warning

This is a Class A product. In a domestic environment this product may cause radio interference in which case you may be required to take adequate measures.



Caution

This equipment is neither designed for, nor intended for operation in installations where it is subject to hazardous voltages and hazardous currents.

Marking of this equipment with the symbol CE indicates compliance with European Council Directive 89/336/EEC - The EMC Directive as amended by 92/31/EEC and 93/68/EEC.



Note

To maintain compliance with the limits and requirements of the EMC Directive, it is required to use quality interfacing cables and connectors when connecting to this device. Refer to the cable specifications in the Hardware Guide for selection of cable types.



Note

The backplane voltage supply for this equipment must be delivered as Separated Extra Low Voltage (SELV).

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